



HIGH-SPEED 3.3V 512K x 18 SYNCHRONOUS BANK-SWITCHABLE DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

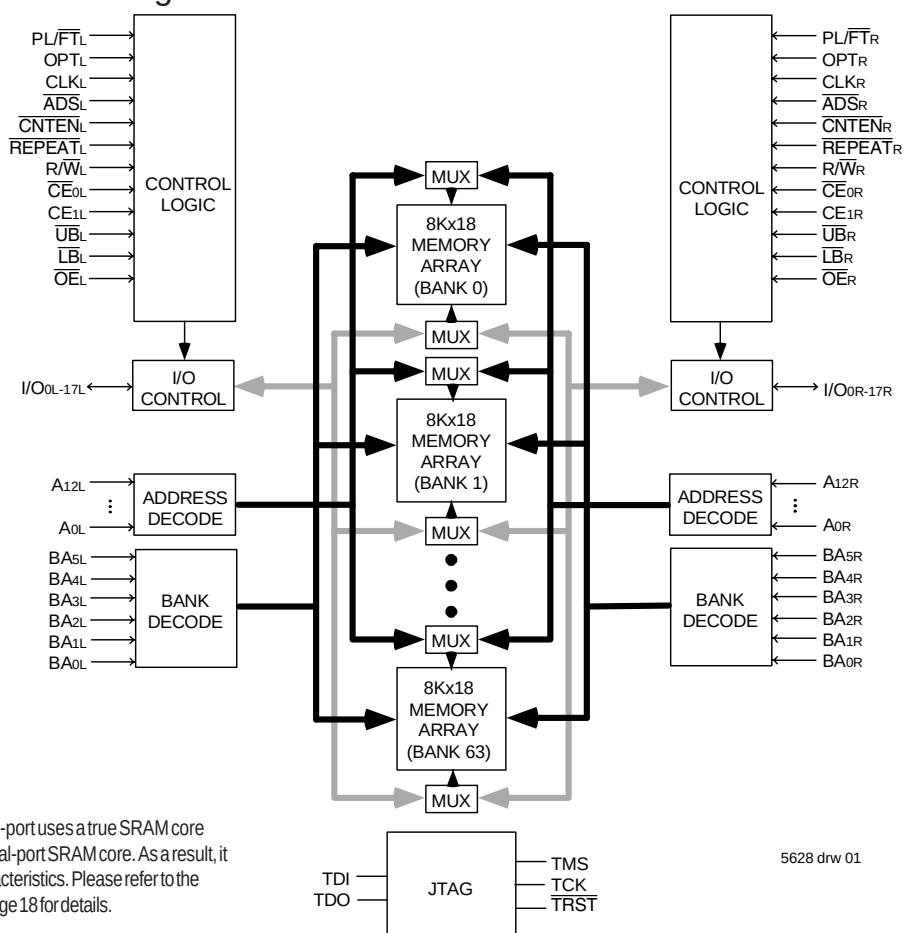
IDT70V7339S

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

Features:

- ♦ **512K x 18 Synchronous Bank-Switchable Dual-ported SRAM Architecture**
 - 64 independent 8K x 18 banks
 - 9 megabits of memory on chip
- ♦ **Bank access controlled via bank address pins**
- ♦ **High-speed data access**
 - Commercial: 3.4ns (200MHz)/3.6ns (166MHz)/4.2ns (133MHz) (max.)
 - Industrial: 3.6ns (166MHz)/4.2ns (133MHz) (max.)
- ♦ **Selectable Pipelined or Flow-Through output mode**
- ♦ **Counter enable and repeat features**
- ♦ **Dual chip enables allow for depth expansion without additional logic**
- ♦ **Full synchronous operation on both ports**
 - 5ns cycle time, 200MHz operation (14Gbps bandwidth)
 - Fast 3.4ns clock to data out
- 1.5ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 200MHz
- Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ♦ **Separate byte controls for multiplexed bus and bus matching compatibility**
- ♦ **LVTTTL-compatible, 3.3V (±150mV) power supply for core**
- ♦ **LVTTTL compatible, selectable 3.3V (±150mV) or 2.5V (±100mV) power supply for I/Os and control signals on each port**
- ♦ **Industrial temperature range (-40°C to +85°C) is available at 166MHz and 133MHz**
- ♦ **Available in 208-pin fine pitch Ball Grid Array (fpBGA) and 256-pin Ball Grid Array (BGA)**
- ♦ **Supports JTAG features compliant with IEEE 1149.1**
- ♦ **Green parts available, see ordering information**

Functional Block Diagram



NOTE:

1. The Bank-Switchable dual-port uses a true SRAM core instead of the traditional dual-port SRAM core. As a result, it has unique operating characteristics. Please refer to the functional description on page 18 for details.

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JUNE 2018

Description:

The IDT70V7339 is a high-speed 512Kx18 (9Mbit) synchronous Bank-Switchable Dual-Ported SRAM organized into 64 independent 8Kx18 banks. The device has two independent ports with separate control, address, and I/O pins for each port, allowing each port to access any 8Kx18 memory block not already accessed by the other port. Accesses by the ports into specific banks are controlled via the bank address pins under the user's direct control.

Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data

register, the IDT70V7339 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by CE0 and CE1, permits the on-chip circuitry of each port to enter a very low standby power mode. The dual chip enables also facilitate depth expansion.

The 70V7339 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (VDD) remains at 3.3V. Please refer also to the functional description on page 18.

Pin Configuration^(1,2,3,4)

A1 IO9L	A2 NC	A3 VSS	A4 TDO	A5 NC	A6 BA3L	A7 A12L	A8 A8L	A9 NC	A10 VDD	A11 CLKL	A12 CNTENL	A13 A4L	A14 A0L	A15 OPTL	A16 NC	A17 VSS	
B1 NC	B2 VSS	B3 NC	B4 TDI	B5 BA4L	B6 BA0L	B7 A9L	B8 NC	B9 CE0L	B10 VSS	B11 ADSL	B12 A5L	B13 A1L	B14 VSS	B15 VDDQR	B16 I/O8L	B17 NC	
C1 VDDQL	C2 I/O9R	C3 VDDQR	C4 PL/FTL	C5 BA5L	C6 BA1L	C7 A10L	C8 UBL	C9 CE1L	C10 VSS	C11 R/WL	C12 A6L	C13 A2L	C14 VDD	C15 I/O8R	C16 NC	C17 VSS	
D1 NC	D2 VSS	D3 I/O10L	D4 NC	D5 BA2L	D6 A11L	D7 A7L	D8 LBL	D9 VDD	D10 OEL	D11 REPEATL	D12 A3L	D13 VDD	D14 NC	D15 VDDQL	D16 I/O7L	D17 I/O7R	
E1 I/O11L	E2 NC	E3 VDDQR	E4 I/O10R	70V7339BF BF-208⁽⁵⁾ 208-Pin fpBGA Top View⁽⁶⁾										E14 I/O6L	E15 NC	E16 VSS	E17 NC
F1 VDDQL	F2 I/O11R	F3 NC	F4 VSS											F14 VSS	F15 I/O6R	F16 NC	F17 VDDQR
G1 NC	G2 VSS	G3 I/O12L	G4 NC											G14 NC	G15 VDDQL	G16 I/O5L	G17 NC
H1 VDD	H2 NC	H3 VDDQR	H4 I/O12R											H14 VDD	H15 NC	H16 VSS	H17 I/O5R
J1 VDDQL	J2 VDD	J3 VSS	J4 VSS											J14 VSS	J15 VDD	J16 VSS	J17 VDDQR
K1 I/O14R	K2 VSS	K3 I/O13R	K4 VSS											K14 I/O3R	K15 VDDQL	K16 I/O4R	K17 VSS
L1 NC	L2 I/O14L	L3 VDDQR	L4 I/O13L											L14 NC	L15 I/O3L	L16 VSS	L17 I/O4L
M1 VDDQL	M2 NC	M3 I/O15R	M4 VSS											M14 VSS	M15 NC	M16 I/O2R	M17 VDDQR
N1 NC	N2 VSS	N3 NC	N4 I/O15L											N14 I/O1R	N15 VDDQL	N16 NC	N17 I/O2L
P1 I/O16R	P2 I/O16L	P3 VDDQR	P4 NC	P5 TRST	P6 BA3R	P7 A12R	P8 A8R	P9 NC	P10 VDD	P11 CLKR	P12 CNTENR	P13 A4R	P14 NC	P15 I/O1L	P16 VSS	P17 NC	
R1 VSS	R2 NC	R3 I/O17R	R4 TCK	R5 BA4R	R6 BA0R	R7 A9R	R8 NC	R9 CE0R	R10 VSS	R11 ADSR	R12 A5R	R13 A1R	R14 VSS	R15 VDDQL	R16 I/O0R	R17 VDDQR	
T1 NC	T2 I/O17L	T3 VDDQL	T4 TMS	T5 BA5R	T6 BA1R	T7 A10R	T8 UBR	T9 CE1R	T10 VSS	T11 R/WR	T12 A6R	T13 A2R	T14 VSS	T15 NC	T16 VSS	T17 NC	
U1 VSS	U2 NC	U3 PL/FTL	U4 NC	U5 BA2R	U6 A11R	U7 A7R	U8 LBR	U9 VDD	U10 OER	U11 REPEATR	U12 A3R	U13 A0R	U14 VDD	U15 OPTR	U16 NC	U17 I/O0L	

NOTES:

1. All VDD pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VIH (3.3V), and 2.5V if OPT pin for that port is set to VIL (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

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Pin Configuration^(1,2,3,4) (con't.)

70V7339BC

BC-256⁽⁵⁾

256-Pin BGA

Top View⁽⁶⁾

A1 NC	A2 TDI	A3 NC	A4 BA _{4L}	A5 BA _{1L}	A6 A _{11L}	A7 A _{8L}	A8 NC	A9 CE _{1L}	A10 OE _L	A11 CNTEN _L	A12 A _{5L}	A13 A _{2L}	A14 A _{0L}	A15 NC	A16 NC
B1 NC	B2 NC	B3 TDO	B4 BA _{5L}	B5 BA _{2L}	B6 A _{12L}	B7 A _{9L}	B8 UB _L	B9 CE _{0L}	B10 R/W _L	B11 REPEAT _L	B12 A _{4L}	B13 A _{1L}	B14 V _{DD}	B15 NC	B16 NC
C1 NC	C2 I/O _{9L}	C3 V _{SS}	C4 BA _{3L}	C5 BA _{0L}	C6 A _{10L}	C7 A _{7L}	C8 NC	C9 LB _L	C10 CLK _L	C11 ADS _L	C12 A _{6L}	C13 A _{3L}	C14 OPT _L	C15 NC	C16 I/O _{8L}
D1 NC	D2 I/O _{9R}	D3 NC	D4 PL/FT _L	D5 VDDQL	D6 VDDQL	D7 VDDQR	D8 VDDQR	D9 VDDQL	D10 VDDQL	D11 VDDQR	D12 VDDQR	D13 VDD	D14 NC	D15 NC	D16 I/O _{8R}
E1 I/O _{10R}	E2 I/O _{10L}	E3 NC	E4 VDDQL	E5 VDD	E6 VDD	E7 VSS	E8 VSS	E9 VSS	E10 VSS	E11 VDD	E12 VDD	E13 VDDQR	E14 NC	E15 I/O _{7L}	E16 I/O _{7R}
F1 I/O _{11L}	F2 NC	F3 I/O _{11R}	F4 VDDQL	F5 VDD	F6 VSS	F7 VSS	F8 VSS	F9 VSS	F10 VSS	F11 VSS	F12 VDD	F13 VDDQR	F14 I/O _{6R}	F15 NC	F16 I/O _{6L}
G1 NC	G2 NC	G3 I/O _{12L}	G4 VDDQR	G5 VSS	G6 VSS	G7 VSS	G8 VSS	G9 VSS	G10 VSS	G11 VSS	G12 VSS	G13 VDDQL	G14 I/O _{5L}	G15 NC	G16 NC
H1 NC	H2 I/O _{12R}	H3 NC	H4 VDDQR	H5 VSS	H6 VSS	H7 VSS	H8 VSS	H9 VSS	H10 VSS	H11 VSS	H12 VSS	H13 VDDQL	H14 NC	H15 NC	H16 I/O _{5R}
J1 I/O _{13L}	J2 I/O _{14R}	J3 I/O _{13R}	J4 VDDQL	J5 VSS	J6 VSS	J7 VSS	J8 VSS	J9 VSS	J10 VSS	J11 VSS	J12 VSS	J13 VDDQR	J14 I/O _{4R}	J15 I/O _{3R}	J16 I/O _{4L}
K1 NC	K2 NC	K3 I/O _{14L}	K4 VDDQL	K5 VSS	K6 VSS	K7 VSS	K8 VSS	K9 VSS	K10 VSS	K11 VSS	K12 VSS	K13 VDDQR	K14 NC	K15 NC	K16 I/O _{3L}
L1 I/O _{15L}	L2 NC	L3 I/O _{15R}	L4 VDDQR	L5 VDD	L6 VSS	L7 VSS	L8 VSS	L9 VSS	L10 VSS	L11 VSS	L12 VDD	L13 VDDQL	L14 I/O _{2L}	L15 NC	L16 I/O _{2R}
M1 I/O _{16R}	M2 I/O _{16L}	M3 NC	M4 VDDQR	M5 VDD	M6 VDD	M7 VSS	M8 VSS	M9 VSS	M10 VSS	M11 VDD	M12 VDD	M13 VDDQL	M14 I/O _{1R}	M15 I/O _{1L}	M16 NC
N1 NC	N2 I/O _{17R}	N3 NC	N4 PL/FT _R	N5 VDDQR	N6 VDDQR	N7 VDDQL	N8 VDDQL	N9 VDDQR	N10 VDDQR	N11 VDDQL	N12 VDDQL	N13 VDD	N14 NC	N15 I/O _{0R}	N16 NC
P1 NC	P2 I/O _{17L}	P3 TMS	P4 BA _{3R}	P5 BA _{0R}	P6 A _{10R}	P7 A _{7R}	P8 NC	P9 LB _R	P10 CLK _R	P11 ADS _R	P12 A _{6R}	P13 A _{3R}	P14 NC	P15 NC	P16 I/O _{0L}
R1 NC	R2 NC	R3 TRST	R4 BA _{5R}	R5 BA _{2R}	R6 A _{12R}	R7 A _{9R}	R8 UB _R	R9 CE _{0R}	R10 R/W _R	R11 REPEAT _R	R12 A _{4R}	R13 A _{1R}	R14 OPT _R	R15 NC	R16 NC
T1 NC	T2 TCK	T3 NC	T4 BA _{4R}	T5 BA _{1R}	T6 A _{11R}	T7 A _{8R}	T8 NC	T9 CE _{1R}	T10 OE _R	T11 CNTEN _R	T12 A _{5R}	T13 A _{2R}	T14 A _{0R}	T15 NC	T16 NC

NOTES:

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1. All V_{DD} pins must be connected to 3.3V power supply.
2. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to V_{IH} (3.3V), and 2.5V if OPT pin for that port is set to V_{IL} (0V).
3. All VSS pins must be connected to ground supply.
4. Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enables
$R/\overline{WL}$	$R/\overline{WR}$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
BA_{0L} - BA_{5L}	BA_{0R} - BA_{5R}	Bank Address ⁽⁴⁾
A_{0L} - A_{12L}	A_{0R} - A_{12R}	Address
I/O_{0L} - I/O_{17L}	I/O_{0R} - I/O_{17R}	Data Input/Output
CLK_L	CLK_R	Clock
$PL/\overline{FT}_L$	$PL/\overline{FT}_R$	Pipeline/Flow-Through
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{REPEAT}_L$	$\overline{REPEAT}_R$	Counter Repeat ⁽³⁾
$\overline{LB}_L$, $\overline{UB}_L$	$\overline{LB}_R$, $\overline{UB}_R$	Byte Enables (9-bit bytes)
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V) ⁽¹⁾
OPT_L	OPT_R	Option for selecting V_{DDQX} ^(1,2)
V_{DD}		Power (3.3V) ⁽¹⁾
V_{SS}		Ground (0V)
TDI		Test Data Input
TDO		Test Data Output
TCK		Test Logic Clock (10MHz)
TMS		Test Mode Select
$\overline{TRST}$		Reset (Initialize TAP Controller)

5628 tbl 01

NOTES:

- V_{DD} , OPT_x , and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- OPT_x selects the operating voltage levels for the I/Os and controls on that port. If OPT_x is set to V_{IH} (3.3V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_x is set to V_{IL} (0V), then that port's I/Os and address controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
- When $\overline{REPEAT}_x$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}_x$.
- Accesses by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory with the shared array that is not currently being accessed by the opposite port (i.e., BA_{0L} - $BA_{5L} \neq BA_{0R}$ - BA_{5R}). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the ports within that bank may be corrupted (in the case that either or both ports are writing) or may result in invalid output (in the case that both ports are trying to read).

Truth Table I—Read/Write and Enable Control^(1,2,3,4)

$\overline{OE}^3$	CLK	$\overline{CE}_0$	CE_1	$\overline{UB}$	$\overline{LB}$	R/ $\overline{W}$	Upper Byte I/O ₉₋₁₇	Lower Byte I/O ₀₋₈	MODE
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	L	L	High-Z	D _{IN}	Write to Lower Byte Only
X	↑	L	H	L	H	L	D _{IN}	High-Z	Write to Upper Byte Only
X	↑	L	H	L	L	L	D _{IN}	D _{IN}	Write to both Bytes
L	↑	L	H	H	L	H	High-Z	D _{OUT}	Read Lower Byte Only
L	↑	L	H	L	H	H	D _{OUT}	High-Z	Read Upper Byte Only
L	↑	L	H	L	L	H	D _{OUT}	D _{OUT}	Read both Bytes
H	X	X	X	X	X	X	High-Z	High-Z	Outputs Disabled

5628 tbl 02

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- $\overline{ADS}$, $\overline{CNTEN}$, $\overline{REPEAT}$ are set as appropriate for address access. Refer to Truth Table II for details.
- $\overline{OE}$ is an asynchronous input signal.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

Truth Table II—Address and Address Counter Control^(1,2,7)

Address	Previous Address	Addr Used	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{REPEAT}^{(6)}$	I/O ⁽⁸⁾	MODE
A _n	X	A _n	↑	L ⁽⁴⁾	X	H	D _{IO} (n)	External Address Used
X	A _n	A _n + 1	↑	H	L ⁽⁵⁾	H	D _{IO} (n+1)	Counter Enabled—Internal Address generation
X	A _n + 1	A _n + 1	↑	H	H	H	D _{IO} (n+1)	External Address Blocked—Counter disabled (A _n + 1 reused)
X	X	A _n	↑	X	X	L ⁽⁴⁾	D _{IO} (0)	Counter Set to last valid $\overline{ADS}$ load

5628 tbl 03

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R/ $\overline{W}$, $\overline{CE}_0$, CE_1 , $\overline{UB}/\overline{LB}$ and $\overline{OE}$.
- Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
- $\overline{ADS}$ and $\overline{REPEAT}$ are independent of all other memory control signals including $\overline{CE}_0$, CE_1 and $\overline{UB}/\overline{LB}$.
- The address counter advances if $\overline{CNTEN}$ = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including $\overline{CE}_0$, CE_1 , $\overline{UB}/\overline{LB}$.
- When $\overline{REPEAT}$ is asserted, the counter will reset to the last valid address loaded via $\overline{ADS}$. This value is not set at power-up: a known location should be loaded via $\overline{ADS}$ during initialization if desired. Any subsequent $\overline{ADS}$ access during operations will update the $\overline{REPEAT}$ address location.
- The counter includes bank address and internal address. The counter will advance across bank boundaries. For example, if the counter is in Bank 0, at address FFFh, and is advanced one location, it will move to address 0h in Bank 1. By the same token, the counter at FFFh in Bank 63 will advance to 0h in Bank 0. Refer to Timing Waveform of Counter Repeat, page 17. Care should be taken during operation to avoid having both counters point to the same bank (i.e., ensure BA_{0L} - BA_{5L} ≠ BA_{0R} - BA_{5R}), as this condition will invalidate the access for both ports. Please refer to the functional description on page 18 for details.

Recommended Operating Temperature and Supply Voltage⁽¹⁾

Grade	Ambient Temperature	GND	V _{DD}
Commercial	0°C to +70°C	0V	3.3V $\pm$ 150mV
Industrial	-40°C to +85°C	0V	3.3V $\pm$ 150mV

5628 tbl 04

NOTE:

1. This is the parameter T_A. This is the "instant on" case temperature.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	50	mA

5628 tbl 06

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{DD} + 150mV for more than 25% of the cycle time or 4ns maximum, and is limited to ≤ 20 mA for the period of V_{TERM} $\geq$ V_{DD} + 150mV.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	2.4	2.5	2.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address & Control Inputs)	1.7	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	1.7	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V

5628 tbl 05a

NOTES:

1. Undershoot of V_{IL} $\geq$ -1.5V for pulse width less than 10ns is allowed.
2. V_{TERM} must not exceed V_{DDQ} + 100mV.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IL} (0V), and V_{DDQx} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	3.15	3.3	3.45	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	3.15	3.3	3.45	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address & Control Inputs) ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IH}	Input High Voltage - I/O ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V

5628 tbl 05b

NOTES:

1. Undershoot of V_{IL} $\geq$ -1.5V for pulse width less than 10ns is allowed.
2. V_{TERM} must not exceed V_{DDQ} + 150mV.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{IH} (3.3V), and V_{DDQx} for that port must be supplied as indicated above.

Capacitance⁽¹⁾

(TA = +25°C, F = 1.0MHz) PQFP ONLY

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	8	pF
C _{OUT} ⁽³⁾	Output Capacitance	V _{OUT} = 3dV	10.5	pF

5628 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{I/O}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 3.3V ± 150mV)

Symbol	Parameter	Test Conditions	70V7339S		Unit
			Min.	Max.	
I _{LI}	Input Leakage Current ⁽¹⁾	V _{DDQ} = Max., V _{IN} = 0V to V _{DDQ}	—	10	μA
I _{LO}	Output Leakage Current ⁽¹⁾	$\overline{CE_0} = V_{IH}$ or $CE_1 = V_{IL}$, V _{OUT} = 0V to V _{DDQ}	—	10	μA
V _{OL} (3.3V)	Output Low Voltage ⁽²⁾	I _{OL} = +4mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (3.3V)	Output High Voltage ⁽²⁾	I _{OH} = -4mA, V _{DDQ} = Min.	2.4	—	V
V _{OL} (2.5V)	Output Low Voltage ⁽²⁾	I _{OL} = +2mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (2.5V)	Output High Voltage ⁽²⁾	I _{OH} = -2mA, V _{DDQ} = Min.	2.0	—	V

5628 tbl 08

NOTES:

- At V_{DD} ≤ 2.0V leakages are undefined.
- V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to page 4 for details.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽⁵⁾ ($V_{DD} = 3.3V \pm 150mV$)

Symbol	Parameter	Test Condition	Version		70V7339S200 ⁽⁷⁾ Com'l Only		70V7339S166 ⁽⁶⁾ Com'l & Ind		70V7339S133 Com'l & Ind		Unit
					Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	
IDD	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	815	950	675	790	550	645	mA
			IND	S	—	—	675	830	550	675	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	340	410	275	340	250	295	mA
			IND	S	—	—	275	355	250	310	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(3)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	690	770	515	640	460	520	mA
			IND	S	—	—	515	660	460	545	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DDQ} - 0.2V$, $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L	S	10	30	10	30	10	30	mA
			IND	S	—	—	10	40	10	40	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DDQ} - 0.2V^{(5)}$ $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	690	770	515	640	460	520	mA
			IND	S	—	—	515	660	460	545	

5628 tbl 09

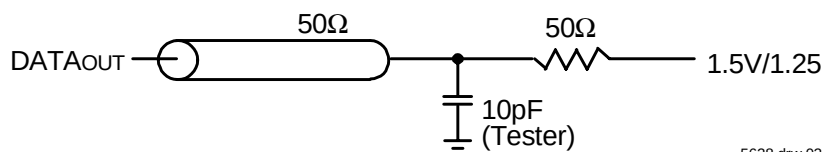
NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{CYC}$, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 3.3V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DDP}(f=0) = 120mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{DDQ} - 0.2V$
 $\overline{CE}_X \geq V_{DDQ} - 0.2V$ means $\overline{CE}_{0X} \geq V_{DDQ} - 0.2V$ or $CE_{1X} \leq 0.2V$
 "X" represents "L" for left port or "R" for right port.
- 166MHz Industrial Temperature not available in BF-208 package.
- This speed grade available when $V_{DDQ} = 3.3V$ for a specific port (i.e., $OPT_X = V_{IH}$). This speed grade is available in BC-256 only.

AC Test Conditions ($V_{DDQ} = 3.3V/2.5V$)

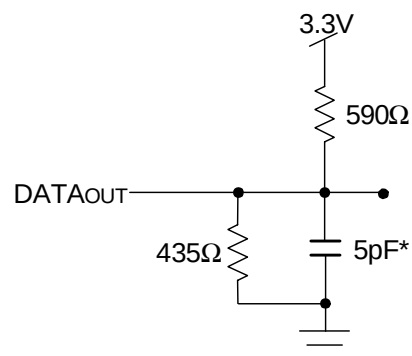
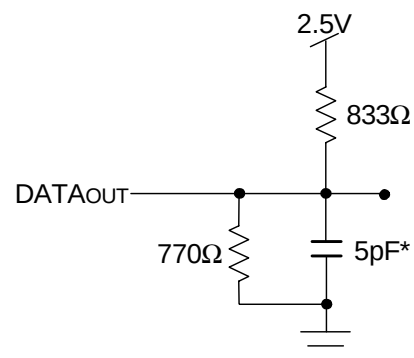
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figures 1 and 2

5628 tbl 10



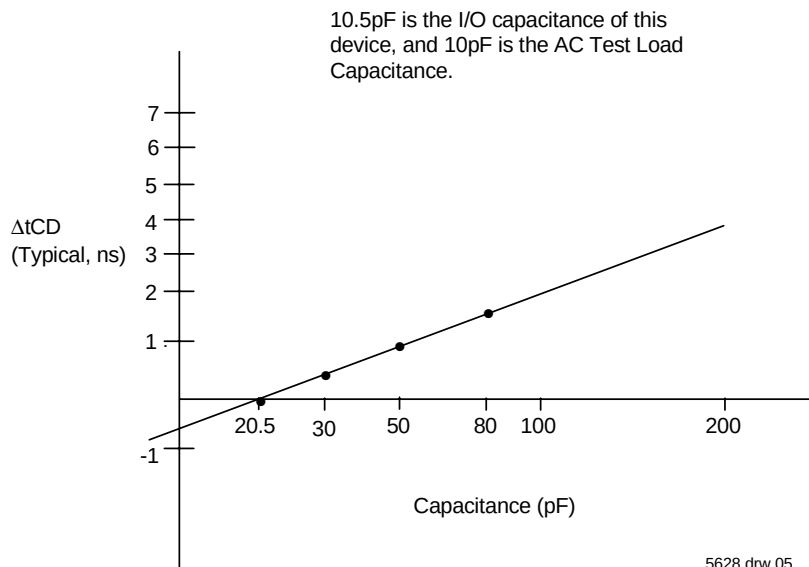
5628 drw 03

Figure 1. AC Output Test load.



5628 drw 04

Figure 2. Output Test Load
(For t_{CKLZ} , t_{CKHZ} , t_{OLZ} , and t_{OHZ}).
*Including scope and jig.



5628 drw 05

Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)^(2,3) ($V_{DD} = 3.3V \pm 150mV$, $T_A = 0^\circ C$ to $+70^\circ C$)

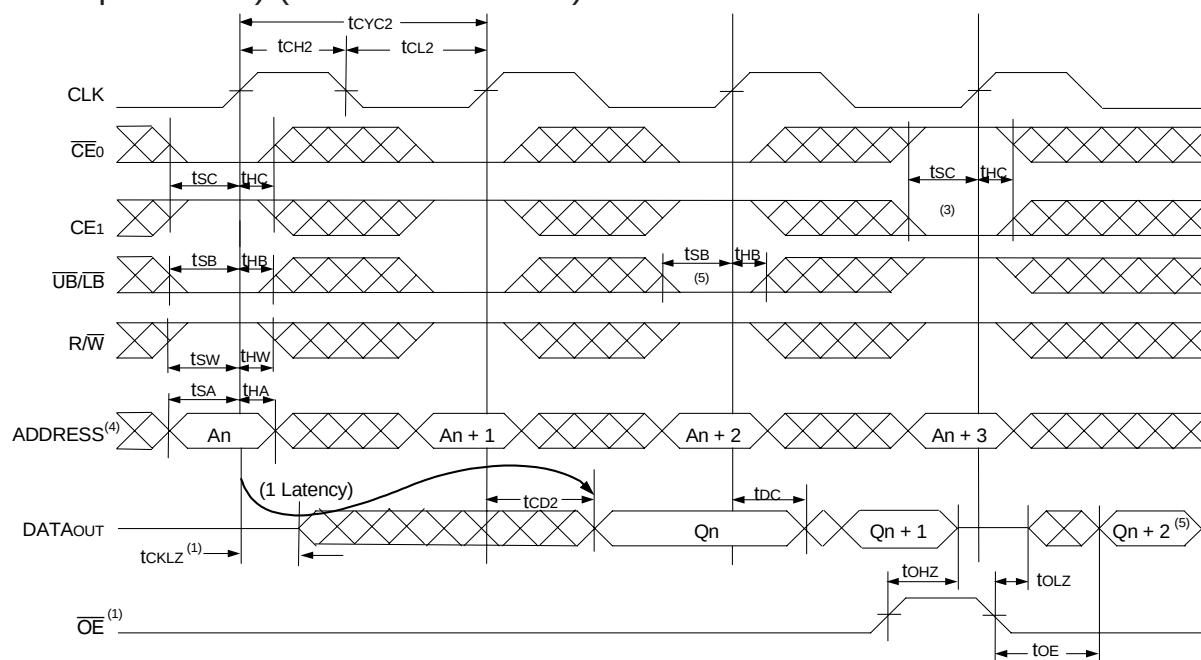
		70V7339S200 ⁽⁵⁾ Com'l Only		70V7339S166 ^(3,4) Com'l & Ind		70V7339S133 ⁽³⁾ Com'l & Ind		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
t _{CYC1}	Clock Cycle Time (Flow-Through) ⁽¹⁾	15	—	20	—	25	—	ns
t _{CYC2}	Clock Cycle Time (Pipelined) ⁽¹⁾	5	—	6	—	7.5	—	ns
t _{CH1}	Clock High Time (Flow-Through) ⁽¹⁾	5	—	6	—	7	—	ns
t _{CL1}	Clock Low Time (Flow-Through) ⁽¹⁾	5	—	6	—	7	—	ns
t _{CH2}	Clock High Time (Pipelined) ⁽²⁾	2.0	—	2.1	—	2.6	—	ns
t _{CL2}	Clock Low Time (Pipelined) ⁽¹⁾	2.0	—	2.1	—	2.6	—	ns
t _r	Clock Rise Time	—	1.5	—	1.5	—	1.5	ns
t _f	Clock Fall Time	—	1.5	—	1.5	—	1.5	ns
t _{SA}	Address Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SC}	Chip Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HC}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SB}	Byte Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HB}	Byte Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SW}	R/W Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HW}	R/W Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SD}	Input Data Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HD}	Input Data Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SAD}	$\overline{ADS}$ Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HAD}	$\overline{ADS}$ Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SCN}	$\overline{CNTEN}$ Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HCN}	$\overline{CNTEN}$ Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SRPT}	$\overline{REPEAT}$ Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HRPT}	$\overline{REPEAT}$ Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{OE}	Output Enable to Data Valid	—	4.0	—	4.0	—	4.2	ns
t _{OLZ}	Output Enable to Output Low-Z	0.5	—	0.5	—	0.5	—	ns
t _{OHZ}	Output Enable to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t _{CD1}	Clock to Data Valid (Flow-Through) ⁽¹⁾	—	10	—	12	—	15	ns
t _{CD2}	Clock to Data Valid (Pipelined) ⁽¹⁾	—	3.4	—	3.6	—	4.2	ns
t _{DC}	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t _{CKHZ}	Clock High to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t _{CKLZ}	Clock High to Output Low-Z	0.5	—	0.5	—	0.5	—	ns
Port-to-Port Delay								
t _{CO}	Clock-to-Clock Offset	5.0	—	6.0	—	7.5	—	ns

5628 tbl 11

NOTES:

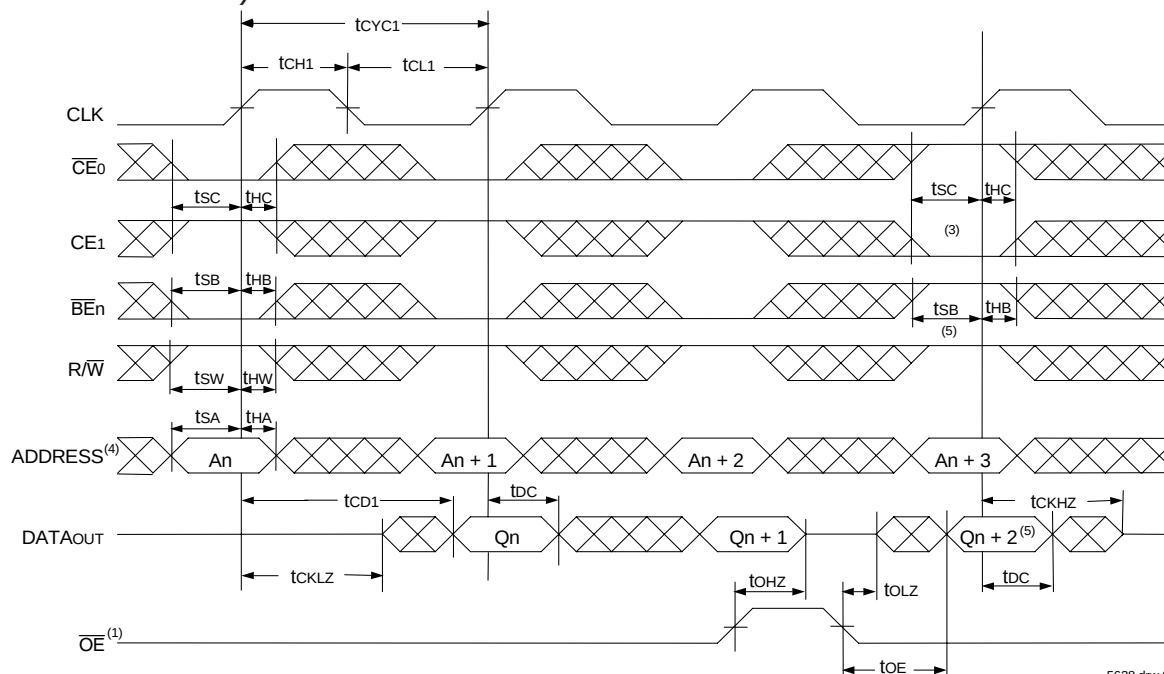
- The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}/PIPE_x = V_{IH}$. Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}/PIPE_x = V_{IL}$ for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ($\overline{OE}$) and $\overline{FT}/PIPE_x$. $\overline{FT}/PIPE_x$ should be treated as a DC signal, i.e. steady state during operation.
- These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 4 for details on selecting the desired operating voltage levels for each port.
- 166MHz Industrial Temperature not available in BF-208 package.
- This speed grade available when $V_{DDQ} = 3.3V$ for a specific port (i.e., $OPT_x = V_{IH}$). This speed grade available in BC-256 package only.

Timing Waveform of Read Cycle for Pipelined Operation ($\overline{\text{ADS}}$ Operation) ($\overline{\text{FT}}/\text{PIPE}'X' = V_{IH}$)⁽²⁾



5628 drw 06

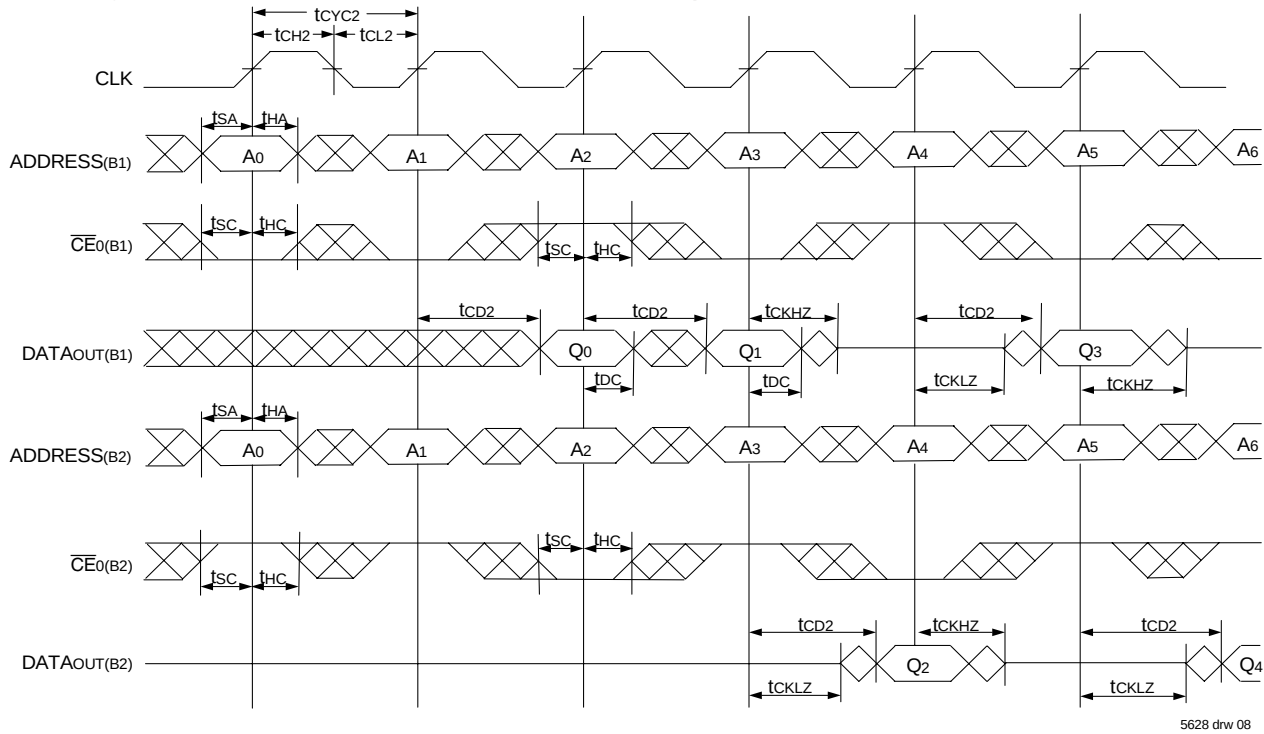
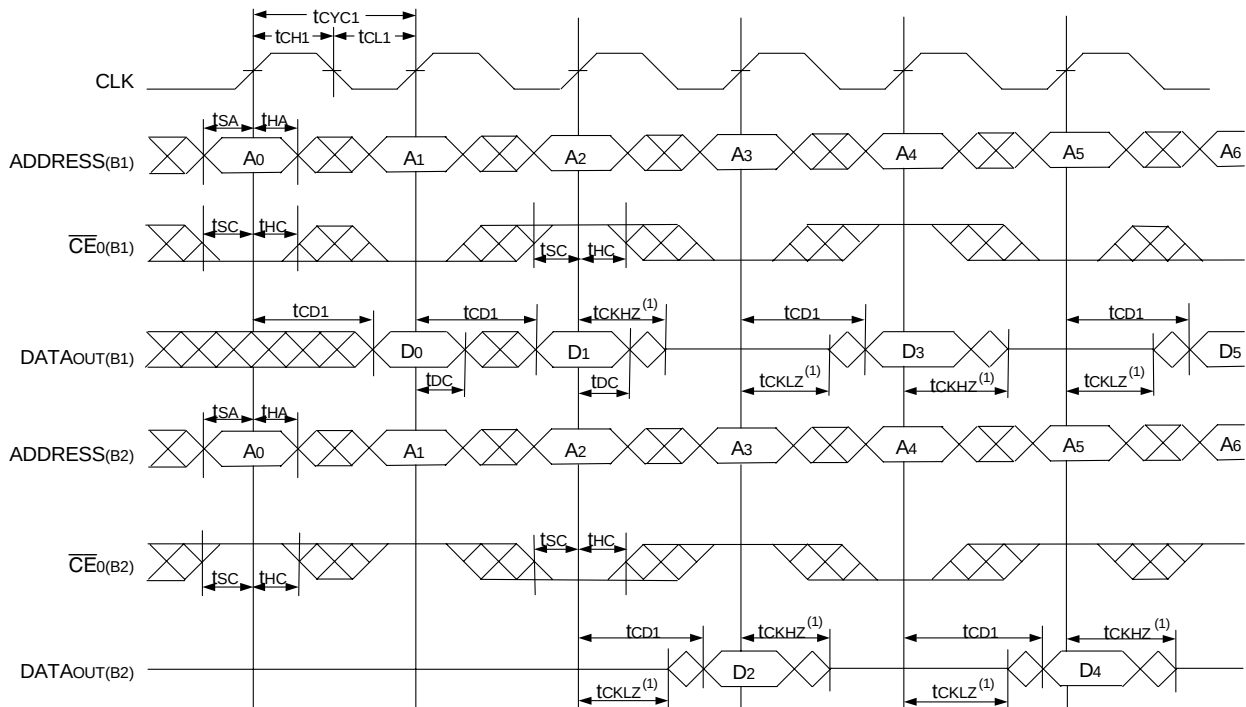
Timing Waveform of Read Cycle for Flow-through Output ($\overline{\text{FT}}/\text{PIPE}'X' = V_{IL}$)^(2,6)



5628 drw 07

NOTES:

1. $\overline{\text{OE}}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
2. $\overline{\text{ADS}} = V_{IL}$, CNTEN and $\text{REPEAT} = V_{IH}$.
3. The output is disabled (High-Impedance state) by $\overline{\text{CE}}_0 = V_{IH}$, $\text{CE}_1 = V_{IL}$, $\overline{\text{UB}}/\overline{\text{LB}} = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
4. Addresses do not have to be accessed sequentially since $\overline{\text{ADS}} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. If $\overline{\text{UB}}/\overline{\text{LB}}$ was HIGH, then the appropriate Byte of DATAout for Q_{n+2} would be disabled (High-Impedance state).
6. "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Multi-Device Pipelined Read^(1,2)Timing Waveform of a Multi-Device Flow-Through Read^(1,2)

NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70V7339 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. UB/LB, OE, and ADS = V_{IL}; CE1(B1), CE1(B2), R/W, CNTEN, and REPEAT = V_{IH}.

The diagram illustrates the timing relationships for a dual-channel memory device. It shows two channels, A and B, each with its own clock (CLK_A, CLK_B), read/write strobe (R/W_A, R/W_B), bank address and address (An), and data input/output (Dn). Key timing parameters are indicated: t_{SW} and t_{HW} for strobe setup and hold; t_{SA} and t_{HA} for address setup and hold; t_{SD} and t_{HD} for data setup and hold; $t_{co(3)}$ for clock-to-output delay; t_{CD2} for clock-to-data delay; and t_{OC} for output delay. The signals are represented by waveforms with cross-hatching for high/active periods.

The diagram illustrates the timing relationships for a dual-channel memory device. It shows two channels, A and B, each with its own clock (CLK "A" and CLK "B"), read/write control (R/W "A" and R/W "B"), bank address (An), and data bus (DATAIN "A" and DATAOUT "B").

Channel A Timing:

- Read Operation:** The R/W "A" signal transitions from high to low. The bank address An is valid for a duration t_{SA} before the R/W transition and t_{HA} after. The data Dn is valid for t_{SD} before and t_{HD} after the R/W transition.
- Write Operation:** The R/W "A" signal transitions from low to high. The bank address An is valid for t_{SA} before and t_{HA} after. The data Dn is valid for t_{SD} before and t_{HD} after.
- Refresh:** The R/W "A" signal transitions from high to high (no change). The bank address An is valid for t_{SA} before and t_{HA} after. The data Dn is valid for t_{SD} before and t_{HD} after.
- Refresh:** The R/W "A" signal transitions from low to low (no change). The bank address An is valid for t_{SA} before and t_{HA} after. The data Dn is valid for t_{SD} before and t_{HD} after.

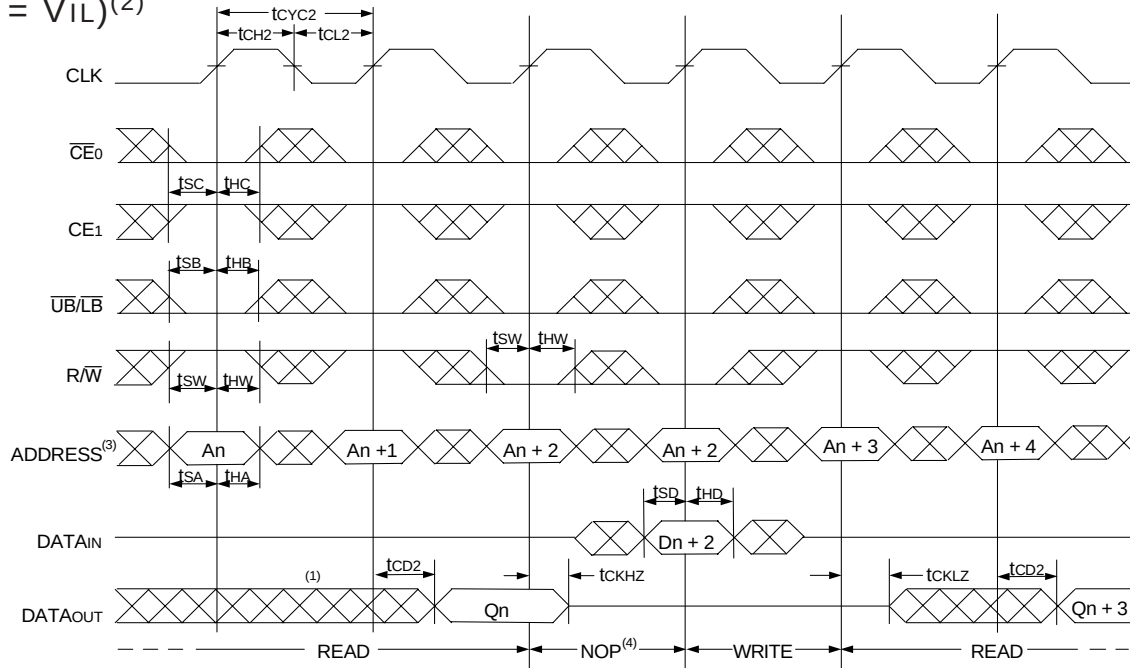
Channel B Timing:

- Read Operation:** The R/W "B" signal transitions from high to low. The bank address An is valid for t_{SA} before and t_{HA} after. The data Dn is valid for t_{SD} before and t_{HD} after.
- Write Operation:** The R/W "B" signal transitions from low to high. The bank address An is valid for t_{SA} before and t_{HA} after. The data Dn is valid for t_{SD} before and t_{HD} after.
- Refresh:** The R/W "B" signal transitions from high to high (no change). The bank address An is valid for t_{SA} before and t_{HA} after. The data Dn is valid for t_{SD} before and t_{HD} after.
- Refresh:** The R/W "B" signal transitions from low to low (no change). The bank address An is valid for t_{SA} before and t_{HA} after. The data Dn is valid for t_{SD} before and t_{HD} after.

Timing Parameters:

- t_{sw} : Setup time for R/W signal before the clock edge.
- t_{hw} : Hold time for R/W signal after the clock edge.
- t_{sa} : Setup time for bank address before the R/W signal transition.
- t_{ha} : Hold time for bank address after the R/W signal transition.
- t_{sd} : Setup time for data before the R/W signal transition.
- t_{hd} : Hold time for data after the R/W signal transition.
- $t_{CO(3)}$: Refresh period for channel A.
- t_{CD1} : Refresh period for channel B.
- t_{DC} : Refresh period for channel A.
- t_{DC} : Refresh period for channel B.

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾

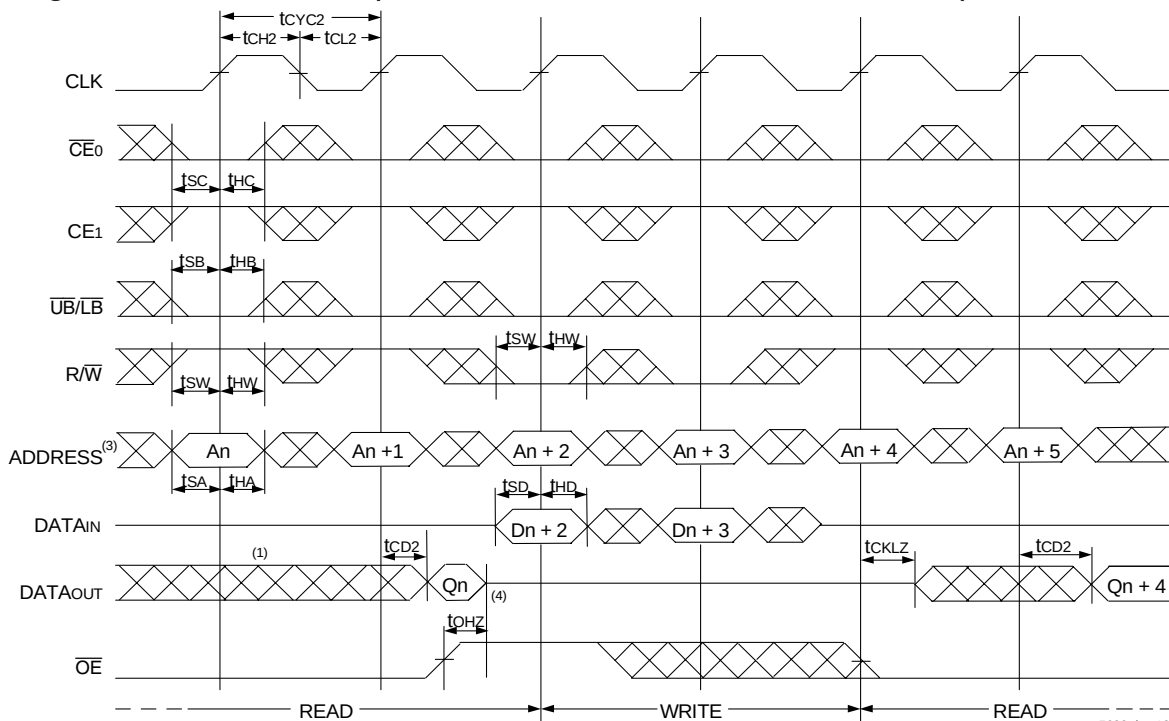


NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{BE}_n$, and $\overline{ADS} = V_{IL}$; $\overline{CE}_1$, $\overline{CNTEN}$, and $\overline{REPEAT} = V_{IH}$. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

5628 drw 12

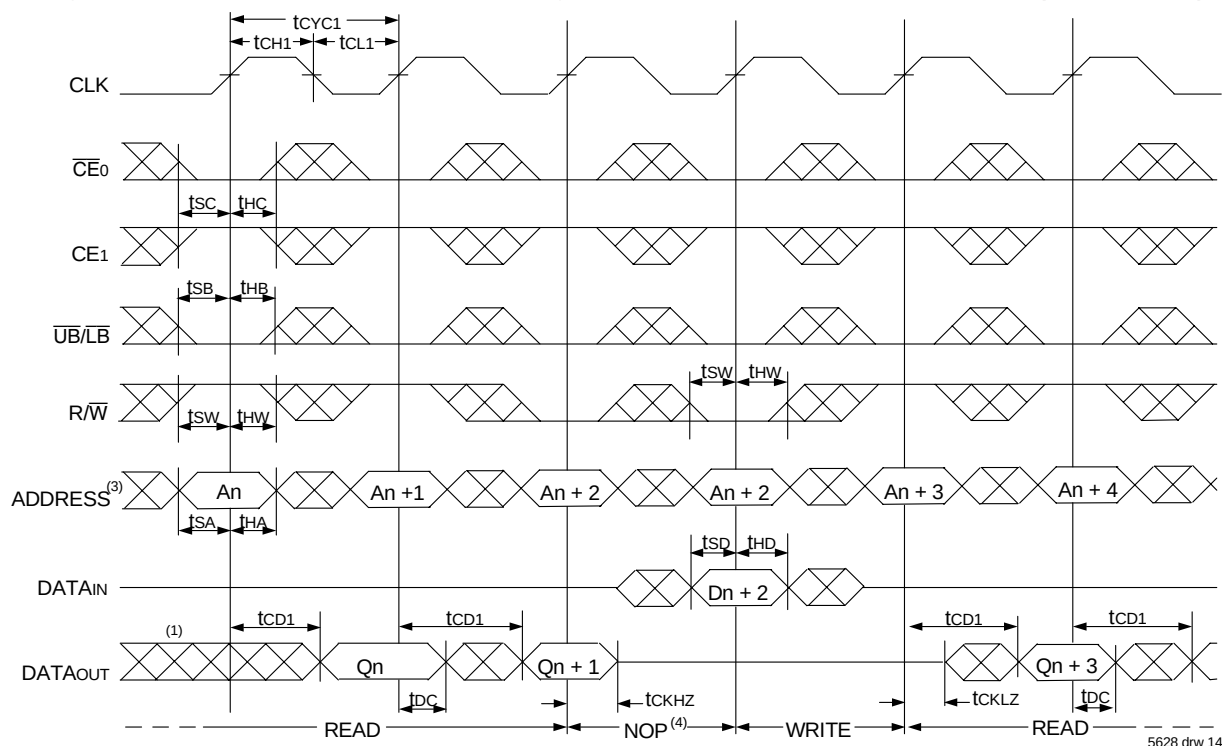
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)⁽²⁾



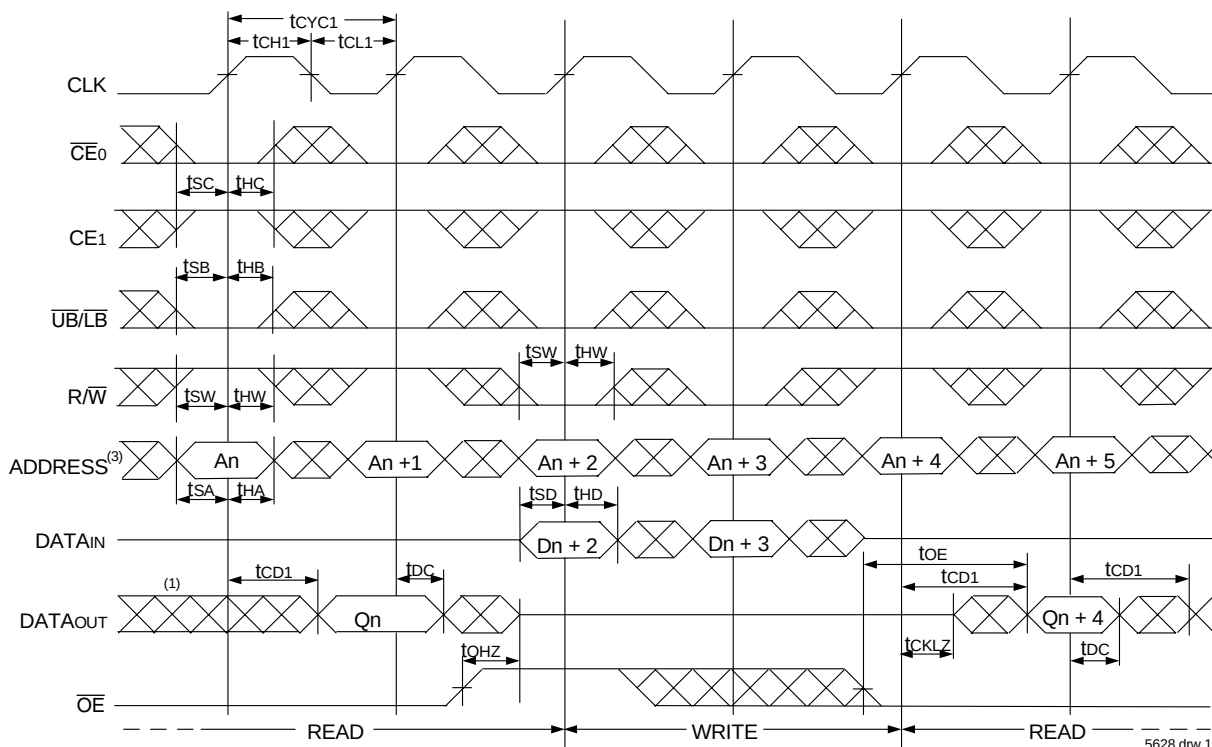
NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{UB/LB}$, and $\overline{ADS} = V_{IL}$; $\overline{CE}_1$, $\overline{CNTEN}$, and $\overline{REPEAT} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

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Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾

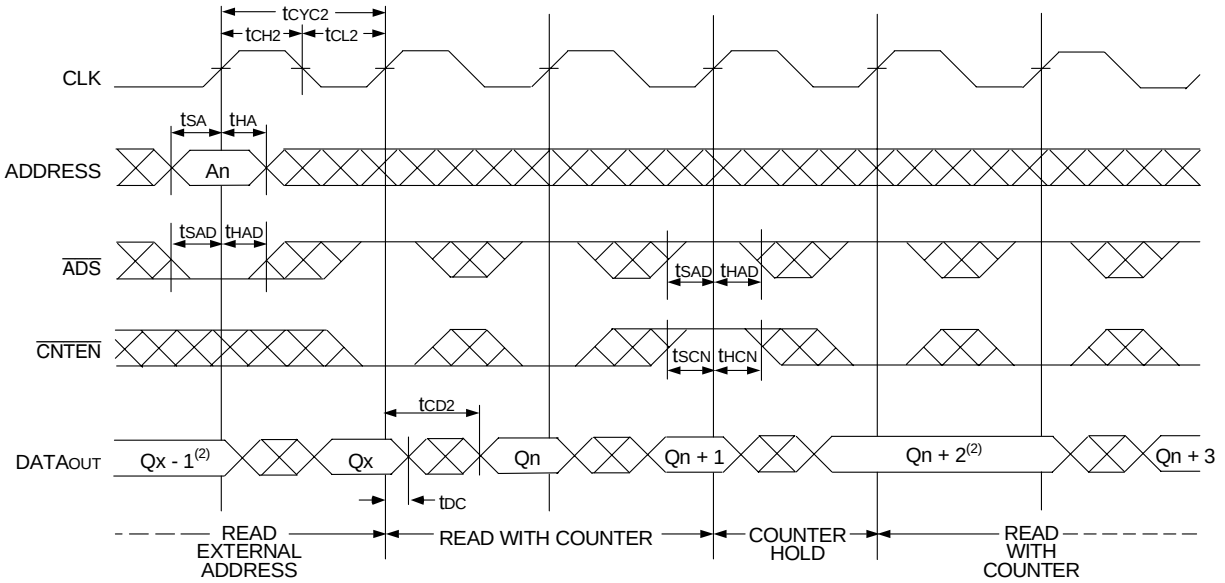
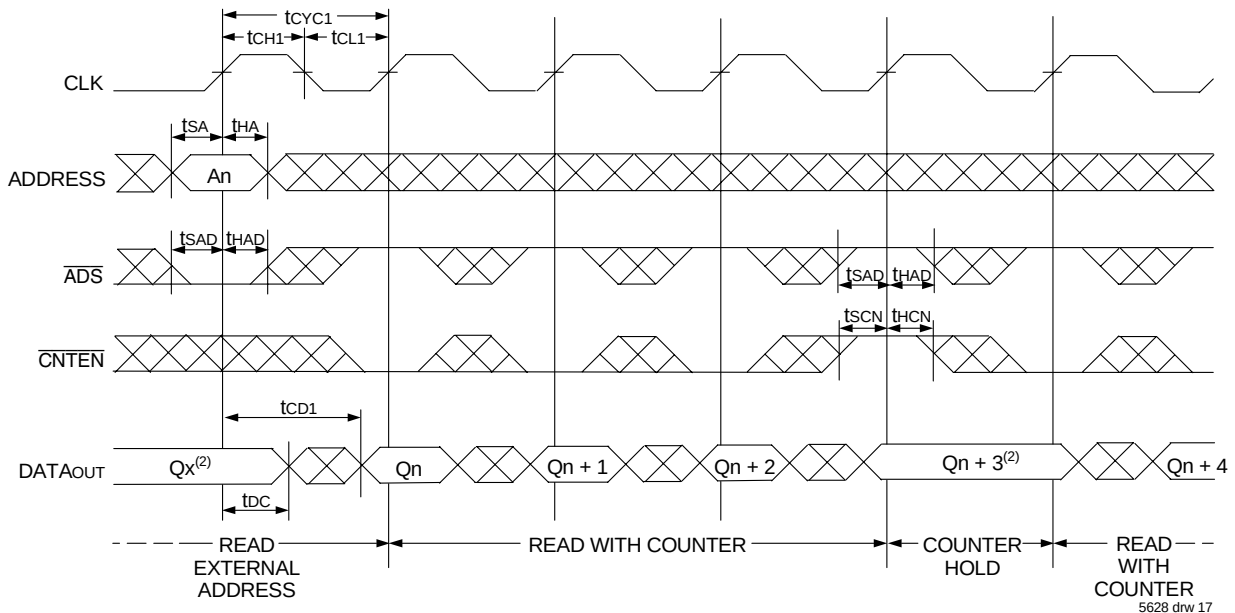
5628 drw 14

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)⁽²⁾

5628 drw 15

NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}_0$, $\overline{UB/LB}$, and $\overline{ADS} = V_{IL}$; $\overline{CE}_1$, $\overline{CNTEN}$, and $\overline{REPEAT} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

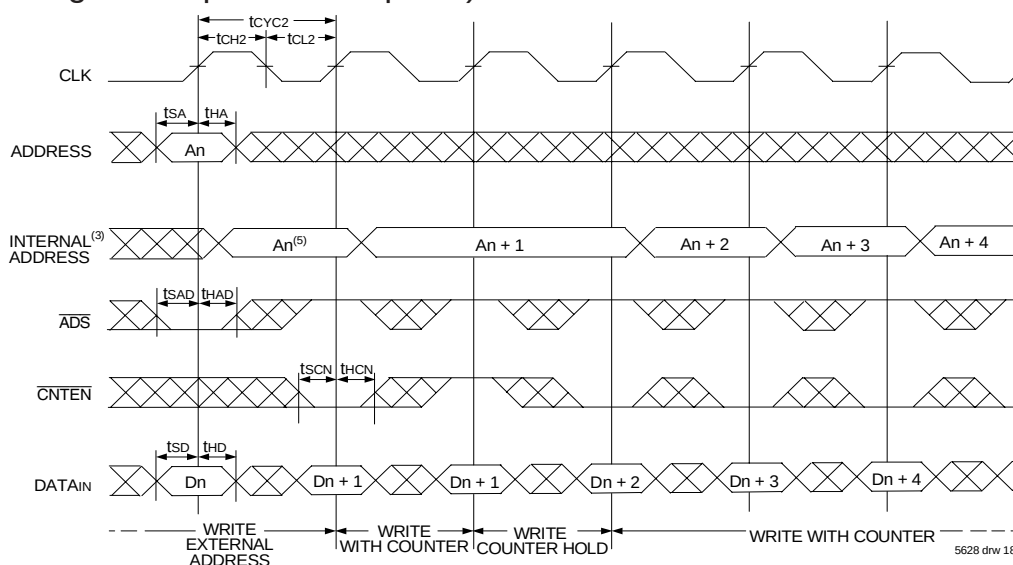
Timing Waveform of Pipelined Read with Address Counter Advance⁽¹⁾Timing Waveform of Flow-Through Read with Address Counter Advance⁽¹⁾

NOTES:

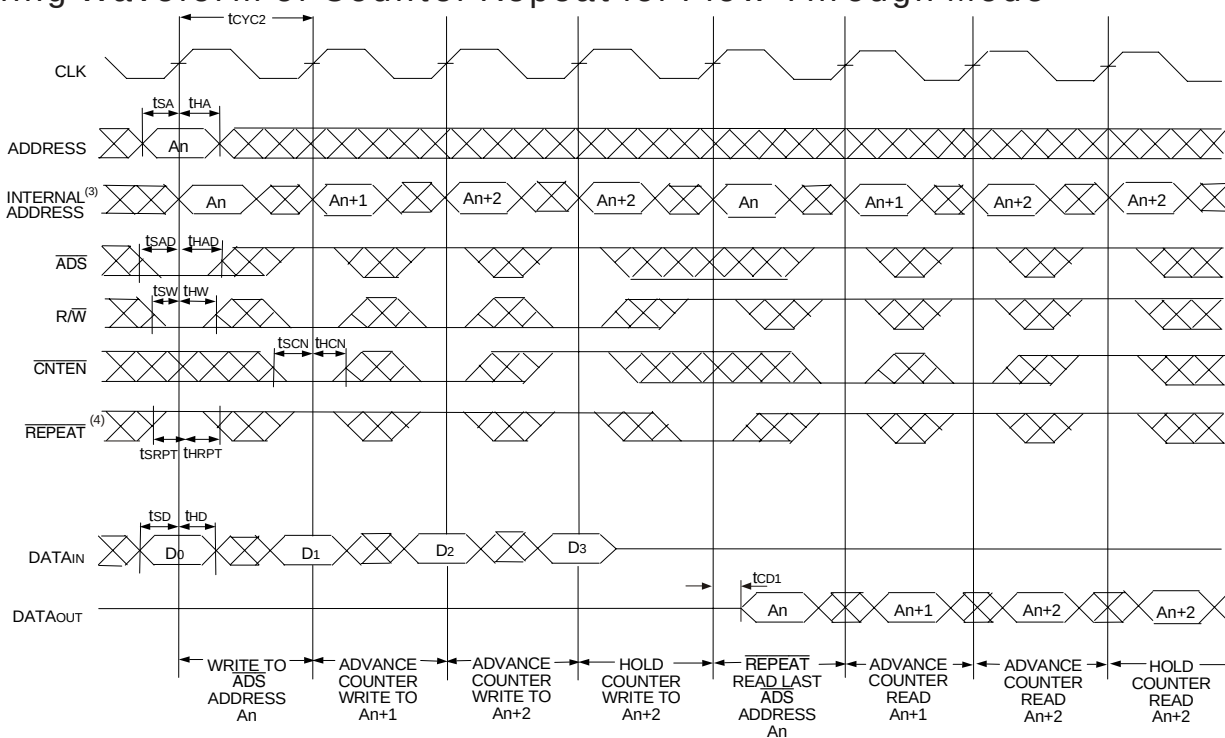
1. $\overline{CE_0}$, $\overline{OE}$, $\overline{UB/LB} = V_{IL}$; $\overline{CE_1}$, $\overline{R/W}$, and $\overline{REPEAT} = V_{IH}$.

2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs)^(1,6)



Timing Waveform of Counter Repeat for Flow Through Mode^(2,6,7)



NOTES:

1. $\overline{CE_0}$, $\overline{UB/LB}$, and $R/\overline{W} = V_{IL}$; CE_1 and $\overline{REPEAT} = V_{IH}$.
2. $\overline{CE_0}$, $\overline{UB/LB} = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. No dead cycle exists during $\overline{REPEAT}$ operation. A READ or WRITE cycle may be coincidental with the counter $\overline{REPEAT}$ cycle: Address loaded by last valid $\overline{ADS}$ load will be accessed. For more information on $\overline{REPEAT}$ function refer to Truth Table II.
5. $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An+1'. The transition shown indicates the time required for the counter to advance. The 'An+1' Address is written to during this cycle.
6. The counter includes bank address and internal address. The counter will advance across bank boundaries. For example, if the counter is in Bank 0, at address FFFh, and is advanced one location, it will move to address 0h in Bank 1. By the same token, the counter at FFFh in Bank 63 will advance to 0h in Bank 0.
7. For Pipelined Mode user should add 1 cycle latency for outputs as per timing waveform of read cycle for pipelined operations.

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Functional Description

The IDT70V7339 is a high-speed 512Kx18 (9 Mbit) synchronous Bank-Switchable Dual-Ported SRAM organized into 64 independent 8Kx18 banks. Based on a standard SRAM core instead of a traditional true dual-port memory core, this bank-switchable device offers the benefits of increased density and lower cost-per-bit while retaining many of the features of true dual-ports. These features include simultaneous, random access to the shared array, separate clocks per port, 166 MHz operating speed, full-boundary counters, and pinouts compatible with the IDT70V3319 (256Kx18) dual-port family.

The two ports are permitted independent, simultaneous access into separate banks within the shared array. Access by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory with the shared array that is not currently being accessed by the opposite port (i.e., $BA_{0L} - BA_{5L} \neq BA_{0R} - BA_{5R}$). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the ports within that bank may be corrupted (in the case that either or both ports are writing) or may result in invalid output (in the case that both ports are trying to read).

The IDT70V7339 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal setup and hold times on address, data and all critical control inputs.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on $\overline{CE_0}$ or a LOW on CE_1 for one clock cycle will power down the internal circuitry on each port (individually controlled) to reduce static power consumption. Dual chip enables allow easier banking of multiple IDT70V7339s for depth expansion configurations. Two cycles are required with $\overline{CE_0}$ LOW and CE_1 HIGH to read valid data on the outputs.

Depth and Width Expansion

The IDT70V7339 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70V7339 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 36-bits or wider.

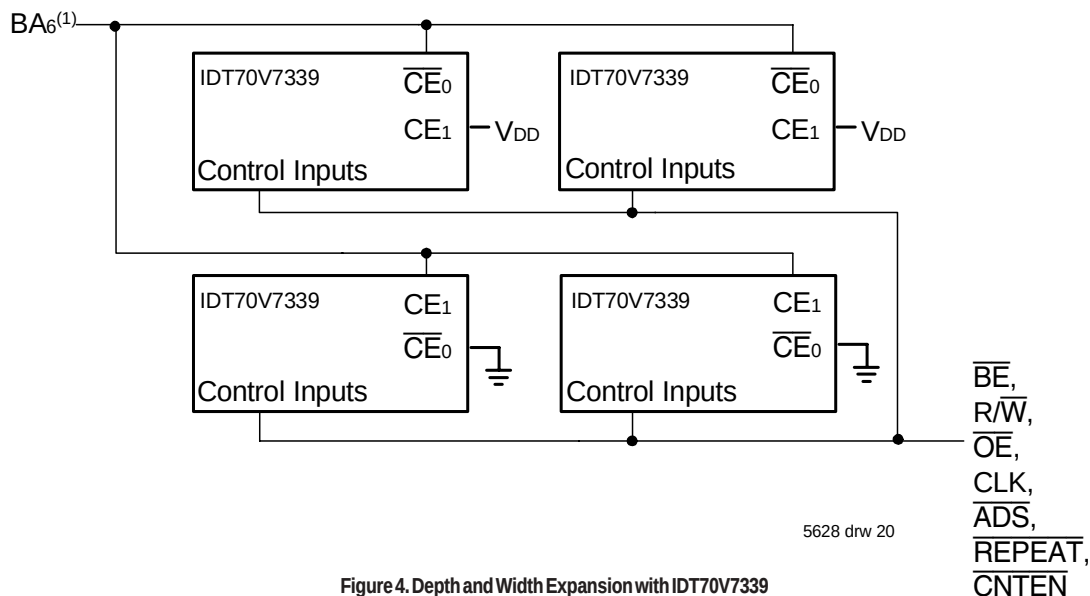


Figure 4. Depth and Width Expansion with IDT70V7339

NOTE:

1. In the case of depth expansion, the additional address pin logically serves as an extension of the bank address. Accesses by the ports into specific banks are controlled by the bank address pins under the user's direct control: each port can access any bank of memory within the shared array that is not currently being accessed by the opposite port (i.e., $BA_{0L} - BA_{6L} \neq BA_{0R} - BA_{6R}$). In the event that both ports try to access the same bank at the same time, neither access will be valid, and data at the two specific addresses targeted by the parts within that bank may be corrupted (in the case that either or both parts are writing) or may result in invalid output (in the case that both ports are trying to read).

JTAG Timing Specifications

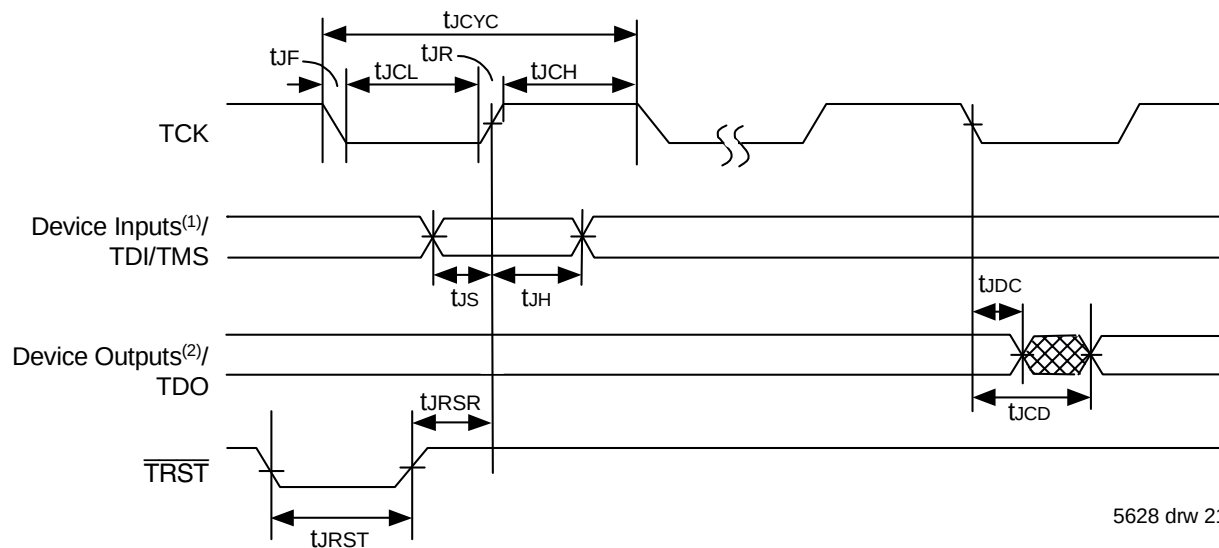


Figure 5. Standard JTAG Timing

NOTES:

1. Device inputs = All device inputs except TDI, TMS, TRST, and TCK.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics^(1,2,3,4)

Symbol	Parameter	70V7339		
		Min.	Max.	Units
t _{JCYC}	JTAG Clock Input Period	100	—	ns
t _{JCH}	JTAG Clock HIGH	40	—	ns
t _{JCL}	JTAG Clock Low	40	—	ns
t _{JR}	JTAG Clock Rise Time	—	3 ⁽¹⁾	ns
t _{JF}	JTAG Clock Fall Time	—	3 ⁽¹⁾	ns
t _{JRST}	JTAG Reset	50	—	ns
t _{JRSR}	JTAG Reset Recovery	50	—	ns
t _{JCD}	JTAG Data Output	—	25	ns
t _{JDC}	JTAG Data Output Hold	0	—	ns
t _{JS}	JTAG Setup	15	—	ns
t _{JH}	JTAG Hold	15	—	ns

5628 tbl 12

NOTES:

1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x301	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

5628 tbl 13

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

5628 tbl 14

System Interface Parameters

Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs ⁽¹⁾ . Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.
CLAMP	0011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs ⁽²⁾ and outputs ⁽¹⁾ to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	All other codes	Several combinations are reserved. Do not use codes other than those identified above.

5628 tbl 15

NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, TRST, and TCK.
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information

XXXXX	A	999	A	A	A	A		
Device Type	Power	Speed	Package		Process/ Temperature Range			
							Blank 8	Tube of Tray Tape and Reel
							Blank 1 ⁽⁴⁾	Commercial (0°C to +70°C) Industrial (-40°C to +85°C)
							G ⁽³⁾	Green
							BF BC	208-pin fpBGA (BF208) 256-pin BGA (BC256)
							200 166 133	Commercial Only ⁽¹⁾ Commercial & Industrial ⁽²⁾ Commercial & Industrial
							S	Standard Power
							70V7339	9Mbit (512K x 18-Bit) Synchronous Bank-Switchable Dual-Port RAM

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NOTES:

1. Available in BC-256 package only.
2. Industrial Temperature at 166MHz not available in the BF-208 package.
3. Green parts available. For specific speeds, packages and powers contact your local sales office.
4. Contact your local sales office for industrial temp range for other speeds, packages and powers

LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Datasheet Document History

01/05/00:	Initial Public Offering
06/20/01:	Page 1 Added JTAG information for TQFP package Page 4 & 22 Changed TQFP package from DA to DD Corrected Pin number on TQFP package from 100 to 110 Page 20 Increased t_{DCD} from 20ns to 25ns
08/06/01:	Page 4 Changed body size for DD package from 22mm x 22mm x 1.6mm to 20mm x 20mm x 1.4mm Page 9 Changed I_{SB3} values for commercial and industrial DC Electrical Characteristics
11/20/01:	Page 2, 3 & 4 Added date revision for pin configurations Page 11 Changed t_{OE} value in AC Electrical Characteristics, please refer to Errata #SMEN-01-05 Page 1 & 22 Replaced TM logo with ® logo
03/18/02:	Page 1, 9, 11 & 22 Added 200MHZ specification Page 9 Tightened power numbers in DC Electrical Characteristics Page 14 Changed waveforms to show INVALID operation if $t_{\text{CO}} < \text{minimum specified}$ Page 1 - 22 Removed "Preliminary" status
12/04/02:	Page 9, 11 & 22 Designated 200Mhz speed grade in BC-256 package only
01/16/04:	Page 11 Added byte enable setup time and byte enable hold time parameters and values to all speed grades in the AC Electrical Characteristics Table
07/25/08:	Page 9 Corrected a typo in the DC Chars table
01/29/09:	Page 22 Removed "IDT" from orderable part number

Datasheet Document History (con't)

04/20/10: Page 1 Added green availability to features
Page 21 Added green indicator to ordering information
Removed the DD 144-pin TQFP (DD-144) Thin Quad Flatpack per PDN: F-08-01

08/11/15: Page 2 & 3 Removed the date from all of the pin configurations BF208 & BC256
Page 21 Added T&R indicator and updated footnotes for Ordering Information

06/22/18: Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018

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