

8-Bit

# XC87xCLM

8-Bit Single-Chip Microcontroller

Data Sheet V1.5 2011-03

Microcontrollers

Edition 2011-03

Published by
Infineon Technologies AG
81726 Munich, Germany
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Microcontrollers



#### XC87x Data Sheet

Revision History: V1.5 2011-03

Previous Versions: V1.4

Subjects (major changes since last revision) Page

Changes from V1.4 2010-08 to V1.5 2011-03

A new variant, SAF-XC874CM-13FVA 5V, has been added in Table 2. Page 3

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## **8-Bit Single-Chip Microcontroller**

XC87xCLM

## 1 Summary of Features

The XC87x has the following features:

- · High-performance XC800 Core
  - compatible with standard 8051 processor
  - two clocks per machine cycle architecture (for memory access without wait state)
  - two data pointers
- · On-chip memory
  - 8 Kbytes of Boot ROM
  - 256 bytes of RAM
  - 3 Kbytes of XRAM
  - 64/52 Kbytes of Flash;
     (includes memory protection strategy)
- I/O port supply at 3.3 V or 5.0 V and core logic supply at 2.5 V (generated by embedded voltage regulator)

(more features on next page)

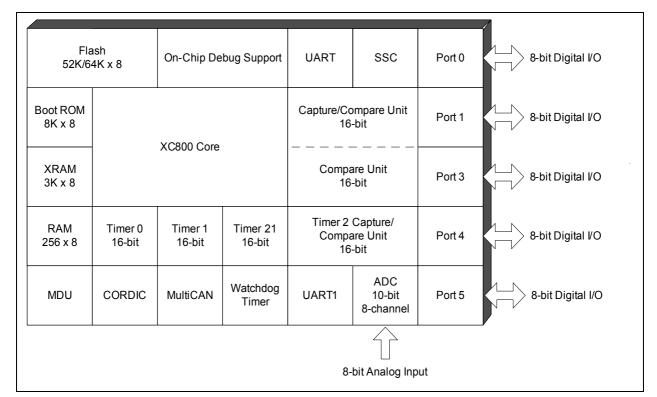


Figure 1 XC87x Functional Units



#### Features: (continued)

- Power-on reset generation
- Brownout detection for core logic supply
- On-chip OSC and PLL for clock generation
  - Loss-of-Clock detection
- Power saving modes
  - slow-down mode
  - idle mode
  - power-down mode with wake-up capability via RXD or EXINTO<sup>1)</sup>
  - clock gating control to each peripheral
- Programmable 16-bit Watchdog Timer (WDT)
- Five ports
  - Up to 40 pins as digital I/O
  - 8 dedicated analog inputs used as A/D converter input
- 8-channel, 10-bit ADC
- Four 16-bit timers
  - Timer 0 and Timer 1 (T0 and T1)
  - Timer 2 and Timer 21 (T2 and T21)
- Multiplication/Division Unit for arithmetic operations (MDU)
- CORDIC Coprocessor for computation of trigonometric, hyperbolic and linear functions
- MultiCAN with 2 nodes, 32 message objects
- Two Capture/compare units
  - Capture/compare unit 6 for PWM signal generation (CCU6)
  - Timer 2 Capture/compare unit for vaious digital signal generation (T2CCU)
- Two full-duplex serial interfaces (UART and UART1)
- Synchronous serial channel (SSC)
- On-chip debug support
  - 1 Kbyte of monitor ROM (part of the 8-Kbyte Boot ROM)
  - 64 bytes of monitor RAM
- Packages:
  - PG-LQFP-64
  - PG-VQFN-48
- Temperature range T<sub>△</sub>:
  - SAF (-40 to 85 °C)
  - SAX (-40 to 105 °C)
  - SAK (-40 to 125 °C)

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<sup>1)</sup> SAK product variant does not support power-down mode.



#### XC87x Variant Devices

The XC87x product family features devices with different configurations, program memory sizes, package options, power supply voltage, temperature and quality profiles (Automotive or Industrial), to offer cost-effective solutions for different application requirements.

The list of XC87x device configurations are summarized in **Table 1**. 2 types of packages are available :

- PG-LQFP-64, which is denoted by XC878 and;
- PG-VQFN-48, which is denoted by XC874

Table 1 Device Configuration

Device Name	CAN Module	LIN BSL Support	MDU Module
XC87x	No	No	No
XC87xM	No	No	Yes
XC87xCM	Yes	No	Yes
XC87xLM	No	Yes	Yes
XC87xCLM	Yes	Yes	Yes

From these 5 different combinations of configuration, each are further made available in many sales types, which are grouped according to device type, program memory sizes, power supply voltage, temperature and quality profiles (Automotive or Industrial), as shown in **Table 2**.

Table 2 Device Profile

Sales Type	Device Type	Program Memory (Kbytes)	Power Supply (V)	Temp- erature (°C)	Quality Profile
SAF-XC878-13FFI 5V	Flash	52	5.0	-40 to 85	Industrial
SAF-XC878M-13FFI 5V	Flash	52	5.0	-40 to 85	Industrial
SAF-XC878CM-13FFI 5V	Flash	52	5.0	-40 to 85	Industrial
SAF-XC878-16FFI 5V	Flash	64	5.0	-40 to 85	Industrial
SAF-XC878M-16FFI 5V	Flash	64	5.0	-40 to 85	Industrial
SAF-XC878CM-16FFI 5V	Flash	64	5.0	-40 to 85	Industrial
SAF-XC878-13FFI 3V3	Flash	52	3.3	-40 to 85	Industrial
SAF-XC878M-13FFI 3V3	Flash	52	3.3	-40 to 85	Industrial



Table 2 Device Profile (cont'd)

Sales Type	Device Type	Program Memory (Kbytes)	Power Supply (V)	Temp- erature (°C)	Quality Profile
SAF-XC878CM-13FFI 3V3	Flash	52	3.3	-40 to 85	Industrial
SAF-XC878-16FFI 3V3	Flash	64	3.3	-40 to 85	Industrial
SAF-XC878M-16FFI 3V3	Flash	64	3.3	-40 to 85	Industrial
SAF-XC878CM-16FFI 3V3	Flash	64	3.3	-40 to 85	Industrial
SAF-XC878-13FFA 5V	Flash	52	5.0	-40 to 85	Automotive
SAF-XC878CM-13FFA 5V	Flash	52	5.0	-40 to 85	Automotive
SAF-XC878LM-13FFA 5V	Flash	52	5.0	-40 to 85	Automotive
SAF-XC878CLM-13FFA 5V	Flash	52	5.0	-40 to 85	Automotive
SAF-XC878-16FFA 5V	Flash	64	5.0	-40 to 85	Automotive
SAF-XC878CM-16FFA 5V	Flash	64	5.0	-40 to 85	Automotive
SAF-XC878LM-16FFA 5V	Flash	64	5.0	-40 to 85	Automotive
SAF-XC878CLM-16FFA 5V	Flash	64	5.0	-40 to 85	Automotive
SAX-XC878-13FFA 5V	Flash	52	5.0	-40 to 105	Automotive
SAX-XC878CM-13FFA 5V	Flash	52	5.0	-40 to 105	Automotive
SAX-XC878LM-13FFA 5V	Flash	52	5.0	-40 to 105	Automotive
SAX-XC878CLM-13FFA 5V	Flash	52	5.0	-40 to 105	Automotive
SAX-XC878-16FFA 5V	Flash	64	5.0	-40 to 105	Automotive
SAX-XC878CM-16FFA 5V	Flash	64	5.0	-40 to 105	Automotive
SAX-XC878LM-16FFA 5V	Flash	64	5.0	-40 to 105	Automotive
SAX-XC878CLM-16FFA 5V	Flash	64	5.0	-40 to 105	Automotive
SAK-XC878-13FFA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC878CM-13FFA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC878LM-13FFA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC878CLM-13FFA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC878-16FFA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC878CM-16FFA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC878LM-16FFA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC878CLM-16FFA 5V	Flash	64	5.0	-40 to 125	Automotive
SAF-XC874LM-16FVA 5V	Flash	64	5.0	-40 to 85	Automotive



**Table 2 Device Profile** (cont'd)

Sales Type	Device Type	Program Memory (Kbytes)	Power Supply (V)	Temp- erature (°C)	Quality Profile
SAF-XC874CM-16FVA 5V	Flash	64	5.0	-40 to 85	Automotive
SAF-XC874CM-13FVA 5V	Flash	52	5.0	-40 to 85	Automotive
SAK-XC874LM-16FVA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC874CM-16FVA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC874-16FVA 5V	Flash	64	5.0	-40 to 125	Automotive
SAK-XC874LM-13FVA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC874CM-13FVA 5V	Flash	52	5.0	-40 to 125	Automotive
SAK-XC874-13FVA 5V	Flash	52	5.0	-40 to 125	Automotive

As this document refers to all the derivatives, some description may not apply to a specific product. For simplicity, all versions are referred to by the term XC87x throughout this document.

#### **Ordering Information**

The ordering code for Infineon Technologies microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery

For the available ordering codes for the XC87x, please refer to your responsible sales representative or your local distributor.



## 2 General Device Information

**Chapter 2** contains the block diagram, pin configurations, definitions and functions of the XC87x.

## 2.1 Block Diagram

The block diagram of the XC87x is shown in Figure 2.

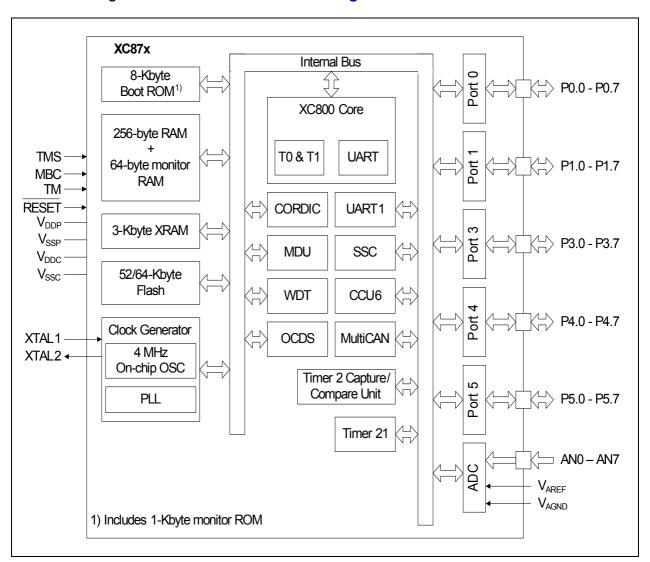


Figure 2 XC87x Block Diagram



## 2.2 Logic Symbol

The logic symbols of the XC878 and XC874 are shown in Figure 3.

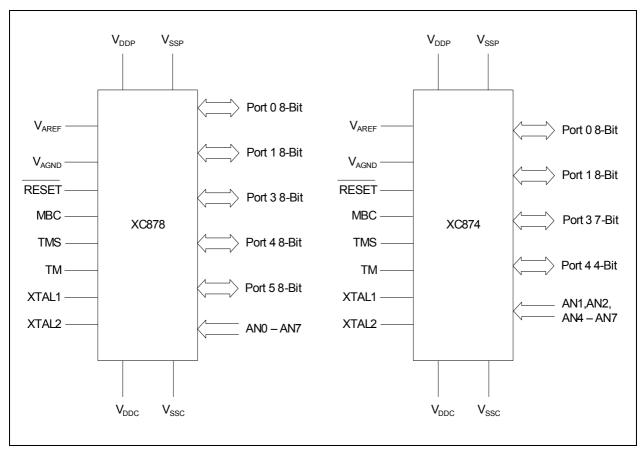


Figure 3 XC878 and XC874 Logic Symbol



## 2.3 Pin Configuration

The pin configuration of the XC878, which is based on the PG-LQFP-64, is shown in **Figure 4**, while that of the XC874, which is based on the PG-VQFN-48 package, is shown in **Figure 5**.

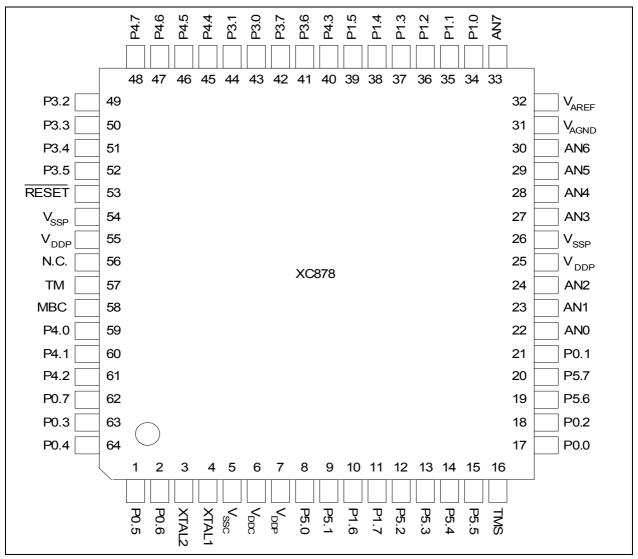


Figure 4 XC878 Pin Configuration, PG-LQFP-64 Package (top view)



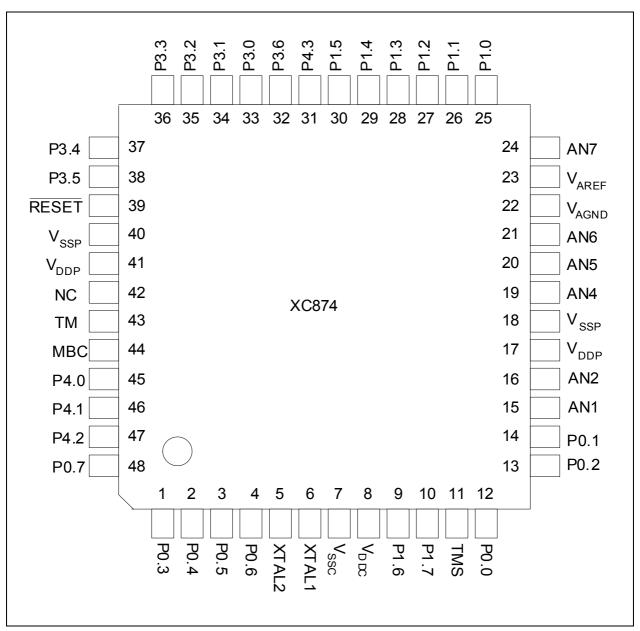


Figure 5 XC874 Pin Configuration, PG-VQFN-48 Package (top view)



## 2.4 Pin Definitions and Functions

The functions and default states of the XC87x external pins are provided in Table 3.

 Table 3
 Pin Definitions and Functions

Symbol	Pin Number (LQFP-64 / VQFN-48)	Туре	Reset State	Function		
P0		I/O		Port 0 Port 0 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, UART1, T2CCU, Timer 21, MultiCAN, SSC and External Bus Interface.  Note: External Bus Interface is not available in XC874.		
P0.0	17/12		Hi-Z	TCK_0 T12HR_1 CC61_1 CLKOUT_0 RXDO_1	CCU6 Timer 12 Hardware Run Input Input/Output of Capture/Compare channel 1	
P0.1	21/14		Hi-Z	TDI_0 T13HR_1 RXD_1 RXDC1_0 COUT61_1 EXF2_1	JTAG Serial Data Input CCU6 Timer 13 Hardware Run Input UART Receive Data Input MultiCAN Node 1 Receiver Input Output of Capture/Compare channel 1 Timer 2 External Flag Output	
P0.2	18/13		PU	CTRAP_2 TDO_0 TXD_1 TXDC1_0	CCU6 Trap Input JTAG Serial Data Output UART Transmit Data Output/Clock Output MultiCAN Node 1 Transmitter Output	



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Туре	Reset State	Function	
P0.3	63/1		Hi-Z	SCK_1 COUT63_1 RXDO1_0	SSC Clock Input/Output Output of Capture/Compare channel 3
				A17	UART1 Transmit Data Output Address Line 17 Output
P0.4	64/2		Hi-Z	MTSR_1	SSC Master Transmit Output/ Slave Receive Input
				CC62_1	Input/Output of Capture/Compare channel 2
				TXD1_0	UART1 Transmit Data Output/Clock Output
				A18	Address Line 18 Output
P0.5	1/3		Hi-Z	MRST_1	SSC Master Receive Input/Slave Transmit Output
				EXINT0_0	External Interrupt Input 0
				T2EX1_1	Timer 21 External Trigger Input
				RXD1_0	UART1 Receive Data Input
				COUT62_1	Output of Capture/Compare channel 2
				A19	Address Line 19 Output
P0.6	2/4		PU	T2CC4_1	Compare Output Channel 4
				WR	External Data Write Control Output
P0.7	62/48		PU	CLKOUT_1 T2CC5_1 RD	Clock Output Compare Output Channel 5 External Data Read Control Output



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Туре	Reset State	Function	
P1		I/O		Port 1 Port 1 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for the JTAG, CCU6, UART, Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN, SSC and External Bus Interface.  Note: External Bus Interface is not available in XC874.	
P1.0	34/25		PU	RXD_0 T2EX_0 RXDC0_0 A8	UART Receive Data Input Timer 2 External Trigger Input MultiCAN Node 0 Receiver Input Address Line 8 Output
P1.1	35/26		PU	EXINT3_0 T0_1 TXD_0 TXDC0_0	External Interrupt Input 3 Timer 0 Input UART Transmit Data Output/Clock Output MultiCAN Node 0 Transmitter Output Address Line 9 Output
P1.2	36/27		PU	SCK_0 A10	SSC Clock Input/Output Address Line 10 Output
P1.3	37/28		PU	MTSR_0 SCK_2 TXDC1_3 A11	SSC Master Transmit Output/Slave Receive Input SSC Clock Input/Output MultiCAN Node 1 Transmitter Output Address Line 11 Output
P1.4	38/29		PU	MRST_0 EXINTO_1 RXDC1_3 MTSR_2 A12	SSC Master Receive Input/ Slave Transmit Output External Interrupt Input 0 MultiCAN Node 1 Receiver Input SSC Master Transmit Output/Slave Receive Input Address Line 12 Output



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Туре	Reset State	Function	
P1.5	39/30		PU	CCPOS0_1 EXINT5_0 T1_1 MRST_2 EXF2_0 RXDO_0	•
P1.6	10/9		PU	CCPOS1_1 T12HR_0 EXINT6_0 RXDC0_2 T21_1	CCU6 Timer 12 Hardware Run Input
P1.7	11/10		PU		CCU6 Hall Input 2 CCU6 Timer 13 Hardware Run Input Timer 2 Input MultiCAN Node 0 Transmitter Output .6 can be used as a software chip t for the SSC.



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Туре	Reset State	Function	
P3		I/O		Port 3 Port 3 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, UART1, T2CCU, Timer 21, MultiCAN and External Bus Interface.  Note: External Bus Interface is not available in XC874.	
P3.0	43/33		Hi-Z	CCPOS1_2 CC60_0 RXDO1_1 T2CC0_1/ EXINT3_2	CCU6 Hall Input 1 Input/Output of Capture/Compare channel 0 UART1 Transmit Data Output External Interrupt Input 3/T2CCU Capture/Compare Channel 0
P3.1	44/34		Hi-Z	CCPOS0_2 CC61_2 COUT60_0 TXD1_1	CCU6 Hall Input 0 Input/Output of Capture/Compare channel 1 Output of Capture/Compare channel 0 UART1 Transmit Data Output/Clock Output
P3.2	49/35		Hi-Z	CCPOS2_2 RXDC1_1 RXD1_1 CC61_0 T2CC1_1/ EXINT4_2	CCU6 Hall Input 2 MultiCAN Node 1 Receiver Input UART1 Receive Data Input Input/Output of Capture/Compare channel 1 External Interrupt Input 4/T2CCU Capture/Compare Channel 1
P3.3	50/36		Hi-Z	COUT61_0 TXDC1_1 T2CC2_1/ EXINT5_2 A13	Output of Capture/Compare channel 1 MultiCAN Node 1 Transmitter Output External Interrupt Input 5/T2CCU Capture/Compare Channel 2 Address Line 13 Output



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Туре	Reset State	Function	
P3.4	51/37		Hi-Z	CC62_0  RXDC0_1 T2EX1_0 T2CC3_1/ EXINT6_3 A14	Input/Output of Capture/Compare channel 2 MultiCAN Node 0 Receiver Input Timer 21 External Trigger Input External Interrupt Input 6/T2CCU Capture/Compare Channel 3 Address Line 14 Output
P3.5	52/38		Hi-Z	COUT62_0 EXF21_0 TXDC0_1 A15	Output of Capture/Compare channel 2 Timer 21 External Flag Output MultiCAN Node 0 Transmitter Output Address Line 15 Output
P3.6	41/32		PU	CTRAP_0	CCU6 Trap Input
P3.7	42/-		Hi-Z	EXINT4_0 COUT63_0 A16	External Interrupt Input 4 Output of Capture/Compare channel 3 Address Line 16 Output



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Туре	Reset State	Function	Function	
P4		I/O		Port 4  Port 4 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for CCU6, Timer 0, Timer 1, T2CCU, Timer 21, MultiCAN and External Bus Interface.  Note: External Bus Interface is not available in XC874.		
P4.0	59/45		Hi-Z	RXDC0_3 CC60_1 T2CC0_0/ EXINT3_1 D0	MultiCAN Node 0 Receiver Input Output of Capture/Compare channel 0 External Interrupt Input 3/T2CCU Capture/Compare Channel 0 Data Line 0 Input/Output	
P4.1	60/46		Hi-Z	TXDC0_3 COUT60_1 T2CC1_0/ EXINT4_1 D1	MultiCAN Node 0 Transmitter Output Output of Capture/Compare channel 0 External Interrupt Input 4/T2CCU Capture/Compare Channel 1 Data Line 1 Input/Output	
P4.2	61/47		PU	EXINT6_1 T21_0 D2	External Interrupt Input 6 Timer 21 Input Data Line 2 Input/Output	
P4.3	40/31		Hi-Z	T2EX_1 EXF21_1 COUT63_2 D3	Timer 2 External Trigger Input Timer 21 External Flag Output Output of Capture/Compare channel 3 Data Line 3 Input/Output	
P4.4	45/-		Hi-Z	CCPOS0_3 T0_0 CC61_4 T2CC2_0/ EXINT5_1 D4	CCU6 Hall Input 0 Timer 0 Input Output of Capture/Compare channel 1 External Interrupt Input 5/T2CCU Capture/Compare Channel 2 Data Line 4 Input/Output	



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Туре	Reset State	Function	
P4.5	46/-		Hi-Z	CCPOS1_3 T1_0 COUT61_2	CCU6 Hall Input 1 Timer 1 Input Output of Capture/Compare channel 1
				T2CC3_0/ EXINT6_2 D5	• •
P4.6	47/-		Hi-Z	CCPOS2_3 T2_0 CC62_2	CCU6 Hall Input 2 Timer 2 Input Output of Capture/Compare channel 2
				T2CC4_0 D6	Compare Output Channel 4 Data Line 6 Input/Output
P4.7	48/-		Hi-Z	CTRAP_3 COUT62_2	CCU6 Trap Input Output of Capture/Compare channel 2
				T2CC5_0 D7	Compare Output Channel 5 Data Line 7 Input/Output



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Туре	Reset State	Function	Function	
P5		I/O		I/O port. It ca	Port 5 is an 8-bit bidirectional general purpose I/O port. It can be used as alternate functions for UART, UART1, T2CCU, JTAG and External	
P5.0	8/-		PU	EXINT1_1 A0	External Interrupt Input 1 Address Line 0 Output	
P5.1	9/-		PU	EXINT2_1 A1	External Interrupt Input 2 Address Line 1 Output	
P5.2	12/-		PU	RXD_2 T2CC2_2/ EXINT5_3 A2	UART Receive Data Input External Interrupt Input 5/T2CCU Capture/Compare Channel 2 Address Line 2 Output	
P5.3	13/-		PU	CCPOS0_0 EXINT1_0 T12HR_2 CC61_3 TXD_2 T2CC5_2 A3	CCU6 Hall Input 0 External Interrupt Input 1 CCU6 Timer 12 Hardware Run Input Input of Capture/Compare channel 1 UART Transmit Data Output/Clock Output Compare Output Channel 5 Address Line 3 Output	
P5.4	14/-		PU		CCU6 Hall Input 1 External Interrupt Input 2 CCU6 Timer 13 Hardware Run Input Input of Capture/Compare channel 2 UART Transmit Data Output Compare Output Channel 4 Address Line 4 Output	



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Туре	Reset State	Function	
P5.5	15/-		PU	CCPOS2_0 CTRAP_1 CC60_3	CCU6 Hall Input 2 CCU6 Trap Input Input of Capture/Compare channel 0
				TDO_1 TXD1_2	JTAG Serial Data Output UART1 Transmit Data Output/ Clock Output
				T2CC0_2/ EXINT3_3 A5	External Interrupt Input 3/T2CCU Capture/Compare Channel 0 Address Line 5 Output
P5.6	19/-		PU	TCK_1 RXDO1_2 T2CC1_2/ EXINT4_3 A6	JTAG Clock Input UART1 Transmit Data Output External Interrupt Input 4/T2CCU Capture/Compare Channel 1 Address Line 6 Output
P5.7	20/-		PU	TDI_1 RXD1_2 T2CC3_2/ EXINT6_4 A7	JTAG Serial Data Input UART1 Receive Data Input External Interrupt Input 6/T2CCU Capture/Compare Channel 3 Address Line 7 Output



 Table 3
 Pin Definitions and Functions (cont'd)

Symbol	Pin Number (LQFP-64 / VQFN-48)	Туре	Reset State	Function
$V_{DDP}$	7, 25, 55/ 17, 41	_	_	I/O Port Supply (3.3 or 5.0 V) Also used by EVR and analog modules. All pins must be connected.
$V_{SSP}$	26, 54/ 18, 40	_	_	I/O Ground All pins must be connected.
$\overline{V_{DDC}}$	6/8	_	_	Core Supply Monitor (2.5 V)
$\overline{V_{SSC}}$	5/7	_	_	Core Supply Ground
$\overline{V_{AREF}}$	32/23	_	_	ADC Reference Voltage
$\overline{V_{AGND}}$	31/22	_	_	ADC Reference Ground
AN0	22/-	I	Hi-Z	Analog Input 0
AN1	23/15	I	Hi-Z	Analog Input 1
AN2	24/16	I	Hi-Z	Analog Input 2
AN3	27/-	I	Hi-Z	Analog Input 3
AN4	28/19	I	Hi-Z	Analog Input 4
AN5	29/20	I	Hi-Z	Analog Input 5
AN6	30/21	I	Hi-Z	Analog Input 6
AN7	33/24	I	Hi-Z	Analog Input 7
XTAL1	4/6	I	Hi-Z	External Oscillator Input (Feedback resistor required, normally NC)
XTAL2	3/5	0	Hi-Z	External Oscillator Output (Feedback resistor required, normally NC)
TMS	16/11	I	PD	JTAG Test Mode Select
RESET	53/39	I	PU	Reset Input
МВС	58/44	I	PU	Monitor & BootStrap Loader Control
ТМ	57/43	_	_	Test Mode (External pull down device required)
NC	56/42	_	_	No Connection



## 3 Functional Description

**Chapter 3** provides an overview of the XC87x functional description.

#### 3.1 Processor Architecture

The XC87x is based on a high-performance 8-bit Central Processing Unit (CPU) that is compatible with the standard 8051 processor. While the standard 8051 processor is designed around a 12-clock machine cycle, the XC87x CPU uses a 2-clock machine cycle. This allows fast access to ROM or RAM memories without wait state. The instruction set consists of 45% one-byte, 41% two-byte and 14% three-byte instructions.

The XC87x CPU provides a range of debugging features, including basic stop/start, single-step execution, breakpoint support and read/write access to the data memory, program memory and Special Function Registers (SFRs).

Figure 6 shows the CPU functional blocks.

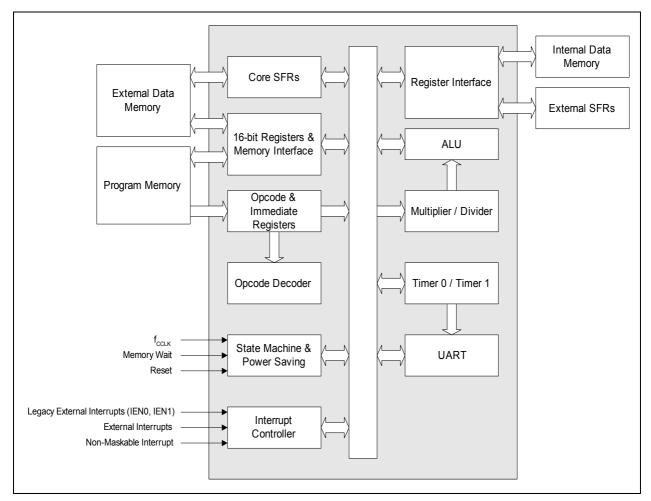


Figure 6 CPU Block Diagram



## 3.2 Memory Organization

The XC87x CPU operates in the following address spaces:

- 8 Kbytes of Boot ROM program memory
- 256 bytes of internal RAM data memory
- 3 Kbytes of XRAM memory (XRAM can be read/written as program memory or external data memory)
- A 128-byte Special Function Register area
- 64/52 Kbytes of Flash program memory (Flash devices)

Figure 7 and Figure 8 illustrate the memory address spaces of the XC87x with 64Kbytes and 52Kbytes embedded Flash respectively.

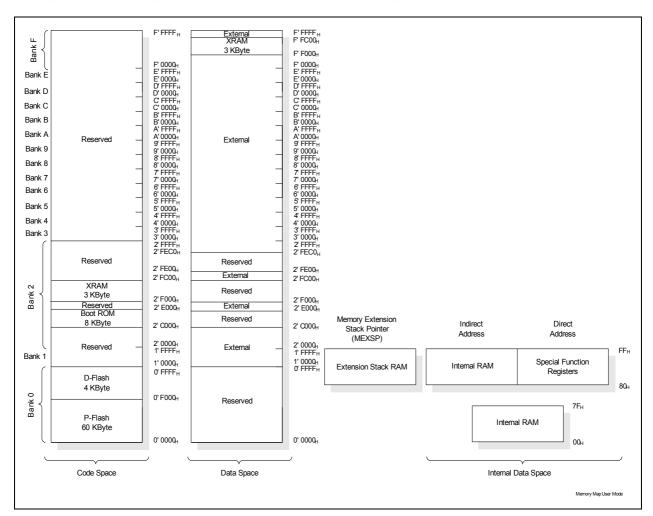


Figure 7 Memory Map of XC87x with 64K Flash Memory in user mode



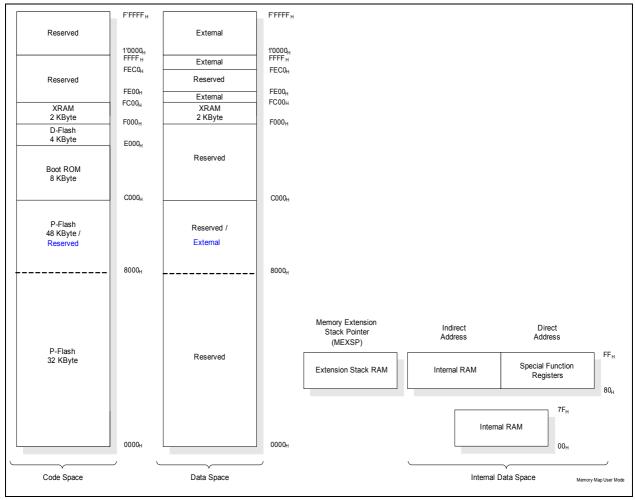


Figure 8 Memory Map of XC87x with 52K Flash Memory in user mode

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## 3.2.1 Memory Protection Strategy

The XC87x memory protection strategy includes:

- Basic protection: The user is able to block any external access via the boot option to any memory
- Read-out protection: The user is able to protect the contents in the Flash
- Flash program and erase protection

These protection strategies are enabled by programming a valid password (16-bit non-one value) via Bootstrap Loader (BSL) mode 6.

## 3.2.1.1 Flash Memory Protection

As long as a valid password is available, all external access to the device, including the Flash, will be blocked.

For additional security, the Flash hardware protection can be enabled to implement a second layer of read-out protection, as well as to enable program and erase protection.

Flash hardware protection is available only for Flash devices and comes in two modes:

- Mode 0: Only the P-Flash is protected; the D-Flash is unprotected
- Mode 1: Both the P-Flash and D-Flash are protected

The selection of each protection mode and the restrictions imposed are summarized in **Table 4**.

Table 4 Flash Protection Modes

Flash Protection	Without hardware protection	With hardware protection		
Hardware Protection Mode	-	0	1	
Activation	Program a valid passwo	rd via BSL mode 6		
Selection	Bit 13 of password = 0	Bit 13 of password = 1 MSB of password = 0	Bit 13 of password = 1 MSB of password = 1	
P-Flash contents can be read by	Read instructions in any program memory	Read instructions in the P-Flash	Read instructions in the P-Flash or D- Flash	
External access to P-Flash	Not possible	Not possible	Not possible	

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Table 4 Flash Protection Modes (cont'd)

Flash Protection	Without hardware protection	With hardware protection				
P-Flash program and erase	Possible	Possible only on the condition that MSB - 1 of password is set to 1	Possible only on the condition that MSB - 1 of password is set to 1			
D-Flash contents can be read by	Read instructions in any program memory	Read instructions in any program memory	Read instructions in the P-Flash or D- Flash			
External access to D-Flash	Not possible	Not possible	Not possible			
D-Flash program	Possible	Possible	Possible, on the condition that MSB - 1 of password is set to 1			
D-Flash erase	Possible	Possible, on these conditions:  • MISC_CON.DFLASH EN bit is set to 1 prior to each erase operation; or  • the MSB - 1 of password is set to 1	Possible, on the condition that MSB - 1 of password is set to 1			

BSL mode 6, which is used for enabling Flash protection, can also be used for disabling Flash protection. Here, the programmed password must be provided by the user. To disable the flash protection, a password match is required. A password match triggers an automatic erase of the protected P-Flash and D-Flash contents, including the programmed password. With a valid password, the Flash hardware protection is then enabled or disabled upon next reset. For the other protection strategies, no reset is necessary.

Although no protection scheme can be considered infallible, the XC87x memory protection strategy provides a very high level of protection for a general purpose microcontroller.

Note: If ROM read-out protection is enabled, only read instructions in the ROM memory can target the ROM contents.

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## 3.2.2 Special Function Register

The Special Function Registers (SFRs) occupy direct internal data memory space in the range  $80_H$  to  $FF_H$ . All registers, except the program counter, reside in the SFR area. The SFRs include pointers and registers that provide an interface between the CPU and the on-chip peripherals. As the 128-SFR range is less than the total number of registers required, address extension mechanisms are required to increase the number of addressable SFRs. The address extension mechanisms include:

- Mapping
- Paging

#### 3.2.2.1 Address Extension by Mapping

Address extension is performed at the system level by mapping. The SFR area is extended into two portions: the standard (non-mapped) SFR area and the mapped SFR area. Each portion supports the same address range  $80_H$  to FF<sub>H</sub>, bringing the number of addressable SFRs to 256. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit RMAP in the system control register SYSCON0 at address  $8F_H$ . To access SFRs in the mapped area, bit RMAP in SFR SYSCON0 must be set. Alternatively, the SFRs in the standard area can be accessed by clearing bit RMAP. The SFR area can be selected as shown in **Figure 9**.

As long as bit RMAP is set, the mapped SFR area can be accessed. This bit is not cleared automatically by hardware. Thus, before standard/mapped registers are accessed, bit RMAP must be cleared/set, respectively, by software.

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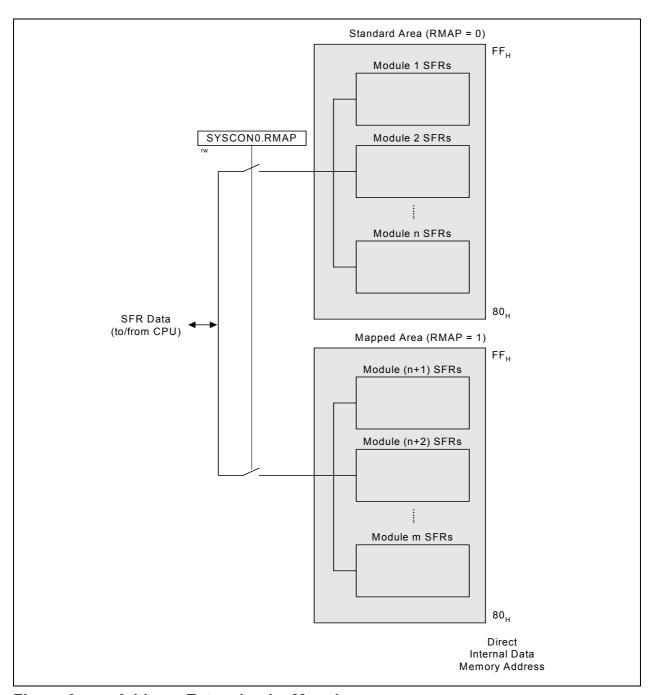


Figure 9 Address Extension by Mapping



Reset Value: 04 L

## SYSCON0 System Control Register 0

7	6	5	4	3	2	1	0
	0	1	IMODE	0	1	0	RMAP
<u></u>	r		rw	r	r	r	rw

Field	Bits	Туре	Description	
RMAP	0	rw	Interrupt Node XINTR0 Enable  O The access to the standard SFR area is enabled  The access to the mapped SFR area is enabled	
1	2	r	Reserved Returns 1 if read; should be written with 1.	
0	[7:5], 3,1	r	Reserved Returns 0 if read; should be written with 0.	

Note: The RMAP bit should be cleared/set by ANL or ORL instructions. The rest bits of SYSCON0 should not be modified.

## 3.2.2.2 Address Extension by Paging

Address extension is further performed at the module level by paging. With the address extension by mapping, the XC87x has a 256-SFR address range. However, this is still less than the total number of SFRs needed by the on-chip peripherals. To meet this requirement, some peripherals have a built-in local address extension mechanism for increasing the number of addressable SFRs. The extended address range is not directly controlled by the CPU instruction itself, but is derived from bit field PAGE in the module page register MOD\_PAGE. Hence, the bit field PAGE must be programmed before accessing the SFR of the target module. Each module may contain a different number of pages and a different number of SFRs per page, depending on the specific requirement. Besides setting the correct RMAP bit value to select the SFR area, the user must also ensure that a valid PAGE is selected to target the desired SFR. A page inside the extended address range can be selected as shown in Figure 10.



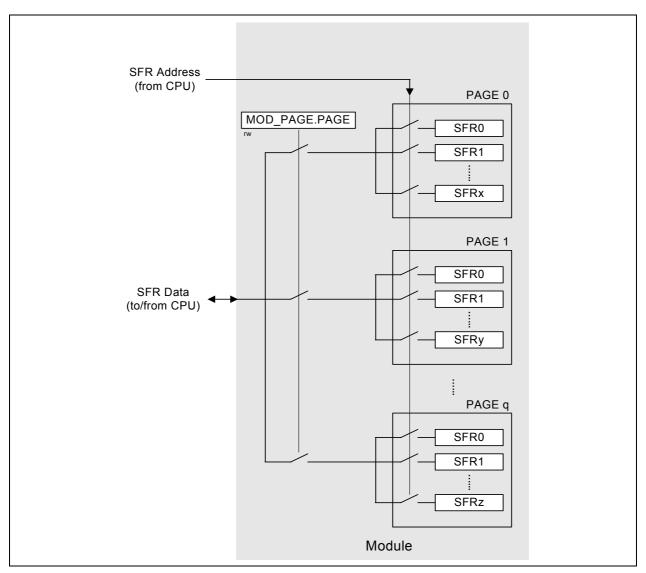


Figure 10 Address Extension by Paging

In order to access a register located in a page different from the actual one, the current page must be exited. This is done by reprogramming the bit field PAGE in the page register. Only then can the desired access be performed.

If an interrupt routine is initiated between the page register access and the module register access, and the interrupt needs to access a register located in another page, the current page setting can be saved, the new one programmed and the old page setting restored. This is possible with the storage fields STx (x = 0 - 3) for the save and restore action of the current page setting. By indicating which storage bit field should be used in parallel with the new page value, a single write operation can:

 Save the contents of PAGE in STx before overwriting with the new value (this is done in the beginning of the interrupt routine to save the current page setting and program the new page number); or



- Overwrite the contents of PAGE with the contents of STx, ignoring the value written to the bit positions of PAGE
  - (this is done at the end of the interrupt routine to restore the previous page setting before the interrupt occurred)

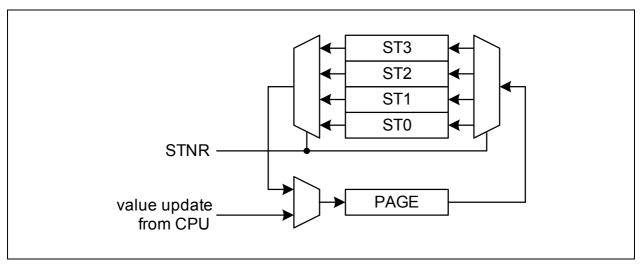


Figure 11 Storage Elements for Paging

With this mechanism, a certain number of interrupt routines (or other routines) can perform page changes without reading and storing the previously used page information. The use of only write operations makes the system simpler and faster. Consequently, this mechanism significantly improves the performance of short interrupt routines.

The XC87x supports local address extension for:

- Parallel Ports
- Analog-to-Digital Converter (ADC)
- Capture/Compare Unit 6 (CCU6)
- System Control Registers

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Reset Value: 00<sub>H</sub>

The page register has the following definition:

# MOD\_PAGE Page Register for module MOD

7	6	5	4	3	2	1	0
0	) <b>P</b>	ST	NR	0		PAGE	1
V	V	V	V	r		rw	

Bits	Туре	Description
[2:0]	rw	Page Bits When written, the value indicates the new page. When read, the value indicates the currently active page.
[5:4]	W	Storage Number This number indicates which storage bit field is the target of the operation defined by bit field OP. If OP = 10 <sub>B</sub> , the contents of PAGE are saved in STx before being overwritten with the new value. If OP = 11 <sub>B</sub> , the contents of PAGE are overwritten by the contents of STx. The value written to the bit positions of PAGE is ignored.  OO ST0 is selected. OO ST0 is selected. OO ST2 is selected. TS73 is selected.
	[2:0]	[2:0] rw



Field	Bits	Туре	Description						
OP	[7:6]	w	<ul> <li>Operation</li> <li>0X Manual page mode. The value of STNR is ignored and PAGE is directly written.</li> <li>10 New page programming with automatic page saving. The value written to the bit positions of PAGE is stored. In parallel, the previous contents of PAGE are saved in the storage bit field STx indicated by STNR.</li> <li>11 Automatic restore page action. The value written to the bit positions PAGE is ignored and instead, PAGE is overwritten by the contents of the storage bit field STx indicated by STNR.</li> </ul>						
0	3	r	Reserved Returns 0 if read; should be written with 0.						

#### 3.2.3 Bit Protection Scheme

The bit protection scheme prevents direct software writing of selected bits (i.e., protected bits) using the PASSWD register. When the bit field MODE is  $11_{\rm B}$ , writing  $10011_{\rm B}$  to the bit field PASS opens access to writing of all protected bits, and writing  $10101_{\rm B}$  to the bit field PASS closes access to writing of all protected bits. In both cases, the value of the bit field MODE is not changed even if PASSWD register is written with  $98_{\rm H}$  or  $A8_{\rm H}$ . It can only be changed when bit field PASS is written with  $11000_{\rm B}$ , for example, writing  $D0_{\rm H}$  to PASSWD register disables the bit protection scheme.

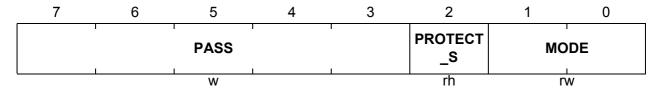
Note that access is opened for maximum 32 CCLKs if the "close access" password is not written. If "open access" password is written again before the end of 32 CCLK cycles, there will be a recount of 32 CCLK cycles. The protected bits include the N- and K-Divider bits, NDIV and KDIV; the Watchdog Timer enable bit, WDTEN; and the power-down and slow-down enable bits, PD and SD.



# 3.2.3.1 Password Register

#### **PASSWD**

Password Register Reset Value: 07<sub>H</sub>



Field	Bits	Туре	Description
MODE	[1:0]	rw	Bit Protection Scheme Control Bits  O Scheme disabled - direct access to the protected bits is allowed.  11 Scheme enabled - the bit field PASS has to be written with the passwords to open and close the access to protected bits. (default)  Others:Scheme Enabled.  These two bits cannot be written directly. To change the value between 11 <sub>B</sub> and 00 <sub>B</sub> , the bit field PASS must be written with 11000 <sub>B</sub> ; only then, will the MODE[1:0] be registered.
PROTECT_S	2	rh	Bit Protection Signal Status Bit This bit shows the status of the protection.  O Software is able to write to all protected bits.  Software is unable to write to any protected bits.
PASS	[7:3]	W	Password Bits The Bit Protection Scheme only recognizes three patterns.  11000 <sub>B</sub> Enables writing of the bit field MODE.  10011 <sub>B</sub> Opens access to writing of all protected bits.  10101 <sub>B</sub> Closes access to writing of all protected bits



#### 3.2.4 XC87x Register Overview

The SFRs of the XC87x are organized into groups according to their functional units. The contents (bits) of the SFRs are summarized in **Chapter 3.2.4.1** to **Chapter 3.2.4.15**.

Note: The addresses of the bitaddressable SFRs appear in bold typeface.

## 3.2.4.1 CPU Registers

The CPU SFRs can be accessed in both the standard and mapped memory areas (RMAP = 0 or 1).

Table 5 CPU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	= 0 or 1		l	I	l	l	I		l	l
81 <sub>H</sub>	SP Reset: 07 <sub>H</sub>	Bit Field				S	P			
	Stack Pointer Register	Туре				r	W			
82 <sub>H</sub>	DPL Reset: 00 <sub>H</sub>	Bit Field	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	DPL1	DPL0
	Data Pointer Register Low	Туре	rw	rw	rw	rw	rw	rw	rw	rw
83 <sub>H</sub>	DPH Reset: 00 <sub>H</sub>	Bit Field	DPH7	DPH6	DPH5	DPH4	DPH3	DPH2	DPH1	DPH0
	Data Pointer Register High	Туре	rw	rw	rw	rw	rw	rw	rw	rw
87 <sub>H</sub>	PCON Reset: 00 <sub>H</sub>	Bit Field	SMOD		0		GF1	GF0	0	IDLE
	Power Control Register	Туре	rw		r		rw	rw	r	rw
88 <sub>H</sub>	TCON Reset: 00 <sub>H</sub>	Bit Field	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
	Timer Control Register	Туре	rwh	rw	rwh	rw	rwh	rw	rwh	rw
89 <sub>H</sub>	TMOD Reset: 00 <sub>H</sub> Timer Mode Register	Bit Field	GATE 1	T1S	T1	1M	GATE 0	T0S	TO	M
		Туре	rw	rw	r	W	rw	rw	r	W
8A <sub>H</sub>	TL0 Reset: 00 <sub>H</sub>	Bit Field				V	AL		•	
	Timer 0 Register Low	Туре				rv	vh			
8B <sub>H</sub>	TL1 Reset: 00 <sub>H</sub>	Bit Field				V	AL			
	Timer 1 Register Low	Туре				rv	vh			
8C <sub>H</sub>	TH0 Reset: 00 <sub>H</sub>	Bit Field				V	AL			
	Timer 0 Register High	Туре				rv	vh			
8D <sub>H</sub>	TH1 Reset: 00 <sub>H</sub>	Bit Field				V	AL			
	Timer 1 Register High	Туре				rv	vh			
94 <sub>H</sub>	MEX1 Reset: 00 <sub>H</sub>	Bit Field		C	В			N	IB	
	Memory Extension Register 1	Туре			r			r	W	
95 <sub>H</sub>	MEX2 Reset: 00 <sub>H</sub>	Bit Field	MCM MCB				IB			
	Memory Extension Register 2	Туре	rw rw				rw			
96 <sub>H</sub>	MEX3 Reset: 00 <sub>H</sub> Memory Extension Register 3	Bit Field	MCB1 9		0	MXB1 9	MXM	MXB		
		Туре	rw		r	rw	rw rw		rw	



Table 5 CPU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
97 <sub>H</sub>	MEXSP Reset: 7FH	Bit Field	0				MXSP			
	Memory Extension Stack Pointer Register	Туре	r				rwh			
98 <sub>H</sub>	SCON Reset: 00 <sub>H</sub>	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
	Serial Channel Control Register	Туре	rw	rw	rw	rw	rw	rwh	rwh	rwh
99 <sub>H</sub>	SBUF Reset: 00 <sub>H</sub>	Bit Field				V	AL			
	Serial Data Buffer Register	Туре				rv	/h			
A2 <sub>H</sub>	EO Reset: 00 <sub>H</sub> Extended Operation Register	Bit Field		0		TRAP_ EN		0		DPSE L0
		Туре		r		rw		r		rw
A8 <sub>H</sub>	IEN0 Reset: 00 <sub>H</sub>	Bit Field	EA	0	ET2	ES	ET1	EX1	ET0	EX0
	Interrupt Enable Register 0	Туре	rw	r	rw	rw	rw	rw	rw	rw
B8 <sub>H</sub>	IP Reset: 00 <sub>H</sub>	Bit Field	(	)	PT2	PS	PT1	PX1	PT0	PX0
	Interrupt Priority Register	Туре	1	r	rw	rw	rw	rw	rw	rw
в9 <sub>Н</sub>	IPH Reset: 00 <sub>H</sub>	Bit Field	(	)	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
	Interrupt Priority High Register	Туре		r	rw	rw	rw	rw	rw	rw
D0 <sub>H</sub>	PSW Reset: 00 <sub>H</sub>	Bit Field	CY	AC	F0	RS1	RS0	OV	F1	Р
	Program Status Word Register	Туре	rwh	rwh	rw	rw	rw	rwh	rw	rh
E0 <sub>H</sub>	ACC Reset: 00 <sub>H</sub>	Bit Field	ACC7	ACC6	ACC5	ACC4	ACC3	ACC2	ACC1	ACC0
	Accumulator Register	Туре	rw	rw	rw	rw	rw	rw	rw	rw
E8 <sub>H</sub>	IEN1 Reset: 00 <sub>H</sub> Interrupt Enable Register 1	Bit Field	ECCIP 3	ECCIP 2	ECCIP 1	ECCIP 0	EXM	EX2	ESSC	EADC
		Туре	rw	rw	rw	rw	rw	rw	rw	rw
F0 <sub>H</sub>	B Reset: 00 <sub>H</sub>	Bit Field	В7	В6	B5	B4	В3	B2	B1	В0
	B Register	Туре	rw	rw	rw	rw	rw	rw	rw	rw
F8 <sub>H</sub>	IP1 Reset: 00 <sub>H</sub> Interrupt Priority 1 Register	Bit Field	PCCIP 3	PCCIP 2	PCCIP 1	PCCIP 0	PXM	PX2	PSSC	PADC
		Туре	rw	rw	rw	rw	rw	rw	rw	rw
F9 <sub>H</sub>	IPH1 Reset: 00 <sub>H</sub> Interrupt Priority 1 High Register	Bit Field	PCCIP 3H	PCCIP 2H	PCCIP 1H	PCCIP 0H	PXMH	PX2H	PSSC H	PADC H
		Туре	rw	rw	rw	rw	rw	rw	rw	rw

# 3.2.4.2 MDU Registers

The MDU SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 6 MDU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	1									
во <sub>Н</sub>	MDUSTAT Reset: 00 <sub>H</sub>	Bit Field			0			BSY	IERR	IRDY
	MDU Status Register	Туре	r					rh	rwh	rwh



Table 6 MDU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0		
в1 <sub>Н</sub>	MDUCON Reset: 00 <sub>H</sub> MDU Control Register	Bit Field	ΙE	IR	RSEL	STAR T		OPC	ODE			
		Туре	rw	rw	rw	rwh		n	N			
B2 <sub>H</sub>	MD0 Reset: 00 <sub>H</sub>	Bit Field				DA	TA					
	MDU Operand Register 0	Туре				r	W					
B2 <sub>H</sub>	MR0 Reset: 00 <sub>H</sub>	Bit Field				DA	TA					
	MDU Result Register 0	Туре				r	h					
вз <sub>Н</sub>	MD1 Reset: 00 <sub>H</sub>	Bit Field				DA	TA					
	MDU Operand Register 1	Туре				r	W					
вз <sub>Н</sub>	MR1 Reset: 00 <sub>H</sub>	Bit Field				DA	TA					
	MDU Result Register 1	Туре				r	h					
B4 <sub>H</sub>	MD2 Reset: 00 <sub>H</sub>	Bit Field				DA	TA					
	MDU Operand Register 2	Туре				r	W					
B4 <sub>H</sub>	MR2 Reset: 00 <sub>H</sub>	Bit Field				DA	TA					
	MDU Result Register 2	Туре				r	h					
В5 <sub>Н</sub>	MD3 Reset: 00 <sub>H</sub>	Bit Field				DA	TA					
	MDU Operand Register 3	Туре				r	W					
В5 <sub>Н</sub>	MR3 Reset: 00 <sub>H</sub>	Bit Field				DA	TA					
	MDU Result Register 3	Туре				r	h					
B6 <sub>H</sub>	MD4 Reset: 00 <sub>H</sub>	Bit Field				DA	TA					
	MDU Operand Register 4	Туре				r	W					
B6 <sub>H</sub>	MR4 Reset: 00 <sub>H</sub>	Bit Field				DA	TA					
	MDU Result Register 4	Туре				r	h					
В7 <sub>Н</sub>	MD5 Reset: 00 <sub>H</sub>	Bit Field				DA	ГА					
	MDU Operand Register 5	Туре				r	N					
В7 <sub>Н</sub>	MR5 Reset: 00 <sub>H</sub>	Bit Field				DA	·ΤΑ					
	MDU Result Register 5	Туре				r	h					

# 3.2.4.3 CORDIC Registers

The CORDIC SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 7 CORDIC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	1									
9A <sub>H</sub>	CD_CORDXL Reset: 00H	Bit Field				DA	TAL			
	CORDIC X Data Low Byte	Туре	rw							
9B <sub>H</sub>	CD_CORDXH Reset: 00H	Bit Field		DATAH						
	CORDIC X Data High Byte	Туре	e rw							



 Table 7
 CORDIC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
9C <sub>H</sub>	CD_CORDYL Reset: 00H	Bit Field				DA	TAL			
	CORDIC Y Data Low Byte	Туре		rw						
9D <sub>H</sub>	CD_CORDYH Reset: 00H	Bit Field	DATAH							
	CORDIC Y Data High Byte	Туре	rw							
9E <sub>H</sub>	CD_CORDZL Reset: 00H	Bit Field				DA	TAL			
	CORDIC Z Data Low Byte	Туре				r	W			
9F <sub>H</sub>	CD_CORDZH Reset: 00H	Bit Field				DA	ГАН			
	CORDIC Z Data High Byte	Туре				r	W			
A0 <sub>H</sub>	CD_STATC Reset: 00 <sub>H</sub> CORDIC Status and Data	Bit Field	KEEP Z	KEEP Y	KEEP X	DMAP	INT_E N	EOC	ERRO R	BSY
	Control Register	Туре	rw	rw	rw	rw	rw	rwh	rh	rh
A1 <sub>H</sub>	CD_CON Reset: 00 <sub>H</sub> CORDIC Control Register	Bit Field	d MPS X_USI ST_M ROTV MODE S GN ODE EC				ST			
		Туре	n	N	rw	rw	rw	r	W	rwh

# 3.2.4.4 System Control Registers

The system control SFRs can be accessed in the mapped memory area (RMAP = 0).

Table 8 SCU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	: 0 or 1	•		•	•		•	•		
8F <sub>H</sub>	SYSCON0 Reset: 04 <sub>H</sub> System Control Register 0	Bit Field 0			IMOD E	0	1	0	RMAP	
		Туре		r		rw	r	r	r	rw
RMAP =	0									
BFH	SCU_PAGE Reset: 00H	Bit Field	С	)P	ST	NR	0		PAGE	
	Page Register	Туре	1	N	١	V	r		rwh	
RMAP =	0, PAGE 0									
вз <sub>Н</sub>	MODPISEL Reset: 00 <sub>H</sub> Peripheral Input Select Register	Bit Field	0	URRIS H	JTAGT DIS	JTAGT CKS	EXINT 2IS	EXINT 1IS	EXINT 0IS	URRIS
		Туре	r	rw	rw	rw	rw	rw	rw	rw
<sup>B4</sup> H	IRCON0 Reset: 00 <sub>H</sub> Interrupt Request Register 0	Bit Field	0	EXINT 6	EXINT 5	EXINT 4	EXINT 3	EXINT 2	EXINT 1	EXINT 0
		Туре	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh
в5 <sub>Н</sub>	IRCON1 Reset: 00 <sub>H</sub> Interrupt Request Register 1	Bit Field	0	CANS RC2	CANS RC1	ADCS R1	ADCS R0	RIR	TIR	EIR
		Туре	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh
в6 <sub>Н</sub>	IRCON2 Reset: 00 <sub>H</sub> Interrupt Request Register 2	Bit Field	_	0		CANS RC3		0		CANS RC0
		Туре		r		rwh		r		rwh



# Table 8 SCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0	
в7 <sub>Н</sub>	EXICON0 Reset: F0H	Bit Field	EXI	NT3	EXI	NT2	EXI	NT1	EXI	NT0	
	External Interrupt Control Register 0	Туре	r	W	n	w	r	w	r	w	
BA <sub>H</sub>	EXICON1 Reset: 3F <sub>H</sub>	Bit Field	(	)	EXI	NT6	EXI	NT5	EXI	NT4	
	External Interrupt Control Register 1	Туре	ı	r	n	W	r	W	r	W	
ввн	NMICON Reset: 00 <sub>H</sub> NMI Control Register	Bit Field	0	NMI ECC	NMI VDDP	0	NMI OCDS	NMI FLASH	NMI PLL	NMI WDT	
		Туре	r	rw	rw	r	rw	rw	rw	rw	
вс <sub>Н</sub>	NMISR Reset: 00 <sub>H</sub> NMI Status Register	Bit Field	0	FNMI ECC	FNMI VDDP	0	FNMI OCDS	FNMI FLASH	FNMI PLL	FNMI WDT	
		Туре	r	rwh	rwh	r	rwh	rwh	rwh	rwh	
BD <sub>H</sub>	BCON Reset: 20 <sub>H</sub> Baud Rate Control Register	Bit Field	BG	SEL	NDOV EN	BRDIS		BRPRE		R	
		Туре	r	W	rw	rw		rw		rw	
BE <sub>H</sub>	BG Reset: 00 <sub>H</sub>	Bit Field				BR_V	ALUE				
	Baud Rate Timer/Reload Register	Туре				rv	vh				
E9 <sub>H</sub>	FDCON Reset: 00 <sub>H</sub> Fractional Divider Control	Bit Field	BGS	SYNE N	ERRS YN	EOFS YN	BRK	NDOV	FDM	FDEN	
	Register	Туре	rw	rw	rwh	rwh	rwh	rwh	rw	rw	
EA <sub>H</sub>	FDSTEP Reset: 00H	Bit Field				ST	EP				
	Fractional Divider Reload Register	Туре				r	W				
EB <sub>H</sub>	FDRES Reset: 00 <sub>H</sub>	Bit Field				RES	SULT				
	Fractional Divider Result Register	Туре				r	h				
RMAP =	0, PAGE 1		1					1			
вз <sub>Н</sub>	ID Reset: 49 <sub>H</sub> Identity Register	Bit Field			PRODID				VERID		
	identity Register	Туре			r				r		
B4 <sub>H</sub>	PMCON0 Reset: 80 <sub>H</sub> Power Mode Control Register 0	Bit Field	VDDP WARN	WDT RST	WKRS	WK SEL	SD	PD	V	/S	
		Туре	rh	rwh	rwh	rw	rw	rwh	r	w	
B5 <sub>H</sub>	PMCON1 Reset: 00 <sub>H</sub> Power Mode Control Register 1	Bit Field	0	CDC_ DIS	CAN_ DIS	MDU_ DIS	T2CC U_DIS	CCU_ DIS	SSC_ DIS	ADC_ DIS	
		Туре	r	rw	rw	rw	rw	rw	rw	rw	
в6 <sub>Н</sub>	OSC_CON Reset: XX <sub>H</sub> OSC Control Register	Bit Field	PLLRD RES	PLLBY P	PLLPD	0	XPD	OSC SS	EORD RES	EXTO SCR	
		Туре	rwh	rwh	rw	r	rw	rwh	rwh	rh	
в7 <sub>Н</sub>	PLL_CON Reset: 18 <sub>H</sub> PLL Control Register	Bit Field			NE	OIV		PLLR PLL_ OCA			
		Туре			n	w		rh rh			
BA <sub>H</sub>	CMCON Reset: 10 <sub>H</sub> Clock Control Register	Bit Field	KE	ΟIV	0	FCCF G	CLKREL				
		Туре	r	w	r	rw	rw				



 Table 8
 SCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
ввн	PASSWD Reset: 07 <sub>H</sub> Password Register	Bit Field			PASS			PROT ECT_S	МС	DDE
		Туре			W			rh	r	W
BE <sub>H</sub>	COCON Reset: 00 <sub>H</sub>	Bit Field	CO	JTS	TLEN	0		CO	REL	
	Clock Output Control Register	Туре	r	W	rw	r		r	W	
E9 <sub>H</sub>	MISC_CON Reset: 00 <sub>H</sub> Miscellaneous Control Register	Bit Field	ADCE TR0_ MUX	ADCE TR1_ MUX			0			DFLAS HEN
		Туре	rw	rw						rwh
EA <sub>H</sub>	PLL_CON1 Reset: 20 <sub>H</sub>	Bit Field		NDIV				PDIV		
	PLL Control Register 1	Туре		rw				rw		
EB <sub>H</sub>	CR_MISC Reset: 00 <sub>H</sub> or 01 <sub>H</sub> Reset Status Register	Bit Field	CCCF G	MDUC CFG	CCUC CFG	T2CCF G		0		HDRS T
		Туре	rw	rw	rw	rw		r		rwh
RMAP =	= 0, PAGE 3									
вз <sub>Н</sub>	XADDRH Reset: F0 <sub>H</sub>	Bit Field				ADI	ORH			
	On-chip XRAM Address Higher Order	Туре				r	W			
B4 <sub>H</sub>	IRCON3 Reset: 00 <sub>H</sub> Interrupt Request Register 3	Bit Field	(	)	CANS RC5	CCU6 SR1	(	0	CANS RC4	CCU6 SR0
		Туре		r	rwh	rwh		r	rwh	rwh
в5 <sub>Н</sub>	IRCON4 Reset: 00 <sub>H</sub> Interrupt Request Register 4	Bit Field	(	)	CANS RC7	CCU6 SR3	(	0	CANS RC6	CCU6 SR2
		Туре	I	r	rwh	rwh		r	rwh	rwh
B6 <sub>H</sub>	MODIEN Reset: 07 <sub>H</sub> Peripheral Interrupt Enable	Bit Field		0		CM5E N	CM4E N	RIREN	TIREN	EIREN
	Register	Туре		r		rw	rw	rw	rw	rw
в7 <sub>Н</sub>	MODPISEL1 Reset: 00 <sub>H</sub> Peripheral Input Select Register	Bit Field		EXINT6IS	S	UR1	IRIS	T21EX IS	(	)
	I	Туре		rw		r	W	rw		r
BA <sub>H</sub>	MODPISEL2 Reset: 00 <sub>H</sub> Peripheral Input Select Register	Bit Field		0		T2EXI S	T21IS	T2IS	T1IS	TOIS
	2	Туре		r		rw	rw	rw	rw	rw
ввн	PMCON2 Reset: 00 <sub>H</sub> Power Mode Control Register 2	Bit Field				0			UART 1_DIS	T21_D IS
		Туре				r			rw	rw
<sub>BDH</sub>	MODSUSP Reset: 01 <sub>H</sub> Module Suspend Control	Bit Field	(	)	CCTS USP	T21SU SP	T2SUS P	T13SU SP	T12SU SP	WDTS USP
	Register	Туре		r	rw	rw	rw	rw	rw	rw
BE <sub>H</sub>	MODPISEL3 Reset: 00 <sub>H</sub>	Bit Field	(	)	С	IS	S	IS	М	IS
	Peripheral Input Select Register 3	Туре		r	r	W	r	W	r	W
EA <sub>H</sub>	MODPISEL4 Reset: 00H	Bit Field	(	)	EXIN	IT5IS	EXIN	IT4IS	EXIN	IT3IS
	Peripheral Input Select Register 4	Туре		r	r	w	r	w	r	w



## 3.2.4.5 WDT Registers

The WDT SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 9 WDT Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	: 1			•		•		•		•
ввн	WDTCON Reset: 00 <sub>H</sub> Watchdog Timer Control	Bit Field		0	WINB EN	WDTP R	0	WDTE N	WDTR S	WDTI N
	Register	Туре		r	rw	rh	r	rw	rwh	rw
всн	WDTREL Reset: 00 <sub>H</sub>	Bit Field	WDTREL							
	Watchdog Timer Reload Register	Туре				r	w			
BD <sub>H</sub>	WDTWINB Reset: 00 <sub>H</sub>	Bit Field				WDT	WINB			
	Watchdog Window-Boundary Count Register	Туре				r	w			
BE <sub>H</sub>	WDTL Reset: 00 <sub>H</sub>	Bit Field				W	DT			
	Watchdog Timer Register Low	Туре	rh							
BF <sub>H</sub>	WDTH Reset: 00 <sub>H</sub>	Bit Field	eld WDT							
	Watchdog Timer Register High	Туре	rh							

# 3.2.4.6 Port Registers

The Port SFRs can be accessed in the standard memory area (RMAP = 0).

**Table 10** Port Register Overview

Addr	Register Name		Bit	7	6	5	4	3	2	1	0
RMAP =	= 0				•						
B2 <sub>H</sub>		t: 00 <sub>H</sub>	Bit Field	0	P	ST	NR	0		PAGE	
	Page Register		Туре	٧	v	V	V	r		rwh	
RMAP =	0, PAGE 0										
80 <sub>H</sub>	P0_DATA Rese	t: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P0 Data Register		Туре	rwh	rwh						
86 <sub>H</sub>		t: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P0 Direction Register		Туре	rw	rw						
90 <sub>H</sub>	P1_DATA Rese	t: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P1 Data Register		Туре	rwh	rwh						
91 <sub>H</sub>		t: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P1 Direction Register		Туре	rw	rw						
92 <sub>H</sub>		t: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P5 Data Register		Туре	rwh	rwh						
93 <sub>H</sub>		t: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P5 Direction Register		Туре	rw	rw						



 Table 10
 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
B0 <sub>H</sub>	P3_DATA Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
"	P3 Data Register	Туре	rwh							
B1 <sub>H</sub>	P3_DIR Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
•••	P3 Direction Register	Туре	rw							
C8H	P4_DATA Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P4 Data Register	Туре	rwh							
C9 <sub>H</sub>	P4_DIR Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P4 Direction Register	Туре	rw							
RMAP =	= 0, PAGE 1									
80 <sub>H</sub>	P0_PUDSEL Reset: FF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P0 Pull-Up/Pull-Down Select Register	Туре	rw							
86 <sub>H</sub>	P0_PUDEN Reset: C4 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P0 Pull-Up/Pull-Down Enable Register	Туре	rw							
90 <sub>H</sub>	P1_PUDSEL Reset: FF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P1 Pull-Up/Pull-Down Select Register	Туре	rw							
91 <sub>H</sub>	P1_PUDEN Reset: FF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P1 Pull-Up/Pull-Down Enable Register	Туре	rw							
92 <sub>H</sub>	P5_PUDSEL Reset: FF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P5 Pull-Up/Pull-Down Select Register	Туре	rw							
93 <sub>H</sub>	P5_PUDEN Reset: FF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P5 Pull-Up/Pull-Down Enable Register	Туре	rw							
во <sub>Н</sub>	P3_PUDSEL Reset: BF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P3 Pull-Up/Pull-Down Select Register	Туре	rw							
B1 <sub>H</sub>	P3_PUDEN Reset: 40 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P3 Pull-Up/Pull-Down Enable Register	Туре	rw							
C8 <sub>H</sub>	P4_PUDSEL Reset: FF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P4 Pull-Up/Pull-Down Select Register	Туре	rw							
C9 <sub>H</sub>	P4_PUDEN Reset: 04 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P4 Pull-Up/Pull-Down Enable Register	Туре	rw							
RMAP =	= 0, PAGE 2	1				1				
80 <sub>H</sub>	P0_ALTSEL0 Reset: 00H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P0 Alternate Select 0 Register	Туре	rw							
86 <sub>H</sub>	P0_ALTSEL1 Reset: 00H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P0 Alternate Select 1 Register	Туре	rw							
90 <sub>H</sub>	P1_ALTSEL0 Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P1 Alternate Select 0 Register	Туре	rw							



 Table 10
 Port Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
91 <sub>H</sub>	P1_ALTSEL1 Reset: 00H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P1 Alternate Select 1 Register	Туре	rw							
92 <sub>H</sub>	P5_ALTSEL0 Reset: 00H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P5 Alternate Select 0 Register	Туре	rw							
93 <sub>H</sub>	P5_ALTSEL1 Reset: 00H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P5 Alternate Select 1 Register	Туре	rw							
во <sub>Н</sub>	P3_ALTSEL0 Reset: 00H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P3 Alternate Select 0 Register	Туре	rw							
В1 <sub>Н</sub>	P3_ALTSEL1 Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P3 Alternate Select 1 Register	Туре	rw							
C8H	P4_ALTSEL0 Reset: 00H	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P4 Alternate Select 0 Register	Туре	rw							
C9H	P4_ALTSEL1 Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P4 Alternate Select 1 Register	Туре	rw							
RMAP =	= 0, PAGE 3									
80 <sub>H</sub>	P0_OD Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P0 Open Drain Control Register	Туре	rw							
86 <sub>H</sub>	P0_DS Reset: FF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P0 Drive Strength Control Register	Туре	rw							
90 <sub>H</sub>	P1_OD Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P1 Open Drain Control Register	Туре	rw							
91 <sub>H</sub>	P1_DS Reset: FF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P1 Drive Strength Control Register	Туре	rw							
92 <sub>H</sub>	P5_OD Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P5 Open Drain Control Register	Туре	rw							
93 <sub>H</sub>	P5_DS Reset: FF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P5 Drive Strength Control Register	Туре	rw							
во <sub>Н</sub>	P3_OD Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P3 Open Drain Control Register	Туре	rw							
В1 <sub>Н</sub>	P3_DS Reset: FF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P3 Drive Strength Control Register	Туре	rw							
C8 <sub>H</sub>	P4_OD Reset: 00 <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P4 Open Drain Control Register	Туре	rw							
C9 <sub>H</sub>	P4_DS Reset: FF <sub>H</sub>	Bit Field	P7	P6	P5	P4	P3	P2	P1	P0
	P4 Drive Strength Control Register	Туре	rw							



# 3.2.4.7 ADC Registers

The ADC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 11 ADC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0		
RMAP =	= 0	I	l	l	l		I			I		
D1 <sub>H</sub>	ADC_PAGE Reset: 00H	Bit Field	C	P	ST	NR	0		PAGE			
	Page Register	Туре	١	V	١	N	r		rw			
RMAP =	= 0, PAGE 0	•					l					
CA <sub>H</sub>	ADC_GLOBCTR Reset: 30H	Bit Field	ANON	DW	C.	TC			)			
	Global Control Register	Туре	rw	rw	r	W			r			
СВН	ADC_GLOBSTR Reset: 00 <sub>H</sub> Global Status Register	Bit Field	(	)		CHNR		0	SAMP LE	BUSY		
		Туре		ſ		rh		r	rh	rh		
cc <sub>H</sub>	ADC_PRAR Reset: 00 <sub>H</sub> Priority and Arbitration Register	Bit Field	ASEN 1	ASEN 0	0	ARBM	CSM1	PRIO1	CSM0	PRIO0		
		Туре	rw	rw	r	rw	rw	rw				
CDH	ADC_LCBR Reset: B7 <sub>H</sub>	Bit Field		BOL	IND1			BOL	BOUND0			
	Limit Check Boundary Register	Туре		r	W			r	rw			
CEH	ADC_INPCR0 Reset: 00H	Bit Field				S	ГС					
	Input Class 0 Register	Туре				r	W		ETRSEL0			
CF <sub>H</sub>	ADC_ETRCR Reset: 00 <sub>H</sub> External Trigger Control	Bit Field	SYNE N1	SYNE N0		ETRSEL1			)			
	Register	Туре	rw	rw		rw			rw			
RMAP =	= 0, PAGE 1											
CA <sub>H</sub>	ADC_CHCTR0 Reset: 00H	Bit Field	0		LCC			0	RESI	RSEL		
	Channel Control Register 0	Туре	r		rw			r	r	W		
СВН	ADC_CHCTR1 Reset: 00 <sub>H</sub>	Bit Field	0		LCC			0	RESI	RSEL		
	Channel Control Register 1	Туре	r		rw			r	r	W		
сс <sub>Н</sub>	ADC_CHCTR2 Reset: 00 <sub>H</sub> Channel Control Register 2	Bit Field	0		LCC		(	0	RESI	RSEL		
	Charmer Control Register 2	Туре	r		rw			r	r	W		
CDH	ADC_CHCTR3 Reset: 00 <sub>H</sub> Channel Control Register 3	Bit Field	0		LCC			0	RESI	RSEL		
	Charmer Control Register 5	Туре	r		rw			r	r	W		
CEH	ADC_CHCTR4 Reset: 00 <sub>H</sub> Channel Control Register 4	Bit Field	0		LCC		(	0	RESI	RSEL		
	Charmer Control Register 4	Туре	r		rw			r rw				
CF <sub>H</sub>	ADC_CHCTR5 Reset: 00 <sub>H</sub> Channel Control Register 5	Bit Field	0		LCC		(	RESRSEL				
	_	Туре	r		rw			r		W		
D2 <sub>H</sub>	ADC_CHCTR6 Reset: 00 <sub>H</sub> Channel Control Register 6	Bit Field	0		LCC			0	RESI	RSEL		
	Ŭ	Туре	r		rw			r rw				
D3 <sub>H</sub>	ADC_CHCTR7 Reset: 00 <sub>H</sub> Channel Control Register 7	Bit Field	0		LCC			0	RESI	RSEL		
	Chamici Control Negister /	Туре	r		rw			r	r	W		



 Table 11
 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0		
RMAP =	= 0, PAGE 2	L					ı		CHNR rh			
CAH	ADC_RESR0L Reset: 00H	Bit Field	RES	SULT	0	VF	DRC		CHNR			
	Result Register 0 Low	Туре	r	h	r	rh	rh		rh			
СВН	ADC_RESR0H Reset: 00 <sub>H</sub>	Bit Field			•	RES	SULT					
	Result Register 0 High	Туре				ı	·h					
сс <sub>Н</sub>	ADC_RESR1L Reset: 00H	Bit Field	RES	SULT	0	VF	DRC		CHNR			
	Result Register 1 Low	Туре	r	h .	r	rh	rh		rh			
CDH	ADC_RESR1H Reset: 00H	Bit Field				RES	SULT					
	Result Register 1 High	Туре				1	h .					
CEH	ADC_RESR2L Reset: 00H	Bit Field	RES	SULT	0	VF	DRC		CHNR			
	Result Register 2 Low	Туре	r	h .	r	rh	rh		rh			
CF <sub>H</sub>	ADC_RESR2H Reset: 00H	Bit Field				RES	SULT					
	Result Register 2 High	Туре				1	h .					
D2 <sub>H</sub>	ADC_RESR3L Reset: 00H	Bit Field	RES	SULT	0	VF	DRC		CHNR rh			
	Result Register 3 Low	Туре	r	h .	r	rh	rh					
D3 <sub>H</sub>	ADC_RESR3H Reset: 00H	Bit Field				RES	SULT					
	Result Register 3 High	Туре				ı	h					
RMAP =	= 0, PAGE 3											
CA <sub>H</sub>	ADC_RESRA0L Reset: 00H	Bit Field		RESULT		VF	DRC		CHNR			
	Result Register 0, View A Low	Туре		rh		rh	rh		CHNR rh			
СВН	ADC_RESRA0H Reset: 00 <sub>H</sub>	Bit Field				RES	SULT					
	Result Register 0, View A High	Туре				ı	h					
сс <sub>Н</sub>	ADC_RESRA1L Reset: 00H	Bit Field		RESULT		VF	DRC		CHNR			
	Result Register 1, View A Low	Туре		rh		rh	rh		rh			
CDH	ADC_RESRA1H Reset: 00H	Bit Field				RES	SULT					
	Result Register 1, View A High	Туре					h .					
CEH	ADC_RESRA2L Reset: 00H	Bit Field		RESULT		VF	DRC		CHNR			
	Result Register 2, View A Low	Туре		rh		rh	rh		rh			
CF <sub>H</sub>	ADC_RESRA2H Reset: 00H	Bit Field				RES	SULT					
	Result Register 2, View A High	Туре					h .					
D2 <sub>H</sub>	ADC_RESRA3L Reset: 00H	Bit Field		RESULT		VF	DRC		CHNR			
	Result Register 3, View A Low	Туре		rh		rh	rh					
D3 <sub>H</sub>	ADC_RESRA3H Reset: 00 <sub>H</sub> Result Register 3, View A High	Bit Field				RES	SULT					
	Tresuit register 3, view A riigh	Туре				1	h					
RMAP =	= 0, PAGE 4			1								
CA <sub>H</sub>	ADC_RCR0 Reset: 00 <sub>H</sub> Result Control Register 0	Bit Field	VFCT R	WFR	0	IEN		0	DRCT R			
		Туре	rw	rw	r	rw		r		rw		



 Table 11
 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
СВН	ADC_RCR1 Reset: 00 <sub>H</sub> Result Control Register 1	Bit Field	VFCT R	WFR	0	IEN		0		DRCT R
		Туре	rw	rw	r	rw		r		rw
сс <sub>Н</sub>	ADC_RCR2 Reset: 00 <sub>H</sub> Result Control Register 2	Bit Field	VFCT R	WFR	0	IEN		0		DRCT R
		Туре	rw	rw	r	rw		r		rw
CDH	ADC_RCR3 Reset: 00 <sub>H</sub> Result Control Register 3	Bit Field	VFCT R	WFR	0	IEN		0		DRCT R
		Туре	rw	rw	r	rw		r		rw
CEH	ADC_VFCR Reset: 00H	Bit Field		(	0		VFC3	VFC2	VFC1	VFC0
	Valid Flag Clear Register	Туре			r		W	W	w	W
RMAP =	0, PAGE 5									
CA <sub>H</sub>	ADC_CHINFR Reset: 00 <sub>H</sub> Channel Interrupt Flag Register	Bit Field	CHINF 7	CHINF 6	CHINF 5	CHINF 4	CHINF 3	CHINF 2	CHINF 1	CHINF 0
		Туре	rh	rh	rh	rh	rh	rh	rh	rh
СВН	ADC_CHINCR Reset: 00 <sub>H</sub> Channel Interrupt Clear Register	Bit Field	CHINC 7	CHINC 6	CHINC 5	CHINC 4	CHINC 3	CHINC 2	CHINC 1	CHINC 0
		Туре	W	W	W	W	W	W	w	w
cc <sup>H</sup>	ADC_CHINSR Reset: 00 <sub>H</sub> Channel Interrupt Set Register	Bit Field	CHINS 7	CHINS 6	CHINS 5	CHINS 4	CHINS 3	CHINS 2	CHINS 1	CHINS 0
		Туре	w	W	W	w	W	w	w	w
CDH	ADC_CHINPR Reset: 00 <sub>H</sub> Channel Interrupt Node Pointer	Bit Field	CHINP 7	CHINP 6	CHINP 5	CHINP 4	CHINP 3	CHINP 2	CHINP 1	CHINP 0
	Register	Туре	rw	rw	rw	rw	rw	rw	rw	rw
CEH	ADC_EVINFR Reset: 00 <sub>H</sub> Event Interrupt Flag Register	Bit Field	EVINF 7	EVINF 6	EVINF 5	EVINF 4		0	EVINF 1	EVINF 0
		Туре	rh	rh	rh	rh		r	rh	rh
CF <sub>H</sub>	ADC_EVINCR Reset: 00 <sub>H</sub> Event Interrupt Clear Flag	Bit Field	EVINC 7	EVINC 6	EVINC 5	EVINC 4		0	EVINC 1	EVINC 0
	Register	Туре	w	W	W	w		r	w	w
D2 <sub>H</sub>	ADC_EVINSR Reset: 00 <sub>H</sub> Event Interrupt Set Flag Register	Bit Field	EVINS 7	EVINS 6	EVINS 5	EVINS 4	(	0	EVINS 1	EVINS 0
		Туре	w	W	W	w		r	w	w
D3 <sub>H</sub>	ADC_EVINPR Reset: 00 <sub>H</sub> Event Interrupt Node Pointer	Bit Field	EVINP 7	EVINP 6	EVINP 5	EVINP 4		0	EVINP 1	EVINP 0
	Register	Туре	rw	rw	rw	rw		r	rw	rw
RMAP =	= 0, PAGE 6									
CA <sub>H</sub>	ADC_CRCR1 Reset: 00 <sub>H</sub> Conversion Request Control	Bit Field	CH7	CH6	CH5	CH4			0	
	Register 1	Туре	rwh	rwh	rwh	rwh			r	
CB <sub>H</sub>	ADC_CRPR1 Reset: 00 <sub>H</sub> Conversion Request Pending	Bit Field Type	CHP7	CHP6	CHP5 rwh	CHP4 rwh			0 r	
	Register 1	71								



# Table 11 ADC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
cc <sub>H</sub>	ADC_CRMR1 Reset: 00 <sub>H</sub> Conversion Request Mode	Bit Field	Rsv	LDEV	CLRP ND	SCAN	ENSI	ENTR	0	ENGT
	Register 1	Туре	r	W	W	rw	rw	rw	r	rw
CDH	ADC_QMR0 Reset: 00 <sub>H</sub> Queue Mode Register 0	Bit Field	CEV	TREV	FLUS H	CLRV	0	ENTR	0	ENGT
		Туре	W	W	W	W	r	rw	r	rw
CEH	ADC_QSR0 Reset: 20 <sub>H</sub> Queue Status Register 0	Bit Field	Rsv	0	EMPT Y	EV	(	0	FILL	
		Туре	r	ŗ	rh	rh		r	r	h
CF <sub>H</sub>	ADC_Q0R0 Reset: 00H	Bit Field	EXTR	ENSI	RF	V	0	F	REQCHNI	2
	Queue 0 Register 0	Туре	rh	rh	rh	rh	r		rh	
D2 <sub>H</sub>	ADC_QBUR0 Reset: 00H	Bit Field	EXTR	ENSI	RF	V	0	F	REQCHNI	2
	Queue Backup Register 0	Туре	rh	rh	rh	rh	r	rh		
D2 <sub>H</sub>	ADC_QINR0 Reset: 00H	Bit Field	EXTR	ENSI	RF	(	)	REQCHNR		2
	Queue Input Register 0	Туре	W	W	W	ļ	-	w		



## 3.2.4.8 Timer 2 Compare/Capture Unit Registers

The Timer 2 Compare/Capture Unit SFRs can be accessed in the standard memory area (RMAP = 0).

Table 12 T2CCU Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0		
RMAP =	= 0			I		I		I.	ı	I.		
C7 <sub>H</sub>	T2_PAGE Reset: 00H	Bit Field	0	P	ST	NR	0		PAGE			
	Page Register	Туре	V	V	٧	V	r		rwh			
RMAP =	= 0, PAGE 0											
C0H	T2_T2CON Reset: 00 <sub>H</sub> Timer 2 Control Register	Bit Field	TF2	EXF2	(	)	EXEN 2	TR2	C/T2	CP/ RL2		
		Туре	rwh	rwh	ا	r	rw	rwh	rw	rw		
C1 <sub>H</sub>	T2_T2MOD Reset: 00 <sub>H</sub> Timer 2 Mode Register	Bit Field	T2RE GS	T2RH EN	EDGE SEL	PREN		T2PRE		DCEN		
		Туре	rw	rw	rw	rw		rw		rw		
C2 <sub>H</sub>	T2_RC2L Reset: 00 <sub>H</sub>	Bit Field				R	C2					
	Timer 2 Reload/Capture Register Low	Туре				rv	vh					
C3 <sub>H</sub>	T2_RC2H Reset: 00H	Bit Field				R	C2					
	Timer 2 Reload/Capture Register High	Туре				rv	vh					
C4 <sub>H</sub>	T2_T2L Reset: 00H	Bit Field				T⊦	IL2					
	Timer 2 Register Low	Туре				rv	vh					
C5 <sub>H</sub>	T2_T2H Reset: 00H	Bit Field				TH	IL2					
	Timer 2 Register High	Туре				rv	vh					
C6 <sub>H</sub>	T2_T2CON1 Reset: 03 <sub>H</sub> Timer 2 Control Register 1	Bit Field			(	)			TF2EN	EXF2E N		
		Туре			l	r			rw	rw		
RMAP =	= 0, PAGE 1											
C0H	T2CCU_CCEN Reset: 00H	Bit Field	CC	:M3	CC	M2	CC	:M1	CC	:M0		
	T2CCU Capture/Compare Enable Register	Туре	n	W	r	W	r	W	r	W		
C1 <sub>H</sub>	T2CCU_CCTBSELReset: 00 <sub>H</sub> T2CCU Capture/Compare Time	Bit Field	CASC	CCTT OV	CCTB 5	CCTB 4	CCTB 3	CCTB 2	CCTB 1	CCTB 0		
	Base Select Register	Туре	rw	rwh	rw	rw	rw	rw	rw	rw		
C2 <sub>H</sub>	T2CCU_CCTRELLReset: 00H	Bit Field				ССТ	REL					
	T2CCU Capture/Compare Timer Reload Register Low	Туре				r	W	ı				
C3 <sub>H</sub>	T2CCU_CCTRELHReset: 00H	Bit Field				ССТ	REL	REL				
	T2CCU Capture/Compare Timer Reload Register High	Туре				r	w					
C4 <sub>H</sub>	T2CCU_CCTL Reset: 00H	Bit Field				C	СТ					
	T2CCU Capture/Compare Timer Register Low	Туре				rv	vh					



# Table 12 T2CCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
C5 <sub>H</sub>	T2CCU_CCTH Reset: 00H	Bit Field			<u>I</u>	C	CT			
	T2CCU Capture/Compare Timer Register High	Туре				rv	vh			
C6 <sub>H</sub>	T2CCU_CCTCON Reset: 00 <sub>H</sub> T2CCU CaptureCcompare	Bit Field		ССТ	PRE		CCTO VF	CCTO VEN	TIMSY N	CCTS T
	Timer Control Register	Туре		r	w		rwh	rw	rw	rw
RMAP =	: 0, PAGE 2									
C0H	T2CCU_COSHDWReset: 00 <sub>H</sub> T2CCU Capture/compare	Bit Field	ENSH DW	TXOV	COOU T5	COOU T4	COOU T3	COOU T2	COOU T1	COOU T0
	Enable Register	Туре	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh
C1 <sub>H</sub>	T2CCU_CC0L Reset: 00 <sub>H</sub> T2CCU Capture/Compare	Bit Field				CC/	/ALL			
	Register 0 Low	Туре				rv	vh			
C2 <sub>H</sub>	T2CCU_CC0H Reset: 00H	Bit Field				CCV	'ALH			
	T2CCU Capture/compare Register 0 High	Туре	•							
C3 <sub>H</sub>	T2CCU_CC1L Reset: 00H	Bit Field								
	T2CCU Capture/compare Register 1 Low	Туре								
C4 <sub>H</sub>	T2CCU_CC1H Reset: 00H	Bit Field								
	T2CCU Capture/compare Register 1 High	Туре	pe rwh							
C5 <sub>H</sub>	T2CCU_CC2L Reset: 00H	Bit Field								
	T2CCU Capture/compare Register 2 Low	Туре				rv	vh			
C6 <sub>H</sub>	T2CCU_CC2H Reset: 00H	Bit Field				CCV	'ALH			
	T2CCU Capture/compare Register 2 High	Туре				rv	vh			
RMAP =	: 0, PAGE 3									
C0H	T2CCU_COCON Reset: 00 <sub>H</sub> T2CCU Compare Control	Bit Field	CCM5	CCM4	CM5F	CM4F	POLB	POLA	CON	ИOD
	Register	Туре	rw	rw	rwh	rwh	rw	rw	n	N
C1 <sub>H</sub>	T2CCU_CC3L Reset: 00H	Bit Field				CC/	/ALL			
	T2CCU Capture/compare Register 3 Low	Туре				rv	vh			
C2 <sub>H</sub>	T2CCU_CC3H Reset: 00H	Bit Field				CCV	'ALH			
	T2CCU Capture/compare Register 3 High	Туре				rv	vh			
C3 <sub>H</sub>	T2CCU_CC4L Reset: 00H	Bit Field				CC/	/ALL			
	T2CCU Capture/compare Register 4 Low	Туре	e rwh							
C4 <sub>H</sub>	T2CCU_CC4H Reset: 00 <sub>H</sub>	Bit Field				CCV	'ALH			
	T2CCU Capture/compare Register 4 High	Туре				rv	vh			
C5 <sub>H</sub>	T2CCU_CC5L Reset: 00 <sub>H</sub> T2CCU Capture/compare	Bit Field				CC/	/ALL			
	Register 5 Low	Туре				rv	vh			
C6 <sub>H</sub>	T2CCU_CC5H Reset: 00 <sub>H</sub>	Bit Field	t Field CCVALH							
	T2CCU Capture/compare Register 5 High	Туре				rv	vh			



Table 12 T2CCU Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	0, PAGE 4									
C2 <sub>H</sub>	T2CCU_CCTDTCLReset: 00H	Bit Field				Dī	ГМ			
	T2CCU Capture/Compare Timer Dead-Time Control Register Low	Туре				r	N			
C3 <sub>H</sub>	T2CCU_CCTDTCHReset: 00 <sub>H</sub> T2CCU Capture/Compare	Bit Field	DTRE S	DTR2	DTR1	DTR0	DTLEV	DTE2	DTE1	DTE0
	Timer Dead-Time Control Register High	Туре	rwh	rh	rh	rh	rw	rw	rw	rw

# 3.2.4.9 Timer 21 Registers

The Timer 21 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 13 T21 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	: 1				•		•			
C0H	T21_T2CON Reset: 00 <sub>H</sub> Timer 2 Control Register	Bit Field	TF2	EXF2	(	)	EXEN 2	TR2	C/T2	CP/ RL2
		Туре	rwh	rwh		r	rw	rwh	rw	rw
C1 <sub>H</sub>	T21_T2MOD Reset: 00 <sub>H</sub> Timer 2 Mode Register	Bit Field	T2RE GS	T2RH EN	EDGE SEL	PREN		T2PRE		DCEN
		Туре	rw	rw	rw	rw	rw	rw	rw	rw
C2 <sub>H</sub>	T21_RC2L Reset: 00H	Bit Field				R	C2			
	Timer 2 Reload/Capture Register Low	Туре				rv	vh			
C3 <sub>H</sub>	T21_RC2H Reset: 00H	Bit Field				R	C2			
	Timer 2 Reload/Capture Register High	Туре				rv	vh			
C4 <sub>H</sub>	T21_T2L Reset: 00 <sub>H</sub>	Bit Field				TH	IL2			
	Timer 2 Register Low	Туре				rv	vh			
C5 <sub>H</sub>	T21_T2H Reset: 00H	Bit Field				TH	IL2			
	Timer 2 Register High	Туре	rwh							
C6 <sub>H</sub>	T21_T2CON1 Reset: 03 <sub>H</sub> Timer 2 Control Register 1	Bit Field					EXF2E N			
		Туре				7			rw	rw

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# 3.2.4.10 CCU6 Registers

The CCU6 SFRs can be accessed in the standard memory area (RMAP = 0).

Table 14 CCU6 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	= 0	•		•						
A3 <sub>H</sub>	CCU6_PAGE Reset: 00H	Bit Field	С	)P	ST	NR	0		PAGE	
	Page Register	Туре	١	N	١	V	r		rwh	
RMAP =	= 0, PAGE 0		•		•		•	•		
9A <sub>H</sub>	CCU6_CC63SRL Reset: 00H	Bit Field				CC6	3SL			
	Capture/Compare Shadow Register for Channel CC63 Low	Туре				r	W			
9B <sub>H</sub>	CCU6_CC63SRH Reset: 00H	Bit Field				CC6	3SH			
	Capture/Compare Shadow Register for Channel CC63 High	Туре				r	W			
9CH	CCU6_TCTR4L Reset: 00 <sub>H</sub> Timer Control Register 4 Low	Bit Field	T12 STD	T12 STR	(	)	DT RES	T12 RES	T12R S	T12R R
		Туре	W	W	ı	r	W	W	W	W
9D <sub>H</sub>	CCU6_TCTR4H Reset: 00 <sub>H</sub> Timer Control Register 4 High	Bit Field	T13 STD	T13 STR		0		T13 RES	T13R S	T13R R
		Туре	W	W		r		W	W	W
9E <sub>H</sub>	CCU6_MCMOUTSL Reset: 00 <sub>H</sub> Multi-Channel Mode Output Shadow	Bit Field	STRM CM	0			MCI	MPS		
	Register Low	Туре	W	r			r	W		
9F <sub>H</sub>	CCU6_MCMOUTSH Reset: 00 <sub>H</sub> Multi-Channel Mode Output Shadow	Bit Field	STRH P	0		CURHS			EXPHS	
	Register High	Туре	W	r		rw			rw	
A4 <sub>H</sub>	CCU6_ISRL Reset: 00 <sub>H</sub> Capture/Compare Interrupt Status	Bit Field	RT12 PM	RT12 OM	RCC6 2F	RCC6 2R	RCC6 1F	RCC6 1R	RCC6 0F	RCC6 0R
	Reset Register Low	Туре	W	W	W	W	W	W	W	W
A5 <sub>H</sub>	CCU6_ISRH Reset: 00 <sub>H</sub> Capture/Compare Interrupt Status	Bit Field	RSTR	RIDLE	RWH E	RCHE	0	RTRP F	RT13 PM	RT13 CM
	Reset Register High	Туре	W	W	W	W	r	W	W	w
A6 <sub>H</sub>	CCU6_CMPMODIFL Reset: 00 <sub>H</sub> Compare State Modification Register	Bit Field	0	MCC6 3S		0		MCC6 2S	MCC6 1S	MCC6 0S
	Low	Туре	r	W		r		W	W	W
A7 <sub>H</sub>	CCU6_CMPMODIFH Reset: 00 <sub>H</sub> Compare State Modification Register	Bit Field	0	MCC6 3R					MCC6 0R	
	High	Туре	r	r w r w w					W	
FA <sub>H</sub>	CCU6_CC60SRL Reset: 00H	Bit Field		CC60SL						
	Capture/Compare Shadow Register for Channel CC60 Low	Туре		rwh						
FBH	CCU6_CC60SRH Reset: 00 <sub>H</sub>	Bit Field		CC60SH						
	Capture/Compare Shadow Register for Channel CC60 High	Туре	/pe rwh							



# Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7 6 5 4 3 2 1 0							0		
FC <sub>H</sub>	CCU6_CC61SRL Reset: 00H	Bit Field		•		CC6	1SL					
	Capture/Compare Shadow Register for Channel CC61 Low	Туре				rv	vh					
FDH	CCU6_CC61SRH Reset: 00H	Bit Field				CC6	1SH					
	Capture/Compare Shadow Register for Channel CC61 High	Туре				rv	vh					
FE <sub>H</sub>	CCU6_CC62SRL Reset: 00H	Bit Field				CC6	2SL					
	Capture/Compare Shadow Register for Channel CC62 Low	Туре				rv	vh					
FFH	CCU6_CC62SRH Reset: 00H	Bit Field				CC6	2SH					
	Capture/Compare Shadow Register for Channel CC62 High	Туре	rwh									
RMAP =	= 0, PAGE 1											
9A <sub>H</sub>	CCU6_CC63RL Reset: 00H	Bit Field				CC6	3VL					
	Capture/Compare Register for Channel CC63 Low	Туре				r	h					
9B <sub>H</sub>	CCU6_CC63RH Reset: 00 <sub>H</sub>	Bit Field				CC6	3VH					
	Capture/Compare Register for Channel CC63 High	Туре				r	h					
9C <sub>H</sub>	CCU6_T12PRL Reset: 00H	Bit Field				T12	PVL					
	Timer T12 Period Register Low	Туре				rv	vh					
9DH	CCU6_T12PRH Reset: 00H	Bit Field				T12	PVH					
	Timer T12 Period Register High	Туре				rv	vh					
9E <sub>H</sub>	CCU6_T13PRL Reset: 00 <sub>H</sub> Timer T13 Period Register Low	Bit Field				T13	PVL					
	-	Туре					vh					
9F <sub>H</sub>	CCU6_T13PRH Reset: 00 <sub>H</sub> Timer T13 Period Register High	Bit Field					PVH					
	-	Type					vh					
<sup>A4</sup> H	CCU6_T12DTCL Reset: 00 <sub>H</sub> Dead-Time Control Register for	Bit Field					ΓM					
	Timer T12 Low	Туре	-		l		w 		l	l		
A5 <sub>H</sub>	CCU6_T12DTCH Reset: 00 <sub>H</sub> Dead-Time Control Register for	Bit Field	0	DTR2	DTR1	DTR0	0	DTE2	DTE1	DTE0		
	Timer T12 High	Туре	r	rh	rh	rh	r	rw	rw	rw		
A6 <sub>H</sub>	CCU6_TCTR0L Reset: 00 <sub>H</sub> Timer Control Register 0 Low	Bit Field	СТМ	CDIR	STE1 2	T12R	T12 PRE		T12CLK			
		Туре	rw	rh	rh	rh	rw		rw			
A7 <sub>H</sub>	CCU6_TCTR0H Reset: 00 <sub>H</sub> Timer Control Register 0 High	Bit Field	(	0	STE1	T13R	T13 PRE		T13CLK			
		Туре	r rh rh rw rw									
FA <sub>H</sub>	CCU6_CC60RL Reset: 00H	Bit Field				CC6	0VL					
	Capture/Compare Register for Channel CC60 Low	Туре				r	h					
FB <sub>H</sub>	CCU6_CC60RH Reset: 00H	Bit Field				CC6	60VH					
	Capture/Compare Register for Channel CC60 High	Туре				r	h					
FCH	CCU6_CC61RL Reset: 00H	Bit Field				CC6	31VL					
	Capture/Compare Register for Channel CC61 Low	Туре				r	rh					



# Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FDH	CCU6_CC61RH Reset: 00H	Bit Field		l.		CC6	1VH	l.	l.	
	Capture/Compare Register for Channel CC61 High	Туре				r	h			
FE <sub>H</sub>	CCU6_CC62RL Reset: 00H	Bit Field				CC6	2VL			
	Capture/Compare Register for Channel CC62 Low	Туре				r	h			
FF <sub>H</sub>	CCU6_CC62RH Reset: 00H	Bit Field				CC6	2VH			
	Capture/Compare Register for Channel CC62 High	Туре				r	h			
RMAP =	= 0, PAGE 2									
9A <sub>H</sub>	CCU6_T12MSELL Reset: 00H	Bit Field	MSEL61				MSEL60			
	T12 Capture/Compare Mode Select Register Low	Туре		r	w			r	w	
9B <sub>H</sub>	CCU6_T12MSELH Reset: 00 <sub>H</sub>	Bit Field	DBYP		HSYNC			MSE	EL62	
	T12 Capture/Compare Mode Select Register High	Туре	rw		rw			r	W	
9CH	CCU6_IENL Reset: 00 <sub>H</sub> Capture/Compare Interrupt Enable Register Low	Bit Field	ENT1 2 PM	ENT1 2 OM	ENCC 62F	ENCC 62R	ENCC 61F	ENCC 61R	ENCC 60F	ENCC 60R
		Туре	rw	rw	rw	rw	rw	rw	rw	rw
9D <sub>H</sub>	CCU6_IENH Reset: 00 <sub>H</sub> Capture/Compare Interrupt Enable	Bit Field	EN STR	EN IDLE	EN WHE	EN CHE	0	EN TRPF	ENT1 3PM	ENT1 3CM
	Register High	Туре	rw	rw	rw	rw	r	rw	rw	rw
9E <sub>H</sub>	CCU6_INPL Reset: 40 <sub>H</sub>	Bit Field	INP	CHE	INPO	CC62	INPCC61		INPO	C60
	Capture/Compare Interrupt Node Pointer Register Low	Туре	r	w	r	w	r	w	r	w
9F <sub>H</sub>	CCU6_INPH Reset: 39 <sub>H</sub>	Bit Field	(	)	INF	T13	INPT12		INP	ERR
	Capture/Compare Interrupt Node Pointer Register High	Туре		r	r	w	rw		r	W
A4 <sub>H</sub>	CCU6_ISSL Reset: 00 <sub>H</sub> Capture/Compare Interrupt Status	Bit Field	ST12 PM	ST12 OM	SCC6 2F	SCC6 2R	SCC6 1F	SCC6 1R	SCC6 0F	SCC6 0R
	Set Register Low	Туре	W	W	w	W	W	W	W	w
A5 <sub>H</sub>	CCU6_ISSH Reset: 00 <sub>H</sub> Capture/Compare Interrupt Status	Bit Field	SSTR	SIDLE	SWHE	SCHE	SWH C	STRP F	ST13 PM	ST13 CM
	Set Register High	Туре	W	W	w	W	W	W	W	W
A6 <sub>H</sub>	CCU6_PSLR Reset: 00 <sub>H</sub> Passive State Level Register	Bit Field	PSL63	0			P	SL		
	Passive State Level Register	Туре	rwh	r			rv	vh		
A7 <sub>H</sub>	CCU6_MCMCTR Reset: 00 <sub>H</sub> Multi-Channel Mode Control Register	Bit Field	(	)	SW	SYN	0		SWSEL	
	Wulti-Charmer Wode Control Negister	Туре	r rw r rw							
FA <sub>H</sub>	CCU6_TCTR2L Reset: 00 <sub>H</sub> Timer Control Register 2 Low	Bit Field	0	0 T13TED T13TEC T13 SSC			T12 SSC			
		Туре	r	r	w		rw		rw	rw
FB <sub>H</sub>	CCU6_TCTR2H Reset: 00 <sub>H</sub> Timer Control Register 2 High	Bit Field			0		T13F	RSEL	T12F	RSEL
	Timor Control Negister 2 High	Туре	r rw			r	W			
FC <sub>H</sub>	CCU6_MODCTRL Reset: 00 <sub>H</sub> Modulation Control Register Low	Bit Field	MCM EN	0			T12M	ODEN		
		Туре	rw	r			r	W		



## Table 14 CCU6 Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
FD <sub>H</sub>	CCU6_MODCTRH Reset: 00 <sub>H</sub> Modulation Control Register High	Bit Field	ECT1 30	0			T13M	ODEN		
		Туре	rw	r			r	W		
FE <sub>H</sub>	CCU6_TRPCTRL Reset: 00 <sub>H</sub> Trap Control Register Low	Bit Field			0			TRPM 2	TRPM 1	TRPM 0
		Туре			r			rw	rw	rw
FF <sub>H</sub>	CCU6_TRPCTRH Reset: 00 <sub>H</sub> Trap Control Register High	Bit Field	TRPP EN	TRPE N13						
		Туре	rw	rw			r	W		
RMAP =	= 0, PAGE 3									
9A <sub>H</sub>	CCU6_MCMOUTL Reset: 00H	Bit Field	0	R			MC	MP		
	Multi-Channel Mode Output Register Low	Туре	r	rh			r	h		
9B <sub>H</sub>	CCU6_MCMOUTH Reset: 00H	Bit Field	(	)		CURH			EXPH	
	Multi-Channel Mode Output Register High	Туре	!	r		rh			rh	
9CH	CCU6_ISL Reset: 00 <sub>H</sub> Capture/Compare Interrupt Status	Bit Field	T12 PM	T12 OM	ICC62 F	ICC62 R	ICC61 F	ICC61 R	ICC60 F	ICC60 R
	Register Low	Туре	rh	rh	rh	rh	rh	rh	rh	rh
9D <sub>H</sub>	CCU6_ISH Reset: 00 <sub>H</sub> Capture/Compare Interrupt Status	Bit Field	STR	IDLE	WHE	CHE	TRPS	TRPF	T13 PM	T13 CM
	Register High	Туре	rh	rh	rh	rh	rh	rh	rh	rh
9E <sub>H</sub>	CCU6_PISEL0L Reset: 00H	Bit Field	IST	RP	ISC	C62	ISC	C61	ISC	C60
	Port Input Select Register 0 Low	Туре	n	W	r	W	r	rw		W
9F <sub>H</sub>	CCU6_PISEL0H Reset: 00H	Bit Field	IST1	2HR	ISP	OS2	ISP	OS1	ISP	OS0
	Port Input Select Register 0 High	Туре	n	W	r	W	r	W	n	W
A4 <sub>H</sub>	CCU6_PISEL2 Reset: 00 <sub>H</sub> Port Input Select Register 2	Bit Field			0		IST1	3HR		
	Port input Select Register 2	Туре			l	r			n	W
FA <sub>H</sub>	CCU6_T12L Reset: 00 <sub>H</sub>	Bit Field				T12	CVL			
	Timer T12 Counter Register Low	Туре				rv	vh			
FBH	CCU6_T12H Reset: 00 <sub>H</sub> Timer T12 Counter Register High	Bit Field				T12	CVH			
	Timer 112 Counter Register High	Туре				rv	vh			
FC <sub>H</sub>	CCU6_T13L Reset: 00 <sub>H</sub> Timer T13 Counter Register Low	Bit Field				T13	CVL			
	Timer 110 Counter Register Low	Туре				rv	vh			
FD <sub>H</sub>	CCU6_T13H Reset: 00 <sub>H</sub> Timer T13 Counter Register High	Bit Field			T13CVH					
	Timor i to Counter Negister High	Туре				rv	vh			
FE <sub>H</sub>	CCU6_CMPSTATL Reset: 00 <sub>H</sub> Compare State Register Low	Bit Field	0	CC63 ST	CC POS2	CC POS1	CC POS0	CC62 ST	CC61 ST	CC60 ST
		Туре	r	rh	rh	rh	rh	rh	rh	rh
FF <sub>H</sub>	CCU6_CMPSTATH Reset: 00 <sub>H</sub> Compare State Register High	Bit Field	T13IM	COUT 63PS	COUT 62PS	CC62 PS	COUT 61PS	CC61 PS	COUT 60PS	CC60 PS
		Туре	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh



## 3.2.4.11 UART1 Registers

The UART1 SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 15 UART1 Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0	
RMAP =	= 1		I.	ı	l.	ı	l.	ı		l .	
C8H	SCON Reset: 00 <sub>H</sub>	Bit Field	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	
	Serial Channel Control Register	Туре	rw	rw	rw	rw	rw	rwh	rwh	rwh	
C9 <sub>H</sub>	SBUF Reset: 00 <sub>H</sub>	Bit Field				V	AL				
	Serial Data Buffer Register	Туре				rv	vh				
CA <sub>H</sub>	BCON Reset: 00 <sub>H</sub>	Bit Field		(	)			BRPRE		R	
	Baud Rate Control Register	Туре			r			rw		rw	
СВН	BG Reset: 00 <sub>H</sub>	Bit Field				BR_V	'ALUE				
	Baud Rate Timer/Reload Register	Туре				rv	vh				
ССН	FDCON Reset: 00 <sub>H</sub>	Bit Field			0			NDOV	FDM	FDEN	
	Fractional Divider Control Register	Туре			r			rwh	rw	rw	
CDH	FDSTEP Reset: 00 <sub>H</sub>	Bit Field				ST	EP				
	Fractional Divider Reload Register	Туре				r	W				
CEH	FDRES Reset: 00 <sub>H</sub>	Bit Field				RES	SULT				
	Fractional Divider Result Register	Туре	rh								
CF <sub>H</sub>	SCON1 Reset: 07 <sub>H</sub> Serial Channel Control Register	Bit Field	eld 0 NDOV TIEN EN					RIEN			
	1	Туре			r			rw	rw	rw	

## 3.2.4.12 SSC Registers

The SSC SFRs can be accessed in the standard memory area (RMAP = 0).

Table 16 SSC Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	0									
A9 <sub>H</sub>	SSC_PISEL Reset: 00H	Bit Field			0			CIS	SIS	MIS
	Port Input Select Register	Туре			r			rw	rw	rw
$AA_H$	SSC_CONL Reset: 00H	Bit Field	LB	РО	PH	НВ		В	М	
	Control Register Low Programming Mode	Туре	rw	rw	rw	rw		r	W	
$AA_H$	SSC_CONL Reset: 00H	Bit Field		(	)			В	С	
	Control Register Low Operating Mode	Туре			r		rh			
AB <sub>H</sub>	SSC_CONH Reset: 00H	Bit Field	EN	MS	0	AREN	BEN	PEN	REN	TEN
	Control Register High Programming Mode	Туре	rw	rw	r	rw	rw	rw	rw	rw



**Table 16** SSC Register Overview (cont'd)

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
AB <sub>H</sub>	SSC_CONH Reset: 00H	Bit Field	EN	MS	0	BSY	BE	PE	RE	TE
	Control Register High Operating Mode	Туре	rw rw r rh rwh rwh rwh						rwh	
AC <sub>H</sub>	SSC_TBL Reset: 00H	Bit Field				TB_V	ALUE			
	Transmitter Buffer Register Lov	Туре				r	W			
$AD_H$	SSC_RBL Reset: 00H	Bit Field				RB_V	ALUE			
	Receiver Buffer Register Low	Туре				r	h			
AE <sub>H</sub>	SSC_BRL Reset: 00H	Bit Field				BR_V	ALUE			
	Baud Rate Timer Reload Register Low	Туре				r	W			
AF <sub>H</sub>	SSC_BRH Reset: 00H	Bit Field	BR_VALUE							
	Baud Rate Timer Reload Register High	Туре	rw						•	

#### 3.2.4.13 MultiCAN Registers

The MultiCAN SFRs can be accessed in the standard memory area (RMAP = 0).

Table 17 CAN Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0		
RMAP =	: 0			•		•			•			
D8 <sub>H</sub>	ADCON Reset: 00H	Bit Field	V3	V2	V1	V0	AUAD		BSY	RWEN		
	CAN Address/Data Control Register	Туре	rw	rw	rw	rw	r	w	rh	rw		
D9 <sub>H</sub>	ADL Reset: 00 <sub>H</sub>	Bit Field	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2		
	CAN Address Register Low	Туре	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh		
DA <sub>H</sub>	ADH Reset: 00 <sub>H</sub>	Bit Field		(	)		CA13	CA12	CA11	CA10		
	CAN Address Register High	Туре			r		rwh	rwh	rwh	rwh		
DB <sub>H</sub>	DATA0 Reset: 00 <sub>H</sub>	Bit Field				С	CD					
	CAN Data Register 0	Туре				rv	wh					
DCH	DATA1 Reset: 00 <sub>H</sub>	Bit Field				С	D					
	CAN Data Register 1	Туре				rv	vh					
DDH	DATA2 Reset: 00 <sub>H</sub>	Bit Field				С	D					
	CAN Data Register 2	Туре				rv	vh					
DEH	DATA3 Reset: 00 <sub>H</sub>	Bit Field	eld CD									
	CAN Data Register 3	Туре	rwh									

## 3.2.4.14 OCDS Registers

The OCDS SFRs can be accessed in the mapped memory area (RMAP = 1).



# Table 18 OCDS Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	: 1					ı		I		
E9 <sub>H</sub>	MMCR2 Reset: 8U <sub>H</sub> Monitor Mode Control 2	Bit Field	STMO DE	EXBC	DSUS P	MBCO N	ALTDI	MMEP	MMOD E	JENA
	Register	Туре	rw	rw	rw	rwh	rw	rwh	rh	rh
EA <sub>H</sub>	MEXTCR Reset: 0U <sub>H</sub>	Bit Field		(	)			BANI	KBPx	
	Memory Extension Control Register	Туре	r rw							
EBH	MMWR1 Reset: 00 <sub>H</sub>	Bit Field	ield MMWR1							
	Monitor Work Register 1	Туре				r	W			
ECH	MMWR2 Reset: 00 <sub>H</sub>	Bit Field				MM	WR2			
	Monitor Work Register 2	Туре				r	W			
F1 <sub>H</sub>	MMCR Reset: 00 <sub>H</sub> Monitor Mode Control Register	Bit Field	MEXIT _P	MEXIT	0	MSTE P	MRAM S_P	MRAM S	TRF	RRF
		Туре	w	rwh	r	rw	W	rwh	rh	rh
F2 <sub>H</sub>	MMSR Reset: 00 <sub>H</sub> Monitor Mode Status Register	Bit Field	MBCA M	MBCIN	EXBF	SWBF	HWB3 F	HWB2 F	HWB1 F	HWB0 F
		Туре	rw	rwh	rwh	rwh	rwh	rwh	rwh	rwh
F3 <sub>H</sub>	MMBPCR Reset: 00 <sub>H</sub> Breakpoints Control Register	Bit Field	SWBC	HW	B3C	HW	B2C	HWB1 C	HW	B0C
		Туре	rw	r	w	r	w	rw	n	w
F4 <sub>H</sub>	MMICR Reset: 00 <sub>H</sub> Monitor Mode Interrupt Control	Bit Field	DVEC T	DRET R	COMR ST	MSTS EL	MMUI E_P	MMUI E	RRIE_ P	RRIE
	Register	Туре	rwh	rwh	rwh	rh	W	rw	w	rw
F5 <sub>H</sub>	MMDR Reset: 00 <sub>H</sub>	Bit Field				MN	IRR			
	Monitor Mode Data Transfer Register Receive	Туре								
F6 <sub>H</sub>	HWBPSR Reset: 00 <sub>H</sub> Hardware Breakpoints Select	Bit Field		0		BPSEL _P		BPS	SEL	
	Register	Туре		r		W		r	W	
F7 <sub>H</sub>	HWBPDR Reset: 00 <sub>H</sub>	Bit Field				HWI	ЗРхх			
	Hardware Breakpoints Data Register	Туре	pe rw							



# 3.2.4.15 Flash Registers

The Flash SFRs can be accessed in the mapped memory area (RMAP = 1).

Table 19 Flash Register Overview

Addr	Register Name	Bit	7	6	5	4	3	2	1	0
RMAP =	: 1							•		
D1 <sub>H</sub>	FCON Reset: 10 <sub>H</sub> P-Flash Control Register	Bit Field	0	FBSY	YE	1	NVST R	MAS1	ERAS E	PROG
		Туре	r	rh	rwh	r	rw	rw	rw	rw
D2 <sub>H</sub>	EECON Reset: 10 <sub>H</sub> D-Flash Control Register	Bit Field	0	EEBS Y	YE	1	NVST R	MAS1	ERAS E	PROG
		Туре	r	rh	rwh	r	rw	rw	rw	rw
D3 <sub>H</sub>	FCS Reset: 80 <sub>H</sub> Flash Control and Status	Bit Field	1	SBEIE	FTEN	0	EEDE RR	EESE RR	FDER R	FSER R
	Register	Туре	r	rw	rwh	r	rwh	rwh	rwh	rwh
D4 <sub>H</sub>	FEAL Reset: 00 <sub>H</sub>	Bit Field				ECCE	ADDR			
	Flash Error Address Register, Low Byte	Туре				r	h			
D5 <sub>H</sub>	FEAH Reset: 00 <sub>H</sub>	Bit Field				ECCE	ADDR			
	Flash Error Address Register, High Byte	Туре				r	h			
D6 <sub>H</sub>	FTVAL Reset: 78 <sub>H</sub>	Bit Field	MODE				OFVAL			
	Flash Timer Value Register	Туре	rw				rw			
DD <sub>H</sub>	FCS1 Reset: 00 <sub>H</sub> Flash Control and Status	Bit Field				0				EEAB ORT
	Register 1	Туре				r				rwh



#### 3.3 Flash Memory

The Flash memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data. It is operated from a single 2.5 V supply from the Embedded Voltage Regulator (EVR) and does not require additional programming or erasing voltage. The pagination of the Flash memory allows each page to be erased independently.

#### **Features**

- In-System Programming (ISP) via UART
- In-Application Programming (IAP)
- Error Correction Code (ECC) for dynamic correction of single-bit errors
- Background program and erase operations for CPU load minimization
- Support for aborting erase operation
- Minimum program width
- · of 1-byte for D-Flash and 2-bytes for P-Flash
- 1-page minimum erase width
- 1-byte read access
- Flash is delivered in erased state (read all ones)
- Operating supply voltage: 2.5 V ± 7.5 %
- Read access time:  $1 \times t_{CCLK} = 38 \text{ ns}^{1)}$
- Program time for 1 wordline: 1.6 ms<sup>2)</sup>
- Page erase time: 20 ms
- · Mass erase time: 200 ms

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<sup>1)</sup> Values shown here are typical values.  $f_{\text{sys}}$  = 144 MHz ± 7.5% ( $f_{\text{CCLK}}$  = 24 MHz ± 7.5 %) is the maximum frequency range for Flash read access.

<sup>2)</sup> Values shown here are typical values.  $f_{\rm sys}$  = 144 MHz ± 7.5% ( $f_{\rm CCLK}$  = 24 MHz ± 7.5%) is the typical frequency range for Flash programming and erasing.  $f_{\rm sysmin}$  is used for obtaining the worst case timing.



Table 20 and Table 21 shows the Flash data retention and endurance targets for Industrial profile and Automotive profile respectively.

Table 20 Flash Data Retention and Endurance for Industrial Profile (Operating Conditions apply)

Retention	Endurance <sup>1)2)</sup>	Size	Remarks
Program Flash	•	•	
15 years	1000 cycles	up to 60 Kbytes	
Data Flash	·	·	•
15 years	1000 cycles	4 Kbytes	
10 years	10,000 cycles	4 Kbytes	
5 years	30,000 cycles	4 Kbytes	
1 year	100,000 cycles	4 Kbytes	SAF and SAX variant
	80,000 cycles		SAK variant

<sup>1)</sup> In Program Flash, one cycle refers to the programming of all pages in the flash bank and a mass erase.

Table 21 Flash Data Retention and Endurance for Automotive Profile (Operating Conditions apply)

Retention	Endurance <sup>1)2)</sup>	Size	Remarks
Program Flash			•
15 years	1000 cycles	up to 60 Kbytes	
Data Flash	•	·	<u> </u>
15 years	1000 cycles	4 Kbytes	
5 years	10,000 cycles	1 Kbytes	
2 years	15,000 cycles	512 Bytes	
2 years	30,000 cycles	256 Bytes	
1 year	100,000 cycles	128 Bytes	

<sup>1)</sup> In Program Flash, one cycle refers to the programming of all pages in the flash bank and a mass erase.

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<sup>2)</sup> In Data Flash, one cycle refers to the programming of all wordlines in a page and a page erase.

<sup>2)</sup> In Data Flash, one cycle refers to the programming of all wordlines in a page and a page erase.



#### 3.3.1 Flash Bank Pagination

The XC87x product family offers Flash devices with either 64 Kbytes or 52 Kbytes of embedded Flash memory. Each Flash device consists of a Program Flash (P-Flash) and a single Data Flash (D-Flash) bank. P-Flash has 120 pages of 8 wordlines per page with 64 bytes per wordline. D-Flash has 64 pages of 2 wordlines per page with 32 bytes per wordline. Both types can be used for code and data storage. The label "Data" neither implies that the D-Flash is mapped to the data memory region, nor that it can only be used for data storage. It is used to distinguish the different page width and wordline of each Flash bank.

The internal structure of each Flash bank represents a page architecture for flexible erase capability. The minimum erase width is always a complete page. The D-Flash bank is divided into smaller size for extended erasing and reprogramming capability; even numbers for each page size are provided to allow greater flexibility and the ability to adapt to a wide range of application requirements.



#### 3.4 Interrupt System

The XC800 Core supports one non-maskable interrupt (NMI) and 14 maskable interrupt requests. In addition to the standard interrupt functions supported by the core, e.g., configurable interrupt priority and interrupt masking, the XC87x interrupt system provides extended interrupt support capabilities such as the mapping of each interrupt vector to several interrupt sources to increase the number of interrupt sources supported, and additional status registers for detecting and determining the interrupt source.

#### 3.4.1 Interrupt Source

Figure 12 to Figure 16 give a general overview of the interrupt sources and nodes, and their corresponding control and status flags.

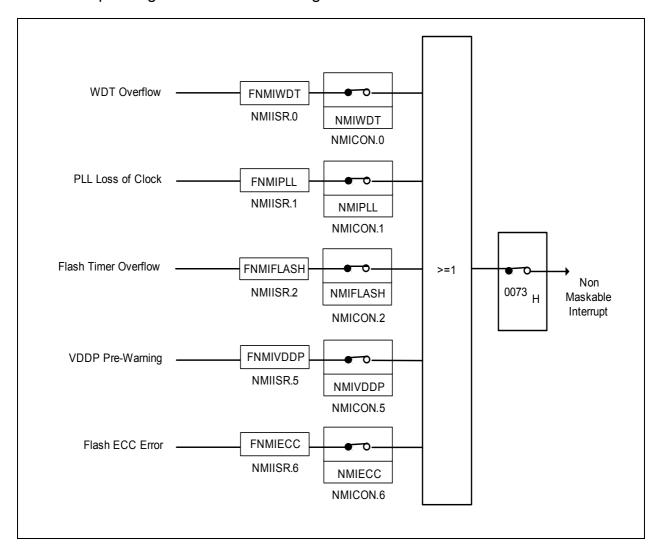


Figure 12 Non-Maskable Interrupt Request Sources



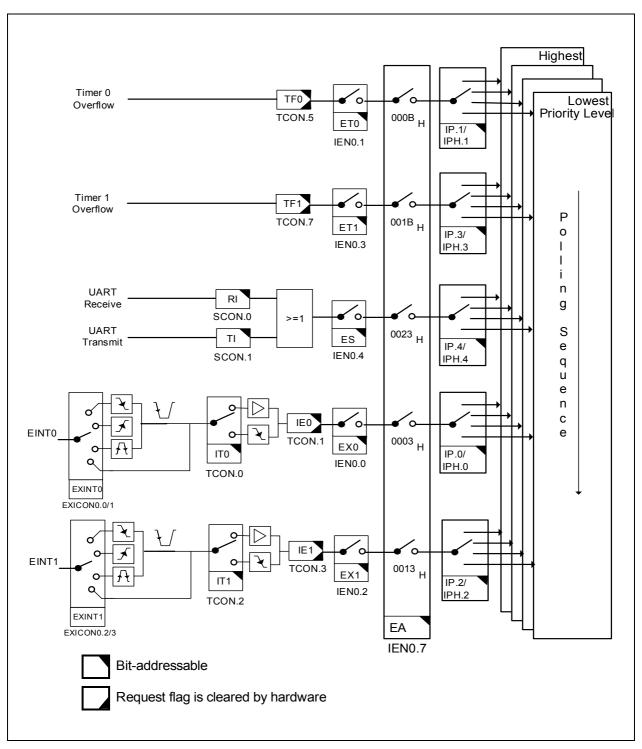


Figure 13 Interrupt Request Sources (Part 1)



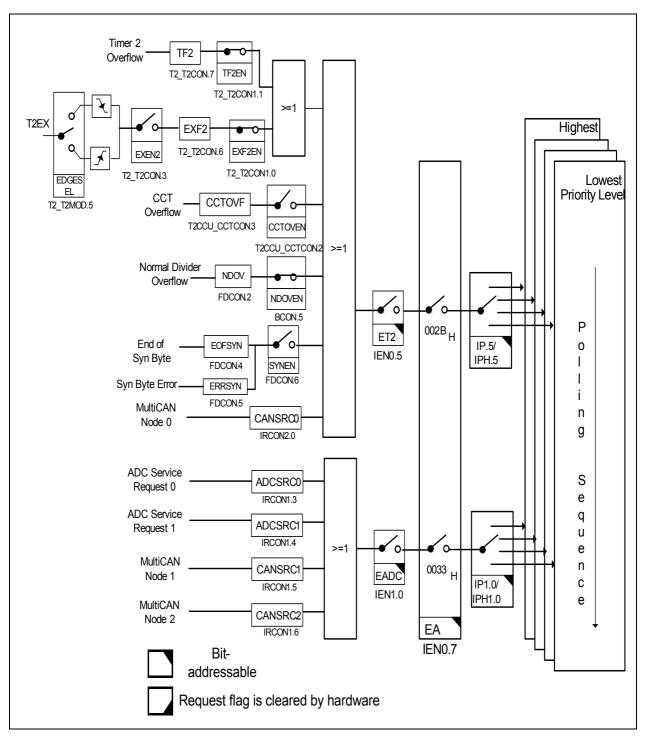


Figure 14 Interrupt Request Sources (Part 2)



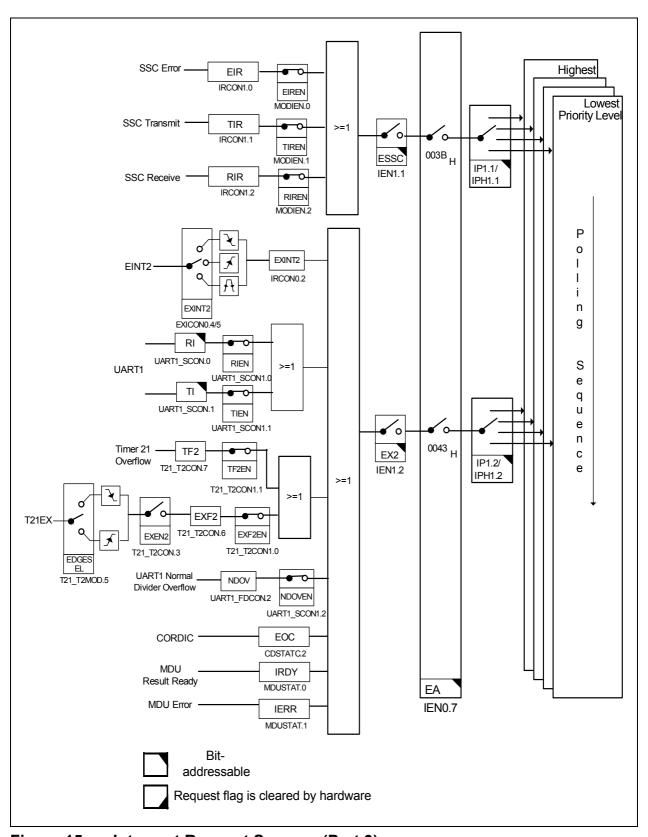


Figure 15 Interrupt Request Sources (Part 3)



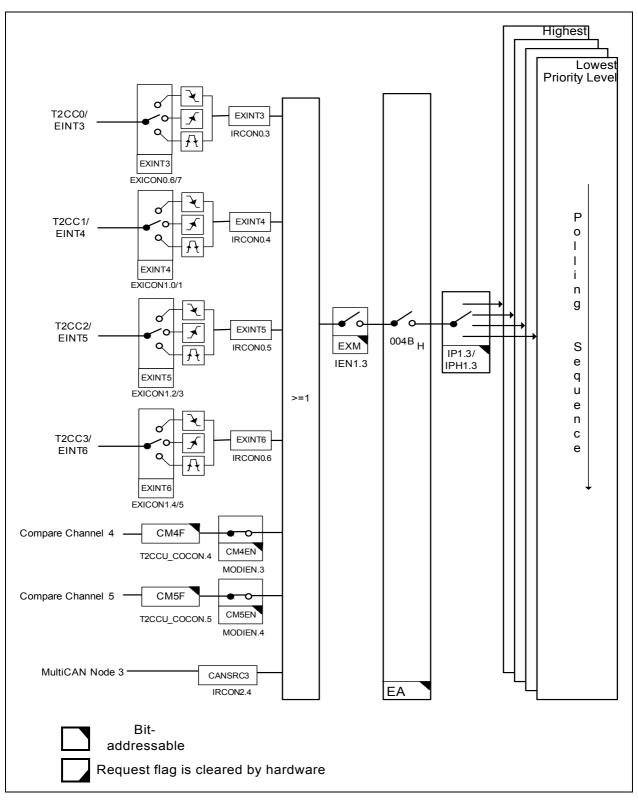


Figure 16 Interrupt Request Sources (Part 4)



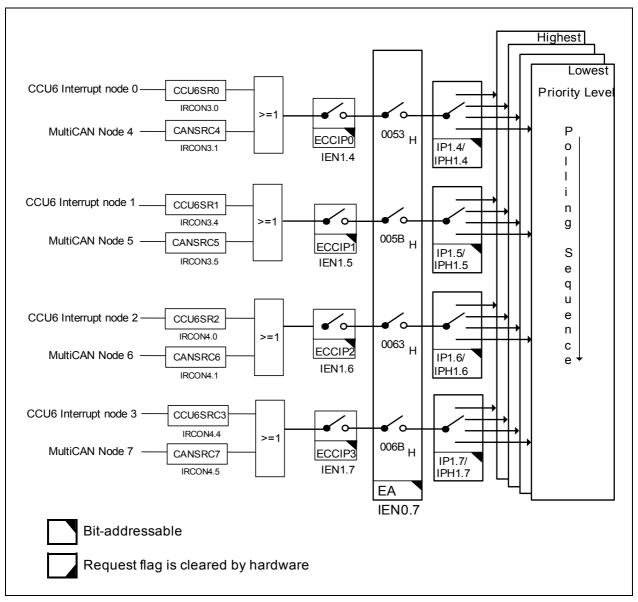


Figure 17 Interrupt Request Sources (Part 5)



# 3.4.2 Interrupt Source and Vector

Each interrupt event source has an associated interrupt vector address for the interrupt node it belongs to. This vector is accessed to service the corresponding interrupt node request. The interrupt service of each interrupt source can be individually enabled or disabled via an enable bit. The assignment of the XC87x interrupt sources to the interrupt vector address and the corresponding interrupt node enable bits are summarized in Table 22.

Table 22 Interrupt Vector Addresses

Interrupt Source	Vector Address	Assignment for XC87x	Enable Bit	SFR
NMI	0073 <sub>H</sub>	Watchdog Timer NMI	NMIWDT	NMICON
		PLL NMI	NMIPLL	
		Flash Timer NMI	NMIFLASH	
		V <sub>DDP</sub> Prewarning NMI	NMIVDDP	
		Flash ECC NMI	NMIECC	
XINTR0	0003 <sub>H</sub>	External Interrupt 0	EX0	IEN0
XINTR1	000B <sub>H</sub>	Timer 0	ET0	7
XINTR2	0013 <sub>H</sub>	External Interrupt 1	EX1	7
XINTR3	001B <sub>H</sub>	Timer 1	ET1	
XINTR4	0023 <sub>H</sub>	UART	ES	
XINTR5	002B <sub>H</sub>	T2CCU	ET2	
		UART Fractional Divider (Normal Divider Overflow)		
		MultiCAN Node 0		
		LIN		



Table 22 Interrupt Vector Addresses (cont'd)

Interrupt Source	Vector Address	Assignment for XC87x	Enable Bit	SFR
XINTR6	0033 <sub>H</sub>	0033 <sub>H</sub> MultiCAN Nodes 1 and 2		IEN1
		ADC[1:0]		
XINTR7	003B <sub>H</sub>	SSC	ESSC	
XINTR8	0043 <sub>H</sub>	External Interrupt 2	EX2	
		T21		
		CORDIC		
		UART1		
		UART1 Fractional Divider (Normal Divider Overflow)		
		MDU[1:0]		
XINTR9	004B <sub>H</sub>	External Interrupt 3	EXM	
		External Interrupt 4		
		External Interrupt 5		
		External Interrupt 6		
		T2CCU		
_		MultiCAN Node 3		
XINTR10	0053 <sub>H</sub>	CCU6 INP0	ECCIP0	
_		MultiCAN Node 4		
XINTR11	005B <sub>H</sub>	CCU6 INP1	ECCIP1	
		MultiCAN Node 5		
XINTR12	0063 <sub>H</sub>	CCU6 INP2	ECCIP2	
		MultiCAN Node 6		
XINTR13	006B <sub>H</sub>	CCU6 INP3	ECCIP3	
		MultiCAN Node 7		



# 3.4.3 Interrupt Priority

An interrupt that is currently being serviced can only be interrupted by a higher-priority interrupt, but not by another interrupt of the same or lower priority. Hence, an interrupt of the highest priority cannot be interrupted by any other interrupt request.

If two or more requests of different priority levels are received simultaneously, the request of the highest priority is serviced first. If requests of the same priority are received simultaneously, then an internal polling sequence determines which request is serviced first. Thus, within each priority level, there is a second priority structure determined by the polling sequence shown in **Table 23**.

Table 23 Priority Structure within Interrupt Level

Source	Level
Non-Maskable Interrupt (NMI)	(highest)
External Interrupt 0	1
Timer 0 Interrupt	2
External Interrupt 1	3
Timer 1 Interrupt	4
UART Interrupt	5
T2CCU,UART Normal Divider Overflow, MultiCAN, LIN Interrupt	6
ADC, MultiCAN Interrupt	7
SSC Interrupt	8
External Interrupt 2, Timer 21, UART1, UART1 Normal Divider Overflow, MDU, CORDIC Interrupt	9
External Interrupt [6:3], MultiCAN Interrupt	10
CCU6 Interrupt Node Pointer 0, MultiCAN interrupt	11
CCU6 Interrupt Node Pointer 1, MultiCAN Interrupt	12
CCU6 Interrupt Node Pointer 2, MultiCAN Interrupt	13
CCU6 Interrupt Node Pointer 3, MultiCAN Interrupt	14



#### 3.5 Parallel Ports

The XC87x has 40 port pins organized into five parallel ports: Port 0 (P0), Port 1 (P1), Port 3 (P3), Port 4 (P4) and Port 5 (P5). Each pin has a pair of internal pull-up and pull-down devices that can be individually enabled or disabled. These ports are bidirectional and can be used as general purpose input/output (GPIO) or to perform alternate input/output functions for the on-chip peripherals. When configured as an output, the open drain mode can be selected.

#### **Bidirectional Port Features**

- Configurable pin direction
- Configurable pull-up/pull-down devices
- Configurable open drain mode
- Configurable drive strength
- Transfer of data through digital inputs and outputs (general purpose I/O)
- Alternate input/output for on-chip peripherals



Figure 18 shows the structure of a bidirectional port pin.

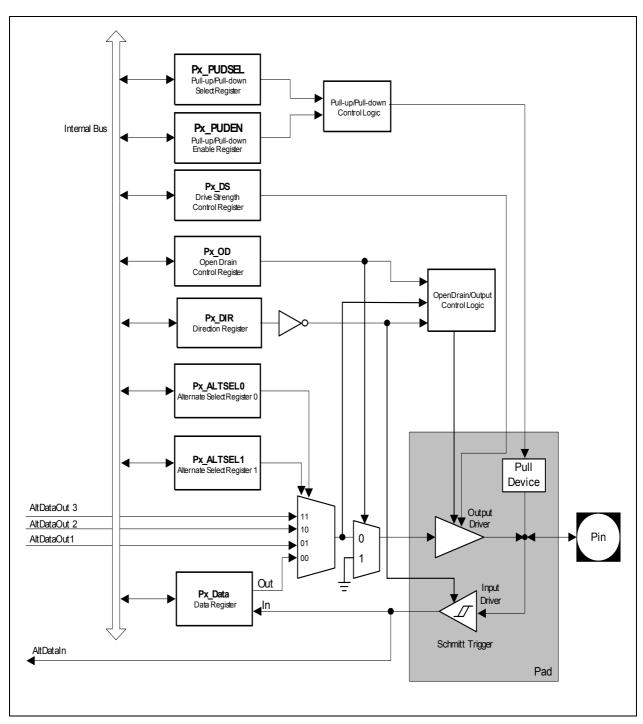


Figure 18 General Structure of Bidirectional Port



# 3.6 Power Supply System with Embedded Voltage Regulator

The XC87x microcontroller requires two different levels of power supply:

- 3.3 V or 5.0 V for the Embedded Voltage Regulator (EVR) and Ports
- 2.5 V for the core, memory, on-chip oscillator, and peripherals

**Figure 19** shows the XC87x power supply system. A power supply of 3.3 V or 5.0 V must be provided from the external power supply pin. The 2.5 V power supply for the logic is generated by the EVR. The EVR helps to reduce the power consumption of the whole chip and the complexity of the application board design.

The EVR consists of a main voltage regulator and a low power voltage regulator. In active mode, both voltage regulators are enabled. In power-down mode<sup>1)</sup>, the main voltage regulator is switched off, while the low power voltage regulator continues to function and provide power supply to the system with low power consumption.

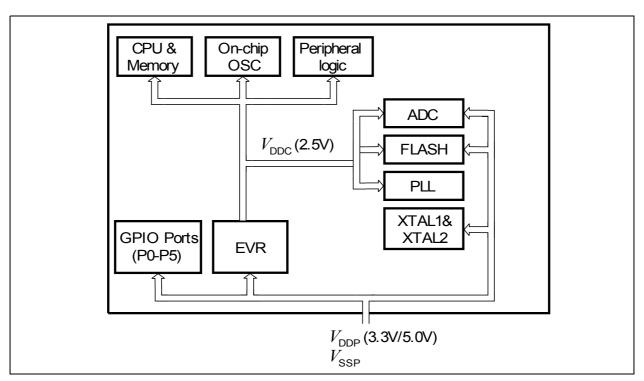


Figure 19 XC87x Power Supply System

#### **EVR Features**

- Input voltage ( $V_{\rm DDP}$ ): 3.3 V/5.0 V
- Output voltage ( $V_{\rm DDC}$ ): 2.5 V ± 7.5%
- Low power voltage regulator provided in power-down mode<sup>1)</sup>
- $V_{\text{DDP}}$  prewarning detection
- $V_{\rm DDC}$  brownout detection

<sup>1)</sup> SAK product variant does not support power-down mode.



#### 3.7 Reset Control

The XC87x has five types of reset: power-on reset, hardware reset, watchdog timer reset, power-down wake-up reset, and brownout reset.

When the XC87x is first powered up, the status of certain pins (see **Table 25**) must be defined to ensure proper start operation of the device. At the end of a reset sequence, the sampled values are latched to select the desired boot option, which cannot be modified until the next power-on reset or hardware reset. This guarantees stable conditions during the normal operation of the device.

The second type of reset in XC87x is the hardware reset. This reset function can be used during normal operation or when the chip is in power-down mode. A reset input pin RESET is provided for the hardware reset.

The Watchdog Timer (WDT) module is also capable of resetting the device if it detects a malfunction in the system.

Another type of reset that needs to be detected is a reset while the device is in power-down mode (wake-up reset). While the contents of the static RAM are undefined after a power-on reset, they are well defined after a wake-up reset from power-down mode.

## 3.7.1 Module Reset Behavior

**Table 24** lists the functions of the XC87x and the various reset types that affect these functions. The symbol "■" signifies that the particular function is reset to its default state.

Table 24 Effect of Reset on Device Functions

Module/ Function	Wake-Up Reset	Watchdog Reset	Hardware Reset	Power-On Reset	Brownout Reset
CPU Core					
Peripherals					
On-Chip Static RAM	Not affected, Reliable	Not affected, Reliable	Not affected, Reliable	Affected, un- reliable	Affected, un- reliable
Oscillator, PLL		Not affected			
Port Pins					
EVR	The voltage regulator is switched on	Not affected	Not affected		
FLASH					
NMI	Disabled	Disabled			



# 3.7.2 Booting Scheme

When the XC87x is reset, it must identify the type of configuration with which to start the different modes once the reset sequence is complete. Thus, boot configuration information that is required for activation of special modes and conditions needs to be applied by the external world through input pins. After power-on reset or hardware reset, the pins MBC, TMS and P0.0 collectively select the different boot options. **Table 25** shows the available boot options in the XC87x.

Table 25 XC87x Boot Selection 1)

MBC	TMS	P0.0	Type of Mode	PC Start Value
1	0	Х	User Mode <sup>2)</sup> ; on-chip OSC/PLL non-bypassed	0000 <sub>H</sub>
0	0	Х	BSL Mode; (LIN Mode <sup>3)</sup> , UART/ MultiCAN Mode <sup>4)5)</sup> and Alternate BSL Mode <sup>6)</sup> ); on-chip OSC/PLL non-bypassed	0000 <sub>H</sub>
0	1	0	OCDS Mode; on-chip OSC/PLL non- bypassed	0000 <sub>H</sub>
1	1	0	User (JTAG) Mode <sup>7)</sup> ; on-chip OSC/PLL non-bypassed (normal)	0000 <sub>H</sub>

- 1) In addition to the pins MBC, TMS and P0.0, TM pin also requires an external pull down for all the boot options.
- 2) BSL mode is automatically entered if no valid password is installed and data at memory address 0000H equals zero.
- 3) If a device is programmed as LIN, LIN BSL is always used instead of UART/MultiCAN.
- 4) UART or MultiCAN BSL is decoded by firmware based on the protocol for product variant with MultiCAN. If no MultiCAN and LIN variant, UART BSL is used.
- 5) In MultiCAN BSL mode, the clock source is switched to XTAL by firmware, bypassing the on-chip oscillator. This avoids any frequency invariance with the on-chip oscillator and allows other frequency clock input, thus ensuring accurate baud rate detection (especially at high bit rates).
- 6) Alternate BSL Mode is a user defined BSL code programmed in Flash. It is entered if the AltBSLPassword is valid.
- 7) Normal user mode with standard JTAG (TCK,TDI,TDO) pins for hot-attach purpose.

Note: The boot options are valid only with the default set of UART and JTAG pins.

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#### 3.8 Clock Generation Unit

The Clock Generation Unit (CGU) allows great flexibility in the clock generation for the XC87x. The power consumption is indirectly proportional to the frequency, whereas the performance of the microcontroller is directly proportional to the frequency. During user program execution, the frequency can be programmed for an optimal ratio between performance and power consumption. Therefore the power consumption can be adapted to the actual application state.

#### **Features**

- Phase-Locked Loop (PLL) for multiplying clock source by different factors
- PLL Base Mode
- Prescaler Mode
- PLL Mode
- Power-down mode support<sup>1)</sup>

The CGU consists of an oscillator circuit and a PLL. In the XC87x, the oscillator can be from either of these two sources: the on-chip oscillator (4 MHz) or the external oscillator (2 MHz to 20 MHz). The term "oscillator" is used to refer to both on-chip oscillator and external oscillator, unless otherwise stated. After the reset, the on-chip oscillator will be used by default. The external oscillator can be selected via software. In addition, the PLL provides a fail-safe logic to perform oscillator run and loss-of-lock detection. This allows emergency routines to be executed for system recovery or to perform system shut down.

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<sup>1)</sup> SAK product variant does not support power-down mode.



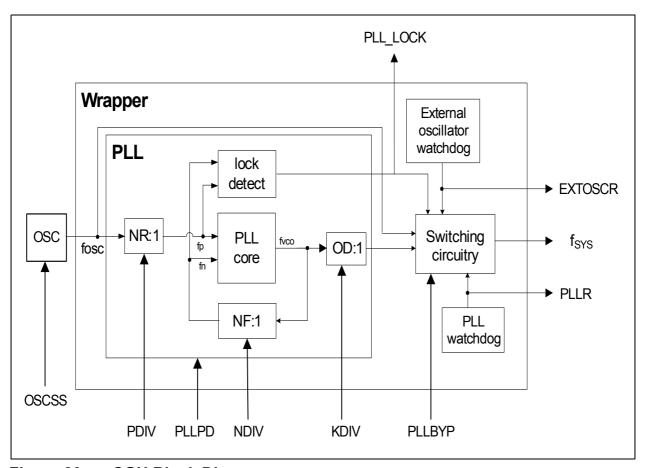


Figure 20 CGU Block Diagram

## **Direct Drive (PLL Bypass Operation)**

During PLL bypass operation, the system clock has the same frequency as the external clock source.

(3.1)

$$f_{SYS} = f_{OSC}$$

## **PLL Mode**

The CPU clock is derived from the oscillator clock, divided by the NR factor (PDIV), multiplied by the NF factor (NDIV), and divided by the OD factor (KDIV). PLL output must



not be bypassed for this PLL mode. The PLL mode is used during normal system operation.

(3.2)

$$f_{SYS} = f_{OSC} x \frac{NF}{NR \times OD}$$

## **System Frequency Selection**

For the XC87x, the value of NF, NR and OD can be selected by bits NDIV, PDIV and KDIV respectively for different oscillator inputs inorder to obtain the required fsys. But the combination of these factors must fulfill the following condition:

- $100 \text{ MHz} < f_{VCO} < 175 \text{ MHz}$
- 800 KHz < f<sub>OSC</sub> / (2 \* NR) < 8 MHz</li>

**Table 26** provides examples on how the typical system frequency of fsys = 144 MHz and maximum frequency of 160 MHz (CPU clock = 26.67 MHz)can be obtained for the different oscillator sources.

value 20 System requests (Vsys					
Oscillator	fosc	N	Р	K	fsys
On-chip	4 MHz	72	2	1	144 MHz
	4 MHz	80	2	1	160 MHz
External	8 MHz	72	4	1	144 MHz
	6 MHz	72	3	1	144 MHz
	4 MHz	72	2	1	144 MHz

Table 26 System frequency ( $f_{sys}$  = 144 MHz)

#### 3.8.1 Recommended External Oscillator Circuits

The oscillator circuit, a Pierce oscillator, is designed to work with both, an external crystal oscillator or an external stable clock source. It basically consists of an inverting amplifier and a feedback element with XTAL1 as input, and XTAL2 as output.

When using a crystal, a proper external oscillator circuitry must be connected to both pins, XTAL1 and XTAL2. The crystal frequency can be within the range of 2 MHz to 20 MHz. Additionally, it is necessary to have two load capacitances  $C_{\rm X1}$  and  $C_{\rm X2}$ , and depending on the crystal type, a series resistor  $R_{\rm X2}$ , to limit the current. A test resistor  $R_{\rm Q}$  may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry.  $R_{\rm Q}$  values are typically specified by the crystal vendor. An external feedback resistor  $R_{\rm f}$  is also required in the external oscillator circuitry. The exact values and related operating range are dependent on the crystal frequency and have to be determined and optimized together with the crystal vendor using the negative

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resistance method. Oscillation measurement with the final target system is strongly recommended to verify the input amplitude at XTAL1 and to determine the actual oscillation allowance (margin negative resistance) for the oscillator-crystal system.

When using an external clock signal, the signal must be connected to XTAL1. XTAL2 is left open (unconnected).

The oscillator can also be used in combination with a ceramic resonator. The final circuitry must also be verified by the resonator vendor. **Figure 21** shows the recommended external oscillator circuitries for both operating modes, external crystal mode and external input clock mode.

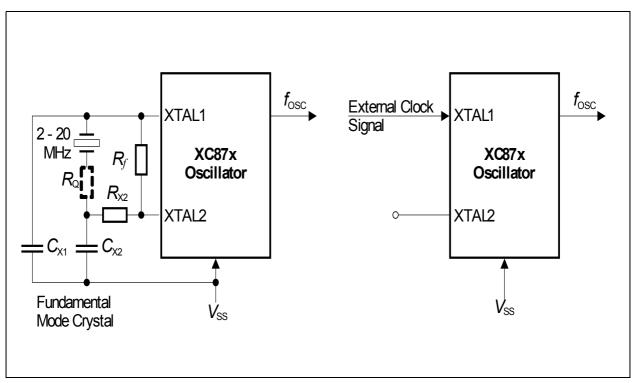


Figure 21 External Oscillator Circuitry

Note: For crystal operation, it is strongly recommended to measure the negative resistance in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the minimum and maximum values of the negative resistance specified by the crystal supplier.

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## 3.8.2 Clock Management

The CGU generates all clock signals required within the microcontroller from a single clock,  $f_{\rm sys}$ . During normal system operation, the typical frequencies of the different modules are as follow:

CPU clock: CCLK, SCLK = 24 MHz

MultiCAN clock: MCANCLK = 24 or 48 MHz

MDU clock : MDUCLK = 24 or 48 MHz

CORDIC clock: CORDICCLK = 24 or 48 MHz

CCU6 clock : CCU6CLK = 24 or 48 MHz

T2CCU clock: T2CCUCLK = 24 or 48 MHz

Peripheral clock: PCLK = 24 MHz

In addition, different clock frequencies can be output to pin CLKOUT (P0.0 or P0.7). The clock output frequency, which is derived from the clock output divider (bit COREL), can further be divided by 2 using toggle latch (bit TLEN is set to 1). The resulting output frequency has a 50% duty cycle. **Figure 22** shows the clock distribution of the XC87x.

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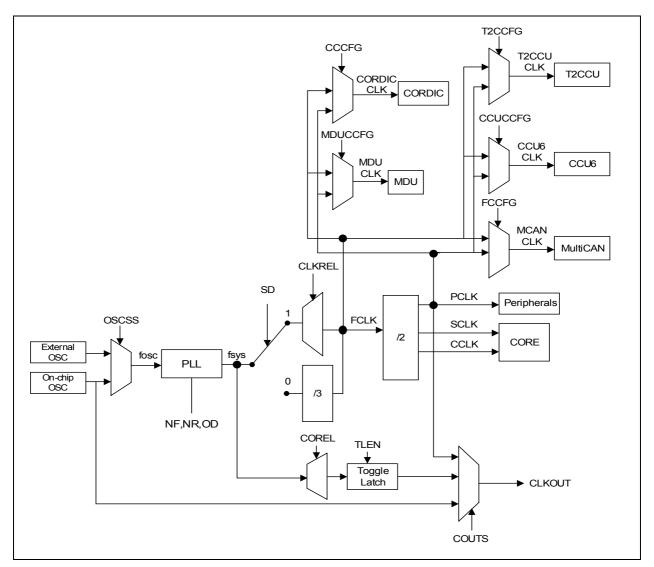


Figure 22 Clock Generation from  $f_{\rm sys}$ 



For power saving purposes, the clocks may be disabled or slowed down according to **Table 27**.

Table 27 System frequency ( $f_{sys} = 144 \text{ MHz}$ )

Power Saving Mode	Action
Idle	Clock to the CPU is disabled.
Slow-down	Clocks to the CPU and all the peripherals are divided by a common programmable factor defined by bit field CMCON.CLKREL.
Power-down <sup>1)</sup>	Oscillator and PLL are switched off.

<sup>1)</sup> SAK product variant does not support power-down mode.

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# 3.9 Power Saving Modes

The power saving modes of the XC87x provide flexible power consumption through a combination of techniques, including:

- Stopping the CPU clock
- · Stopping the clocks of individual system components
- Reducing clock speed of some peripheral components
- Power-down of the entire system with fast restart capability

After a reset, the active mode (normal operating mode) is selected by default (see Figure 23) and the system runs in the main system clock frequency. From active mode, different power saving modes can be selected by software. They are:

- Idle mode
- Slow-down mode
- Power-down mode

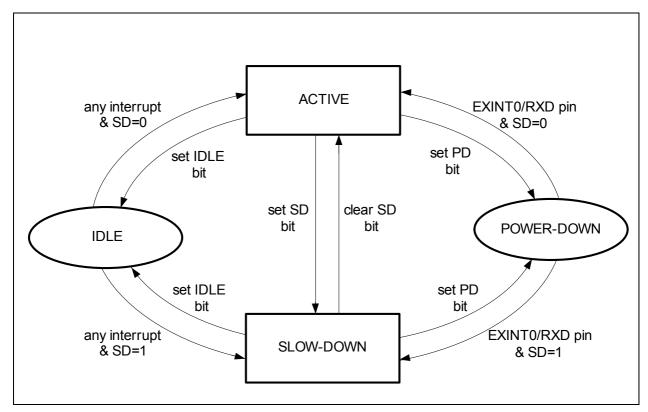


Figure 23 Transition between Power Saving Modes

Note: SAK product variant does not support power-down mode.



# 3.10 Watchdog Timer

The Watchdog Timer (WDT) provides a highly reliable and secure way to detect and recover from software or hardware failures. The WDT is reset at a regular interval that is predefined by the user. The CPU must service the WDT within this interval to prevent the WDT from causing an XC87x system reset. Hence, routine service of the WDT confirms that the system is functioning properly. This ensures that an accidental malfunction of the XC87x will be aborted in a user-specified time period.

In debug mode, the WDT is default suspended and stops counting. Therefore, there is no need to refresh the WDT during debugging.

#### **Features**

- 16-bit Watchdog Timer
- Programmable reload value for upper 8 bits of timer
- Programmable window boundary
- Selectable input frequency of  $f_{PCLK}/2$  or  $f_{PCLK}/128$
- Time-out detection with NMI generation and reset prewarning activation (after which a system reset will be performed)

The WDT is a 16-bit timer incremented by a count rate of  $f_{\rm PCLK}/2$  or  $f_{\rm PCLK}/128$ . This 16-bit timer is realized as two concatenated 8-bit timers. The upper 8 bits of the WDT can be preset to a user-programmable value via a watchdog service access in order to modify the watchdog expire time period. The lower 8 bits are reset on each service access. Figure 24 shows the block diagram of the WDT unit.

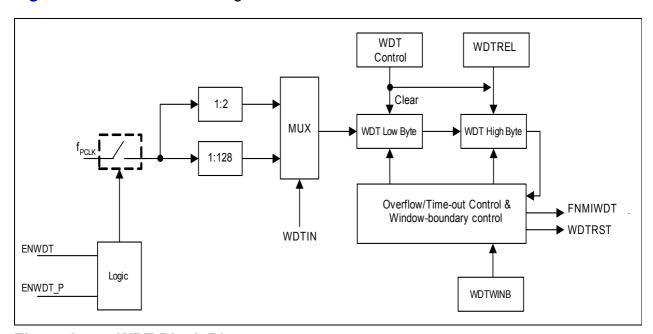


Figure 24 WDT Block Diagram



If the WDT is not serviced before the timer overflow, a system malfunction is assumed. As a result, the WDT NMI is triggered (assert FNMIWDT) and the reset prewarning is entered. The prewarning period lasts for  $30_{\rm H}$  count, after which the system is reset (assert WDTRST).

The WDT has a "programmable window boundary" which disallows any refresh during the WDT's count-up. A refresh during this window boundary constitutes an invalid access to the WDT, causing the reset prewarning to be entered but without triggering the WDT NMI. The system will still be reset after the prewarning period is over. The window boundary is from  $0000_{\rm H}$  to the value obtained from the concatenation of WDTWINB and  $00_{\rm H}$ .

After being serviced, the WDT continues counting up from the value (<WDTREL> \* 2<sup>8</sup>). The time period for an overflow of the WDT is programmable in two ways:

- The input frequency to the WDT can be selected to be either  $f_{\rm PCLK}/2$  or  $f_{\rm PCLK}/128$
- The reload value WDTREL for the high byte of WDT can be programmed in register WDTREL

The period,  $P_{\rm WDT}$ , between servicing the WDT and the next overflow can be determined by the following formula:

$$P_{WDT} \, = \, \frac{2^{(1 \, + \, WDTIN \, \times \, 6)} \, \times (2^{16} - WDTREL \, \times \, 2^{8})}{f_{PCLK}}$$

(3.3)

If the Window-Boundary Refresh feature of the WDT is enabled, the period  $P_{\rm WDT}$  between servicing the WDT and the next overflow is shortened if WDTWINB is greater than WDTREL, see **Figure 25**. This period can be calculated using the same formula by replacing WDTREL with WDTWINB. For this feature to be useful, WDTWINB cannot be smaller than WDTREL.

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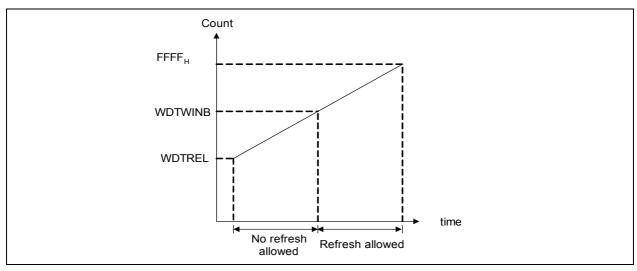


Figure 25 WDT Timing Diagram

**Table 28** lists the possible watchdog time ranges that can be achieved using a certain module clock. Some numbers are rounded to 3 significant digits.

Table 28 Watchdog Time Ranges

Reload value	Prescaler for $f_{PCLK}$				
In WDTREL	2 (WDTIN = 0)	128 (WDTIN = 1)			
	24 MHz	24 MHz			
FF <sub>H</sub>	21.3 μs	1.37 ms			
FF <sub>H</sub> 7F <sub>H</sub>	2.75 ms	176 ms			
00 <sub>H</sub>	5.46 ms	350 ms			



# 3.11 Multiplication/Division Unit

The Multiplication/Division Unit (MDU) provides fast 16-bit multiplication, 16-bit and 32-bit division as well as shift and normalize features. It has been integrated to support the XC87x Core in real-time control applications, which require fast mathematical computations.

#### **Features**

- Fast signed/unsigned 16-bit multiplication
- Fast signed/unsigned 32-bit divide by 16-bit and 16-bit divide by 16-bit operations
- 32-bit unsigned normalize operation
- 32-bit arithmetic/logical shift operations

**Table 29** specifies the number of clock cycles used for calculation in various operations.

**Table 29** MDU Operation Characteristics

Operation	Result	Remainder	No. of Clock Cycles used for calculation
Signed 32-bit/16-bit	32-bit	16-bit	33
Signed 16-bit/16bit	16-bit	16-bit	17
Signed 16-bit x 16-bit	32-bit	-	16
Unsigned 32-bit/16-bit	32-bit	16-bit	32
Unsigned 16-bit/16-bit	16-bit	16-bit	16
Unsigned 16-bit x 16-bit	32-bit	-	16
32-bit normalize	-	-	No. of shifts + 1 (Max. 32)
32-bit shift L/R	-	-	No. of shifts + 1 (Max. 32)



## 3.12 CORDIC Coprocessor

The CORDIC Coprocessor provides CPU with hardware support for the solving of circular (trigonometric), linear (multiply-add, divide-add) and hyperbolic functions.

#### **Features**

- Modes of operation
  - Supports all CORDIC operating modes for solving circular (trigonometric), linear (multiply-add, divide-add) and hyperbolic functions
  - Integrated look-up tables (LUTs) for all operating modes
- Circular vectoring mode: Extended support for values of initial X and Y data up to full range of [-2<sup>15</sup>,(2<sup>15</sup>-1)] for solving angle and magnitude
- Circular rotation mode: Extended support for values of initial Z data up to full range of  $[-2^{15},(2^{15}-1)]$ , representing angles in the range  $[-\pi,((2^{15}-1)/2^{15})\pi]$  for solving trigonometry
- Implementation-dependent operational frequency of up to 80 MHz
- Gated clock input to support disabling of module
- 16-bit accessible data width
  - 24-bit kernel data width plus 2 overflow bits for X and Y each
  - 20-bit kernel data width plus 1 overflow bit for Z
  - With KEEP bit to retain the last value in the kernel register for a new calculation
- 16 iterations per calculation: Approximately 41 clock-cycles or less, from set of start (ST) bit to set of end-of-calculation flag, excluding time taken for write and read access of data bytes.
- · Twos complement data processing
  - Only exception: X result data with user selectable option for unsigned result
- X and Y data generally accepted as integer or rational number; X and Y must be of the same data form
- Entries of LUTs are 20-bit signed integers
  - Entries of atan and atanh LUTs are integer representations (S19) of angles with the scaling such that  $[-2^{15},(2^{15}-1)]$  represents the range  $[-\pi,((2^{15}-1)/2^{15})\pi]$
  - Accessible Z result data for circular and hyperbolic functions is integer in data form of S15
- Emulated LUT for linear function
  - Data form is 1 integer bit and 15-bit fractional part (1.15)
  - Accessible Z result data for linear function is rational number with fixed data form of S4.11 (signed 4Q16)
- Truncation Error
  - The result of a CORDIC calculation may return an approximation due to truncation of LSBs
  - Good accuracy of the CORDIC calculated result data, especially in circular mode
- Interrupt
  - On completion of a calculation



Interrupt enabling and corresponding flag

#### 3.13 UART and UART1

The XC87x provides two Universal Asynchronous Receiver/Transmitter (UART and UART1) modules for full-duplex asynchronous reception/transmission. Both are also receive-buffered, i.e., they can commence reception of a second byte before a previously received byte has been read from the receive register. However, if the first byte still has not been read by the time reception of the second byte is complete, one of the bytes will be lost.

#### **Features**

- Full-duplex asynchronous modes
  - 8-bit or 9-bit data frames, LSB first
  - Fixed or variable baud rate
- Receive buffered
- Multiprocessor communication
- Interrupt generation on the completion of a data transmission or reception

The UART modules can operate in the four modes shown in Table 30.

Table 30 UART Modes

Operating Mode	Baud Rate
Mode 0: 8-bit shift register	$f_{PCLK}/2$
Mode 1: 8-bit shift UART	Variable
Mode 2: 9-bit shift UART	$f_{PCLK}/32 \text{ or } f_{PCLK}/64^{1)}$
Mode 3: 9-bit shift UART	Variable

<sup>1)</sup> For UART1 module, the baud rate is fixed at f<sub>PCLK</sub>/64.

There are several ways to generate the baud rate clock for the serial port, depending on the mode in which it is operating. In mode 0, the baud rate for the transfer is fixed at  $f_{\rm PCLK}/2$ . In mode 2, the baud rate is generated internally based on the UART input clock and can be configured to either  $f_{\rm PCLK}/32$  or  $f_{\rm PCLK}/64$ . For UART1 module, only  $f_{\rm PCLK}/64$  is available. The variable baud rate is set by the underflow rate on the dedicated baud-rate generator. For UART module, the variable baud rate alternatively can be set by the overflow rate on Timer 1.

#### 3.13.1 Baud-Rate Generator

Both UART modules have their own dedicated baud-rate generator, which is based on a programmable 8-bit reload value, and includes divider stages (i.e., prescaler and



fractional divider) for generating a wide range of baud rates based on its input clock  $f_{PCLK}$ , see **Figure 26**.

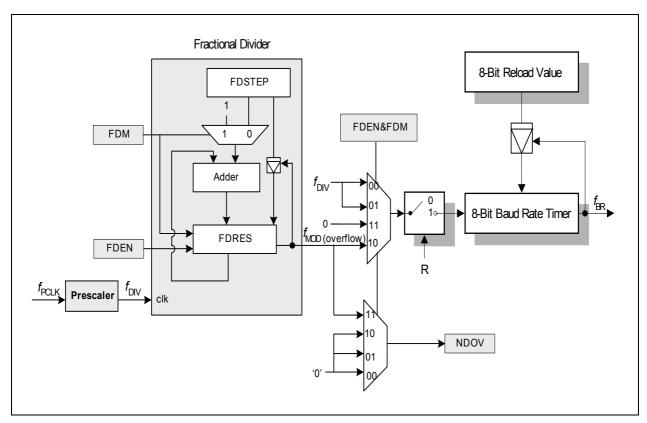


Figure 26 Baud-rate Generator Circuitry

The baud rate timer is a count-down timer and is clocked by either the output of the fractional divider ( $f_{MOD}$ ) if the fractional divider is enabled (FDCON.FDEN = 1), or the output of the prescaler ( $f_{DIV}$ ) if the fractional divider is disabled (FDEN = 0). For baud rate generation, the fractional divider must be configured to fractional divider mode (FDCON.FDM = 0). This allows the baud rate control run bit BCON.R to be used to start or stop the baud rate timer. At each timer underflow, the timer is reloaded with the 8-bit reload value in register BG and one clock pulse is generated for the serial channel.

Enabling the fractional divider in normal divider mode (FDEN = 1 and FDM = 1) stops the baud rate timer and nullifies the effect of bit BCON.R. See **Section 3.14**.

The baud rate ( $f_{BR}$ ) value is dependent on the following parameters:

- Input clock  $f_{PCLK}$
- Prescaling factor (2<sup>BRPRE</sup>) defined by bit field BRPRE in register BCON
- Fractional divider (STEP/256) defined by register FDSTEP
   (to be considered only if fractional divider is enabled and operating in fractional divider mode)
- 8-bit reload value (BR\_VALUE) for the baud rate timer defined by register BG

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The following formulas calculate the final baud rate without and with the fractional divider respectively:

baud rate = 
$$\frac{f_{PCLK}}{16 \times 2^{BRPRE} \times (BR\_VALUE + 1)}$$
 where  $2^{BRPRE} \times (BR\_VALUE + 1) > 1$ 

baud rate = 
$$\frac{f_{PCLK}}{16 \times 2^{BRPRE} \times (BR_VALUE + 1)} \times \frac{STEP}{256}$$

(3.5)

The maximum baud rate that can be generated is limited to  $f_{\rm PCLK}/32$ . Hence, for a module clock of 24 MHz, the maximum achievable baud rate is 0.75 MBaud.

Standard LIN protocol can support a maximum baud rate of 20 kHz, the baud rate accuracy is not critical and the fractional divider can be disabled. Only the prescaler is used for auto baud rate calculation. For LIN fast mode, which supports the baud rate of 20 kHz to 57.6 kHz, the higher baud rates require the use of the fractional divider for greater accuracy.

**Table 31** lists the various commonly used baud rates with their corresponding parameter settings and deviation errors. The fractional divider is disabled and a module clock of 24 MHz is used.

Table 31 Typical Baud rates for UART with Fractional Divider disabled

Baud rate	Prescaling Factor (2BRPRE)	Reload Value (BR_VALUE + 1)	Deviation Error
19.2 kBaud	1 (BRPRE=000 <sub>B</sub> )	78 (4E <sub>H</sub> )	0.17 %
9600 Baud	1 (BRPRE=000 <sub>B</sub> )	156 (9C <sub>H</sub> )	0.17 %
4800 Baud	2 (BRPRE=001 <sub>B</sub> )	156 (9C <sub>H</sub> )	0.17 %
2400 Baud	4 (BRPRE=010 <sub>B</sub> )	156 (9C <sub>H</sub> )	0.17 %

The fractional divider allows baud rates of higher accuracy (lower deviation error) to be generated. **Table 32** lists the resulting deviation errors from generating a baud rate of 57.6 kHz, using different module clock frequencies. The fractional divider is enabled (fractional divider mode) and the corresponding parameter settings are shown.

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Table 32 Deviation Error for UART with Fractional Divider enabled

$f_{ t PCLK}$	Prescaling Factor (2BRPRE)	Reload Value (BR_VALUE + 1)	STEP	Deviation Error
24 MHz	1	6 (6 <sub>H</sub> )	59 (3B <sub>H</sub> )	+0.03 %
12 MHz	1	3 (3 <sub>H</sub> )	59 (3B <sub>H</sub> )	+0.03 %
8 MHz	1	2 (2 <sub>H</sub> )	59 (3B <sub>H</sub> )	+0.03 %
6 MHz	1	6 (6 <sub>H</sub> )	236 (EC <sub>H</sub> )	+0.03 %

## 3.13.2 Baud Rate Generation using Timer 1

In UART modes 1 and 3 of UART module, Timer 1 can be used for generating the variable baud rates. In theory, this timer could be used in any of its modes. But in practice, it should be set into auto-reload mode (Timer 1 mode 2), with its high byte set to the appropriate value for the required baud rate. The baud rate is determined by the Timer 1 overflow rate and the value of SMOD as follows:

Mode 1, 3 band rate= 
$$\frac{2^{\text{SMOD}} \times f_{\text{PCLK}}}{32 \times 2 \times (256 - \text{TH1})}$$

(3.6)

# 3.14 Normal Divider Mode (8-bit Auto-reload Timer)

Setting bit FDM in register FDCON to 1 configures the fractional divider to normal divider mode, while at the same time disables baud rate generation (see Figure 26). Once the fractional divider is enabled (FDEN = 1), it functions as an 8-bit auto-reload timer (with no relation to baud rate generation) and counts up from the reload value with each input clock pulse. Bit field RESULT in register FDRES represents the timer value, while bit field STEP in register FDSTEP defines the reload value. At each timer overflow, an overflow flag (FDCON.NDOV) will be set and an interrupt request generated. This gives an output clock  $f_{\text{MOD}}$  that is 1/n of the input clock  $f_{\text{DIV}}$ , where n is defined by 256 - STEP.

The output frequency in normal divider mode is derived as follows:

$$f_{MOD} = f_{DIV} \times \frac{1}{256 - STEP}$$

(3.7)



#### 3.15 LIN Protocol

The UART module can be used to support the Local Interconnect Network (LIN) protocol for both master and slave operations. The LIN baud rate detection feature, which consists of the hardware logic for Break and Synch Byte detection, provides the capability to detect the baud rate within LIN protocol using Timer 2. This allows the UART to be synchronized to the LIN baud rate for data transmission and reception.

Note: The LIN baud rate detection feature is available for use only with UART. To use UART1 for LIN communication, software has to be implemented to detect the Break and Synch Byte.

LIN is a holistic communication concept for local interconnected networks in vehicles. The communication is based on the SCI (UART) data format, a single-master/multiple-slave concept, a clock synchronization for nodes without stabilized time base. An attractive feature of LIN is self-synchronization of the slave nodes without a crystal or ceramic resonator, which significantly reduces the cost of hardware platform. Hence, the baud rate must be calculated and returned with every message frame.

The structure of a LIN frame is shown in Figure 27. The frame consists of the:

- Header, which comprises a Break (13-bit time low), Synch Byte (55<sub>H</sub>), and ID field
- Response time
- Data bytes (according to UART protocol)
- Checksum

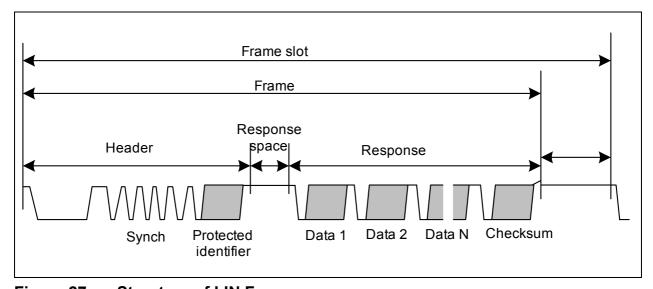


Figure 27 Structure of LIN Frame

#### 3.15.1 LIN Header Transmission

LIN header transmission is only applicable in master mode. In the LIN communication, a master task decides when and which frame is to be transferred on the bus. It also identifies a slave task to provide the data transported by each frame. The information



needed for the handshaking between the master and slave tasks is provided by the master task through the header portion of the frame.

The header consists of a break and synch pattern followed by an identifier. Among these three fields, only the break pattern cannot be transmitted as a normal 8-bit UART data. The break must contain a dominant value of 13 bits or more to ensure proper synchronization of slave nodes.

In the LIN communication, a slave task is required to be synchronized at the beginning of the protected identifier field of frame. For this purpose, every frame starts with a sequence consisting of a break field followed by a synch byte field. This sequence is unique and provides enough information for any slave task to detect the beginning of a new frame and be synchronized at the start of the identifier field.

Upon entering LIN communication, a connection is established and the transfer speed (baud rate) of the serial communication partner (host) is automatically synchronized in the following steps:

STEP 1: Initialize interface for reception and timer for baud rate measurement

STEP 2: Wait for an incoming LIN frame from host

STEP 3: Synchronize the baud rate to the host

STEP 4: Enter for Master Request Frame or for Slave Response Frame

Note: Re-synchronization and setup of baud rate are always done for **every** Master Request Header or Slave Response Header LIN frame.

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# 3.16 High-Speed Synchronous Serial Interface

The High-Speed Synchronous Serial Interface (SSC) supports full-duplex and half-duplex synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-bit baud-rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

#### **Features**

- Master and slave mode operation
  - Full-duplex or half-duplex operation
- · Transmit and receive buffered
- Flexible data format
  - Programmable number of data bits: 2 to 8 bits
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: idle low or high state for the shift clock
  - Programmable clock/data phase: data shift with leading or trailing edge of the shift clock
- Variable baud rate
- Compatible with Serial Peripheral Interface (SPI)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error)

Data is transmitted or received on lines TXD and RXD, which are normally connected to the pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output via line MS\_CLK (Master Serial Shift Clock) or input via line SS\_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

Figure 28 shows the block diagram of the SSC.



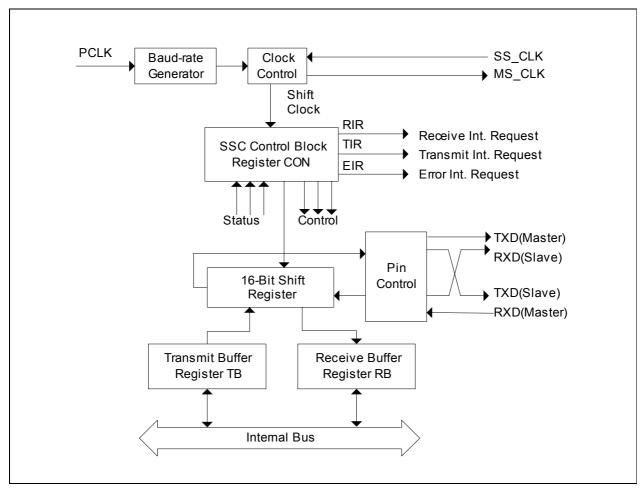


Figure 28 SSC Block Diagram



#### 3.17 Timer 0 and Timer 1

Timer 0 and Timer 1 can function as both timers or counters. When functioning as a timer, Timer 0 and Timer 1 are incremented every machine cycle, i.e. every 2 input clocks (or 2 PCLKs). When functioning as a counter, Timer 0 and Timer 1 are incremented in response to a 1-to-0 transition (falling edge) at their respective external input pins, T0 or T1.

Timer 0 and 1 are fully compatible and can be configured in four different operating modes for use in a variety of applications, see **Table 33**. In modes 0, 1 and 2, the two timers operate independently, but in mode 3, their functions are specialized.

Table 33 Timer 0 and Timer 1 Modes

Mode	Operation
0	13-bit timer The timer is essentially an 8-bit counter with a divide-by-32 prescaler. This mode is included solely for compatibility with Intel 8048 devices.
1	16-bit timer The timer registers, TLx and THx, are concatenated to form a 16-bit counter.
2	8-bit timer with auto-reload The timer register TLx is reloaded with a user-defined 8-bit value in THx upon overflow.
3	Timer 0 operates as two 8-bit timers The timer registers, TL0 and TH0, operate as two separate 8-bit counters. Timer 1 is halted and retains its count even if enabled.



#### 3.18 Timer 2 and Timer 21

Timer 2 and Timer 21 are 16-bit general purpose timers (THL2) that are fully compatible and have two modes of operation, a 16-bit auto-reload mode and a 16-bit one channel capture mode, see **Table 34**. As a timer, the timers count with an input clock of PCLK/12 (if prescaler is disabled). As a counter, they count 1-to-0 transitions on pin T2. In the counter mode, the maximum resolution for the count is PCLK/24 (if prescaler is disabled).

Table 34	Timer 2 Modes
Mode	Description
Auto-reload	<ul> <li>Up/Down Count Disabled</li> <li>Count up only</li> <li>Start counting from 16-bit reload value, overflow at FFFF<sub>H</sub></li> <li>Reload event configurable for trigger by overflow condition only, or by negative/positive edge at input pin T2EX as well</li> <li>Programmble reload value in register RC2</li> <li>Interrupt is generated with reload event</li> </ul>
	<ul> <li>Up/Down Count Enabled</li> <li>Count up or down, direction determined by level at input pin T2EX</li> <li>No interrupt is generated</li> <li>Count up         <ul> <li>Start counting from 16-bit reload value, overflow at FFFF<sub>H</sub></li> <li>Reload event triggered by overflow condition</li> <li>Programmble reload value in register RC2</li> </ul> </li> <li>Count down         <ul> <li>Start counting from FFFF<sub>H</sub>, underflow at value defined in register RC2</li> <li>Reload event triggered by underflow condition</li> <li>Reload value fixed at FFFF<sub>H</sub></li> </ul> </li> </ul>
Channel capture	<ul> <li>Count up only</li> <li>Start counting from 0000<sub>H</sub>, overflow at FFFF<sub>H</sub></li> <li>Reload event triggered by overflow condition</li> <li>Reload value fixed at 0000<sub>H</sub></li> <li>Capture event triggered by falling/rising edge at pin T2EX</li> <li>Captured timer value stored in register RC2</li> <li>Interrupt is generated with reload or capture event</li> </ul>



## 3.19 Timer 2 Capture/Compare Unit

The T2CCU (Timer 2 Capture/Compare Unit) consists of the standard Timer 2 unit and a Capture/compare unit (CCU). The Capture/Compare Timer (CCT) is part of the CCU. Control is available in the T2CCU to select individually for each of its 16-bit capture/compare channel, either the Timer 2 or the Capture/Compare Timer (CCT) as the time base. Both timers have a resolution of 16 bits. The clock frequency of T2CCU,  $f_{T2CCU}$ , could be set at PCLK frequency or 2 times the PCLK frequency.

The T2CCU can be used for various digital signal generation and event capturing like pulse generation, pulse width modulation, pulse width measuring etc. Target applications include various automotive control as well as industrial (frequency generation, digital-to-analog conversion, process control etc.).

#### **T2CCU Features**

- Option to select individually for each channel, either Timer 2 or Capture/Compare Timer as time base
- Extremely flexible Capture/Compare Timer count rate by cascading with Timer 2
- Capture/Compare Timer may be 'reset' immediately by triggering overflow event
- 16-bit resolution
- Six compare channels in total
- Four capture channels multiplexed with the compare channels, in total
- Shadow register for each compare register
  - Transfer via software control or on timer overflow.
- Compare Mode 0: Compare output signal changes from the inactive level to active level on compare match. Returns to inactive level on timer overflow.
  - Active level can be defined by register bit for channel groups A and B.
  - Support of 0% to 100% duty cycle in compare mode 0.
- Compare Mode 1: Full control of the software on the compare output signal level, for the next compare match.
- Concurrent Compare Mode with channel 0
- Capture Mode 0: Capture on any external event (rising/falling/both edge) at the 4 pins T2CC0 to T2CC3.
- Capture Mode 1: Capture upon writing to the low byte of the corresponding channel capture register.
- Capture mode 0 or 1 can be established independently on the 4 capture channels.

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## 3.20 Capture/Compare Unit 6

The Capture/Compare Unit 6 (CCU6) provides two independent timers (T12, T13), which can be used for Pulse Width Modulation (PWM) generation, especially for AC-motor control. The CCU6 also supports special control modes for block commutation and multi-phase machines.

The timer T12 can function in capture and/or compare mode for its three channels. The timer T13 can work in compare mode only.

The multi-channel control unit generates output patterns, which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

#### **Timer T12 Features**

- Three capture/compare channels, each channel can be used either as a capture or as a compare channel
- Supports generation of a three-phase PWM (six outputs, individual signals for highside and lowside switches)
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- Generation of center-aligned and edge-aligned PWM
- Supports single-shot mode
- Supports many interrupt request sources
- Hysteresis-like control mode

#### **Timer T13 Features**

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock frequency
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Supports single-shot mode

#### **Additional Features**

- Implements block commutation for Brushless DC-drives
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal (CTRAP)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

The block diagram of the CCU6 module is shown in Figure 29.



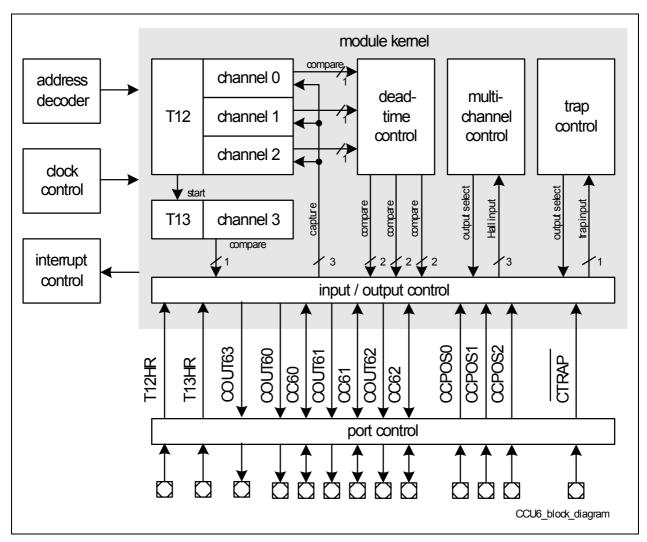


Figure 29 CCU6 Block Diagram



## 3.21 Controller Area Network (MultiCAN)

The MultiCAN module contains two Full-CAN nodes operating independently or exchanging data and remote frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 B active. Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share a common set of message objects, where each message object may be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects may be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double chained lists, where each CAN node has it's own list of message objects. A CAN node stores frames only into message objects that are allocated to the list of the CAN node. It only transmits messages from objects of this list. A powerful, command driven list controller performs all list operations.

The bit timings for the CAN nodes are derived from the peripheral clock ( $f_{\text{CAN}}$ ) and are programmable up to a data rate of 1 MBaud. A pair of receive and transmit pins connects each CAN node to a bus transceiver.

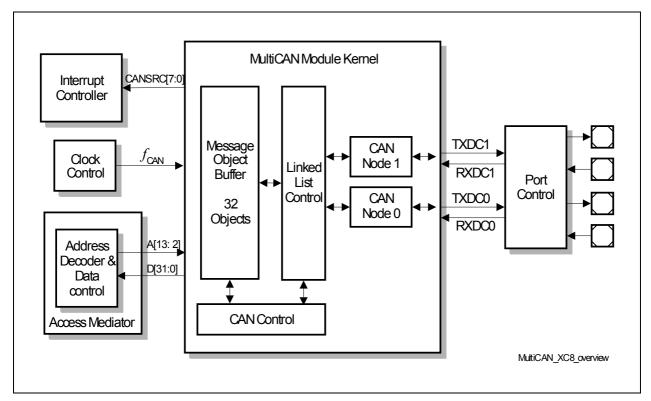


Figure 30 Overview of the MultiCAN

#### **Features**

Compliant to ISO 11898.



- CAN functionality according to CAN specification V2.0 B active.
- Dedicated control registers are provided for each CAN node.
- A data transfer rate up to 1 MBaud is supported.
- Flexible and powerful message transfer control and error handling capabilities are implemented.
- Advanced CAN bus bit timing analysis and baud rate detection can be performed for each CAN node via the frame counter.
- Full-CAN functionality: A set of 32 message objects can be individually
  - allocated (assigned) to any CAN node
  - configured as transmit or receive object
  - setup to handle frames with 11-bit or 29-bit identifier
  - counted or assigned a timestamp via a frame counter
  - configured to remote monitoring mode
- Advanced Acceptance Filtering:
  - Each message object provides an individual acceptance mask to filter incoming frames.
  - A message object can be configured to accept only standard or only extended frames or to accept both standard and extended frames.
  - Message objects can be grouped into 4 priority classes.
  - The selection of the message to be transmitted first can be performed on the basis of frame identifier, IDE bit and RTR bit according to CAN arbitration rules.
- Advanced Message Object Functionality:
  - Message Objects can be combined to build FIFO message buffers of arbitrary size, which is only limited by the total number of message objects.
  - Message objects can be linked to form a gateway to automatically transfer frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways may be defined.
- Advanced Data Management:
  - The Message objects are organized in double chained lists.
  - List reorganizations may be performed any time, even during full operation of the CAN nodes.
  - A powerful, command driven list controller manages the organization of the list structure and ensures consistency of the list.
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation.
  - Static Allocation Commands offer compatibility with TwinCAN applications, which are not list based.
- Advanced Interrupt Handling:
  - Up to 8 interrupt output lines are available. Most interrupt requests can be individually routed to one of the 8 interrupt output lines.
  - Message postprocessing notifications can be flexibly aggregated into a dedicated register field of 64 notification bits.

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### 3.22 Analog-to-Digital Converter

The XC87x includes a high-performance 10-bit Analog-to-Digital Converter (ADC) with eight multiplexed analog input channels. The ADC uses a successive approximation technique to convert the analog voltage levels from up to eight different sources. The analog input channels of the ADC are available at ANO - AN7.

#### **Features**

- Successive approximation
- 8-bit or 10-bit resolution
- · Eight analog channels
- Four independent result registers
- Result data protection for slow CPU access (wait-for-read mode)
- Single conversion mode
- Autoscan functionality
- · Limit checking for conversion results
- Data reduction filter (accumulation of up to 2 conversion results)
- Two independent conversion request sources with programmable priority
- Selectable conversion request trigger
- Flexible interrupt generation with configurable service nodes
- Programmable sample time
- Programmable clock divider
- Cancel/restart feature for running conversions
- Integrated sample and hold circuitry
- Compensation of offset errors
- Low power modes

## 3.22.1 ADC Clocking Scheme

A common module clock  $f_{\rm ADC}$  generates the various clock signals used by the analog and digital parts of the ADC module:

- $f_{\rm ADCA}$  is input clock for the analog part.
- $f_{\rm ADCI}$  is internal clock for the analog part (defines the time base for conversion length and the sample time). This clock is generated internally in the analog part, based on the input clock  $f_{\rm ADCA}$  to generate a correct duty cycle for the analog components.
- $f_{\rm ADCD}$  is input clock for the digital part.

**Figure 31** shows the clocking scheme of the ADC module. The prescaler ratio is selected by bit field CTC in register GLOBCTR. A prescaling ratio of 32 can be selected when the maximum performance of the ADC is not required.



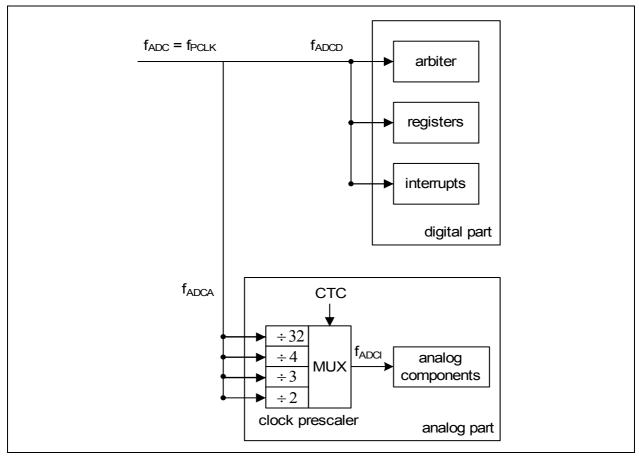


Figure 31 ADC Clocking Scheme

For module clock  $f_{ADC}$  = 24 MHz, the analog clock  $f_{ADCI}$  frequency can be selected as shown in **Table 35**.

Table 35  $f_{ADCI}$  Frequency Selection

Module Clock $f_{ADC}$	СТС	Prescaling Ratio	Analog Clock $f_{ADCI}$
24 MHz	00 <sub>B</sub>	÷ 2	12 MHz
	01 <sub>B</sub>	÷ 3	8 MHz
	10 <sub>B</sub>	÷ 4	6 MHz
	11 <sub>B</sub> (default)	÷ 32	750 kHz

During slow-down mode,  $f_{\rm ADC}$  may be reduced further, for example, to 12 MHz or 6 MHz. However, it is important to note that the conversion error could increase due to loss of charges on the capacitors, if  $f_{\rm ADC}$  becomes too low during slow-down mode.

## 3.22.2 ADC Conversion Sequence

The analog-to-digital conversion procedure consists of the following phases:



- Synchronization phase (t<sub>SYN</sub>)
- Sample phase  $(t_S)$
- Conversion phase
- Write result phase (t<sub>WR</sub>)

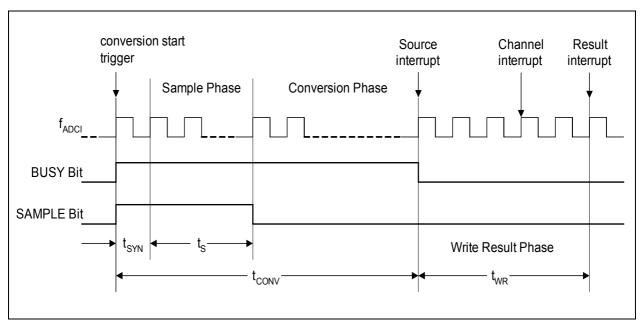


Figure 32 ADC Conversion Timing



### 3.23 On-Chip Debug Support

The On-Chip Debug Support (OCDS) provides the basic functionality required for the software development and debugging of XC800-based systems.

The OCDS design is based on these principles:

- Use the built-in debug functionality of the XC800 Core
- Add a minimum of hardware overhead
- Provide support for most of the operations by a Monitor Program
- Use standard interfaces to communicate with the Host (a Debugger)

#### **Features**

- Set breakpoints on instruction address and on address range within the Program Memory
- Set breakpoints on internal RAM address range
- Support unlimited software breakpoints in Flash/RAM code region
- Process external breaks via JTAG and upon activating a dedicated pin
- Step through the program code

The OCDS functional blocks are shown in **Figure 33**. The Monitor Mode Control (MMC) block at the center of OCDS system brings together control signals and supports the overall functionality. The MMC communicates with the XC800 Core, primarily via the Debug Interface, and also receives reset and clock signals.

After processing memory address and control signals from the core, the MMC provides proper access to the dedicated extra-memories: a Monitor ROM (holding the code) and a Monitor RAM (for work-data and Monitor-stack).

The OCDS system is accessed through the JTAG<sup>1)</sup>, which is an interface dedicated exclusively for testing and debugging activities and is not normally used in an application. The dedicated MBC pin is used for external configuration and debugging control.

Note: All the debug functionality described here can normally be used only after XC87x has been started in OCDS mode.

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<sup>1)</sup> The pins of the JTAG port can be assigned to either the primary port (Port 0) or either of the secondary ports (Ports 1 and 2/Port 5).

User must set the JTAG pins (TCK and TDI) as input during connection with the OCDS system.



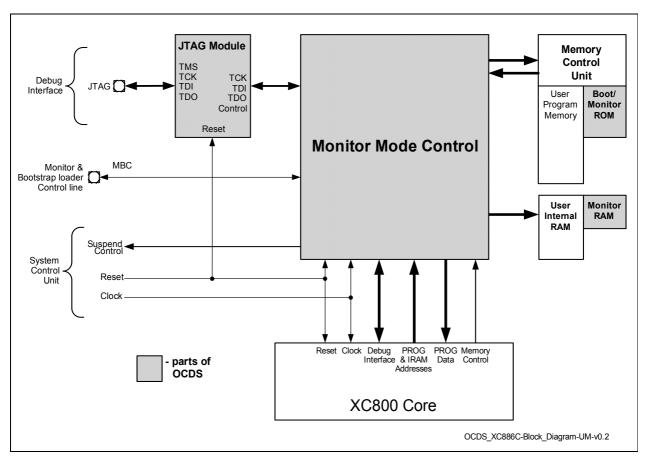


Figure 33 OCDS Block Diagram

### 3.23.1 JTAG ID Register

This is a read-only register located inside the JTAG module, and is used to recognize the device(s) connected to the JTAG interface. Its content is shifted out when INSTRUCTION register contains the IDCODE command (opcode  $04_{\rm H}$ ), and the same is also true immediately after reset.

The JTAG ID register contents for the XC87x Flash devices are given in **Table 36**.

Table 36 JTAG ID Summary

Device Type	Device Name	JTAG ID				
Flash	XC87x*-16FF	1018 2083 <sub>H</sub>				
	XC87x*-13FF	1018 3083 <sub>H</sub>				

Note: The asterisk (\*) above denotes all possible device configurations.



### 3.24 Chip Identification Number

The XC87x identity (ID) register is located at Page 1 of address  $B3_H$ . The value of ID register is  $49_H$ . However, for easy identification of product variants, the Chip Identification Number, which is an unique number assigned to each product variant, is available. The differentiation is based on the product, variant type and device step information.

Two methods are provided to read a device's chip identification number:

- In-application subroutine, GET\_CHIP\_INFO
- Bootstrap loader (BSL) mode A

Table 37 lists the chip identification numbers of available XC87x Flash device variants.

**Table 37** Chip Identification Number

<b>Product Variant</b>	Chip Identification Number AC-step						
Flash Devices							
XC878-16FF 5V	4B580063 <sub>H</sub>						
XC878M-16FF 5V	4B580023 <sub>H</sub>						
XC878CM-16FF 5V	4B580003 <sub>H</sub>						
XC878LM-16FF 5V	4B500023 <sub>H</sub>						
XC878CLM-16FF 5V	4B500003 <sub>H</sub>						
XC878-13FF 5V	4B590463 <sub>H</sub>						
XC878M-13FF 5V	4B590423 <sub>H</sub>						
XC878CM-13FF 5V	4B590403 <sub>H</sub>						
XC878LM-13FF 5V	4B510423 <sub>H</sub>						
XC878CLM-13FF 5V	4B510403 <sub>H</sub>						
XC878-16FF 3V3	4B180063 <sub>H</sub>						
XC878M-16FF 3V3	4B180023 <sub>H</sub>						
XC878CM-16FF 3V3	4B180003 <sub>H</sub>						
XC878-13FF 3V3	4B190463 <sub>H</sub>						
XC878M-13FF 3V3	4B190423 <sub>H</sub>						
XC878CM-13FF 3V3	4B190403 <sub>H</sub>						
XC874CM-16FV 5V	4B580002 <sub>H</sub>						
XC874LM-16FV 5V	4B500022 <sub>H</sub>						
XC874-16FV 5V	4B580062 <sub>H</sub>						



 Table 37
 Chip Identification Number (cont'd)

<b>Product Variant</b>	Chip Identification Number
	AC-step
XC874CM-13FV 5V	4B590402 <sub>H</sub>
XC874LM-13FV 5V	4B510422 <sub>H</sub>
XC874-13FV 5V	4B590462 <sub>H</sub>



### 4 Electrical Parameters

**Chapter 4** provides the characteristics of the electrical parameters which are implementation-specific for the XC87x.

#### 4.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in **Section 4.2** and **Section 4.3**.

### 4.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XC87x and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

#### · cc

These parameters indicate **C**ontroller **C**haracteristics, which are distinctive features of the XC87x and must be regarded for a system design.

#### SR

These parameters indicate **S**ystem **R**equirements, which must be provided by the microcontroller system in which the XC87x is designed in.

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### 4.1.2 Absolute Maximum Rating

Maximum ratings are the extreme limits to which the XC87x can be subjected to without permanent damage.

Table 38 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit	Values	Unit	Notes
		min.	max.		
Ambient temperature	$T_{A}$	-40	125	°C	under bias
Storage temperature	$T_{ST}$	-65	150	°C	
Junction temperature	$T_{J}$	-40	140	°C	under bias
Voltage on power supply pin with respect to V <sub>SS</sub>	$V_{DDP}$	-0.5	6	V	
Voltage on any pin with respect to $V_{\rm SS}$	V <sub>IN</sub>	-0.5	V <sub>DDP</sub> + 0.5 or max. 6	V	Whatever is lower
Input current on any pin during overload condition	$I_{IN}$	-10	10	mA	
Absolute sum of all input currents during overload condition	$\Sigma  I_{IN} $	_	50	mA	

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ( $V_{\rm IN} > V_{\rm DDP}$  or  $V_{\rm IN} < V_{\rm SS}$ ) the voltage on  $V_{\rm DDP}$  pin with respect to ground ( $V_{\rm SS}$ ) must not exceed the values defined by the absolute maximum ratings.



## 4.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the XC87x. All parameters mentioned in the following table refer to these operating conditions, unless otherwise noted.

**Table 39 Operating Condition Parameters** 

Parameter	Symbol	Limit	Values	Unit	Notes/	
		min.	max.		Conditions	
Digital power supply voltage	$V_{DDP}$	4.5	5.5	V	5V Device	
Digital power supply voltage	$V_{DDP}$	3.0	3.6	V	3.3V Device	
Digital ground voltage	$V_{SS}$	0		V		
CPU Clock Frequency <sup>1)</sup>	$f_{CCLK}$		26.67 <sup>2)</sup>	MHz		
Ambient temperature	$T_{A}$	-40	85	°C	SAF-XC878/874	
		-40	105	°C	SAX-XC878	
		-40	125	°C	SAK-XC878/874	

<sup>1)</sup>  $f_{\rm CCLK}$  is the input frequency to the XC800 core. Please refer to Figure 22 for detailed description.

<sup>2)</sup> Default setting of  $f_{\rm CCLK}$  upon reset is 24 MHz.



### 4.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

## 4.2.1 Input/Output Characteristics

**Table 40** provides the characteristics of the input/output pins of the XC87x.

 Table 40
 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit	Limit Values		Test Conditions	
				min. max.			
$\overline{V_{\text{DDP}}}$ = 5 V Range							
Output low voltage	$V_{OL}$	CC	_	0.6	V	$I_{OL}$ = 9 mA (DS = 0) <sup>1)</sup> $I_{OL}$ = 12 mA (DS = 1) <sup>2)</sup>	
Output high voltage	$V_{OH}$	CC	2.4	_	V	$I_{OH}$ = -20 mA (DS = 0) <sup>1)</sup> $I_{OH}$ = -25 mA (DS = 1) <sup>2)</sup>	
Input low voltage	$V_{IL}$	SR	-0.3	0.8	V	CMOS Mode	
Input high voltage	$V_{IH}$	SR	2.2	$V_{DDP}$	V	CMOS Mode	
Input Hysteresis	HYS	CC	0.35	_	V	CMOS Mode <sup>3)7)</sup>	
Input low voltage at XTAL1	$V_{ILX}$	SR	-0.3	0.8	V		
Input high voltage at XTAL1	$V_{IHX}$	SR	3.4	$V_{DDP}$	V		
Pull-up current	$I_{PU}$	SR	_	-20	μΑ	$V_{IH,min}$	
			-88	_	μΑ	$V_{IL,max}$	
Pull-down current	$I_{PD}$	SR	_	10	μΑ	$V_{IL,max}$	
			66	_	μΑ	$V_{IH,min}$	
Input leakage current	$I_{OZ1}$	CC	-1	1	μА	$0 < V_{IN} < V_{DDP},$ $T_{A} \le 105^{\circ}C^{4)}$	
Overload current on any pin	$I_{OV}$	SR	-5	5	mA		
Absolute sum of overload currents	$\Sigma  I_{OV} $	SR	_	25	mA	5)	
Voltage on any pin during $V_{\rm DDP}$ power off	$V_{PO}$	SR	_	0.3	V	6)	



Table 40 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit	Values	Unit	Test Conditions
			min.	max.		
Maximum current per pin (excluding $V_{\rm DDP}$ and $V_{\rm SS}$ )	$I_{M}SR$	SR	_	25	mA	
Maximum current for all pins (excluding $V_{\mathrm{DDP}}$ and $V_{\mathrm{SS}}$ )	$\Sigma  I_{M} $	SR	_	150	mA	
$\begin{array}{c} {\rm Maximum~current~into} \\ V_{\rm DDP} \end{array}$	$I_{\mathrm{MVDDP}}$	SR	_	200	mA	5)
$\begin{array}{c} \text{Maximum current out} \\ \text{of } V_{\text{SS}} \end{array}$	$I_{MVSS}$	SR	_	200	mA	5)
$V_{\rm DDP}$ = 3.3 V Range						
Output low voltage	$V_{OL}$	CC	_	0.5	V	$I_{\rm OL}$ = 6 mA (DS = 0) <sup>1)</sup> $I_{\rm OL}$ = 8 mA (DS = 1) <sup>2)</sup>
Output high voltage	$V_{OH}$	CC	2.2	_	V	$I_{OH}$ = -5 mA (DS = 0) <sup>1)</sup> $I_{OH}$ = -7 mA (DS = 1) <sup>2)</sup>
Input low voltage	$V_{IL}$	SR	-0.3	0.7	V	CMOS Mode
Input high voltage	$V_{IH}$	SR	2	$V_{DDP}$	V	CMOS Mode
Input Hysteresis	HYS	CC	0.28	_	V	CMOS Mode <sup>3)7)</sup>
Input low voltage at XTAL1	$V_{ILX}$	SR	-0.3	0.7	V	
Input high voltage at XTAL1	$V_{IHX}$	SR	2.3	$V_{DDP}$	V	
Pull-up current	$I_{PU}$	SR	_	-7	μΑ	$V_{IH,min}$
			-35	_	μΑ	$V_{\mathrm{IL,max}}$
Pull-down current	$I_{PD}$	SR		12	μΑ	$V_{\mathrm{IL,max}}$
			60		μА	$V_{\mathrm{IH,min}}$
Input leakage current	$I_{OZ1}$	CC	-1	1	μΑ	$0 < V_{IN} < V_{DDP},$ $T_A \le 105^{\circ}C^{4)}$
Overload current on any pin	$I_{OV}$	SR	-5	5	mA	
Absolute sum of overload currents	$\Sigma  I_{OV} $	SR	_	25	mA	5)



Table 40 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbo	Symbol		Values	Unit	Test Conditions
			min.	max.		
	$V_{PO}$	SR	_	0.3	V	6)
	$I_{M}SR$	SR	_	8	mA	
	$\Sigma  I_{M} $	SR	_	150	mA	
$\begin{tabular}{ll} \hline & & & \\ & & & $	$I_{MVDDP}$	SR	_	200	mA	5)
$\begin{tabular}{ll} \hline \textbf{Maximum current out} \\ \textbf{of } V_{\rm SS} \\ \hline \end{tabular}$	$I_{MVSS}$	SR	_	200	mA	5)

- 1) DS = 0 refers to the pin having a weak drive strength which is programmable via Px\_DS register.
- 2) DS = 1 refers to the pin having a strong drive strength which is programmable via Px DS register.
- 3) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
- 4) An additional error current ( $I_{INJ}$ ) will flow if an overload current flows through an adjacent pin. TMS pin and RESET pin have internal pull devices and are not included in the input leakage current characteristic.
- 5) Not subjected to production test, verified by design/characterization.
- 6) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when  $V_{\text{DDP}}$  is powered off.
- 7) P0.1 has a minimum input hysteresis of 0.25V.

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## 4.2.2 Supply Threshold Characteristics

Table 41 provides the characteristics of the supply threshold in the XC87x.

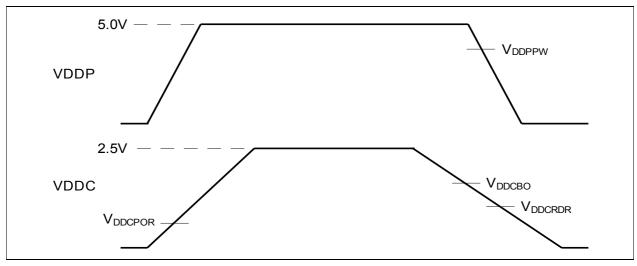


Figure 34 Supply Threshold Parameters

Table 41 Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol			Unit		
			min.	typ.	max.	
$\overline{V_{\rm DDC}}$ brownout voltage <sup>1)</sup>	$V_{DDCBO}$	CC	1.7	1.9	2.2	V
RAM data retention voltage	$V_{\mathtt{DDCRDR}}$	CC	1.2	_	_	V
$V_{\rm DDP}$ prewarning voltage <sup>2)</sup>	$V_{DDPPW}$	CC	3.8	4.2	4.5	V
Power-on reset voltage <sup>1)3)</sup>	$V_{DDCPOR}$	CC	1.7	1.9	2.2	V

- 1) Detection is enabled in both active and power-down mode.
- Detection is enabled for 5.0V power supply variant.
   Detection is disabled for 3.3V power supply variant.
- 3) The reset of EVR is extended by 300  $\mu$ s typically after the VDDC reaches the power-on reset voltage.

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#### 4.2.3 ADC Characteristics

The values in the table below are given for an analog power supply between 4.5 V to 5.5 V. The ADC can be used with an analog power supply down to 3 V. But in this case, the analog parameters may show a reduced performance. All ground pins ( $V_{\rm SS}$ ) must be externally connected to one single star point in the system. The voltage difference between the ground pins must not exceed 200mV.

Table 42 ADC Characteristics (Operating Conditions apply;  $V_{DDP} = 5V$  Range)

Parameter	Symbol		Lir	nit Val	ues	Unit	Test Conditions/
			min.	typ.	max.		Remarks
Analog reference voltage	$V_{AREF}$	SR	V <sub>AGND</sub> + 1	$V_{DDP}$	V <sub>DDP</sub> + 0.05	V	1)
Analog reference ground	$V_{AGND}$	SR	V <sub>SS</sub> - 0.05	$V_{SS}$	V <sub>AREF</sub>	V	1)
Analog input voltage range	$V_{AIN}$	SR	$V_{AGND}$	_	$V_{AREF}$	V	
ADC clocks	$f_{ADC}$		_	24	_	MHz	module clock <sup>1)</sup>
	$f_{ADCI}$		_	_	14 <sup>2)</sup>	MHz	internal analog clock <sup>1)</sup> See <b>Figure 31</b>
Sample time	$t_{\rm S}$	CC	$t_{ADCI}$	PCR0.	STC) ×	μS	1)
Conversion time	$t_{C}$	CC	See Se	ection	4.2.3.1	μS	1)
Differential Nonlinearity	$ EA_{DNL} $	CC	_	_	1.5	LSB	10-bit conversion
Integral Nonlinearity	$ EA_{INL} $	СС	_	_	2	LSB	10-bit conversion
Offset	$ EA_{OFF} $	CC	_	_	3	LSB	10-bit conversion
Gain	$ EA_{GAIN} $	CC	_	_	2.5	LSB	10-bit conversion
Switched capacitance at the reference voltage input	$C_{AREFSW}$	CC	_	10	14	pF	1)3)
Switched capacitance at the analog voltage inputs	$C_{AINSW}$	CC	_	4	5	pF	1)4)



Table 42 ADC Characteristics (Operating Conditions apply;  $V_{\text{DDP}}$  = 5V Range)

Parameter	Symbol		Lir	nit Val	ues	Unit	Test Conditions/
			min.	typ.	max.		Remarks
Input resistance of the reference input	$R_{AREF}$	CC	_	1	2	kΩ	1)
Input resistance of the selected analog channel	$R_{AIN}$	CC	_	1	3	kΩ	1)

- 1) Not subjected to production test, verified by design/characterization.
- 2) This value includes the maximum oscillator deviation.
- 3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.
- 4) The sampling capacity of the conversion C-Network is pre-charged to  $V_{\mathsf{AREF}}/2$  before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than  $V_{\mathsf{AREF}}/2$ .

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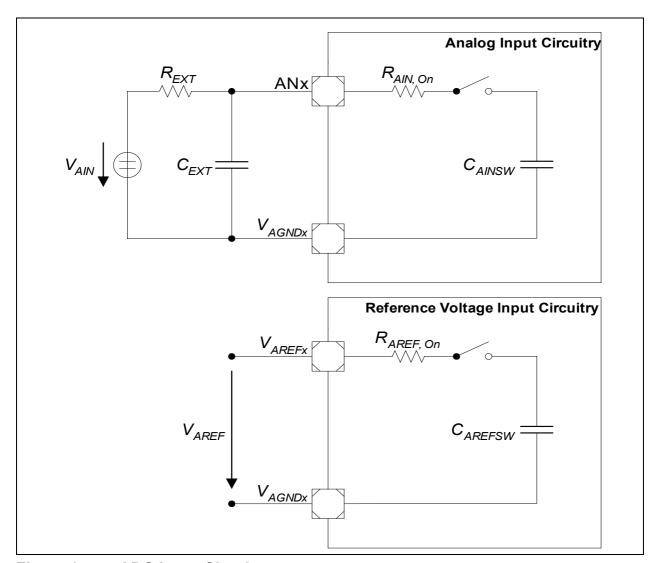


Figure 35 ADC Input Circuits

## 4.2.3.1 ADC Conversion Timing

```
Conversion time, t_{\rm C} = t_{\rm ADC} × (1 + r × (3 + n + STC)), where r = CTC + 2 for CTC = 00_{\rm B}, 01_{\rm B} or 10_{\rm B}, r = 32 for CTC = 11_{\rm B}, CTC = Conversion Time Control (GLOBCTR.CTC), STC = Sample Time Control (INPCR0.STC), n = 8 or 10 (for 8-bit and 10-bit conversion respectively), t_{\rm ADC} = 1 / f_{\rm ADC}
```



### 4.2.4 Power Supply Current

Table 43, Table 44, Table 45 and Table 46 provide the characteristics of the power supply current in the XC87x.

Table 43 Power Supply Current Parameters (Operating Conditions apply;  $V_{\text{DDP}} = 5V \text{ range}$ )

Parameter	Symbol	Limit \	Values	Unit	Test Conditions
		typ. <sup>1)</sup>	max. <sup>2)</sup>		
$V_{\rm DDP}$ = 5V Range				•	
Active Mode	$I_{DDP}$	37.5	45	mA	3) SAF and SAX variants
		40.5	48	mA	3) SAK variant
Idle Mode	$I_{DDP}$	29.2	35	mA	<sup>4)</sup> SAF and SAX variants
		32.2	38	mA	4) SAK variant
Active Mode with slow-	$I_{DDP}$	10	15	mA	5) SAF and SAX variants
down enabled		13	18	mA	5) SAK variant
Idle Mode with slow-	$I_{DDP}$	9.2	14	mA	6) SAF and SAX variants
down enabled		12.2	17	mA	6) SAK variant

<sup>1)</sup> The typical  $I_{\rm DDP}$  values are based on preliminary measurements and are to be used as reference only. These values are periodically measured at  $T_{\rm A}$  = + 25 °C and  $V_{\rm DDP}$  = 5.0 V.

- 2) The maximum  $I_{\rm DDP}$  values are measured under worst case conditions ( $T_{\rm A}$  = + 105 °C and  $V_{\rm DDP}$  = 5.5 V).
- 3)  $I_{\rm DDP}$  (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz with onchip oscillator of 4 MHz,  $\overline{\rm RESET} = V_{\rm DDP}$ ; all other pins are disconnected, no load on ports.
- 4)  $I_{\text{DDP}}$  (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz,  $\overline{\text{RESET}} = V_{\text{DDP}}$ ; all other pins are disconnected, no load on ports.
- 5)  $I_{\rm DDP}$  (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 1 MHz by setting CLKREL in CMCON to  $1000_{\rm B}$ ,  $\overline{\rm RESET} = V_{\rm DDP}$ ; all other pins are disconnected, no load on ports.
- 6)  $I_{\rm DDP}$  (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 1 MHz by setting CLKREL in CMCON to 1000<sub>B</sub>, RESET =  $V_{\rm DDP}$ ; all other pins are disconnected, no load on ports.

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Table 44 Power Down Current<sup>1)</sup>(Operating Conditions apply;  $V_{DDP} = 5V$  range)

Parameter	Symbol	Limit	Limit Values		<b>Test Conditions</b>
		typ. <sup>2)</sup> max. <sup>3)</sup>			
$V_{\rm DDP}$ = 5V Range	•				
Power-Down Mode	$I_{PDP}$	20	80	μА	$T_{A}$ = + 25 °C <sup>4)5)</sup>
		-	250	μА	$T_{A}$ = + 85 °C <sup>5)6)</sup>

- 1) The table is only applicable to SAF and SAX variants. SAK variant does not support power-down mode
- 2) The typical  $I_{\rm PDP}$  values are based on preliminary measurements and are to be used as reference only. These values are measured at  $V_{\rm DDP}$  = 5.0 V.
- 3) The maximum  $I_{\rm PDP}$  values are measured at  $V_{\rm DDP}$  = 5.5 V.
- 4)  $I_{PDP}$  has a maximum value of 450  $\mu$ A at  $T_A$  = + 105  $^{\circ}$ C.
- 5)  $I_{\text{PDP}}$  is measured with:  $\overline{\text{RESET}} = V_{\text{DDP}}$ ,  $V_{\text{AGND}} = V_{\text{SS}}$ , RXD/INT0 =  $V_{\text{DDP}}$ ; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.
- 6) Not subjected to production test, verified by design/characterization.

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Table 45 Power Supply Current Parameters<sup>1)</sup> (Operating Conditions apply;  $V_{\text{DDP}} = 3.3 \text{V range}$ )

Parameter	Symbol	Limit	Values	Unit	Test
	typ. <sup>2)</sup>		max. <sup>3)</sup>		Conditions
V <sub>DDP</sub> = 3.3V Range	•	_		1	
Active Mode	$I_{DDP}$	35.4	43	mA	4)
Idle Mode	$I_{DDP}$	27.6	33	mA	5)
Active Mode with slow-down enabled	$I_{DDP}$	8.6	13	mA	6)
Idle Mode with slow-down enabled	$I_{DDP}$	8	12	mA	7)

- 1) The table is only applicable to SAF and SAX variants.
- 2) The typical  $I_{\rm DDP}$  values are based on preliminary measurements and are to be used as reference only. These values are periodically measured at  $T_{\rm A}$  = + 25 °C and  $V_{\rm DDP}$  = 3.3 V.
- 3) The maximum  $I_{\rm DDP}$  values are measured under worst case conditions ( $T_{\rm A}$  = + 105 °C and  $V_{\rm DDP}$  = 3.6 V).
- 4)  $I_{\text{DDP}}$  (active mode) is measured with: CPU clock and input clock to all peripherals running at 24 MHz with onchip oscillator of 4 MHz,  $\overline{\text{RESET}} = V_{\text{DDP}}$ ; all other pins are disconnected, no load on ports.
- 5)  $I_{\rm DDP}$  (idle mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 24 MHz,  $\overline{\rm RESET} = V_{\rm DDP}$ ; all other pins are disconnected, no load on ports.
- 6)  $I_{\text{DDP}}$  (active mode with slow-down mode) is measured with: CPU clock and input clock to all peripherals running at 1 MHz by setting CLKREL in CMCON to  $1000_{\text{B}}$ ,  $\overline{\text{RESET}} = V_{\text{DDP}}$ ; all other pins are disconnected, no load on ports.
- 7)  $I_{\rm DDP}$  (idle mode with slow-down mode) is measured with: CPU clock disabled, watchdog timer disabled, input clock to all peripherals enabled and running at 1 MHz by setting CLKREL in CMCON to 1000<sub>B</sub>, RESET =  $V_{\rm DDP}$ ; all other pins are disconnected, no load on ports.

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Table 46 Power Down Current<sup>1)</sup>(Operating Conditions apply;  $V_{\rm DDP}$  = 3.3V range)

Parameter	Symbol	Limit	Values	Unit	Test Conditions
		typ. <sup>2)</sup>	max. <sup>3)</sup>		
$V_{\rm DDP}$ = 3.3V Range					
Power-Down Mode	$I_{PDP}$	20	80	μА	$T_{A}$ = + 25 °C <sup>4)5)</sup>
		-	250	μА	$T_{\rm A}$ = + 85 °C <sup>5)6)</sup>

- 1) The table is only applicable to SAF and SAX variants.
- 2) The typical  $I_{\rm PDP}$  values are based on preliminary measurements and are to be used as reference only. These values are measured at  $V_{\rm DDP}$  = 3.3 V.
- 3) The maximum  $I_{\rm PDP}$  values are measured at  $V_{\rm DDP}$  = 3.6 V.
- 4)  $I_{\rm PDP}$  has a maximum value of 450  $\mu A$  at  $T_{\rm A}$  = + 105  $^{\circ} C$ .
- 5)  $I_{\text{PDP}}$  is measured with:  $\overline{\text{RESET}} = V_{\text{DDP}}$ ,  $V_{\text{AGND}} = V_{\text{SS}}$ , RXD/INT0 =  $V_{\text{DDP}}$ ; rest of the ports are programmed to be input with either internal pull devices enabled or driven externally to ensure no floating inputs.
- 6) Not subjected to production test, verified by design/characterization.

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#### 4.3 AC Parameters

The electrical characteristics of the AC Parameters are detailed in this section.

## 4.3.1 Testing Waveforms

The testing waveforms for rise/fall time, output delay and output high impedance are shown in Figure 36, Figure 37 and Figure 38.

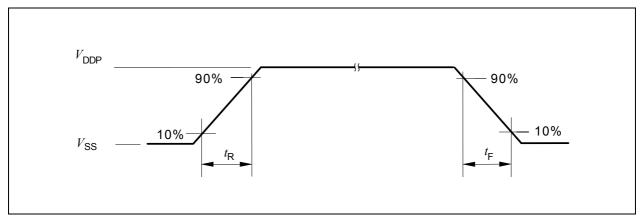


Figure 36 Rise/Fall Time Parameters

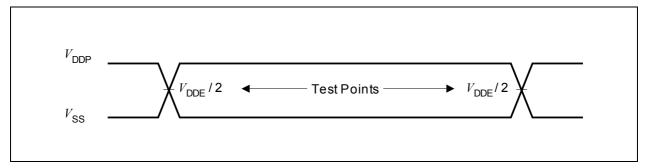


Figure 37 Testing Waveform, Output Delay

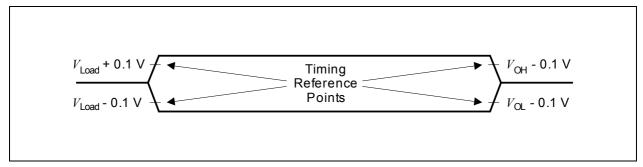


Figure 38 Testing Waveform, Output High Impedance



## 4.3.2 Output Rise/Fall Times

Table 47 provides the characteristics of the output rise/fall times in the XC87x.

Table 47 Output Rise/Fall Times Parameters (Operating Conditions apply)

•				` •	•	,				
Parameter	Symbol	Limit Values min. max.		_		_		Unit	Test Conditions	
$V_{\text{DDP}}$ = 5V Range										
Rise/fall times	t <sub>R</sub> , t <sub>F</sub>	_	10	ns	20 pF. <sup>1) 2)3)</sup>					
$V_{\rm DDP}$ = 3.3V Range										
Rise/fall times	$t_R, t_F$	_	10	ns	20 pF. <sup>1) 2)4)</sup>					

- 1) Rise/Fall time measurements are taken with 10% 90% of pad supply.
- 2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.
- 3) Additional rise/fall time valid for  $C_{\rm L}$  = 20pF 100pF @ 0.125 ns/pF.
- 4) Additional rise/fall time valid for  $C_{\rm L}$  = 20pF 100pF @ 0.225 ns/pF.

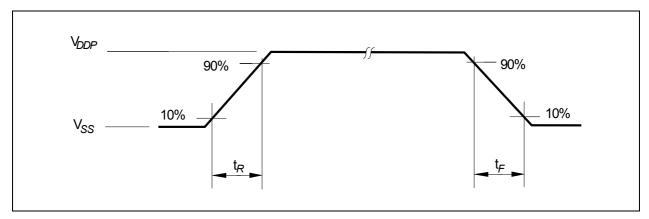


Figure 39 Rise/Fall Times Parameters



### 4.3.3 Power-on Reset and PLL Timing

Table 48 provides the characteristics of the power-on reset and PLL timing in the XC87x.

Table 48 Power-On Reset and PLL Timing (Operating Conditions apply)

Parameter	Symbol	Lir	nit Va	lues	Unit	<b>Test Conditions</b>	
			min.	typ.	max.		
On-Chip Oscillator start-up time	$t_{OSCST}$	CC	_	-	500	ns	1)
PLL lock-in in time	$t_{LOCK}$	CC	_	_	200	μS	1)
PLL accumulated jitter	$D_{P}$		_	_	1.8	ns	1)2)

- 1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.
- 2) PLL lock at 144 MHz using a 4 MHz external oscillator. The PLL Divider settings are K = 2, N = 72 and P = 1.

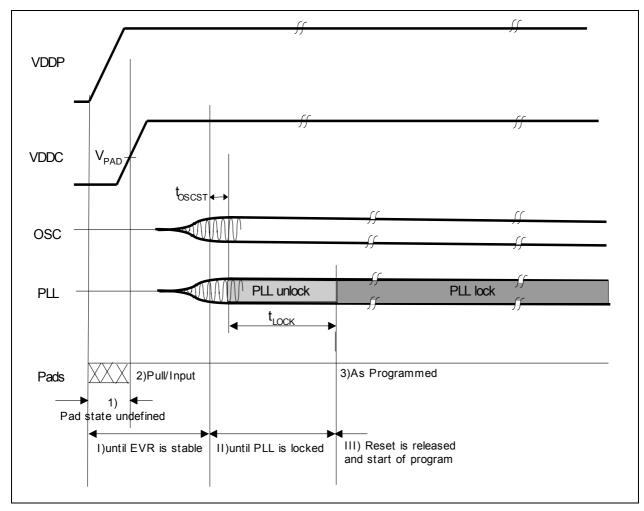


Figure 40 Power-on Reset Timing

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## 4.3.4 On-Chip Oscillator Characteristics

Table 49 provides the characteristics of the on-chip oscillator in the XC87x.

 Table 49
 On-chip Oscillator Characteristics (Operating Conditions apply)

Parameter	Sym	bol	Lin	nit Values		Unit	Test Conditions
			min.	typ.	max.		
Nominal frequency	$f_{NOM}$	CC	3.88	4	4.12	MHz	under nominal conditions <sup>1)</sup> after IFX-backend trimming
Long term frequency deviation	$\Delta f_{LT}$	CC	-5	_	5	%	with respect to $f_{\rm NOM}$ , over lifetime and temperature (-40°C to 105°C), for one given device after trimming
Short term frequency deviation	$\Delta f_{ST}$	CC	-1.0	_	1.0	%	within one LIN message (<10 ms 100 ms)

<sup>1)</sup> Nominal condition:  $V_{\rm DDC}$  = 2.5 V,  $T_{\rm A}$  = + 25°C.



## 4.3.5 External Data Memory Characteristics

**Table 50** shows the timing of the external data memory read cycle.

Table 50 External Data Memory Read Timing<sup>1)</sup> (Operating Conditions apply)

Parameter	Symbol	Limi	t Values	Unit	Test
		Min.	Max.		Conditions
RD pulse width	$t_1$ CC	2*f <sub>CCLK</sub> - 17	-	ns	2)
Address valid to RD	$t_2$ CC	$f_{\rm CCLK}$ - 12	-	ns	2)
RD to valid data in	$t_3$ SF		1.5* $f_{\text{CCLK}}$ - 27	ns	2)
Address to valid data in	$t_4$ SF		3*f <sub>CCLK</sub> - 7	ns	2)
Data hold after RD	$t_5$ SF	$0.5*f_{\text{CCLK}}$ -17	7 -	ns	2)

<sup>1)</sup> External Bus Interface is not available in XC874.

<sup>2)</sup> Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

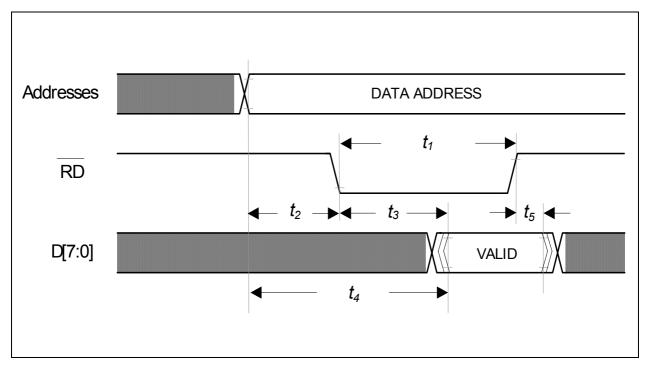


Figure 41 External Data Memory Read Cycle



Table 51 shows the timing of the external data memory write cycle.

Table 51 External Data Memory Write Timing<sup>1)</sup> (Operating Conditions apply)

Parameter	Symbol		Limit Va	lues	Unit	Test
			Min.	Max.		Conditions
WR pulse width	$t_1$	CC	f <sub>CCLK</sub> - 10	-	ns	2)
Address valid to WR	$t_2$	CC	2*f <sub>CCLK</sub> - 7	-	ns	2)
Data valid to WR transition	$t_3$	SR	$f_{\rm CCLK}$ - 5	-	ns	2)
Data setup before WR	$t_4$	SR	9*f <sub>CCLK</sub> - 13	-	ns	2)
Data hold after WR	<i>t</i> <sub>5</sub>	SR	6*f <sub>CCLK</sub> - 3	-	ns	2)

<sup>1)</sup> External Bus Interface is not available in XC874.

<sup>2)</sup> Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

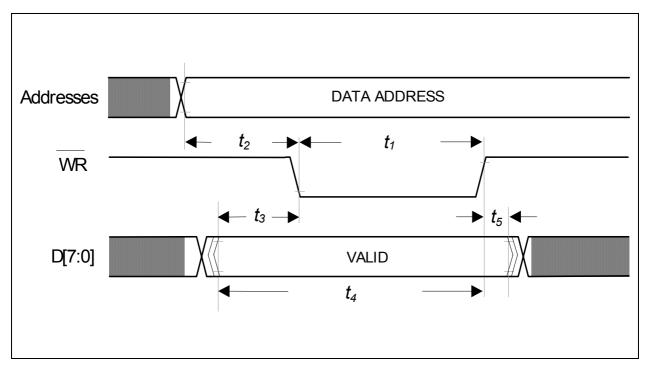


Figure 42 External Data Memory Write Cycle



#### 4.3.6 External Clock Drive XTAL1

**Table 52** shows the parameters that define the external clock supply for XC87x. These timing parameters are based on the direct XTAL1 drive of clock input signals. They are not applicable if an external crystal or ceramic resonator is considered.

Table 52 External Clock Drive Characteristics (Operating Conditions apply)

Parameter	Symbo	Symbol		t Values	Unit	Test Conditions
			Min.	Max.		
Oscillator period	$t_{ m osc}$	SR	50	500	ns	1)2)
High time	$t_1$	SR	15	-	ns	2)3)
Low time	$t_2$	SR	15	-	ns	2)3)
Rise time	$t_3$	SR	-	10	ns	2)3)
Fall time	$t_4$	SR	-	10	ns	2)3)

- 1) The clock input signals with 45-55% duty cycle are used.
- 2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.
- 3) The clock input signal must reach the defined levels  $V_{\rm ILX}$  and  $V_{\rm IHX}$ .

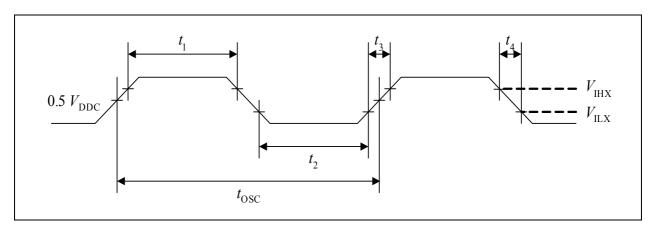


Figure 43 External Clock Drive XTAL1



## 4.3.7 JTAG Timing

**Table 53** provides the characteristics of the JTAG timing in the XC87x.

Table 53 TCK Clock Timing (Operating Conditions apply; CL = 50 pF)

Parameter	Sym	Symbol		nits	Unit	<b>Test Conditions</b>	
			min	max			
TCK clock period	$t_{TCK}$	SR	50	-	ns	1)	
TCK high time	<i>t</i> <sub>1</sub>	SR	20	-	ns	1)	
TCK low time	$t_2$	SR	20	-	ns	1)	
TCK clock rise time	$t_3$	SR	-	4	ns	1)	
TCK clock fall time	$t_4$	SR	-	4	ns	1)	

<sup>1)</sup> Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

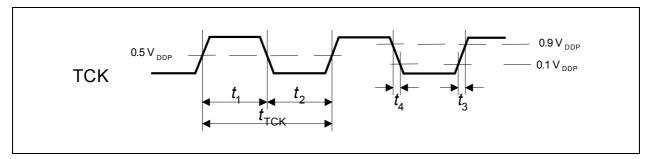


Figure 44 TCK Clock Timing

Table 54 JTAG Timing (Operating Conditions apply; CL = 50 pF)

Parameter	Syn	nbol	Lir	nits	Unit	<b>Test Conditions</b>
			min	max		
TMS setup to TCK  _√	$t_1$	SR	8	-	ns	1)
TMS hold to TCK  _√	$t_2$	SR	0	-	ns	1)
TDI setup to TCK	$t_1$	SR	8	-	ns	1)
TDI hold to TCK  _√	$t_2$	SR	4	-	ns	1)
TDO valid output from TCK	$t_3$	CC	-	24	ns	5V Device <sup>1)</sup>
			-	31	ns	3.3V Device <sup>1)</sup>



Table 54 JTAG Timing (Operating Conditions apply; CL = 50 pF) (cont'd)

Parameter		nbol	Lir	nits	Unit	<b>Test Conditions</b>	
			min	max			
TDO high impedance to valid output from TCK	$t_4$	CC	-	18	ns	5V Device <sup>1)</sup>	
			-	21	ns	3.3V Device <sup>1)</sup>	
TDO valid output to high impedance from TCK	<i>t</i> <sub>5</sub>	CC	-	21	ns	5V Device <sup>1)</sup>	
			-	20	ns	3.3V Device <sup>1)</sup>	

<sup>1)</sup> Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

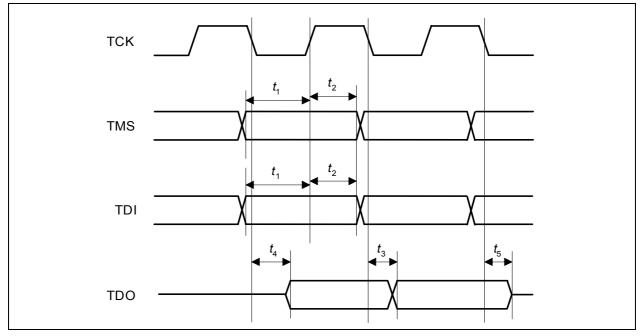


Figure 45 JTAG Timing

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## 4.3.8 SSC Master Mode Timing

**Table 55** provides the characteristics of the SSC timing in the XC87x.

Table 55 SSC Master Mode Timing (Operating Conditions apply; CL = 50 pF)

Parameter	Syn	nbol	Limit Values		Unit	<b>Test Conditions</b>	
			min.	max.			
SCLK clock period	$t_0$	CC	2*T <sub>SSC</sub>	_	ns	1)2)	
MTSR delay from SCLK	$t_1$	CC	0	5	ns	2)	
MRST setup to SCLK	$t_2$	SR	13	_	ns	2)	
MRST hold from SCLK	$t_3$	SR	0	_	ns	2)	

<sup>1)</sup>  $T_{SSCmin} = T_{CPU} = 1/f_{CPU}$ . When  $f_{CPU} = 24$  MHz,  $t_0 = 83.3$ ns.  $T_{CPU}$  is the CPU clock period.

<sup>2) 1</sup>Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

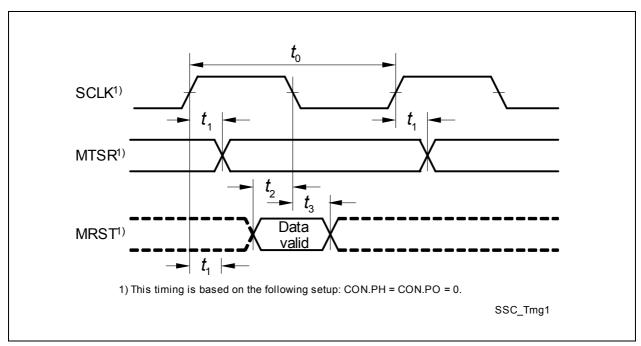


Figure 46 SSC Master Mode Timing

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## 5 Package and Quality Declaration

**Chapter 5** provides the information of the XC87x package and reliability section.

## 5.1 Package Parameters

**Table 56** provides the thermal characteristics of the package used in XC878 and XC874.

Table 56 Thermal Characteristics of the Packages

Parameter	Symbol		Lim	nit Values	Unit	Notes
			Min. Max.			
PG-LQFP-64-4 (XC878)				1	1	- 1
Thermal resistance junction case <sup>1)</sup>	$R_{TJC}$	CC	-	13.8	K/W	-
Thermal resistance junction lead <sup>1)</sup>	$R_{TJL}$	CC	-	34.6	K/W	-
PG-VQFN-48-22 (XC874)						
Thermal resistance junction case <sup>1)</sup>	$R_{TJC}$	CC	-	16.6	K/W	-
Thermal resistance junction lead <sup>1)</sup>	$R_{TJL}$	CC	-	30.7	K/W	-

<sup>1)</sup> The thermal resistances between the case and the ambient  $(R_{\mathsf{TCA}})$ , the lead and the ambient  $(R_{\mathsf{TLA}})$  are to be combined with the thermal resistances between the junction and the case  $(R_{\mathsf{TJC}})$ , the junction and the lead  $(R_{\mathsf{TJL}})$  given above, in order to calculate the total thermal resistance between the junction and the ambient  $(R_{\mathsf{TJA}})$ . The thermal resistances between the case and the ambient  $(R_{\mathsf{TCA}})$ , the lead and the ambient  $(R_{\mathsf{TLA}})$  depend on the external system (PCB, case) characteristics, and are under user responsibility.

- a) simply adding only the two thermal resistances (junction lead and lead ambient), or
- b) by taking all four resistances into account, depending on the precision needed.

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The junction temperature can be calculated using the following equation:  $T_J = T_A + R_{TJA} \times P_D$ , where the  $R_{TJA}$  is the total thermal resistance between the junction and the ambient. This total junction ambient resistance  $R_{TJA}$  can be obtained from the upper four partial thermal resistances, by



## 5.2 Package Outline

Figure 47 shows the package outlines of the XC878.

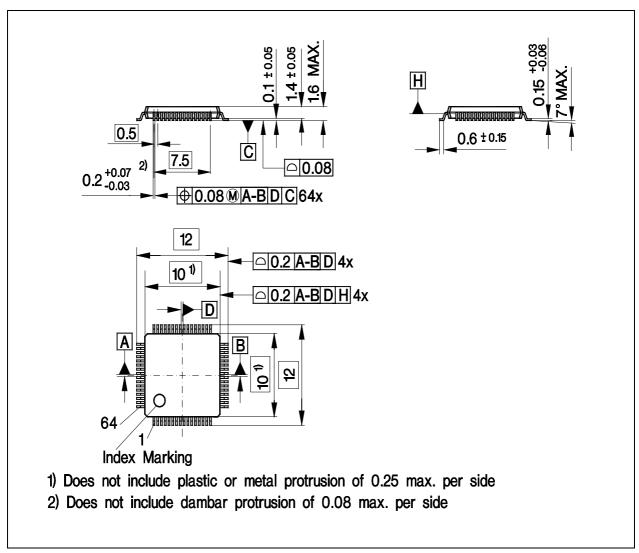


Figure 47 PG-LQFP-64-4 Package Outline



Figure 48 shows the package outlines of the XC874.

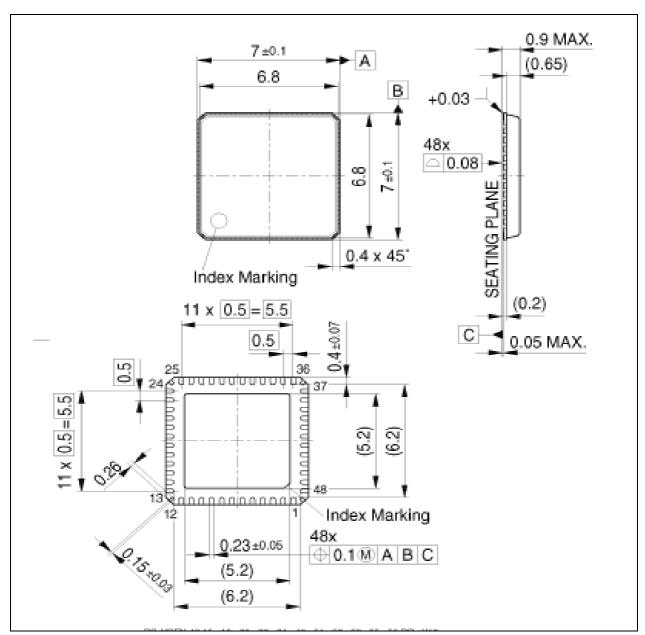


Figure 48 PG-VQFN-48-22 Package Outline

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# 5.3 Quality Declaration

Table 57 shows the characteristics of the quality parameters in the XC87x.

**Table 57** Quality Parameters

Parameter	Symbol	Limit Va	lues	Unit	Notes	
		Min.	Max.	1		
Operation Lifetime when the device is used at the two stated $T_{\rm J}^{1)}$	t <sub>OP1</sub>	-	15000	hours	T <sub>J</sub> = 110°C	
		-	2000	hours	$T_{\rm J} = -40^{\circ}{\rm C}$	
Operation Lifetime when the device is used at the five stated $T_{\rm J}^{1)}$	t <sub>OP2</sub>	-	120	hours	<i>T</i> <sub>J</sub> = 140°C	
		-	960	hours	<i>T</i> <sub>J</sub> = 135°C	
		-	7800	hours	T <sub>J</sub> = 91°C	
		-	2400	hours	T <sub>J</sub> = 38°C	
		-	720	hours	<i>T</i> <sub>J</sub> = -25°C	
ESD susceptibility according to Human Body Model (HBM)	$V_{HBM}$	-	2000	V	Conforming to EIA/JESD22- A114-B	
ESD susceptibility according to Charged Device Model (CDM) pins	$V_{CDM}$	-	750	V	Conforming to JESD22-C101-C	

<sup>1)</sup> This lifetime refers only to the time when device is powered-on.

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