CY7C65213

USB-UART LP Bridge Controller

Features

- USB 2.0 certified, Full-Speed (12 Mbps)
  - Supports communication driver class (CDC), personal health care device class (PHDC), and vendor-specific drivers
  - Battery charger detection (BCD) compliant with USB Battery Charging Specification Rev. 1.2 (peripheral detect only)
  - Integrated USB termination resistors
- Single-channel configurable UART interfaces
  - Data rates up to 3 Mbps
  - 256 bytes for each transmit and receive buffer
  - Data format:
    - 7 to8 data bits
    - 1 to 2 stop bits
    - No parity, even, odd, mark, or space parity
  - Supports parity, overrun, and framing errors
  - Supports flow control using CTS, RTS, DTR, DSR
- General-purpose input/output (GPIO): 8 pins
- Configuration utility (Windows) to configure the following:
  - Vendor ID (VID), Product ID (PID), and Product and Manufacturer descriptors
  - UART
  - Charger detection
  - GPIO
- Driver support for VCOM and DLL
  - Windows 8: 32- and 64-bit versions
  - Windows 7: 32- and 64-bit versions
  - Windows Vista: 32- and 64-bit versions
  - Windows XP: 32- and 64-bit versions
  - Windows CE
  - Mac OS-X: 10.6, 10.7
  - Linux: Kernel version 2.6.35 and later versions
  - Android: Gingerbread and later versions
- 512-byte flash for storing configuration parameters
- Clocking: Integrated 48-MHz clock oscillator
- USB suspend mode for low power
- Supports bus-/self-powered configurations
- Compatible with USB 2.0 and USB 3.0 host controllers
- Operating voltage: 1.71 to 5.50 V
- Operating temperature: –40 °C to 85 °C
- ESD protection: 2.2-kV HBM
- RoHS-compliant package
  - 32-pin QFN (5 × 5 × 1 mm, 0.5-mm pitch)
- Ordering part number
  - CY7C65213-32LTXI

Applications

- Blood glucose meter
- Battery-operated devices
- USB-to-UART cables
- Enables USB connectivity in legacy peripherals with UART
- Point-of-Sale (POS) terminals
- Industrial and T&M devices

USB Compliant

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The USB-UART LP Bridge controller (CY7C65213) is fully compliant with the USB 2.0 specification, USB-IF Test-ID (TID) 40860041.

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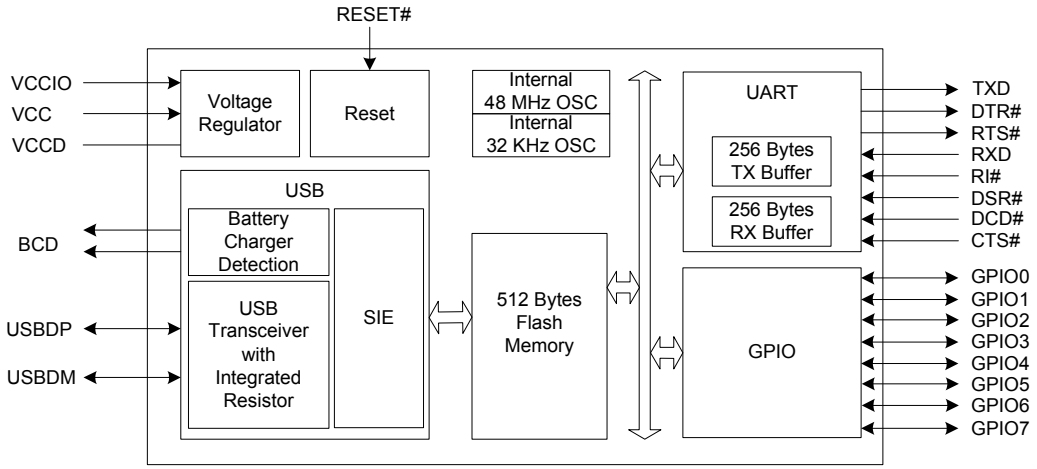
Block Diagram



Functional Overview

CY7C65213 is a fully integrated USB-to-UART bridge that provides a simple method to upgrade UART-based devices to USB with a minimal number of components. CY7C65213 includes a USB 2.0 Full-Speed controller, a UART transceiver, an internal regulator, an internal oscillator, and a 512-byte flash in a 32-pin QFN package.

The internal flash is used to store custom-specific USB descriptors and GPIO configuration. This is done in-system using a configuration utility that communicates over the USB interface.

Cypress provides royalty-free Virtual COM Port (VCP) device drivers. The drivers allow the device to appear as a COM port in PC applications. All UART signals, including handshaking and control signals, are implemented.

USB and Charger Detect

USB

CY7C65213 has a built-in USB 2.0 Full-Speed transceiver. The transceiver incorporates an internal USB series termination resistor on the USB data lines and a 1.5-kΩ pull-up resistor on the USBDP.

Charger Detection

CY7C65213 supports BCD for Peripheral Detect only and complies with the USB Battery Charging Specification, Rev. 1.2. It supports the following charging ports:

- Standard Downstream Port (SDP): Allows the system to draw up to 500-mA current from the host
- Charging Downstream Port (CDP): Allows the system to draw up to 1.5-A current from the host
- Dedicated Charging Port (DCP): Allows the system to draw up to 1.5-A of current from the wall charger

UART Interface

The UART interface provides asynchronous serial communication with other UART devices operating at speeds of up to 3 Mbits/second. It supports 7 to 8 data bits, 1 to 2 stop bits, odd, even, mark, space, and no parity. The UART interface supports full-duplex communication with a signaling format compatible with the standard UART protocol. The UART pins may be interfaced to industry-standard RS-232 transceivers to manage different voltage levels.

Common UART functions, such as parity error and frame error, are supported. A 256-byte buffer is available in both TX and RX directions. CY7C65213 supports baud rates ranging from 300 baud to 3 Mbaud. UART baud rates can be set using the configuration utility.

UART Flow Control

The CY7C65213 device supports UART hardware flow control using control signal pairs, such as RTS# (Request to Send) /-CTS# (Clear to Send) and DTR# (Data Terminal Ready) / DSR# (Data Set Ready). Data flow control is enabled by default. Flow control can be disabled using the configuration utility.

The following sections describe the flow control signals:

- CTS# (Input) / RTS# (Output)

CTS# can pause or resume data transmission over the UART interface. Data transmission can be paused by de-asserting the CTS signal and resumed by using CTS# assertion. The pause and resume operation does not affect data integrity. The receive buffer has a watermark level of 80%. After the data in the receive buffer reaches that level, the RTS# signal is de-asserted, instructing the transmitting device to stop data transmission. The start of data consumption by the application reduces device data backlog. After it reaches the 50% watermark level, the RTS# signal is asserted to resume data reception.

- DSR# (Input) / DTR# (Output)

The DSR#/DTR# signals are used to establish a communication link with the UART. These signals complement each other in their functionality, similar to CTS# and RTS#.

GPIO Interface

CY7C65213 has eight GPIOs. The configuration utility lets you configure the GPIO pins. The configurable options are as follows:

- TRISTATE: GPIO tristated
- DRIVE 1: Output static 1
- DRIVE 0: Output static 0
- POWER#: Power control for bus power designs
- TXLED#: Drives LED during USB transmit
- RXLED#: Drives LED during USB receive
- TX or RX LED#: Drives LED during USB transmit or receive

  GPIO can be configured to drive LED at 8-mA drive strength.
- SLEEP#: Indicates USB suspend
- BCD0/1: Two-pin output to indicate the type of USB charger
- BUSDETECT: Connects VBUS pin for USB host detection

Memory

CY7C65213 has a 512-byte flash. Flash is used to store USB parameters, such as VID/PID, serial number, and Product and Manufacturer Descriptors, which can be programmed by the configuration utility.

System Resources

Power System

CY7C65213 supports the USB Suspend mode to control power usage. CY7C65215 operates in bus-powered or self-powered modes over a range of 3.15 V to 5.25 V.

Clock System

CY7C65213 has a fully integrated clock and does not require any external crystal. The clock system is responsible for providing clocks to all subsystems.

Internal 48-MHz Oscillator

The internal 48-MHz oscillator is the primary source of internal clocking in the CY7C65213 device.

Internal 32-kHz Oscillator

The internal 32-kHz oscillator, which is low-power and relatively inaccurate, is primarily used to generate clocks for peripheral operation in the USB Suspend mode.

Reset

The reset block ensures reliable power-on reset or reconfiguration to a known state. The RESET# (active low) pin can be used by external devices to reset the CY7C65213.

Suspend and Resume

The CY7C65213 device asserts the SLEEP# pin when the USB bus goes into the suspend state. This helps to meet the stringent suspend current requirements of the USB 2.0 specification, while using the device in bus-powered mode. The device resumes from the suspend state under either of the following two conditions:

1. Any activity is detected on the USB bus
2. The RI# (configured as wakeup) pin is asserted to generate remote wakeup to the host.

WAKEUP

The RI# (configured as wakeup) pin is used to generate the remote wakeup signal on the USB bus. The remote wakeup signal is sent only if the host enables this feature through the SET_FEATURE request. The device communicates support for the remote wakeup to the host through the configuration descriptor during the USB enumeration process. The CY7C65213 device allows enabling/disabling of the remote wakeup feature through the configuration utility.

Software

Cypress delivers a complete set of software drivers and a configuration utility to enable product configuration during system development.

Drivers for Linux Operating Systems

Cypress provides a User Mode USB driver library (*libcyusb-serial.so*) that abstracts vendor commands for the UART interface and provides a simplified API interface for user applications. This library uses the standard open-source libUSB library to enable USB communication. The Cypress serial library supports the USB plug-and-play feature using the Linux 'udev' mechanism.

CY7C65213 supports the standard USB CDC UART-class driver, which is bundled with the Linux kernel.

Android Support

The CY7C65213 solution also includes an Android Java class–CyUsbSerial.java–which exposes a set of interface functions to communicate with the device.

Drivers for Mac OSx

Cypress delivers a dynamically linked shared library (*CyUSB-Serial.dylib*) based on libUSB, which enables communication to the CY7C65213 device.

In addition, the device also supports the native Mac OSx CDC UART-class driver.

Drivers for Windows Operating Systems

For Windows operating systems (XP, Vista, Win7, and Win8), Cypress delivers a User Mode dynamically linked library–CyUSBSerial DLL.This library abstracts the vendor-specific interface of the CY7C65213 devices and provides convenient APIs to the user. It provides interface APIs for vendor-specific UART and class-specific APIs for PHDC.

A virtual COM port driver–CyUSBSerial.sys–is also delivered, which implements the USB CDC class driver. The Cypress Windows drivers are:

- Windows Driver Foundation (WDF) compliant
- Compatible with any USB 2.0-compliant device
- Compatible with Cypress USB 3.0-compliant devices

They also support Windows plug-and-play and power management and USB Remote Wake-up

CY7C65213 also works with the Windows-standard USB CDC UART class driver.

Windows-CE support

The CY7C65213 solution also includes a dynamically linked library (DLL) and a CDC UART driver library for Windows-CE platforms.

Device Configuration Utility (Windows only)

A Windows-based configuration utility is available to configure device initialization parameters. This graphical user application provides an interactive interface to define boot parameters stored in the device flash.

This utility allows the user to save a user-selected configuration to text or xml formats. It also allows users to load a selected configurations from text or xml formats. The configuration utility allows the following operations:

- View current device configuration
- Select and configure UART, battery charging, and GPIOs
- Configure USB VID, PID, and string descriptors
- Save or Load configuration

You can download the free configuration utility and drivers at www.cypress.com.

Internal Flash Configuration

The internal flash memory can be used to store configuration parameters as shown in the following table. A free configuration utility is provided to configure the parameters listed in the table to meet application-specific requirements over a USB interface. The configuration utility can be downloaded at www.cypress.com.

Table 1. Internal Flash Configuration

Parameter	Default Value	Description
USB Configuration		
USB Vendor ID (VID)	0x04B4	Default Cypress VID. Can be configured to customer VID
USB Product ID (PID)	0x0003	Default Cypress PID. Can be configured to customer PID
Manufacturer string	Cypress	Can be configured with any string up to 64 characters
Product string	USB-UART LP	Can be configured with any string up to 64 characters
Serial string		Can be configured with any string up to 64 characters
Power mode	Bus powered	Can be configured to bus-powered or self-powered mode
Max current draw	100 mA	Can be configured to any value from 0 to 500 mA. The configuration descriptor will be updated based on this.
Remote wakeup	Enabled	Can be disabled. Remote wakeup is initiated by driving #RI low
USB interface protocol	CDC	Can be configured to function in CDC, PHDC, or Cypress vendor class
BCD	Disabled	Charger detect is disabled by default. When BCD is enabled, three of the GPIOs must be configured for BCD
GPIO Configuration		
GPIO0	TXLED#	GPIO can be configured as shown in Table 11 on page 11.
GPIO1	RXLED#	
GPIO2	TRISTATE	
GPIO3	POWER#	
GPIO4	SLEEP#	
GPIO5	BUSDETECT	
GPIO6	BCD0	
GPIO7	BCD1	

Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings [1] may shorten the useful life of the device.

Storage temperature ..... –55 °C to +100 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Supply voltage to ground potential

V_{CCIO} ..... 6.0 V

V_{CC} ..... 6.0 V

V_{CCD} ..... 1.95 V

V_{GPIO} ..... V_{CCIO} + 0.5

Static discharge voltage ESD protection levels:

■ 2.2-kV HBM per JESD22-A114

Latch-up current ..... 140 mA

Maximum current per GPIO ..... 25 mA

Operating Conditions

T_A (ambient temperature under bias)

Industrial ..... –40 °C to +85 °C

V_{CC} supply voltage ..... 3.15 V to 5.25 V

V_{CCIO} supply voltage ..... 1.71 V to 5.50 V

V_{CCD} supply voltage ..... 1.71 V to 1.89 V

Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C, T_J ≤ 100 °C, and 1.71 V to 5.50 V, except where noted.

Table 2. DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{CC}	V_{CC} supply voltage	3.15	3.30	3.45	V	Set and configure correct voltage range using the configuration utility for V_{CC}. Default 5 V.
		4.35	5.00	5.25	V	
V_{CCIO}	V_{CCIO} supply voltage	1.71	1.80	1.89	V	Used to set I/O voltage. Set and configure the correct voltage range using the configuration utility for V_{CCIO}. Default 3.3 V.
		2.0	3.3	5.5	V	
V_{CCD}	Output voltage (for core logic)	–	1.80	–	V	Do not use this supply to drive the external device. • 1.71 V ≤ VCCIO ≤ 1.89 V: Short V_{CCD} pin with the V_{CCIO} pin • V_{CCIO} > 2 V – connect a 1-µF capacitor (Cefc) between the V_{CCD} pin and ground
Cefc	External Regulator voltage bypass	1.00	1.30	1.60	µF	X5R ceramic or better
I_{CC1}	Operating supply current	–	20	–	mA	USB 2.0 FS, UART at 1-Mbps single channel, no GPIO switching
I_{CC2}	USB Suspend supply current	–	5	–	µA	Does not include current through the pull-up resistor on USBDP

Table 3. AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_1	Frequency	47.04	48	48.96	Mhz	Non-USB mode
F_2		47.88	48	48.12		USB mode
Z_{OUT}	USB driver output impedance	28	–	44	Ω	
Twakeup	Wakeup from USB Suspend mode	–	25	–	µs	

Note

1. Usage above the absolute maximum conditions may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

GPIO

Table 4. GPIO DC Specification

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}[2]	Input voltage high threshold	0.7 × V_{CCIO}	–	–	V	CMOS Input
V_{IL}	Input voltage low threshold	–	–	0.3 × V_{CCIO}	V	CMOS Input
V_{IH}[2]	LVTTL input, V_{CCIO}< 2.7 V	0.7 × V_{CCIO}	–	–	V	
V_{IL}	LVTTL input, V_{CCIO} < 2.7 V	–	–	0.3 × V_{CCIO}	V	
V_{IH}[2]	LVTTL input, V_{CCIO} ≥ 2.7 V	2	–	–	V	
V_{IL}	LVTTL input, V_{CCIO} ≥ 2.7 V	–	–	0.8	V	
V_{OH}	Output voltage high level	V_{CCIO} –0.4	–	–	V	I_{OH} = 4 mA, V_{CCIO} = 5 V +/- 10%
V_{OH}	Output voltage high level	V_{CCIO} –0.6	–	–	V	I_{OH} = 4 mA, V_{CCIO} = 3.3 V +/- 10%
V_{OH}	Output voltage high level	V_{CCIO} –0.5	–	–	V	I_{OH} = 1 mA, V_{CCIO} = 1.8 V +/- 5%
V_{OL}	Output voltage low level	–	–	0.4	V	I_{OL} = 8 mA, V_{CCIO} = 5 V +/- 10%
V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 8 mA, V_{CCIO} = 3.3 V +/- 10%
V_{OL}	Output voltage low level	–	–	0.6	V	I_{OL} = 4 mA, V_{CCIO} = 1.8 V +/- 5%
Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	
Rpulldown	Pull-down resistor	3.5	5.6	8.5	kΩ	
I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, V_{CCIO} = 3.0 V
C_{IN}	Input Capacitance	–	–	7	pF	
Vhysttl	Input hysteresis LVTTL; V_{CCIO} > 2.7 V	25	40	–	mV	
Vhyscmos	Input hysteresis CMOS	0.05 × V_{CCIO}	–	–	mV	

Table 5. GPIO AC Specification

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
$T_{RiseFast1}$	Rise Time in Fast mode	2	–	12	ns	V_{CCIO} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{FallFast1}$	Fall Time in Fast mode	2	–	12	ns	V_{CCIO} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{RiseSlow1}$	Rise Time in Slow mode	10	–	60	ns	V_{CCIO} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{FallSlow1}$	Fall Time in Slow mode	10	–	60	ns	V_{CCIO} = 3.3 V/ 5.5 V, Cload = 25 pF
$T_{RiseFast2}$	Rise Time in Fast mode	2	–	20	ns	V_{CCIO} = 1.8 V, Cload = 25 pF
$T_{FallFast2}$	Fall Time in Fast mode	20	–	100	ns	V_{CCIO} = 1.8 V, Cload = 25 pF
$T_{RiseSlow2}$	Rise Time in Slow mode	2	–	20	ns	V_{CCIO} = 1.8 V, Cload = 25 pF
$T_{FallSlow2}$	Fall Time in Slow mode	20	–	100	ns	V_{CCIO} = 1.8 V, Cload = 25 pF

Note
2. V_{IH} must not exceed V_{CCIO} + 0.2 V.

Reset

Table 6. Reset DC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
V_{IH}	Input voltage high threshold	$0.7 \times V_{CCIO}$	–	–	V	
V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{CCIO}$	V	
Rpullup	Pull-up resistor	3.5	5.6	8.5	kΩ	
C_{IN}	Input capacitance	–	5	–	pF	
Vhysxres	Input voltage hysteresis	–	100	–	mV	

Table 7. Reset AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Tresetwidth	Reset pulse width	1	–	–	µs	

Table 8. UART AC Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
F_{UART}	UART bit rate	0.3	–	3,000	kbps	

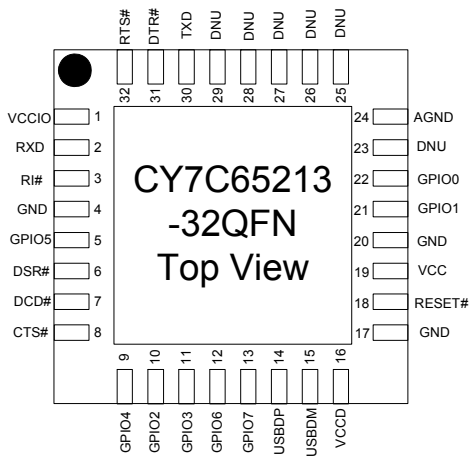
Table 9. Flash Memory Specifications

Parameter	Description	Min	Typ	Max	Units	Details/Conditions
Fend	Flash endurance	100K	–	–	cycles	
Fret	Flash retention. $T_A \leq 85$ °C, 10 K program/erase cycles	10	–	–	years	

Pin Description

Table 10. CY7C65213 Pin Description [3, 4]

Pin	Name	Type	Default	Description
1	VCCIO	Power	–	Supply to the device core and Interface, 1.71 to 5.5 V
2	RXD	Input	–	Receiving asynchronous data input
3	RI#	Input	–	Ring indicator control input. Can be configured as wake-up; low signal on this pin is used to wake up the USB Host controller out of the suspend state
4	GND	Power	–	Digital Ground
5	GPIO5	I/O	TRISTATE	Configurable GPIO. See Table 11.
6	DSR#	Input	–	Data set ready control input
7	DCD#	Input	–	Data carrier detect control input
8	CTS#	Input	–	Clear to send control input
9	GPIO4	I/O	SLEEP#	Configurable GPIO. See Table 11.
10	GPIO2	I/O	TRISTATE	Configurable GPIO. See Table 11.
11	GPIO3	I/O	POWER#	Configurable GPIO. See Table 11.
12	GPIO6	I/O	TRISTATE	Configurable GPIO. See Table 11.
13	GPIO7	I/O	TRISTATE	Configurable GPIO. See Table 11.
14	USBDP	USBIO	–	USB Data Signal Plus, integrating termination resistor and a 1.5-kΩ pull-up resistor
15	USBDM	USBIO	–	USB Data Signal Minus, integrating termination resistor
16	VCCD	Power	–	Decouple this pin to ground using a 1-µF capacitor or connecting a 1.8-V supply
17	GND	Power	–	Digital Ground
18	RESET#	XRES	–	Chip reset, active low. Can be left unconnected or have a pull-up resistor connected if not used.
19	VCC	Power	–	Supply voltage (USB) 3.15 to 5.25 V
20	GND	Power	–	Digital Ground
21	GPIO1	I/O	RXLED#	Configurable GPIO. See Table 11.
22	GPIO0	I/O	TXLED#	Configurable GPIO. See Table 11.
23	DNU	-	–	Do Not Use
24	AGND	Power	–	Analog Ground
25	DNU	-	–	Do Not Use
26	DNU	-	–	Do Not Use
27	DNU	-	–	Do Not Use
28	DNU	-	–	Do Not Use
29	DNU	-	–	Do Not Use



Notes
3. All active low signals for the signal name are indicated by a # in this document.
4. Any pin acting as an Input pin should not be left unconnected.

Table 10. CY7C65213 Pin Description *(continued)* [3, 4]

Pin	Name	Type	Default	Description	
30	TXD	Output	–	Transmit asynchronous data output	
31	DTR#	Output	–	Data terminal ready control output	
32	RTS#	Output	–	Request to send control output	

Table 11. GPIO Configuration

(The following signal options can be configured on the GPIO pins using a Cypress-provided configuration utility, which you can download at www.cypress.com)

GPIO Configuration Option	Description
TRISTATE	I/O tristated
DRIVE 1	Output static 1
DRIVE 0	Output static 0
POWER#	This output is used to control power to an external logic through a switch to cut off power prior to USB configuration and during USB suspend. 0 - USB device in Configured state 1 - USB device in Unconfigured state or during USB suspend mode
TXLED#	Drives LED during USB transmit
RXLED#	Drives LED during USB receive
TX and RX LED#	Drives LED during USB transmit and receive
SLEEP#	When low indicates USB suspend
BCD0	Configurable battery charger detect pins to indicate the type of USB charger (SDP, CDP, or DCP) Configuration example: 00 - Draw up to 100 mA (Unconfigured state) 01 - SDP (up to 500 mA) 10 - CDP/DCP (up to 1.5 A) 11 - Suspend (up to 2.5 mA) This truth table can be configured using a configuration utility
BCD1	
BUSDETECT	VBUS detection. Connect VBUS to this pin for VBUS detection when using the BCD feature[5].

Note

5. When VBUS = VCCIO, connect VBUS to BUSDETECTION with a 10-K series resistor
   When VBUS > VCCIO, connect VBUS to BUSDETECTION via the resistor divider network. Select R1 and R2 values as follows:
   R1 ≥ 10 k
   R2 / (R1 + R2) = VCCIO/VBUS

USB Power Configuration

The following section describes possible USB power configurations for the CY7C65213. Refer to the Pin Description on page 10 for signal details.

USB Bus-Powered Configuration

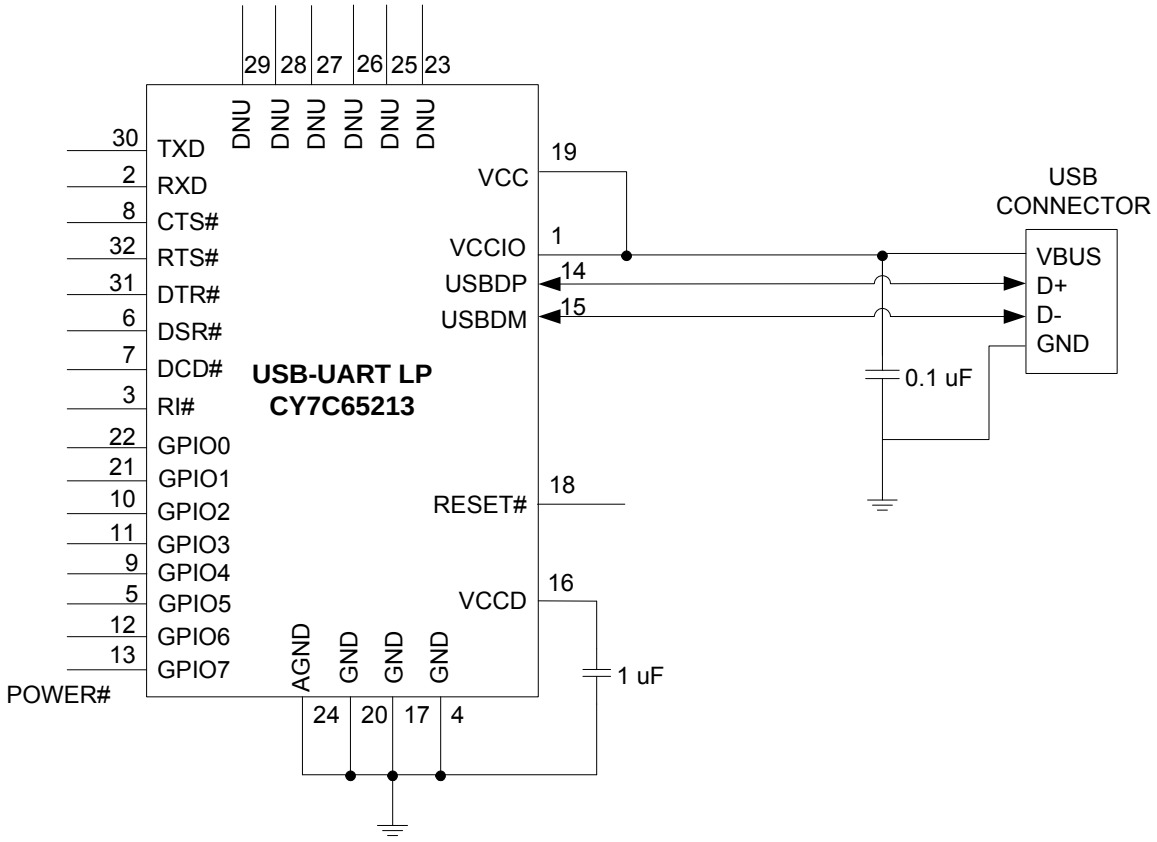
Figure 1 shows an example of the CY7C65213 in a bus-powered design. VBUS is connected directly to the CY7C65213 because it has an internal regulator.

The USB bus-powered system must comply with the following requirements:

1. The system should not draw more than 100 mA prior to USB enumeration (unconfigured state).
2. The system should not draw more than 2.5 mA during USB Suspend mode.
3. A high-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration and 2.5 mA during USB Suspend state.
4. The system should not draw more than 500 mA from the USB host.

The configuration descriptor in the CY7C65213 flash should be updated to indicate bus power and the maximum current required by the system using a configuration utility.

Figure 1. Bus-Powered Configuration



Self-Powered Configuration

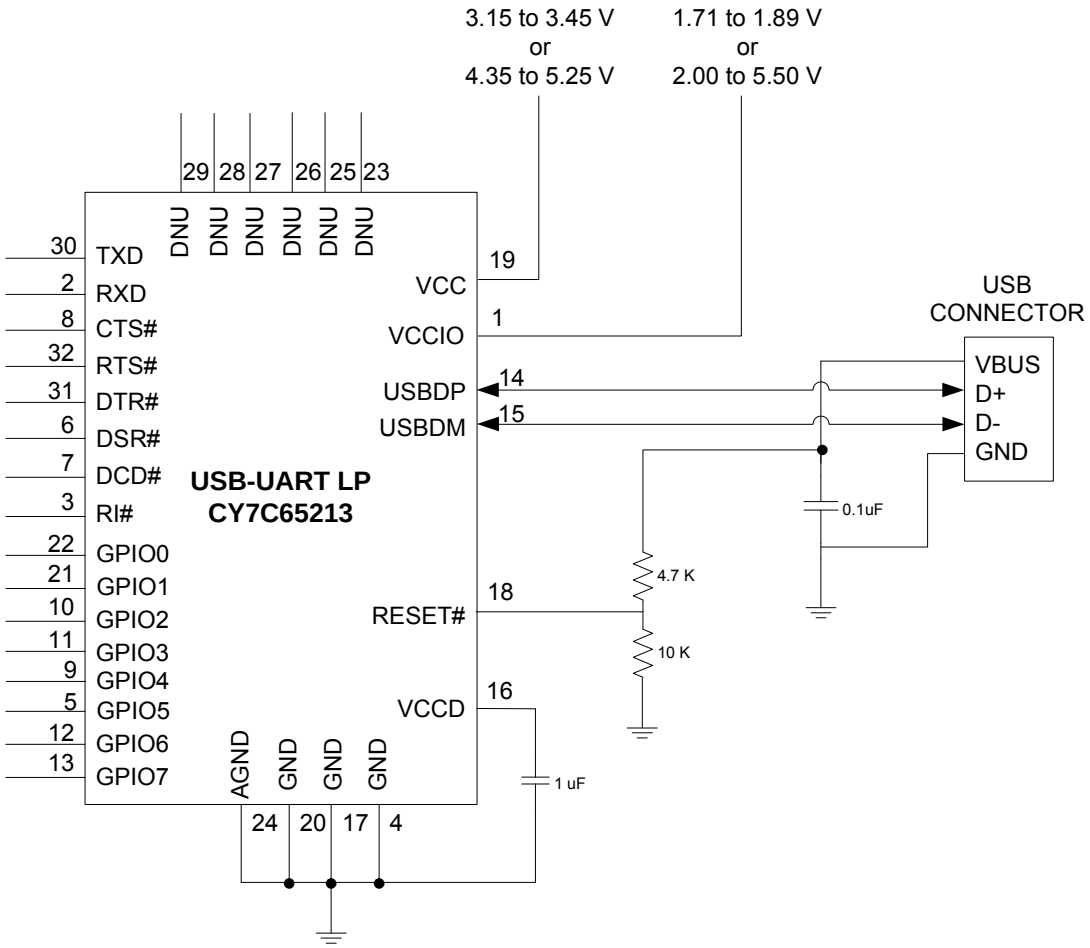
Figure 2 shows an example of CY7C65213 in a self-powered design. A self-powered system does not use VBUS from the host to power the system but has its own power supply. A self-powered system has no restriction on current consumption because it does not draw any current from the VBUS.

The VBUS of the USB host is used to control the RESET# pin of CY7C65213. When the VBUS is present, reset to CY7C65213 is de-asserted and the device enables an internal, 1.5-kΩ pull-up resistor on USBDP. When the VBUS is absent (the USB host is powered down), reset to CY7C65213 is asserted, which causes the device to remove the 1.5-kΩ pull-up resistor on USBDP. This ensures that no current flows from the USBDP to the USB host through a 1.5-kΩ pull-up resistor, to comply with USB 2.0 specification.

When reset is asserted to CY7C65213, all the I/O pins are tristated.

Using the configuration utility, the configuration descriptor in the CY7C65213 flash should be updated to indicate that it is self-powered.

Figure 2. Self-Powered Configuration



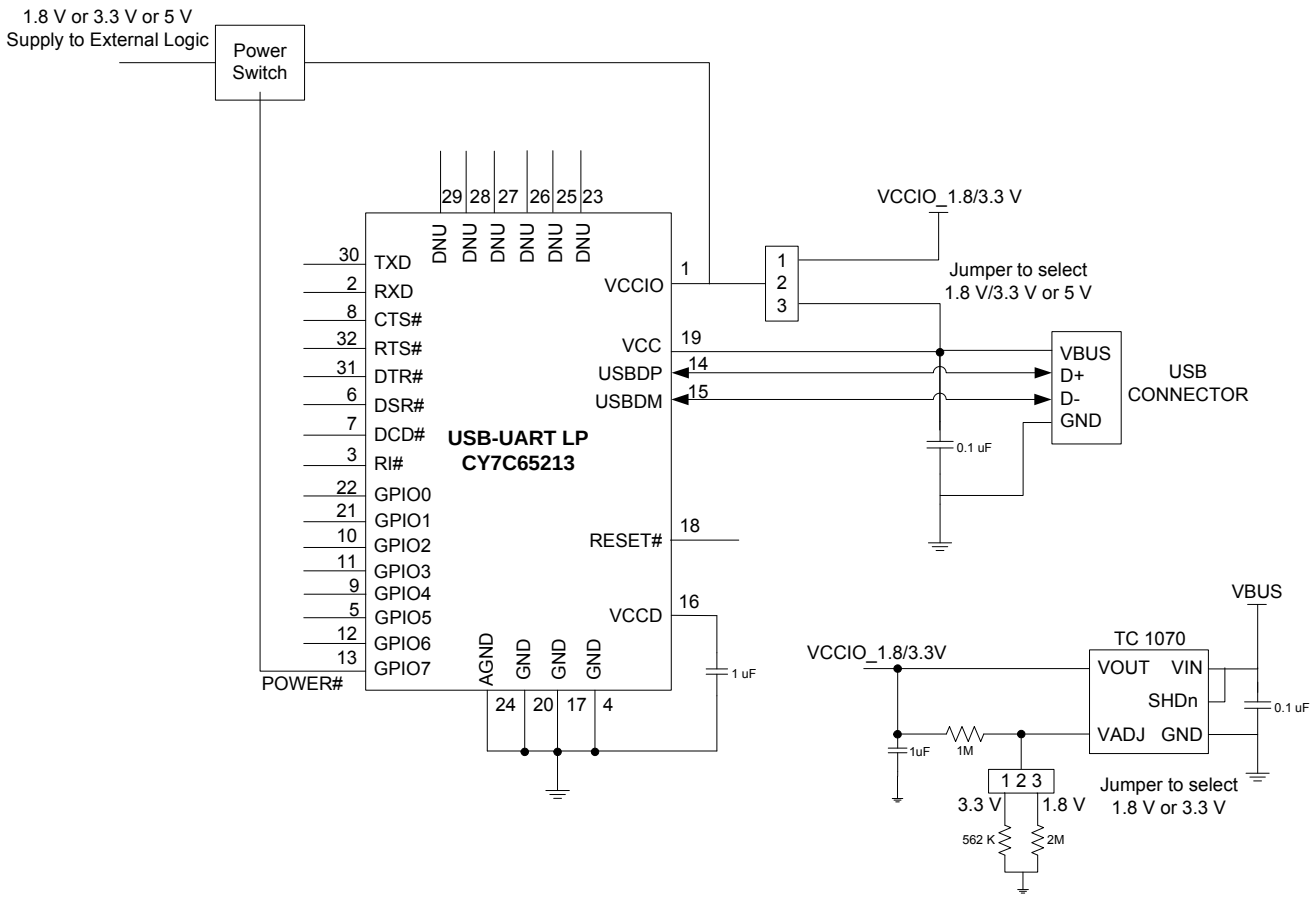
USB Bus Powered with Variable I/O Voltage

Figure 3 shows the CY7C65213 in a bus-powered system with variable I/O voltage. A low dropout (LDO) regulator is used to supply 1.8 V or 3.3 V (using a jumper switch) the input of which is 5 V from the VBUS. Another jumper switch is used to select VCCIO_1.8/3.3 V or 5 V from the VBUS for the VCCIO pin of CY7C65213. This allows I/O voltage and supply to external logic to be selected among 1.8 V, 3.3 V, or 5 V.

The USB bus-powered system must comply with the following:

1. The system should not draw more than 100 mA prior to USB enumeration (Unconfigured state).
2. The system should not draw more than 2.5 mA during USB Suspend mode.
3. A hjgh-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration and 2.5 mA during USB Suspend state.

Figure 3. USB Bus-Powered with 1.8-V, 3.3-V, or 5-V Variable I/O Voltage [6]



Note

6. 1.71 V ≤ V_{CCIO} ≤ 1.89 V - Short V_{CCD} pin with V_{CCIO} pin; V_{CCIO} > 2 V - connect a 1-uF decoupling capacitor to the V_{CCD} pin.

Application Examples

The following section provides CY7C65213 application examples.

USB to RS232 Converter

CY7C65213 can connect any embedded system, with a serial port, to a host PC through USB. CY7C65213 enumerates as a COM port on the host PC.

The RS232 protocol follows bipolar signaling, that is, the output signal toggles between negative and positive polarity. The valid RS232 signal is either in the –3-V to –15-V range or in the +3-V to +15-V range, and the range between –3 V to +3 V is invalid. In RS232, Logic 1 is called "Mark" and corresponds to a negative voltage range. Logic 0 is called "Space" and corresponds to a positive voltage range. The RS232 level converter facilitates this polarity inversion and the voltage-level translation between the CY7C65213's UART interface and RS232 signaling.

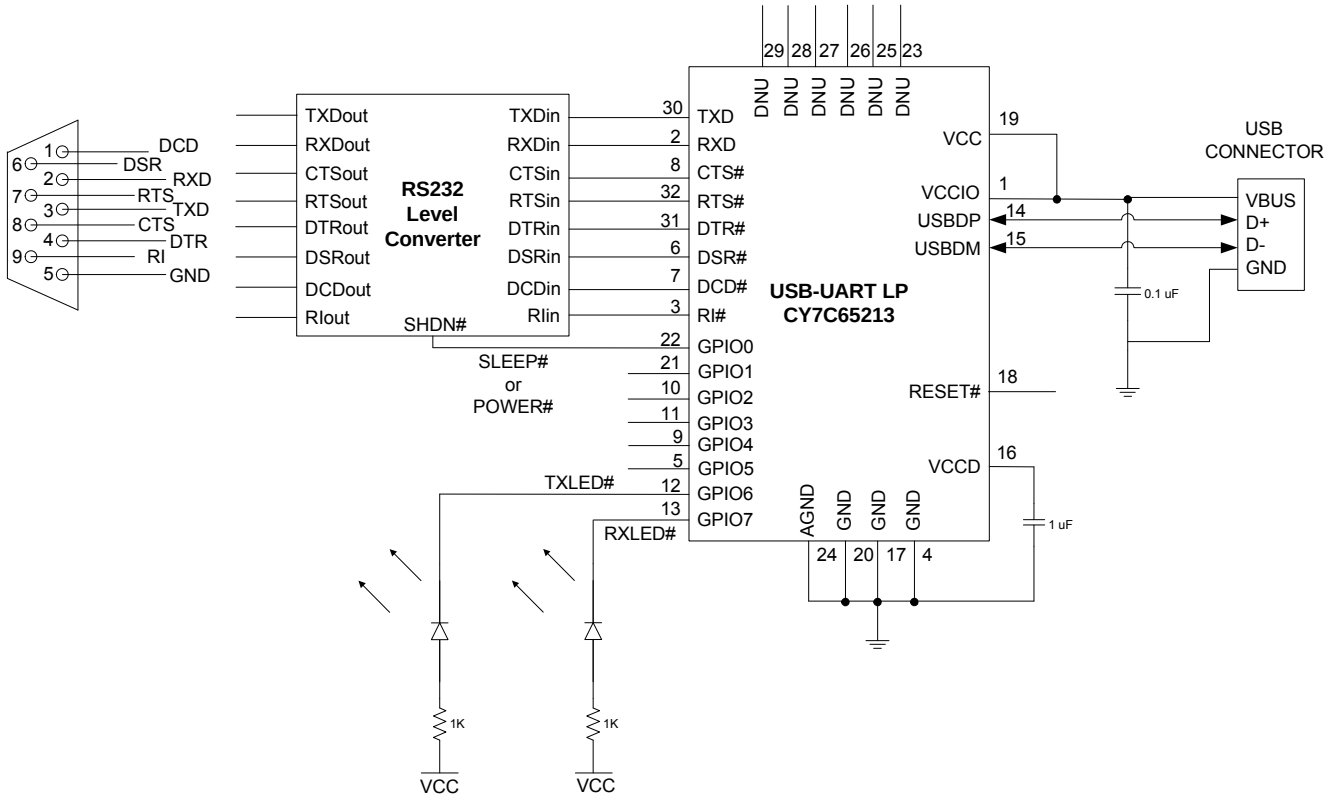
In this application, as shown in Figure 4, GPIO0 can be configured as SLEEP# or POWER# and connected to the SHDN# pin of the RS232-level converter. If GPIO0 is configured as SLEEP#, a low on this pin indicates USB suspend; if GPIO0 is configured as POWER#, a high on this pin indicates a state prior to USB configuration or USB suspend. GPIO6 and GPIO7 are configured as TXLED# and RXLED# to drive two LEDs, indicating data transmit and receive, respectively.

CY7C65213 has been tested with Maxim's MAX3245 transceiver.

A simple loop-back test can be performed on the USB-to-RS232 converter as follows: Connect the TX and RX lines of the RS232 interface with a jumper, transmit data to the converter through a COM Port communication terminal (such as Hyper Terminal or Tera Term), and verify if the same data is received.

For detailed steps to test a USB-to-RS232 solution, refer to the section 'Testing a USB to RS232 solution' in the application note AN85514.

Figure 4. USB to RS232 Converter



Battery Operated Bus-Powered USB to MCU with Battery Charge Detection

Figure 5 illustrates CY7C65213 as a USB-to-microcontroller interface. The TXD and RXD lines are used for data transfer, and the RTS# and CTS# lines are used for handshaking. GPIO0 is configured as SLEEP# to indicate to the MCU if the device is in the USB Suspend mode, and the RI# pin is configured to wake up the USB host controller from the Suspend mode.

This application illustrates a battery-operated system, which is bus-powered. CY7C65213 implements the battery charger detection functionality based on the USB Battery Charging Specification Rev. 1.2.

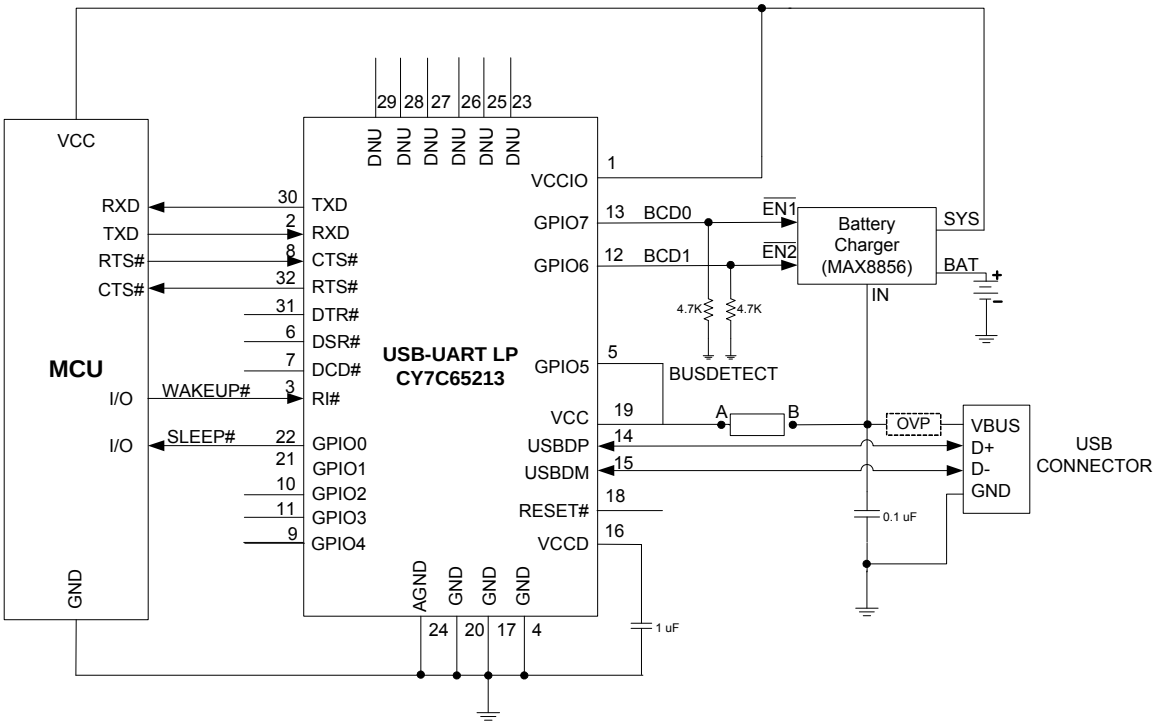
Battery-operated bus power systems must comply with the following conditions:

1. The system can be powered from the battery (if not discharged) and can be operational if the VBUS is not connected or powered down.
2. The system should not draw more than 100 mA from the VBUS prior to USB enumeration and USB Suspend.
3. The system should not draw more than 500 mA for SDP and 1.5 A for CDP/DCP.

To comply with the first requirement, the VBUS from the USB host is connected to the battery charger and to CY7C65213, as shown inFigure 5. When the VBUS is connected, CY7C65213 initiates battery charger detection and indicates the type of USB charger over BCD0 and BCD1. If the USB charger is SDP or CDP, CY7C65213 enables a 1.5-KΩ pull-up resistor on the USBDP for Full-Speed enumeration. When the VBUS is disconnected, CY7C65213 indicates an absence of the USB charger over BCD0 and BCD1, and removes the 1.5-KΩ pull-up resistor on the USBDP. Removing this resistor ensures that no current flows from the supply to the USB host through the USBDP pin, to comply with the USB 2.0 specification.

To comply with the second and third requirements, the BCD0 and BCD1 signals are configured over GPIO to communicate the type of USB charger and the amount of current the battery charger can draw from the VBUS. The BCD0 and BCD1 signals can be configured using the configuration utility.

Figure 5. Battery-Operated Bus-Powered USB to MCU with Battery Charge Detection[7]

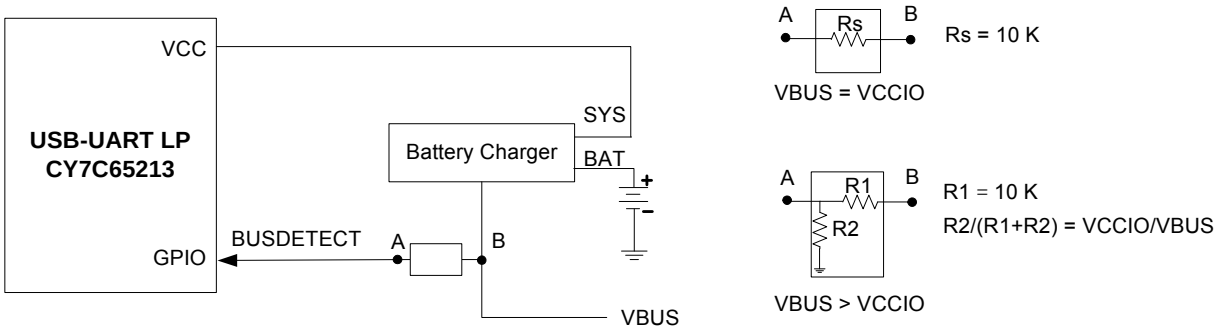


Notes

7. Add a 100KΩ pull-down resistor on the VBUS pin for quick discharge.

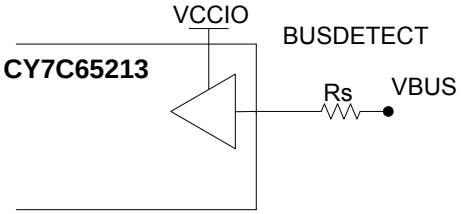
In a battery charger system, a 9-V spike on the VBUS is possible. The CY7C65213 VCC pin is intolerant to voltage above 6 V. In the absence of over-voltage protection (OVP) on the VBUS line, the VBUS should be connected to BUSDETECT (GPIO configured) using the resistive network and the output of the battery charger to the VCC pin of CY7C65213, as shown in the following figure.

Figure 6. GPIO VBUS Detect (BUSDETECT)



When VBUS and VCCIO are at the same voltage potential, the VBUS can be connected to GPIO using a series resistor (Rs). This is shown in the following figure. If there is a charger failure and the VBUS becomes 9 V, then the 10-kΩ resistor plays two roles. It reduces the amount of current flowing into the now forward-biased diodes in the GPIO, and it reduces the voltage seen on the pad.

Figure 7. GPIO VBUS Detection, VBUS = VCCIO



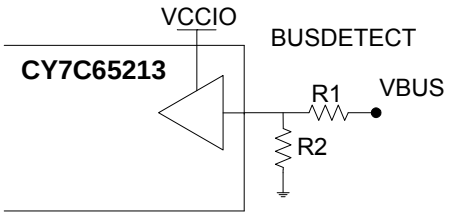
When VBUS > VCCIO, a resistor voltage divider is required to reduce the voltage from the VBUS down to VCCIO for the GPIO sensing the VBUS voltage. This is shown in Figure 8.

The resistors should be sized as follows:

- R1 ≥ 10 k
- R2 / (R1 + R2) = VCCIO / VBUS

The first condition limits the voltage and current for the charger failure situation, as described in the previous paragraph, while the second condition allows for normal-operation VBUS detection.

Figure 8. GPIO VBUS Detection, VBUS > VCCIO



LED Interface

Any GPIO can be configured to drive an LED. Three configuration options (TXLED#, RXLED#, and TX or RX LED#) are available for driving LEDs. Refer to Table 11 on page 11.

The following figure shows an example of the CY7C65213 drive single-LED configuration and dual-LED configurations, respectively. In the single-LED configuration, the GPIO pin is used to indicate when data is transmitted or received over USB by the device (TX or RX LED#). In the dual-LED configuration, when data is transmitted or received over USB, the respective GPIO pins will drive the LED to indicate the transfer.

Figure 9. Single-LED Configuration

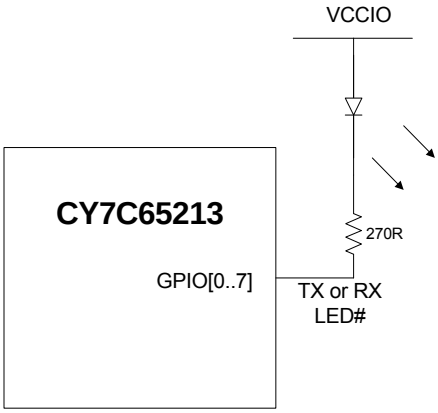
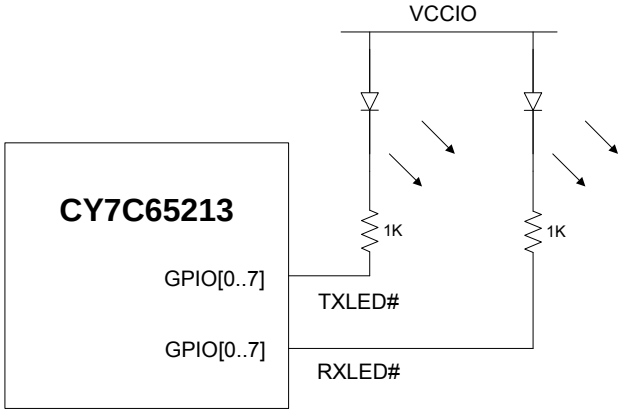


Figure 10. Double-LED Configuration



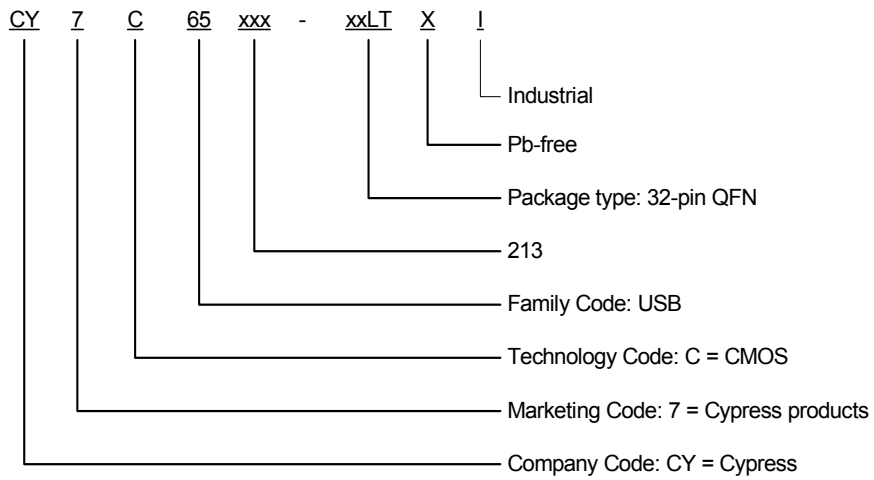
Ordering Information

Table 12 lists the CY7C65213 key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are seeking, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

Table 12. Key Features and Ordering Information

Package	Ordering Code	Operating Range
32-pin QFN (5 × 5 × 1 mm, 0.5 mm pitch) (Pb-free)	CY7C65213-32LTXI	Industrial

Ordering Code Definitions



Package Information

The package planned to be supported is the 32-pin QFN, which is a current Cypress package.

Figure 11. 32-pin QFN 5 × 5 × 1.0 mm LT32B 3.5 × 3.5 EPAD (Sawn)

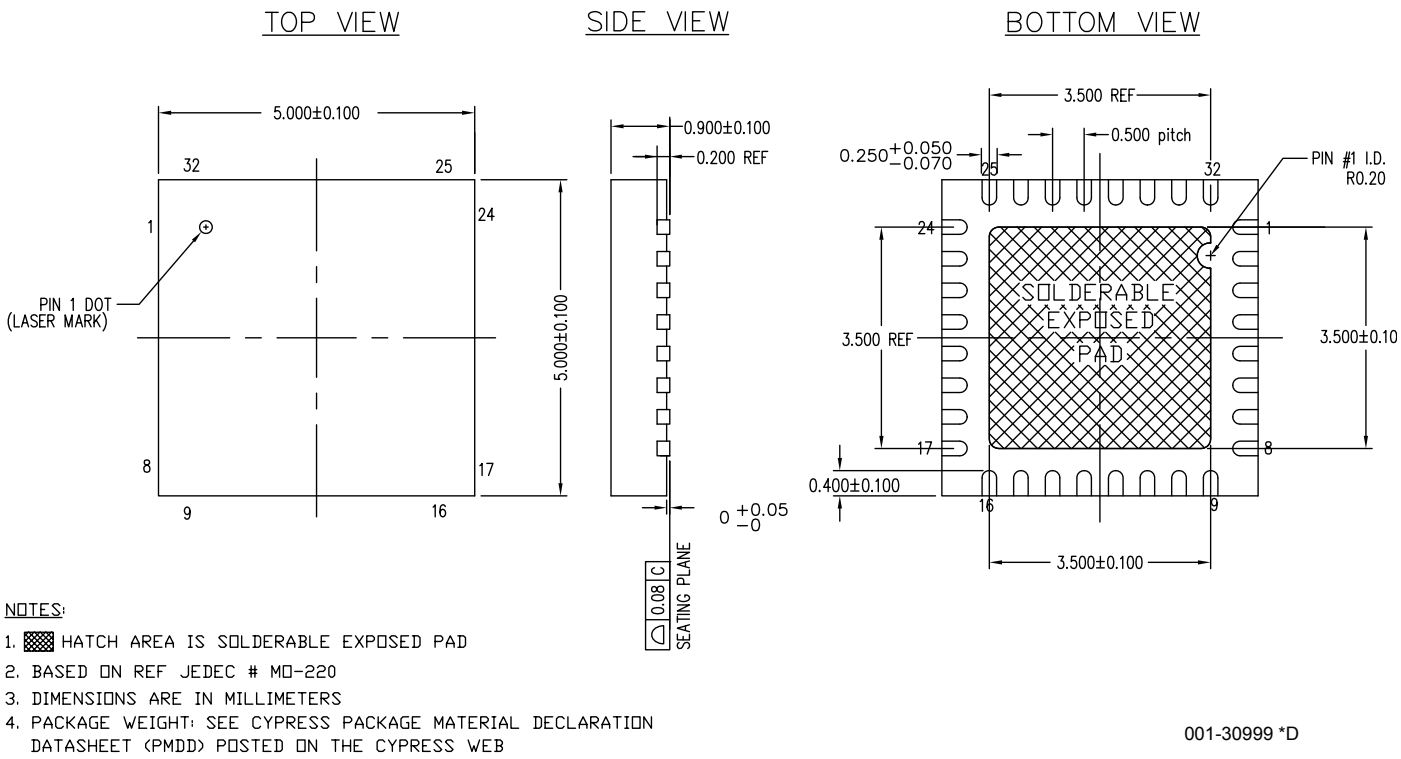


Table 13. Package Characteristics

Parameter	Description	Min	Typ	Max	Units
T_A	Operating ambient temperature	–40	25	85	°C
THJ	Package θ_{JA}	–	19	–	°C/W

Table 14. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
32-pin QFN	260 °C	30 seconds

Table 15. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
32-pin QFN	MSL 3

Acronyms

Table 16. Acronyms Used in this Document

Acronym	Description
BCD	battery charger detection
CDC	communication driver class
CDP	charging downstream port
DCP	dedicated charging port
DLL	dynamic link library
ESD	electrostatic discharge
GPIO	general-purpose input/output
HBM	human-body model
MCU	microcontroller unit
OSC	oscillator
PHDC	personal health care device class
PID	product identification
SDP	standard downstream port
SIE	serial interface engine
VCOM	virtual communication port
USB	Universal Serial Bus
UART	universal asynchronous receiver transmitter
VID	vendor identification

Document Conventions

Units of Measure

Table 17. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
DMIPS	Dhrystone million instructions per second
kΩ	kilo-ohm
KB	kilobyte
kHz	kilohertz
kV	kilovolt
Mbps	megabits per second
MHz	megahertz
mm	millimeter
V	volt

Document History Page

Document Title: CY7C65213 USB-UART LP Bridge Controller Document Number: 001-81011				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3657798	ZKR	06/28/2012	New data sheet.
*A	3714911	ZKR	08/24/2012	Moved datasheet status to Preliminary. Added electrical specs and pin information.
*B	3814090	ZKR	12/19/2012	Removed reference to HID. Updated description for Vhysttl parameter. Updated Pin Description. Added USB Power Configuration and Application Examples sections.
*C	3947144	ZKR	03/28/2013	Removed “4-KB SRAM” from Features and Contents. Updated Functional Overview and System Resources. Removed CPU, Flash, and SRAM sections. Updated USB PID in Internal Flash ConfigurationTable 1. Removed VCC2 and VCCIO2 parameter descriptions in DC Specifications. Changed CPU Frequency parameter to Frequency parameter in AC Specifications. Updated GPIO AC Specification Updated Pin Description and Battery Operated Bus-Powered USB to MCU with Battery Charge Detection sections. Added Figure 6. Removed Flash/SRAM feature from Ordering Information.
*D	4002280	ZKR	05/16/2013	Updated flash size to 512 bytes. Added a note about compliance with the USB 2.0 specification. Added a note for Absolute Maximum Ratings. Updated maximum current per GPIO from 100 mA to 25 mA. Added note for V_{IH} parameter in GPIO DC specifications. Updated content in USB to RS232 Convertor section. Updated USB to MCU with BCD schematic.
*E	4019327	ZKR	06/13/2013	Changed status from Preliminary to Final. Updated Features. Updated Block Diagram. Updated Functional Overview. Updated Electrical Specifications. Updated Pin Description. Updated USB Power Configuration. Updated Application Examples.

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