

8-Bit I/O Expander with Open-Drain Outputs

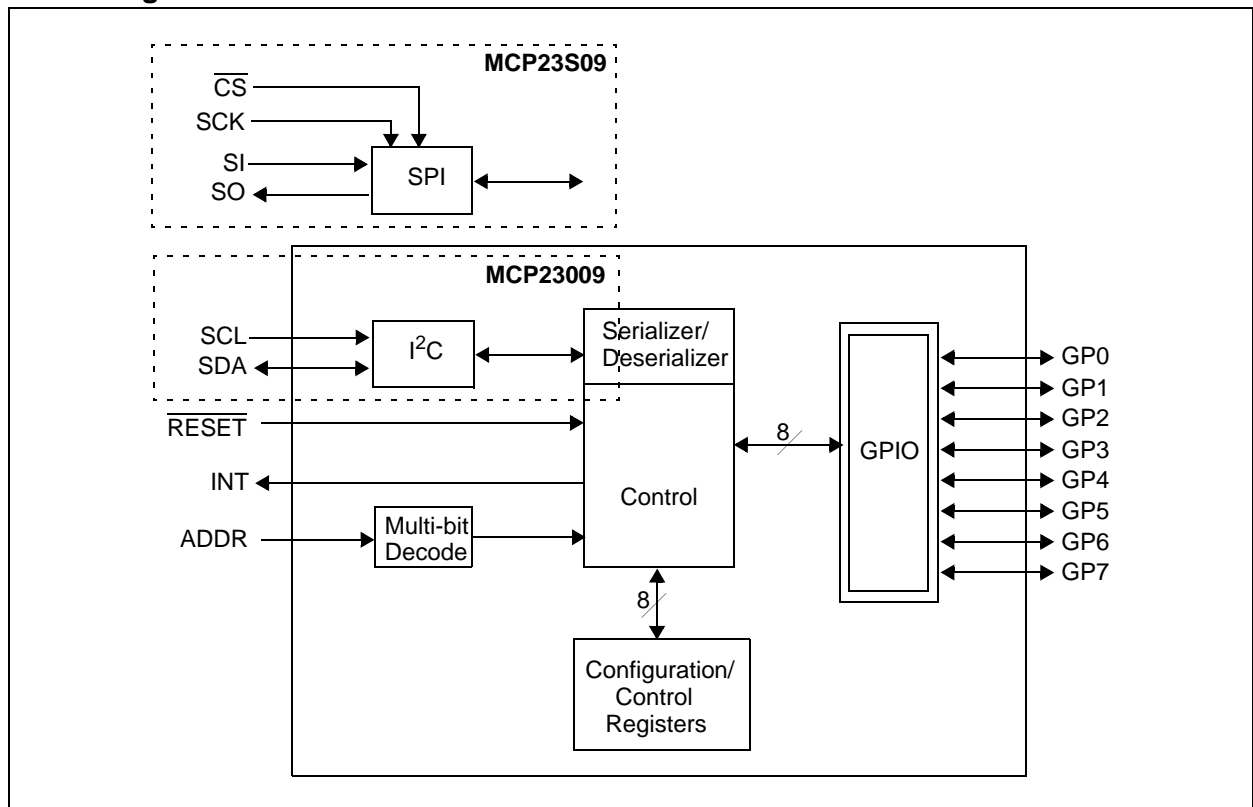
Features

- 8-bit remote bidirectional I/O port:
 - I/O pins default to input
- Open-drain outputs:
 - 5.5V tolerant
 - 25 mA sink capable (per pin)
 - 200 mA total
- High-speed I²C™ interface: **(MCP23009)**
 - 100 kHz
 - 400 kHz
 - 3.4 MHz
- High-speed SPI interface: **(MCP23S09)**
 - 10 MHz
- Single hardware address pin: **(MCP23009)**
 - Voltage input to allow up to eight devices on the bus
- Configurable interrupt output pins:
 - Configurable as active-high, active-low or open-drain
- Configurable interrupt source:
 - Interrupt-on-change from configured defaults or pin change
- Polarity inversion register to configure the polarity of the input port data
- External reset input
- Low standby current:
 - 1 μ A (-40°C \leq TA \leq +85°C)
 - 6 μ A (+85°C \leq TA \leq +125°C)
- Operating voltage:
 - 1.8V to 5.5V

Packages

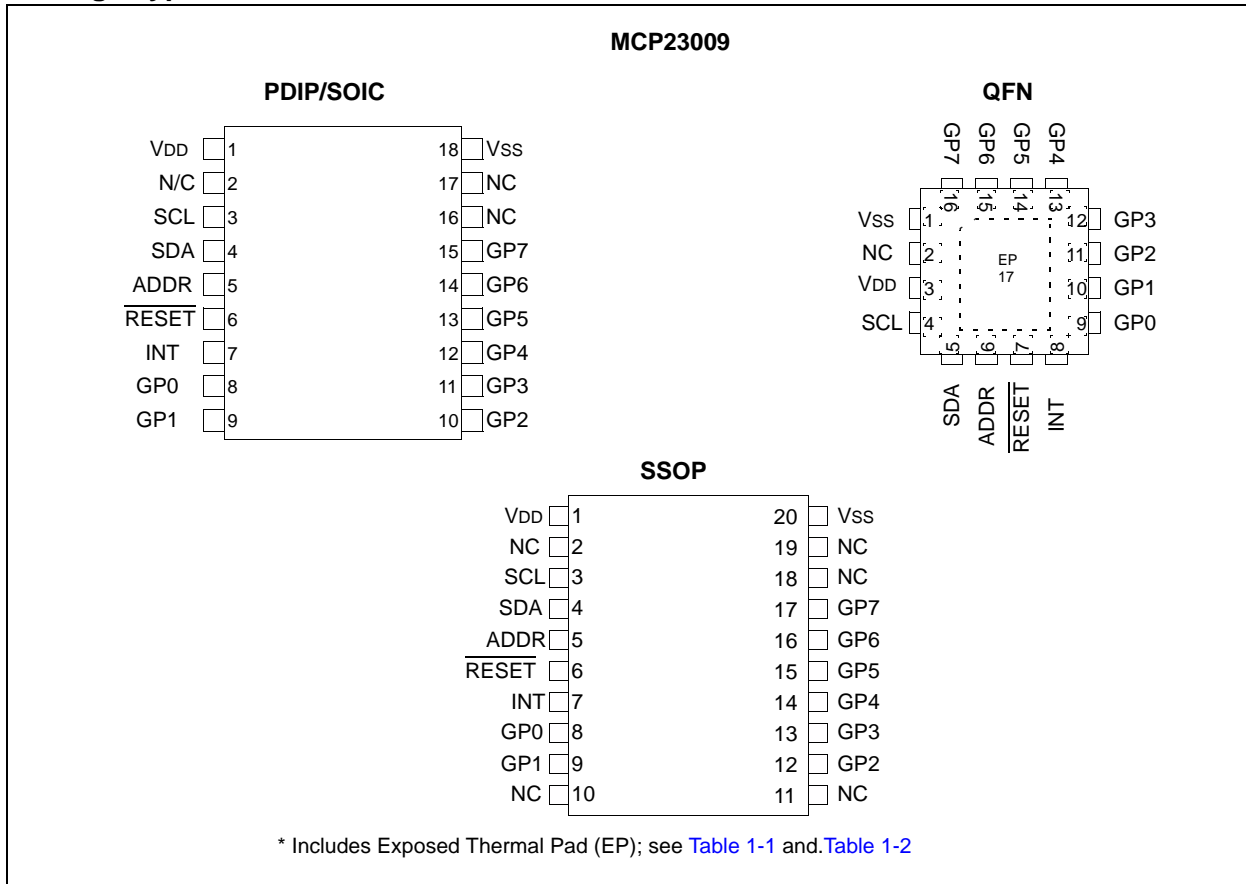
- 16-pin QFN (3x3 [mm])
- 18-pin PDIP (300 mil)
- 18-pin SOIC (300 mil)
- 20-pin SSOP

Block Diagram

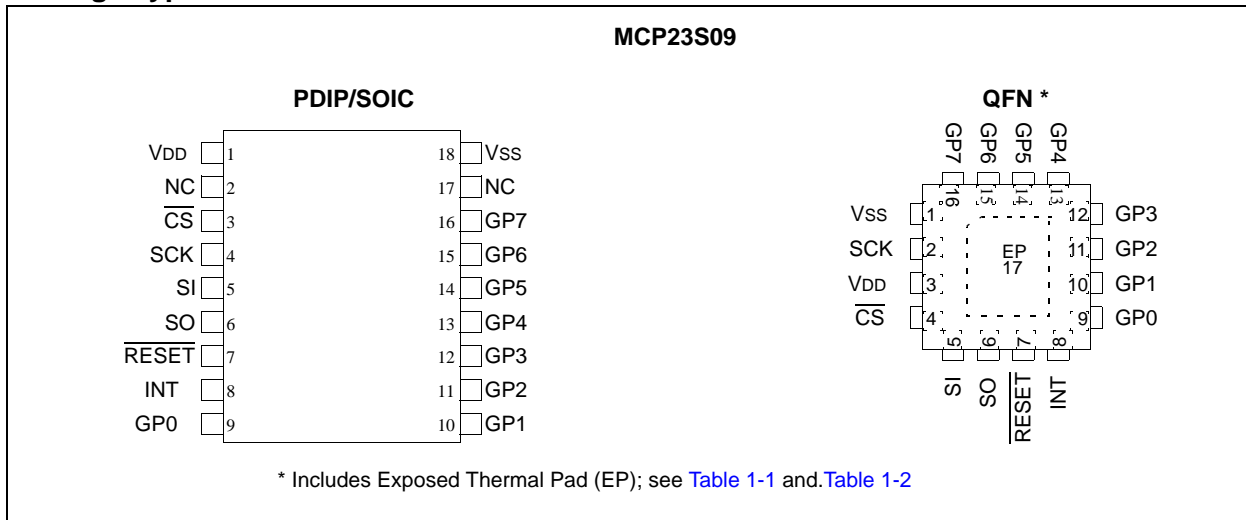


MCP23009/MCP23S09

Package Types:



Package Types:



1.0 DEVICE OVERVIEW

The MCP23X09 device provides 8-bit, general purpose parallel I/O expansion for I²C bus or SPI applications. The two devices differ only in the serial interface.

- MCP23009 - I²C interface
- MCP23S09 - SPI interface

The MCP23X09 consists of multiple 8-bit configuration registers for input, output and polarity selection. The system master can enable the I/Os as either inputs or outputs by writing the I/O configuration bits. The data for each input or output is kept in the corresponding input or output register. The polarity of the input port register can be inverted with the polarity inversion register. All registers can be read by the system master.

The interrupt output can be configured to activate under two conditions (mutually exclusive):

1. When any input state differs from its corresponding input port register state. This is used to indicate to the system master that an input state has changed.
2. When an input state differs from a pre-configured register value (DEFVAL register).

The Interrupt Capture register captures port values at the time of the interrupt, thereby saving the condition that caused the interrupt.

The Power-on Reset (POR) sets the registers to their default values and initializes the device state machine.

The hardware address pin is used to determine the device address.

MCP23009/MCP23S09

1.1 Pin Descriptions

TABLE 1-1: I²C PINOUT DESCRIPTION (MCP23009)

| Pin Name | 18LD PDIP/ SOIC | 16LD QFN | 20LD SSOP | Pin Type | Standard Function |
|----------|-----------------|----------|----------------|----------|---|
| VDD | 1 | 3 | 1 | P | Power |
| VSS | 18 | 1 | 20 | P | Ground |
| SCL | 3 | 4 | 3 | I | Serial clock input |
| SDA | 4 | 5 | 4 | I/O | Serial data I/O |
| ADDR | 5 | 6 | 5 | I | Hardware address pin allows up to 8 slave devices on the bus |
| RESET | 6 | 7 | 6 | I | Hardware reset |
| INT | 7 | 8 | 7 | O | Interrupt output for port. Can be configured as active high, active low, or open-drain. |
| GP0 | 8 | 9 | 8 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP1 | 9 | 10 | 9 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP2 | 10 | 11 | 12 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP3 | 11 | 12 | 13 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP4 | 12 | 13 | 14 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP5 | 13 | 14 | 15 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP6 | 14 | 15 | 16 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP7 | 15 | 16 | 17 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| NC | 2, 16, 17 | 2 | 2,10, 11,19,18 | | Not connected |
| EP | — | 17 | | | Exposed Thermal Pad (EP). Do not electrically connect. Can connect to VSS. |

MCP23009/MCP23S09

TABLE 1-2: SPI PINOUT DESCRIPTION (MCP23S09)

| Pin Name | 18LD PDIP/ SOIC | 16LD QFN | Pin Type | Standard Function |
|----------|-----------------|----------|----------|---|
| VDD | 1 | 3 | P | Power (high current capable) |
| VSS | 18 | 1 | P | Ground (high current capable) |
| CS | 3 | 4 | I | Chip select |
| SCK | 4 | 2 | I | Serial clock input |
| SI | 5 | 5 | I | Serial data input |
| SO | 6 | 6 | O | Serial data out |
| RESET | 7 | 7 | I | Hardware reset (must be externally biased) |
| INT | 8 | 8 | O | Interrupt output for port. Can be configured as active high, active low, or open-drain. |
| GP0 | 9 | 9 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP1 | 10 | 10 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP2 | 11 | 11 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP3 | 12 | 12 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP4 | 13 | 13 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP5 | 14 | 14 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP6 | 15 | 15 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| GP7 | 16 | 16 | I/O | Bidirectional I/O Pin (5.5 volt tolerant inputs; open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor. |
| NC | 2, 17 | — | — | Not connected |
| EP | — | 17 | — | Exposed Thermal Pad (EP). Do not electrically connect, Can connect to VSS. |

MCP23009/MCP23S09

1.2 Power-on Reset (POR)

The on-chip POR circuit holds the device in reset until VDD has reached a high enough voltage to deactivate the POR circuit (i.e., release the device from reset). The maximum VDD rise time is specified in the electrical specification section.

When the device exits the POR condition (releases reset), device operating parameters (i.e., voltage, temperature, serial bus frequency, etc.) must be met to ensure proper operation.

1.3 Serial Interface

This block handles the functionality of the I²C (MCP23009) or SPI (MCP23S09) interface protocol. The MCP23X09 contains eleven (11) individual registers which can be addressed through the Serial Interface block (Table 1-3).

TABLE 1-3: REGISTER ADDRESSES

| Address | Access to: |
|---------|--------------------|
| 00h | IODIR |
| 01h | IPOL |
| 02h | GPINTEN |
| 03h | DEFVAL |
| 04h | INTCON |
| 05h | IOCON |
| 06h | GPPU |
| 07h | INTF |
| 08h | INTCAP (Read-only) |
| 09h | GPIO |
| 0Ah | OLAT |

1.3.1 BYTE MODE AND SEQUENTIAL MODE

The MCP23X09 has the ability to operate in “Byte Mode” or “Sequential Mode” (IOCON.SEQOP). Byte mode and sequential mode are not to be confused with I²C byte operations and sequential operations. The modes explained here relate to the device’s internal address pointer and whether or not it is incremented after each byte is clocked on the serial interface.

Byte Mode disables automatic address pointer incrementing. When operating in Byte Mode, the MCP23X09 does not increment its internal address counter after each byte during the data transfer. This gives the ability to continually access the same address by providing extra clocks (without additional control bytes). This is useful for polling the GPIO register for data changes or for continually writing to the output latches.

Sequential Mode enables automatic address pointer incrementing. When operating in Sequential Mode, the MCP23X09 increments its address counter after each

byte during the data transfer. The address pointer automatically rolls over to address 00h after accessing the last register.

These two modes are not to be confused with single writes/reads and continuous writes/reads which are serial protocol sequences. For example, the device may be configured for Byte Mode and the master may perform a continuous read. In this case, the MCP23X09 would not increment the address pointer and would repeatedly drive data from the same location.

1.3.2 I²C INTERFACE

1.3.2.1 I²C Write Operation

The I²C write operation includes the control byte and register address sequence, as shown in the bottom of Figure 1-1. This sequence is followed by eight bits of data from the master and an Acknowledge (ACK) from the MCP23009. The operation is ended with a stop (P) or restart (SR) condition being generated by the master.

Data is written to the MCP23009 after every byte transfer. If a stop or restart condition is generated during a data transfer, the data will not be written to the MCP23009.

Both “byte mode” and “sequential mode” are supported by the MCP23009. If sequential mode is enabled (default), the MCP23009 increments its address counter after each ACK during the data transfer.

1.3.2.2 I²C Read Operation

I²C read operations include the control byte sequence, as shown in the bottom of Figure 1-1. This sequence is followed by another control byte (including the Start condition and ACK) with the R/W bit equal to a logic one (R/W = 1). The MCP23009 then transmits the data contained in the addressed register. The sequence is ended with the master generating a Stop or Restart condition.

1.3.2.3 I²C Sequential Write/Read

For sequential operations (Write or Read), instead of transmitting a Stop or Restart condition after the data transfer, the master clocks the next byte pointed to by the address pointer (see Section 1.3.1 “Byte Mode and Sequential Mode” for details regarding sequential operation control).

The sequence ends with the master sending a Stop or Restart condition.

The MCP23009 address pointer will roll over to address zero after reaching the last register address.

Refer to Figure 1-1.

1.3.3 SPI INTERFACE

The MCP23S09 operates in Mode 0,0 and Mode 1,1. The difference between the two modes is the idle state of the clock.

Mode 0,0: The idle state of the clock is LOW. Input data is latched on the rising edge of the clock; output data is driven on the falling edge of the clock.

Mode 1,1: The idle state of the clock is HIGH. Input data is latched on the rising edge of the clock; output data is driven on the falling edge of the clock.

1.3.3.1 SPI Write Operation

The SPI write operation is started by lowering \overline{CS} . The write command (slave address with R/W bit cleared) is then clocked into the device. The opcode is followed by an address and at least one data byte.

1.3.3.2 SPI Read Operation

The SPI read operation is started by lowering \overline{CS} . The SPI read command (slave address with R/W bit set) is then clocked into the device. The opcode is followed by an address, with at least one data byte being clocked out of the device.

1.3.3.3 SPI Sequential Write/Read

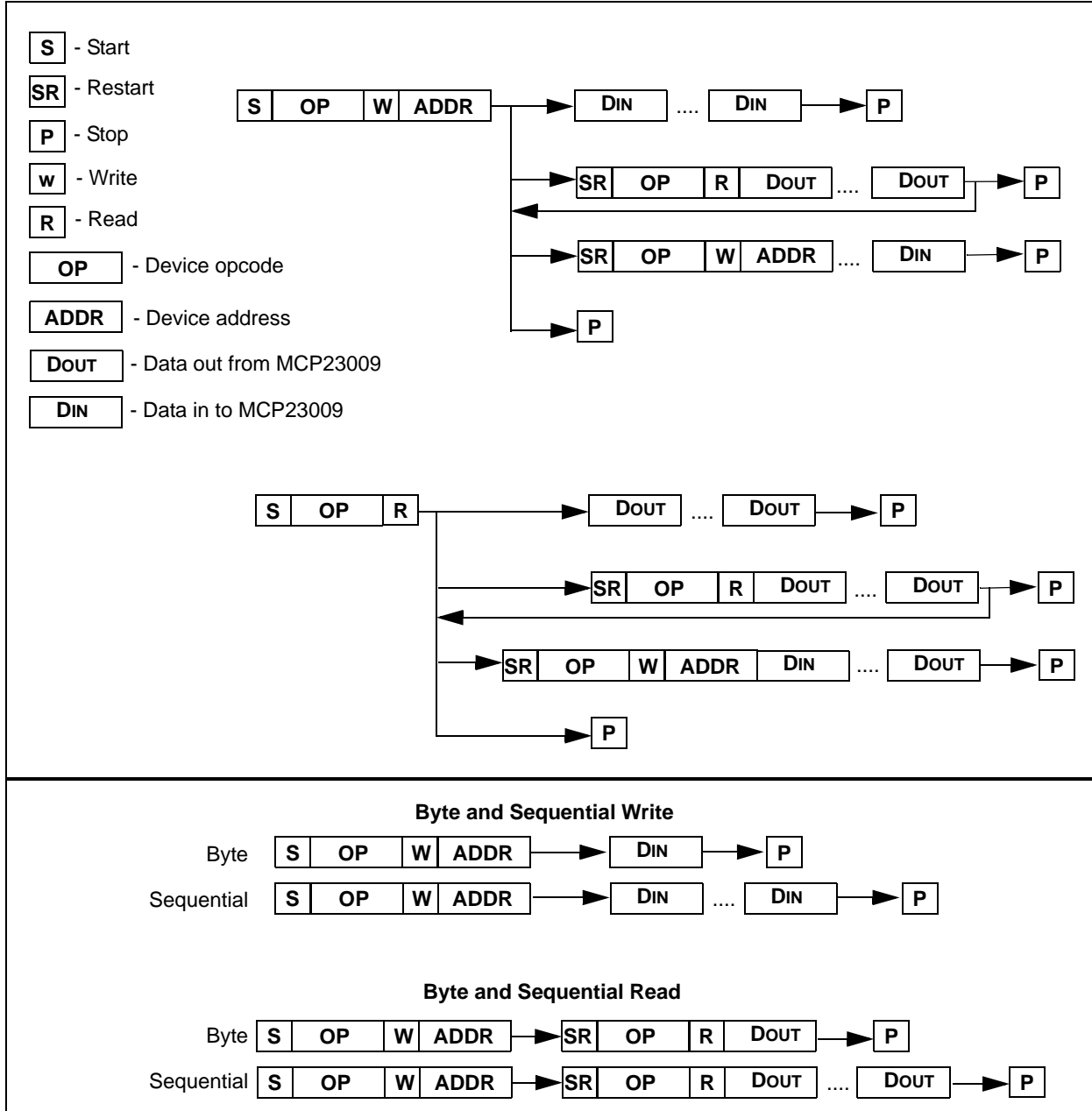
For sequential operations, instead of deselecting the device by raising \overline{CS} , the master clocks the next byte pointed to by the address pointer. (see **Section 1.3.1 “Byte Mode and Sequential Mode”** for details regarding sequential operation control).

The sequence ends by the raising of \overline{CS} .

The MCP23S09 address pointer will roll over to address zero after reaching the last register address.

MCP23009/MCP23S09

FIGURE 1-1: MCP23009 I²C™ DEVICE PROTOCOL



1.4 Multi-bit Address Decoder

The ADDR pin is used to set the slave address of the MCP23009 (I²C only) to allow up to eight devices on the bus using only a single pin. Typically, this would require three pins.

The multi-bit Address Decoder employs a basic FLASH ADC architecture (Figure 1-4). The seven comparators generate 8 unique values based on the analog input. This value is converted to a 3-bit code which corresponds to the address bits (A2, A1, A0) in the serial OPCODE.

Sequence of Operation (see Figure 1-5 for timings):

1. Upon power up (after VDD stabilizes) the module becomes active after time tADEN. Note, the analog value on the ADDR pin must be stable before this point to ensure accurate address assignment.

2. The 3-bit address is latched after tADDRLAT.
3. The module powers down after the first rising edge of the serial clock is detected (tADDIS).

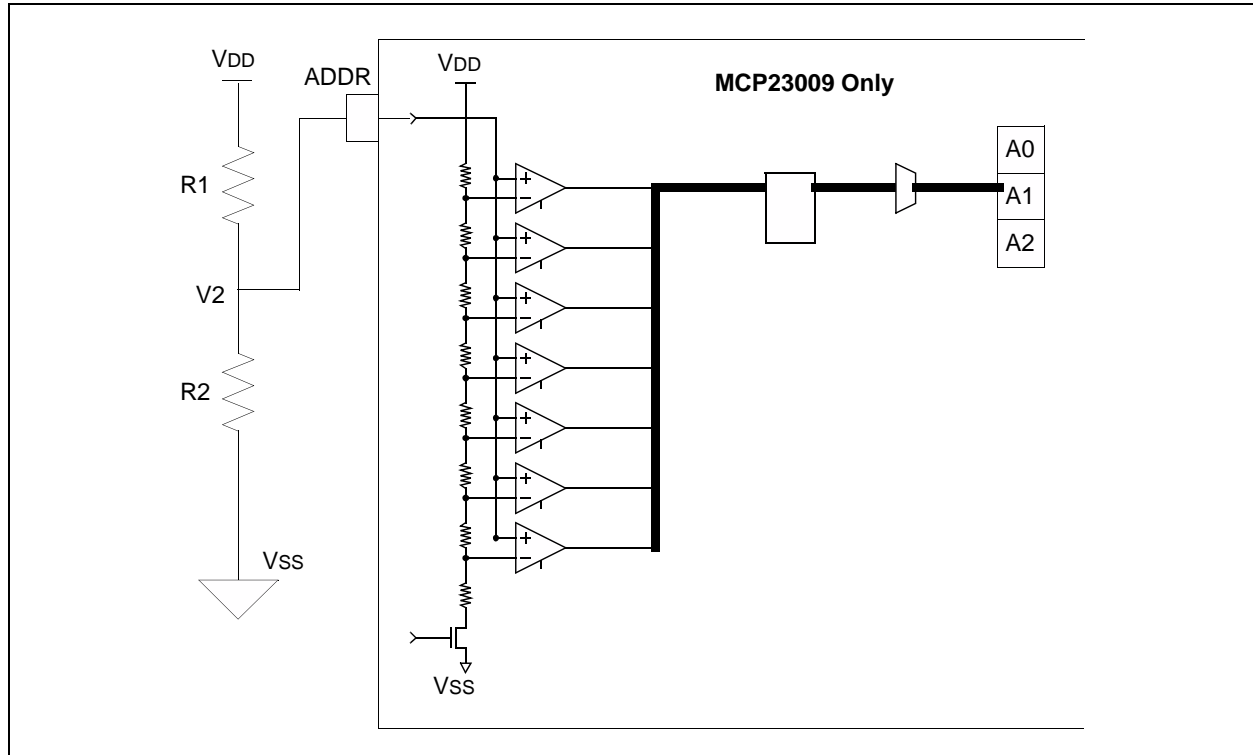
Once the address bits are latched, the device will keep the slave address until a POR or reset condition occurs.

1.4.1 CALCULATING VOLTAGE ON ADDR

When calculating the required voltage on the ADDR pin (V2), the set point should be the mid-point of the LSb of the ADC.

The examples in Figure 1-2 and Figure 1-3 show how to determine the mid point voltage (V2) and the range of voltages based on a voltage divider circuit. The maximum tolerance is 20%, however, it is recommended to use 5% tolerance worst case (10% total tolerance).

FIGURE 1-2: VOLTAGE DIVIDER EXAMPLE



MCP23009/MCP23S09

FIGURE 1-3: VOLTAGE AND CODE EXAMPLE

Assume:

$n = A2, A1, A0$ in opcode

ratio = $R2/(R1+R2)$

$V2$ = voltage on ADDR pin

$V2(\text{min}) = V2 - (VDD/8) \times \% \text{tolerance}$

$V2(\text{max}) = V2 + (VDD/8) \times \% \text{tolerance}$

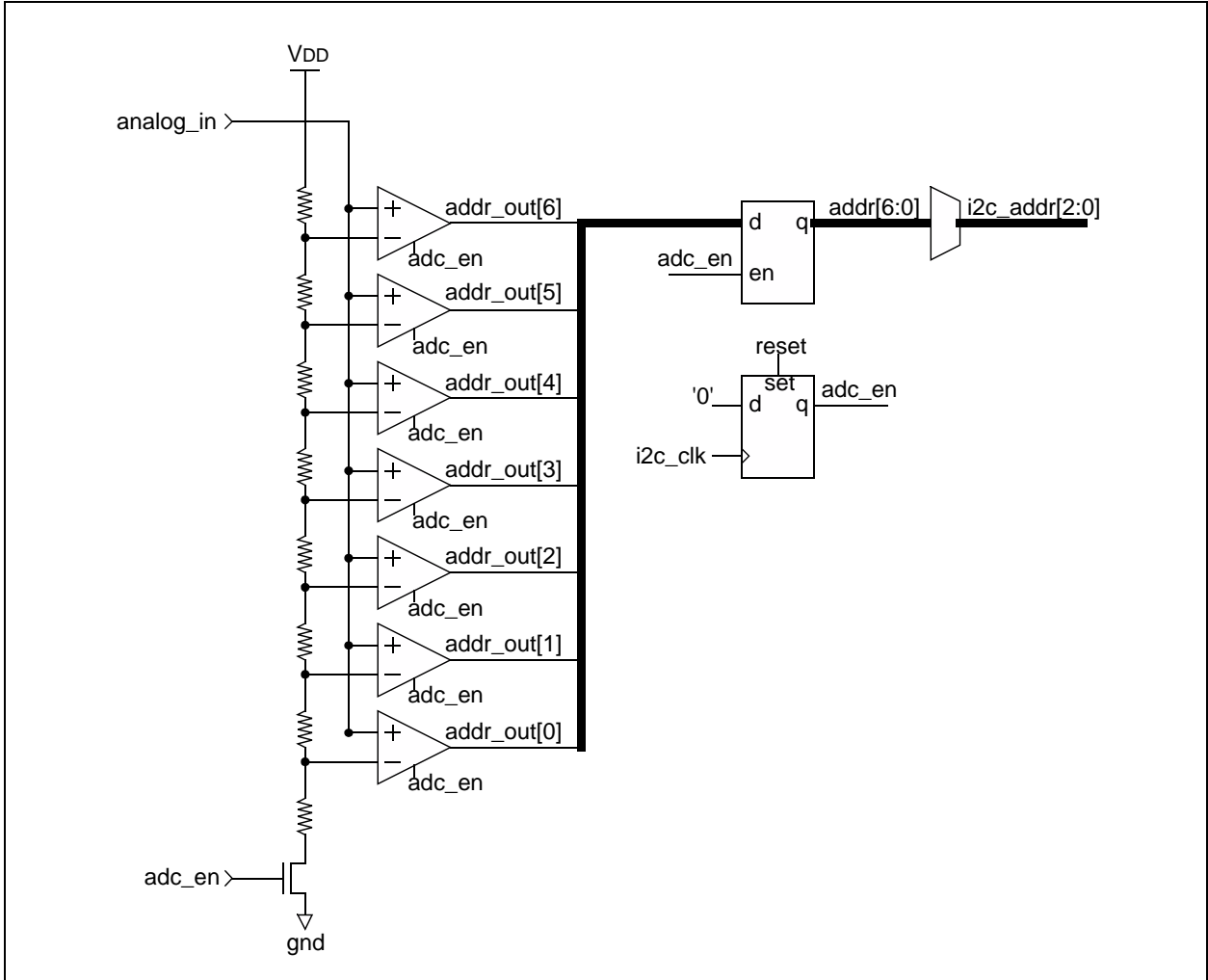
| VDD= 1.8 | | | | | 10% Tolerance (total) | |
|----------|---------|----------|------------|--------------|-----------------------|---------|
| n | R2=2n+1 | R1=16-R2 | R2/(R1+R2) | V2 | V2(min) | V2(max) |
| 0 | 1 | 15 | 0.0625 | 0.113 | 0.00 | 0.14 |
| 1 | 3 | 13 | 0.1875 | 0.338 | 0.32 | 0.36 |
| 2 | 5 | 11 | 0.3125 | 0.563 | 0.54 | 0.59 |
| 3 | 7 | 9 | 0.4375 | 0.788 | 0.77 | 0.81 |
| 4 | 9 | 7 | 0.5625 | 1.013 | 0.99 | 1.04 |
| 5 | 11 | 5 | 0.6875 | 1.238 | 1.22 | 1.26 |
| 6 | 13 | 3 | 0.8125 | 1.463 | 1.44 | 1.49 |
| 7 | 15 | 1 | 0.9375 | 1.688 | 1.67 | 1.80 |

| VDD= 2.7 | | | | | 10% Tolerance (total) | |
|----------|---------|----------|------------|--------------|-----------------------|---------|
| n | R2=2n+1 | R1=16-R2 | R2/(R1+R2) | V2 | V2(min) | V2(max) |
| 0 | 1 | 15 | 0.0625 | 0.169 | 0.00 | 0.19 |
| 1 | 3 | 13 | 0.1875 | 0.506 | 0.48 | 0.53 |
| 2 | 5 | 11 | 0.3125 | 0.844 | 0.82 | 0.87 |
| 3 | 7 | 9 | 0.4375 | 1.181 | 1.16 | 1.20 |
| 4 | 9 | 7 | 0.5625 | 1.519 | 1.50 | 1.54 |
| 5 | 11 | 5 | 0.6875 | 1.856 | 1.83 | 1.88 |
| 6 | 13 | 3 | 0.8125 | 2.194 | 2.17 | 2.22 |
| 7 | 15 | 1 | 0.9375 | 2.531 | 2.51 | 2.70 |

| VDD= 3.3 | | | | | 10% Tolerance (total) | |
|----------|---------|----------|------------|--------------|-----------------------|---------|
| n | R2=2n+1 | R1=16-R2 | R2/(R1+R2) | V2 | V2(min) | V2(max) |
| 0 | 1 | 15 | 0.0625 | 0.206 | 0.00 | 0.23 |
| 1 | 3 | 13 | 0.1875 | 0.619 | 0.60 | 0.64 |
| 2 | 5 | 11 | 0.3125 | 1.031 | 1.01 | 1.05 |
| 3 | 7 | 9 | 0.4375 | 1.444 | 1.42 | 1.47 |
| 4 | 9 | 7 | 0.5625 | 1.856 | 1.83 | 1.88 |
| 5 | 11 | 5 | 0.6875 | 2.269 | 2.25 | 2.29 |
| 6 | 13 | 3 | 0.8125 | 2.681 | 2.66 | 2.70 |
| 7 | 15 | 1 | 0.9375 | 3.094 | 3.07 | 3.30 |

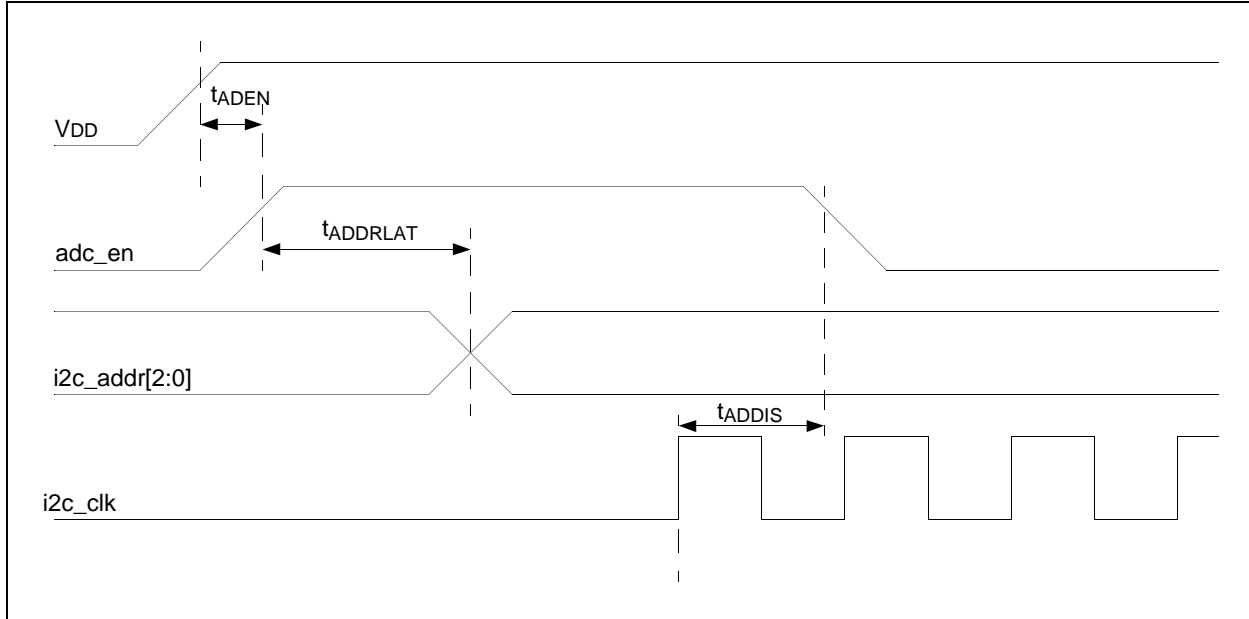
| VDD= 5.5 | | | | | 10% Tolerance (total) | |
|----------|---------|----------|------------|--------------|-----------------------|---------|
| n | R2=2n+1 | R1=16-R2 | R2/(R1+R2) | V2 | V2(min) | V2(max) |
| 0 | 1 | 15 | 0.0625 | 0.344 | 0.00 | 0.37 |
| 1 | 3 | 13 | 0.1875 | 1.031 | 1.01 | 1.05 |
| 2 | 5 | 11 | 0.3125 | 1.719 | 1.70 | 1.74 |
| 3 | 7 | 9 | 0.4375 | 2.406 | 2.38 | 2.43 |
| 4 | 9 | 7 | 0.5625 | 3.094 | 3.07 | 3.12 |
| 5 | 11 | 5 | 0.6875 | 3.781 | 3.76 | 3.80 |
| 6 | 13 | 3 | 0.8125 | 4.469 | 4.45 | 4.49 |
| 7 | 15 | 1 | 0.9375 | 5.156 | 5.13 | 5.50 |

FIGURE 1-4: FLASH ADC BLOCK DIAGRAM



MCP23009/MCP23S09

FIGURE 1-5: HARDWARE ADDRESS DECODE TIMING



1.4.2 ADDRESSING I²C DEVICES (MCP23009)

The MCP23009 is a slave I²C device that supports 7-bit slave addressing, with the read/write bit filling out the control byte. The slave address contains four fixed bits and three user-defined hardware address bits (configured via ADDR pin). [Figure 1-6](#) shows the control byte format.

1.4.3 ADDRESSING SPI DEVICES (MCP23S09)

The MCP23S09 is a slave SPI device. The slave address contains seven fixed bits (no address bits) with the read/write bit filling out the control byte. [Figure 1-7](#) shows the control byte format.

FIGURE 1-6: I²C™ CONTROL BYTE FORMAT

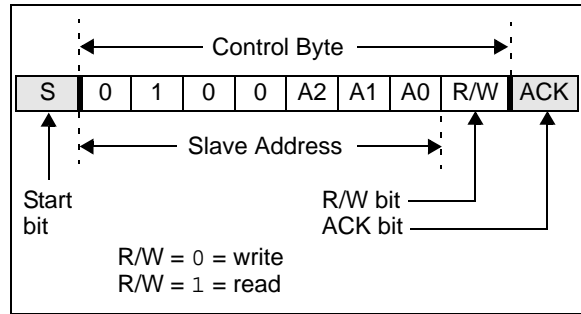


FIGURE 1-7: SPI CONTROL BYTE FORMAT

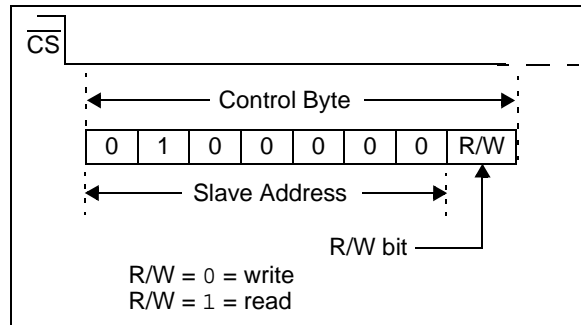


FIGURE 1-8: I²C™ ADDRESSING REGISTERS

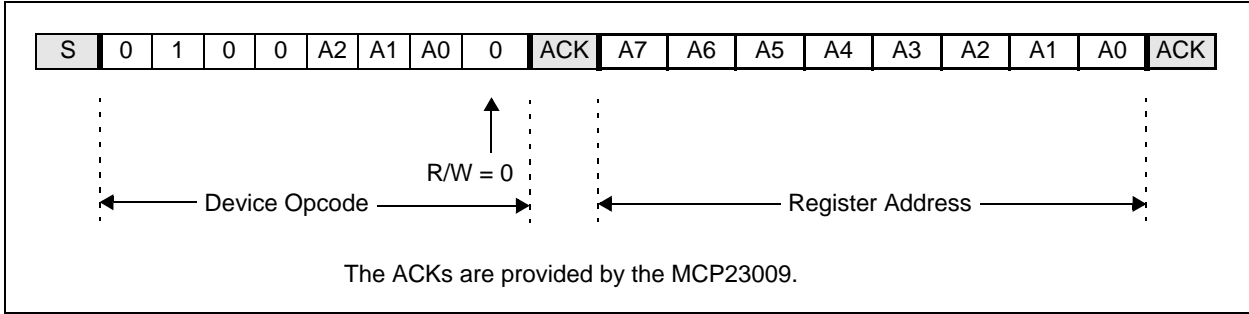
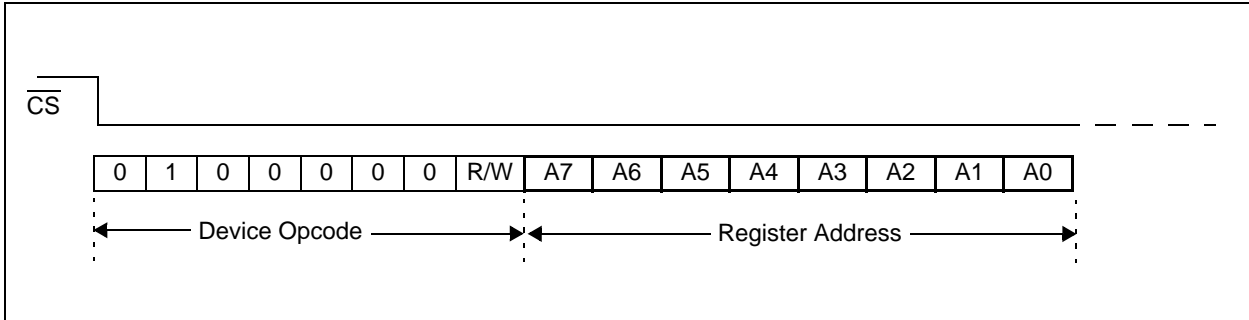


FIGURE 1-9: SPI ADDRESSING REGISTERS



MCP23009/MCP23S09

1.5 GPIO Port

The GPIO module is a general purpose 8-bit wide bidirectional port.

The outputs are open-drain.

The GPIO module contains the data ports (GPIO_n), internal pull up resistors and the Output Latches (OLAT_n).

The pull up resistors are individually configured and can be enabled when the pin is configured as an input or output.

Reading the GPIO_n register reads the value on the port. Reading the OLAT_n register only reads the latches, not the actual value on the port.

Writing to the GPIO_n register actually causes a write to the latches (OLAT_n). Writing to the OLAT_n register forces the associated output drivers to drive to the level in OLAT_n. Pins configured as inputs turn off the associated output driver and put it in high-impedance.

1.6 Configuration and Control Registers

There are eleven (11) registers associated with the MCP23X09 as shown in [Table 1-4](#).

TABLE 1-4: CONFIGURATION AND CONTROL REGISTER

| Register Name | Address (hex) | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | POR/RST value |
|---------------|---------------|--------|--------|--------|--------|--------|--------|--------|--------|---------------|
| IODIRA | 00 | IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 | 1111 1111 |
| IPOLA | 01 | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 | 0000 0000 |
| GPINTENA | 02 | GPINT7 | GPINT6 | GPINT5 | GPINT4 | GPINT3 | GPINT2 | GPINT1 | GPINT0 | 0000 0000 |
| DEFVALA | 03 | DEF7 | DEF6 | DEF5 | DEF4 | DEF3 | DEF2 | DEF1 | DEF0 | 0000 0000 |
| INTCONA | 04 | IOC7 | IOC6 | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 | 0000 0000 |
| IOCON | 05 | — | — | SEQOP | — | — | ODR | INTPOL | INTCC | 0000 0000 |
| GPPUA | 06 | PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PU0 | 0000 0000 |
| INTFA | 07 | INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 | INT0 | 0000 0000 |
| INTCAPA | 08 | ICP7 | ICP6 | ICP5 | ICP4 | ICP3 | ICP2 | ICP1 | ICP0 | 0000 0000 |
| GPIOA | 09 | GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 | 0000 0000 |
| OLATA | 0A | OL7 | OL6 | OL5 | OL4 | OL3 | OL2 | OL1 | OL0 | 0000 0000 |

MCP23009/MCP23S09

1.6.1 I/O DIRECTION REGISTER

Controls the direction of the data I/O.

When a bit is set, the corresponding pin becomes an input. When a bit is clear, the corresponding pin becomes an output.

REGISTER 1-1: IODIR – I/O DIRECTION REGISTER

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IO7 | IO6 | IO5 | IO4 | IO3 | IO2 | IO1 | IO0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **IO7:IO0:** Controls the direction of data I/O <7:0>

1 = Pin is configured as an input

0 = Pin is configured as an output

1.6.2 INPUT POLARITY REGISTER

This register allows the user to configure the polarity on the corresponding GPIO port bits.

If a bit is set, the corresponding GPIO register bit will reflect the inverted value on the pin.

REGISTER 1-2: IPOL – INPUT POLARITY PORT REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

IP7:IP0: Controls the polarity inversion of the input pins <7:0>

1 = GPIO register bit will reflect the opposite logic state of the input pin

0 = GPIO register bit will reflect the same logic state of the input pin

MCP23009/MCP23S09

1.6.3 INTERRUPT-ON-CHANGE CONTROL REGISTER

The GPINTEN register controls the interrupt-on-change feature for each pin.

If a bit is set, the corresponding pin is enabled for interrupt-on-change. The DEFVAL and INTCON registers must also be configured if any pins are enabled for interrupt-on-change.

REGISTER 1-3: GPINTEN – INTERRUPT-ON-CHANGE PINS

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| GPINT7 | GPINT6 | GPINT5 | GPINT4 | GPINT3 | GPINT2 | GPINT1 | GPINT0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0 **GPINT7:GPINT0:** General purpose I/O interrupt-on-change pins <7:0>

1 = Enable GPIO input pin for interrupt-on-change event

0 = Disable GPIO input pin for interrupt-on-change event

Refer to INTCON and DEFVAL.

1.6.4 DEFAULT COMPARE REGISTER FOR INTERRUPT-ON-CHANGE

The default comparison value is configured in the DEFVAL register. If enabled (via GPINTEN and INTCON) to compare against the DEFVAL register, an opposite value on the associated pin will cause an interrupt to occur.

REGISTER 1-4: DEFVAL – DEFAULT VALUE REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DEF7 | DEF6 | DEF5 | DEF4 | DEF3 | DEF2 | DEF1 | DEF0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

DEF7:DEF0: Sets the compare value for pins configured for interrupt-on-change from defaults <7:0>. Refer to INTCON.

If the associated pin level is the opposite from the register bit, an interrupt occurs.

Refer to INTCON and GPINTEN.

MCP23009/MCP23S09

1.6.5 INTERRUPT CONTROL REGISTER

The INTCON register controls how the associated pin value is compared for the interrupt-on-change feature. If a bit is set, the corresponding I/O pin is compared against the associated bit in the DEFVAL register. If a bit value is clear, the corresponding I/O pin is compared against the previous value.

REGISTER 1-5: INTCON – INTERRUPT-ON-CHANGE CONTROL REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOC7 | IOC6 | IOC5 | IOC4 | IOC3 | IOC2 | IOC1 | IOC0 |
| bit 7 | | | | | | | bit 0 |

| | | | |
|-------------------|------------------|------------------------------------|--------------------|
| Legend: | | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-0 **IOC7:IOC0:** Controls how the associated pin value is compared for interrupt-on-change <7:0>.
1 = Pin value is compared against the associated bit in DEFVAL register
0 = Pin value is compared against the previous pin value

Refer to DEFVAL and GPINTEN.

MCP23009/MCP23S09

1.6.6 CONFIGURATION REGISTER

The Sequential Operation (**SEQOP**) controls the incrementing function of the address pointer. If the address pointer is disabled, the address pointer does not automatically increment after each byte is clocked during a serial transfer. This feature is useful when it is desired to continuously poll (read) or modify (write) a register.

The Open-Drain (**ODR**) control bit enables/disables the INT pin for open-drain configuration.

The Interrupt Polarity (**INTPOL**) sets the polarity of the INT pin. This bit is functional only when the ODR bit is cleared, configuring the INT pin as active push-pull.

The Interrupt Clearing Control (**INTCC**) configures how interrupts are cleared. When set (INTCC = 1), the interrupt is cleared when the INTCAP register is read. When cleared (INTCC = 0), the interrupt is cleared when the GPIO register is read.

The interrupt can only be cleared when the interrupt condition is inactive. Refer to **Section 1.7.4 “Clearing Interrupts”** for details.

REGISTER 1-6: IOCON – I/O EXPANDER CONFIGURATION REGISTER

| | | | | | | | |
|-------|-----|-------|-----|-----|-------|--------|-------|
| U-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
| - | - | SEQOP | - | - | ODR | INTPOL | INTCC |
| bit 7 | | | | | | | bit 0 |

Legend:

| | | |
|-------------------|------------------|------------------------------------|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared |
| | | x = Bit is unknown |

- bit 7 **Unimplemented:** Reads as 0
- bit 6 **Unimplemented:** Reads as 0
- bit 5 **SEQOP:** Sequential Operation mode bit.
1 = Sequential operation disabled, address pointer does not increment
0 = Sequential operation enabled, address pointer increments
- bit 4 **Unimplemented:** Reads as 0
- bit 3 **Unimplemented:** Reads as 0
- bit 2 **ODR:** Configures the INT pin as an open-drain output.
1 = Open-drain output (overrides the INTPOL bit)
0 = Active driver output (INTPOL bit sets the polarity)
- bit 1 **INTPOL:** Sets the polarity of the INT output pin.
1 = Active-high
0 = Active-low
- bit 0 **INTCC:** Interrupt Clearing Control
1 = Reading INTCAP register clears the interrupt
0 = Reading GPIO register clears the interrupt

MCP23009/MCP23S09

1.6.7 PULL-UP RESISTOR CONFIGURATION REGISTER

The GPPU register controls the pull-up resistors for the port pins. If a bit is set the corresponding port pin is internally pulled up with an internal resistor.

REGISTER 1-7: GPPU – GPIO PULL-UP RESISTOR REGISTER

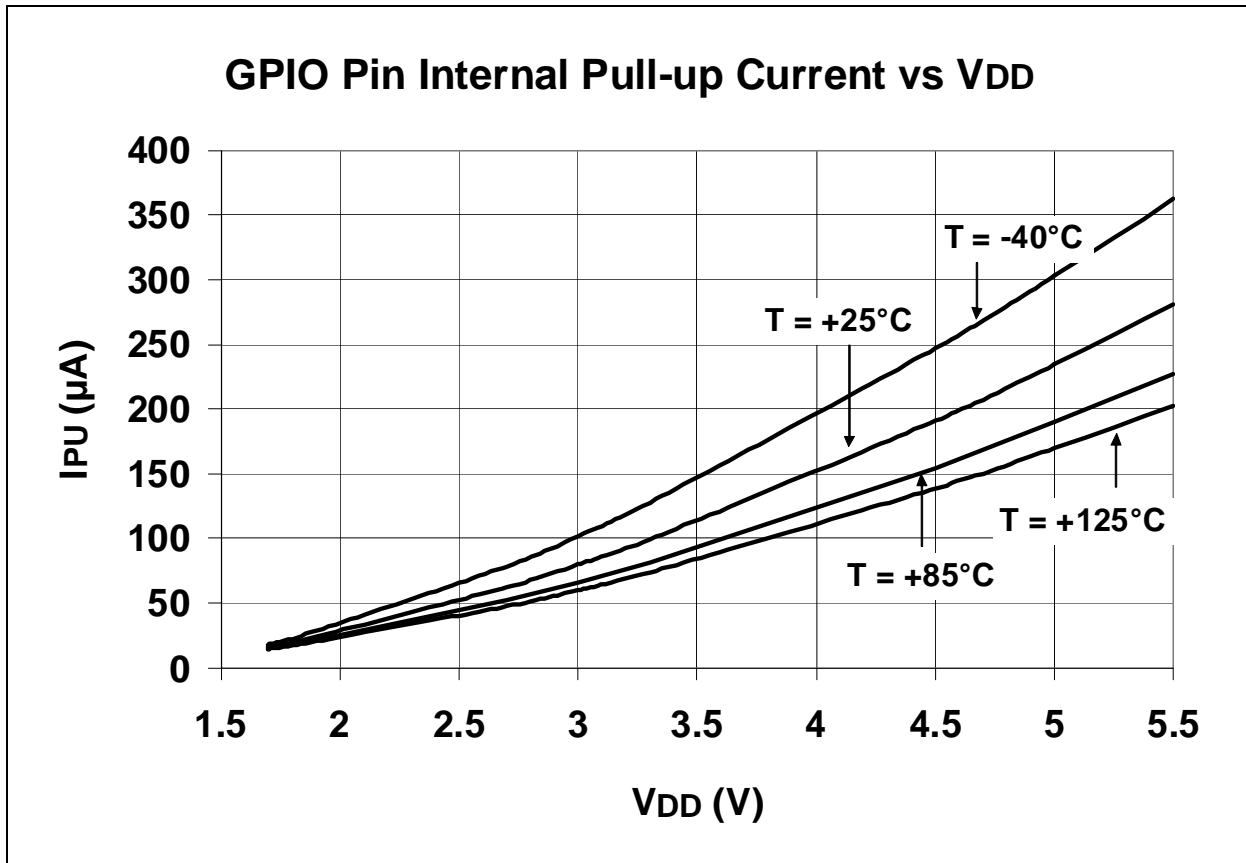
| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PU7 | PU6 | PU5 | PU4 | PU3 | PU2 | PU1 | PU0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-0 **PU7:PU0:** Controls the internal pull-up resistors on each pin (when configured as an input or output) <7:0>.
 1 = Pull-up enabled
 0 = Pull-up disabled

FIGURE 1-10: TYPICAL PERFORMANCE CURVE FOR THE INTERNAL PULL-UP RESISTORS



1.6.8 INTERRUPT FLAG REGISTER

The INTF register reflects the interrupt condition on the port pins of any pin that is enabled for interrupts via the GPINTEN register. A 'set' bit indicates that the associated pin caused the interrupt.

This register is 'read only'. Writes to this register will be ignored.

REGISTER 1-8: INTF – INTERRUPT FLAG REGISTER

| | | | | | | | |
|-------|------|------|------|------|------|------|-------|
| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
| INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 | INT0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

INT7:INT0: Reflects the interrupt condition on the port. Will reflect the change only if interrupts are enabled (GPINTEN) <7:0>.

1 = Pin caused interrupt

0 = Interrupt not pending

MCP23009/MCP23S09

1.6.9 INTERRUPT CAPTURE REGISTER

The INTCAP register captures the GPIO port value at the time the interrupt occurred. The register is 'read only' and is updated only when an interrupt occurs. The register will remain unchanged until the interrupt is cleared via a read of INTCAP or GPIO.

REGISTER 1-9: INTCAP – INTERRUPT CAPTURED VALUE FOR PORT REGISTER

| R-x | R-x | R-x | R-x | R-x | R-x | R-x | R-x |
|-------|------|------|------|------|------|------|-------|
| ICP7 | ICP6 | ICP5 | ICP4 | ICP3 | ICP2 | ICP1 | ICP0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

ICP7:ICP0: Reflects the logic level on the port pins at the time of interrupt due to pin change <7:0>.

1 = Logic-high

0 = Logic-low

1.6.10 PORT REGISTER

The GPIO register reflects the value on the port. Reading from this register reads the port. Writing to this register modifies the Output Latch (OLAT) register.

REGISTER 1-10: GPIO – GENERAL PURPOSE I/O PORT REGISTER

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| GP7 | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

GP7:GP0: Reflects the logic level on the pins <7:0>.

1 = Logic-high

0 = Logic-low

MCP23009/MCP23S09

1.6.11 OUTPUT LATCH REGISTER (OLAT)

The OLAT register provides access to the output latches. A read from this register results in a read of the OLAT and not the port itself. A write to this register modifies the output latches that modifies the pins configured as outputs.

REGISTER 1-11: OLAT – OUTPUT LATCH REGISTER 0

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OL7 | OL6 | OL5 | OL4 | OL3 | OL2 | OL1 | OL0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 7-0

OL7:OL0: Reflects the logic level on the output latch <7:0>.

1 = Logic-high

0 = Logic-low

1.7 Interrupt Logic

If enabled, the MCP23X09 activates the INT interrupt output when one of the port pins changes state or when a pin does not match the pre-configured default. Each pin is individually configurable as follows:

- Enable/disable interrupt via GPINTEN
- Can interrupt on either pin change or change from default as configured in DEFVAL

Both conditions are referred to as Interrupt on Change (IOC).

The Interrupt Control Module uses the following registers/bits:

- GPINTEN - Interrupt enable register
- INTCON - Controls the source for the IOC
- DEFVAL - Contains the register default for IOC operation
- IOCON (ODR and INTPOL) - configures the INT pin as push-pull, open-drain, and active level (high or low).

1.7.1 IOC FROM PIN CHANGE

If enabled, the MCP23X09 will generate an interrupt if a mismatch condition exists between the current port value and the previous port value. Only IOC enabled pins will be compared. See GPINTEN and INTCON registers.

1.7.2 IOC FROM REGISTER DEFAULT

If enabled, the MCP23X09 will generate an interrupt if a mismatch occurs between the DEFVAL register and the port. Only IOC enabled pins will be compared. See GPINTEN, INTCON, and DEFVAL registers.

1.7.3 INTERRUPT OPERATION

The INT interrupt output can be configured as “active low”, “active high”, or “open-drain” via the IOCON register.

Only those pins that are configured as an input (IODIR register) with interrupt-on-change (IOC) enabled (GPINTEN register) can cause an interrupt. Pins configured as an output have no effect on the interrupt output pin.

Input change activity on a port input pin that is enabled for IOC will generate an internal device interrupt and the device will capture the value of the port and copy it into INTCAP.

The first interrupt event will cause the port contents to be copied into the INTCAP register. Subsequent interrupt conditions on the port will not cause an interrupt to occur as long as the interrupt is not cleared by a read of INTCAP or GPIO.

1.7.4 CLEARING INTERRUPTS

The interrupt will remain active until the INTCAP or GPIO register is read (depending on IOCON.INTCC). Writing to these registers will not affect the interrupt. The interrupt condition will be cleared after the LSB of the data is clocked out during a Read operation of GPIO or INTCAP (depending on IOCON.INTCC).

Note: Assuming IOCON.INTCC = 0 (INT cleared on GPIO read): The value in INTCAP can be lost if GPIO is read before INTCAP while another IOC is pending. After reading GPIO, the interrupt will clear and then set due to the pending IOC, causing the INTCAP register to update.

MCP23009/MCP23S09

1.7.5 INTERRUPT CONDITIONS

There are two possible configurations to cause interrupts (configured via INTCON):

1. Pins configured for **interrupt-on-pin-change** will cause an interrupt to occur if a pin changes to the opposite state. The default state is reset after an interrupt occurs. For example, an interrupt occurs by an input changing from 1 to 0. The new initial state for the pin is a logic 0.
2. Pins configured for **interrupt-on-change from register value** will cause an interrupt to occur if the corresponding input pin differs from the register bit. The interrupt condition will remain as long as the condition exists, regardless if the INTAP or GPIO is read.

See [Figure 1-11](#) and [Figure 1-12](#) for more information on interrupt operations.

FIGURE 1-11: INTERRUPT-ON-PIN-CHANGE

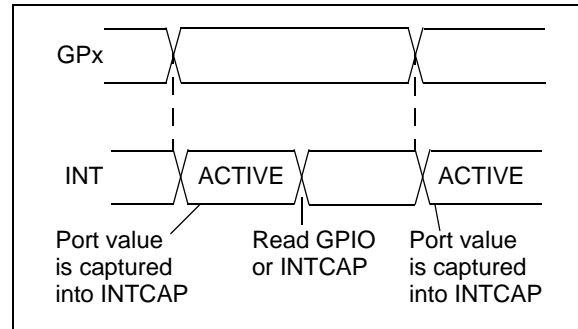
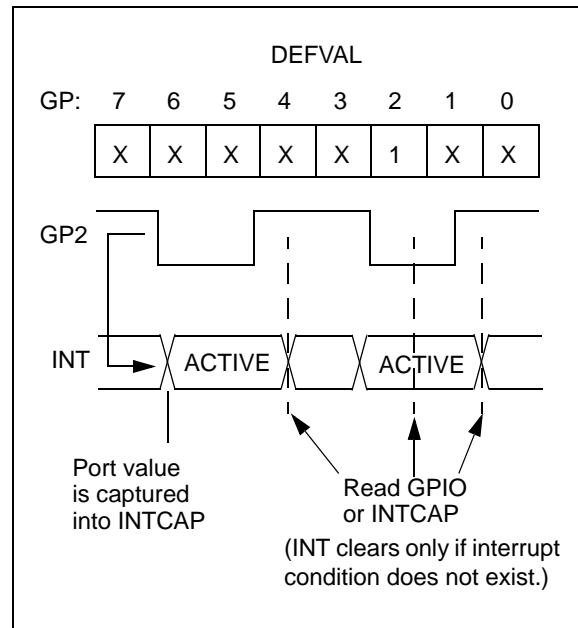


FIGURE 1-12: INTERRUPT-ON-CHANGE FROM REGISTER DEFAULT



2.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings ^(†)

| | |
|--|-----------------------|
| Ambient temperature under bias | -40°C to +125°C |
| Storage temperature | -65°C to +150°C |
| Voltage on VDD with respect to VSS | -0.3V to +7.0V |
| Voltage on $\overline{\text{RESET}}$ with respect to VSS | -0.3V to +14V |
| Voltage on all other pins with respect to VSS (except VDD and GPIOA/B) | -0.6V to (VDD + 0.6V) |
| Voltage on GPIO Pins: | -0.6V to 5.5V |
| Total power dissipation (Note 1)..... | 700 mW |
| Maximum current out of VSS pin | 200 mA |
| Maximum current into VDD pin | 125 mA |
| Input clamp current, I _{IK} (V _I < 0 or V _I > VDD)..... | ±20 mA |
| Output clamp current, I _{OK} (V _O < 0 or V _O > VDD) | ±20 mA |
| Maximum output current sunk by any Output pin..... | 25 mA |
| Maximum output current sunk by any Output pin (VDD = 1.8V) | 10 mA |

Note: Power dissipation is calculated as follows:
 $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

MCP23009/MCP23S09

2.1 DC CHARACTERISTICS

| DC Characteristics | | Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C | | | | | |
|--|--|--|-----------|--------------------|---------|-------|--|
| Param No. | Characteristic | Sym | Min | Typ ⁽²⁾ | Max | Units | Conditions |
| D001 | Supply Voltage | VDD | 1.8 | — | 5.5 | V | |
| D002 | VDD Start Voltage to Ensure Power-on Reset | VPOR | — | VSS | — | V | |
| D003 | VDD Rise Rate to Ensure Power-on Reset | SVDD | 0.05 | — | — | V/ms | Design guidance only. Not tested. |
| D004 | Supply Current | IDD | — | — | 1 | mA | SCL/SCK = 1 MHz |
| D005 | Standby (Idle) current | IDDS | — | — | 1 | μA | -40°C ≤ TA ≤ +85°C |
| | | | — | — | 6 | μA | +85°C ≤ TA ≤ +125°C |
| Input Low-Voltage | | | | | | | |
| D031 | $\overline{\text{CS}}$, GPIO, SCL/SCK, SDA, SI, RESET | VIL | VSS | — | 0.2 VDD | V | |
| Input High-Voltage | | | | | | | |
| D041 | $\overline{\text{CS}}$, SCL/SCK, SDA, SI, RESET | VIH | 0.8 VDD | — | VDD | V | |
| | GPIO | VIH | 0.8 VDD | — | 5.5 | V | |
| Input Leakage Current | | | | | | | |
| D060 | I/O port pins | IIL | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD, |
| Output Leakage Current | | | | | | | |
| D065 | I/O port pins | ILO | — | — | ±1 | μA | VSS ≤ VPIN ≤ VDD, |
| D070 | GPIO internal pull-up current | IPU | — | 220 | — | μA | VDD = 5V, GP Pins = VSS Note 1 |
| Output Low-Voltage | | | | | | | |
| D080 | GPIO | VOL | — | — | 0.6 | V | IOL = 8.5 mA, VDD = 4.5V (open-drain) |
| | INT | | — | — | 0.6 | V | IOL = 1.6 mA, VDD = 4.5V |
| | SO, SDA | | — | — | 0.6 | V | IOL = 3.0 mA, VDD = 1.8V |
| | SDA | | — | — | 0.8 | V | IOL = 3.0 mA, VDD = 4.5V |
| Output High-Voltage | | | | | | | |
| D090 | INT, SO | VOH | VDD - 0.7 | — | — | V | IOH = -3.0 mA, VDD = 4.5V |
| | | | VDD - 0.7 | — | — | | IOH = -400 μA, VDD = 1.8V |
| Capacitive Loading Specs on Output Pins | | | | | | | |
| D101 | GPIO, SO, INT | CIO | — | — | 50 | pF | |
| D102 | SDA | CB | — | — | 400 | pF | |

Note 1: This parameter is characterized, not 100% tested.

2: Data in the Typical ("Typ") column is at 5V, +25°C unless otherwise stated.

2.2 AC CHARACTERISTICS

FIGURE 2-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

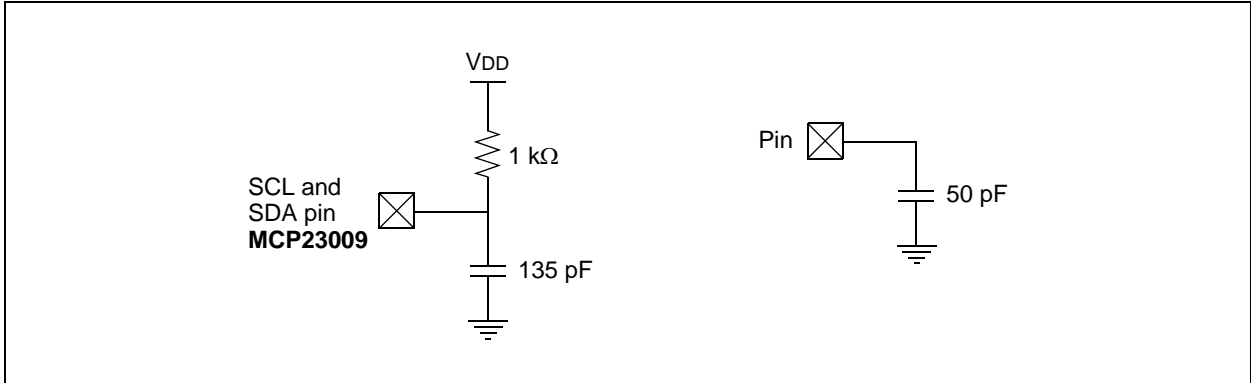


FIGURE 2-2: RESET AND DEVICE RESET TIMER TIMING

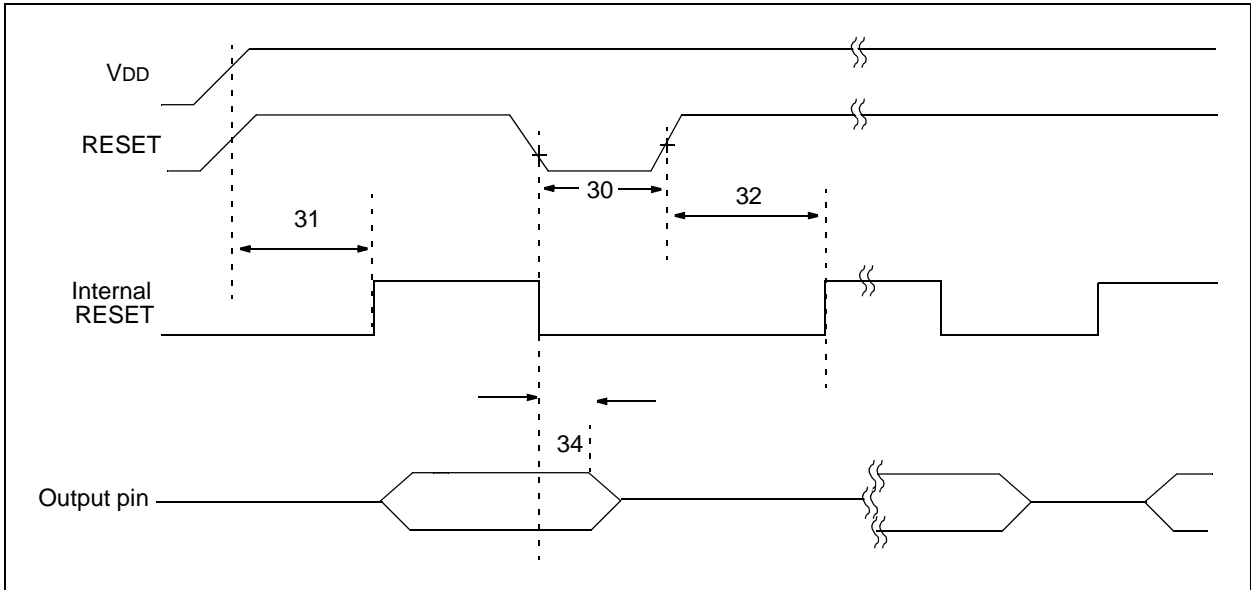


TABLE 2-1: RESET AND DEVICE RESET TIMER REQUIREMENTS

| AC Characteristics Standard Operating Conditions (unless otherwise specified) 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C. | | | | | | | |
|--|-------|------------------------------------|-----|--------------------|-----|-------|------------|
| Parameter No. | Sym | Characteristic | Min | Typ ⁽²⁾ | Max | Units | Conditions |
| 30 | TRSTL | RESET Pulse Width (low) | 1 | — | — | μs | VDD = 5.0V |
| 32 | THLD | Device active after reset high | — | 0 | — | μs | VDD = 5.0V |
| 31 | TPOR | POR at device power up | — | 20 | — | μs | VDD = 5.0V |
| 34 | Tioz | Output Hi-impedance from RESET Low | — | — | 1 | μs | |

Note 1: This parameter is characterized, not 100% tested.

2: Data in the Typical ("Typ") column is at 5V, +25°C, unless otherwise stated.

MCP23009/MCP23S09

TABLE 2-2: GP AND INT PINS

| AC Characteristics Standard Operating Conditions (unless otherwise specified) 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C. | | | | | | | |
|--|---------|-----------------------------------|-----|--------------------|-----|-------|---------------|
| Parameter No. | Sym | Characteristic | Min | Typ ⁽²⁾ | Max | Units | Conditions |
| 50 | tGPOV | Serial data to output valid | — | — | 500 | ns | |
| 51 | tINTD | Interrupt pin disable time | — | — | 600 | ns | |
| 52 | tGPIV | GP input change to register valid | — | 450 | — | ns | Note 1 |
| 53 | tGPINT | IOC event to INT active | — | — | 600 | ns | |
| 54 | tGLITCH | Glitch filter on GP pins | — | — | 50 | ns | Note 1 |

Note 1: This parameter is characterized, not 100% tested.

2: Data in the Typical ("Typ") column is at 5V, +25°C, unless otherwise stated.

FIGURE 2-3: GPIO AND INT TIMING

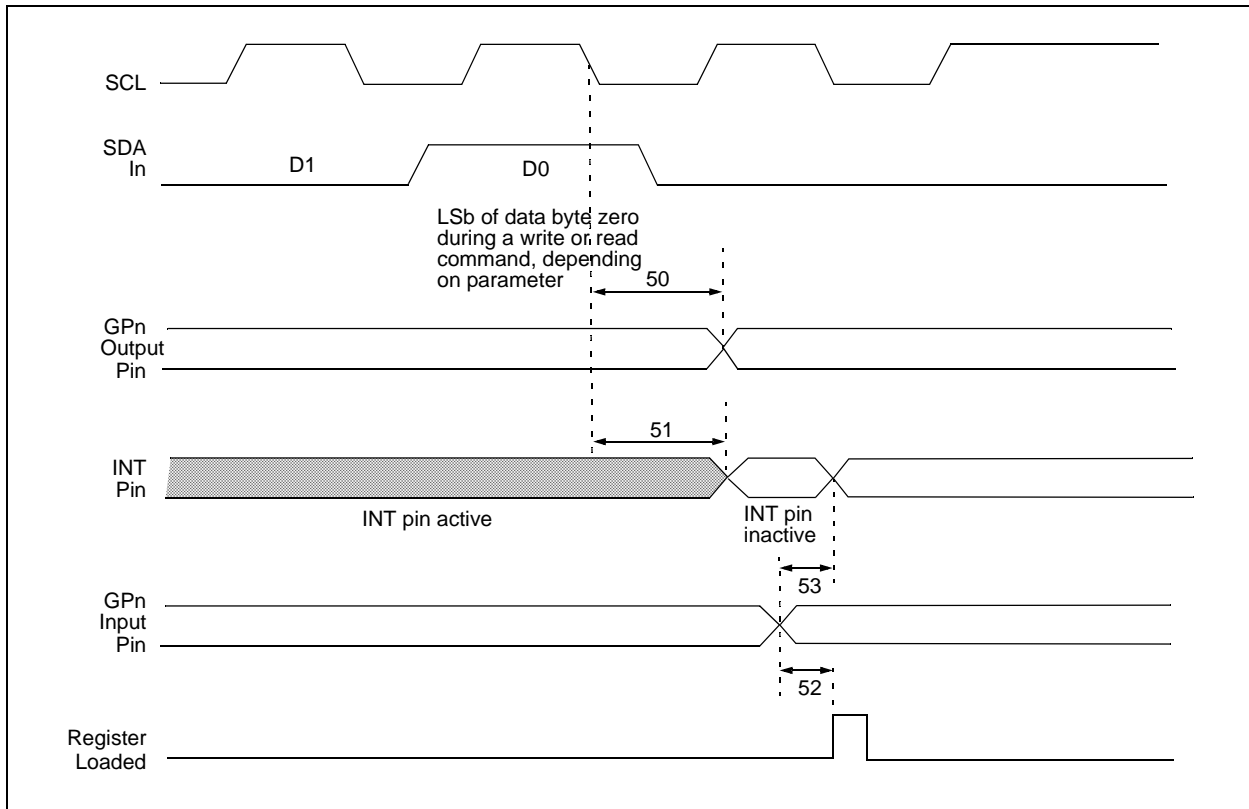


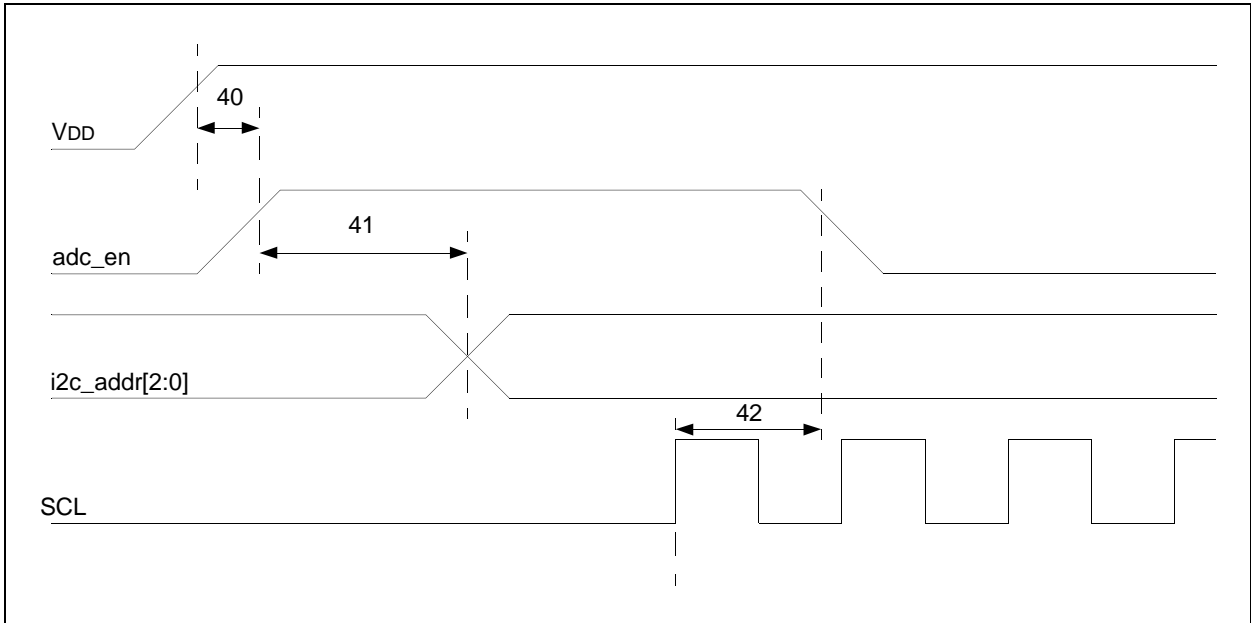
TABLE 2-3: HARDWARE ADDRESS LATCH TIMING

| AC Characteristics Standard Operating Conditions (unless otherwise specified) 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C. | | | | | | | |
|--|----------|---|-----|--------------------|-----|-------|------------|
| Parameter No. | Sym | Characteristic | Min | Typ ⁽²⁾ | Max | Units | Conditions |
| 40 | tADEN | Time from VDD stable after POR to ADC enable | — | 0 | — | μs | Note 1 |
| 41 | tADDRLAT | Time from ADC enable to address decode and latch | — | 50 | — | ns | Note 1 |
| 42 | tADDIS | Time from raising edge of serial clock to ADC disable | — | 10 | — | ns | Note 1 |

Note 1: This parameter is characterized, not 100% tested.

Note 2: Data in the Typical (“Typ”) column is at 5V, +25°C, unless otherwise stated..

FIGURE 2-4: HARDWARE ADDRESS LATCH TIMING



MCP23009/MCP23S09

FIGURE 2-5: I²C BUS START/STOP BITS TIMING

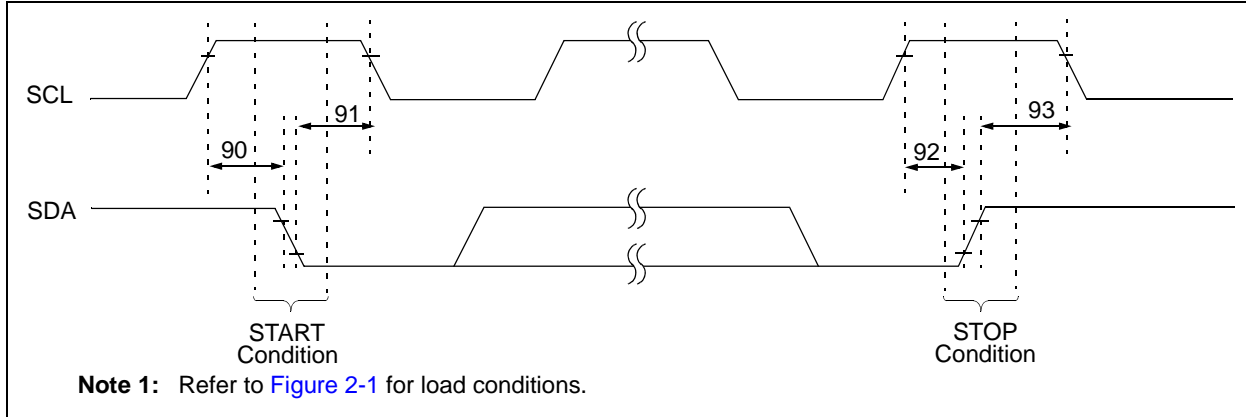
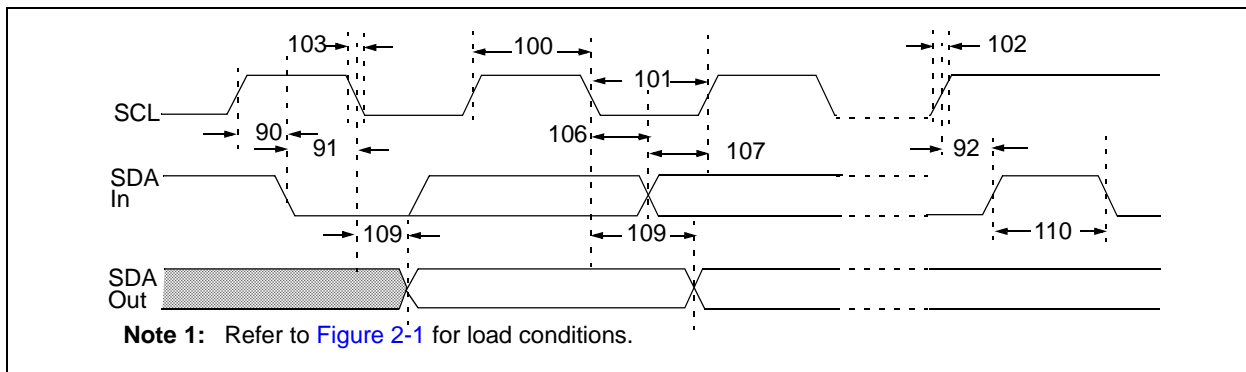


FIGURE 2-6: I²C BUS DATA TIMING



MCP23009/MCP23S09

TABLE 2-4: I²C BUS DATA REQUIREMENTS (SLAVE MODE)

| I ² C™ AC Characteristics | | Operating Conditions (unless otherwise indicated): 1.8V ≤ V _{DD} ≤ 5.5V at -40°C ≤ T _A ≤ +125°C R _{PU} (SCL, SDA) = 1 kΩ, C _L (SCL, SDA) = 135 pF. | | | | | |
|--------------------------------------|-----------------------------|--|--|-----|------|-------|-------------|
| Param No. | Characteristic | Sym | Min | Typ | Max | Units | Conditions |
| 100 | Clock High Time: | T _{HIGH} | | | | | |
| | 100 kHz mode | | 4.0 | — | — | μs | 1.8V – 5.5V |
| | 400 kHz mode | | 0.6 | — | — | μs | 1.8V – 5.5V |
| | 3.4 MHz mode | | 0.06 | — | — | μs | 2.7V – 5.5V |
| 101 | Clock Low Time: | T _{LOW} | | | | | |
| | 100 kHz mode | | 4.7 | — | — | μs | 1.8V – 5.5V |
| | 400 kHz mode | | 1.3 | — | — | μs | 1.8V – 5.5V |
| | 3.4 MHz mode | | 0.16 | — | — | μs | 2.7V – 5.5V |
| 102 | SDA and SCL Rise Time: | T _R (Note 1) | | | | | |
| | 100 kHz mode | | — | — | 1000 | ns | 1.8V – 5.5V |
| | 400 kHz mode | | 20 + 0.1 C _B ⁽²⁾ | — | 300 | ns | 1.8V – 5.5V |
| | 3.4 MHz mode | | 10 | — | 80 | ns | 2.7V – 5.5V |
| 103 | SDA and SCL Fall Time: | T _F (Note 1) | | | | | |
| | 100 kHz mode | | — | — | 300 | ns | 1.8V – 5.5V |
| | 400 kHz mode | | 20 + 0.1 C _B ⁽²⁾ | — | 300 | ns | 1.8V – 5.5V |
| | 3.4 MHz mode | | 10 | — | 80 | ns | 2.7V – 5.5V |
| 90 | START Condition Setup Time: | TSU:STA | | | | | |
| | 100 kHz mode | | 4.7 | — | — | μs | 1.8V – 5.5V |
| | 400 kHz mode | | 0.6 | — | — | μs | 1.8V – 5.5V |
| | 3.4 MHz mode | | 0.16 | — | — | μs | 2.7V – 5.5V |
| 91 | START Condition Hold Time: | THD:STA | | | | | |
| | 100 kHz mode | | 4.0 | — | — | μs | 1.8V – 5.5V |
| | 400 kHz mode | | 0.6 | — | — | μs | 1.8V – 5.5V |
| | 3.4 MHz mode | | 0.16 | — | — | μs | 2.7V – 5.5V |
| 106 | Data Input Hold Time: | THD:DAT | | | | | |
| | 100 kHz mode | | 0 | — | 3.45 | μs | 1.8V – 5.5V |
| | 400 kHz mode | | 0 | — | 0.9 | μs | 1.8V – 5.5V |
| | 3.4 MHz mode | | 0 | — | 0.07 | μs | 2.7V – 5.5V |
| 107 | Data Input Setup Time: | TSU:DAT | | | | | |
| | 100 kHz mode | | 250 | — | — | ns | 1.8V – 5.5V |
| | 400 kHz mode | | 100 | — | — | ns | 1.8V – 5.5V |
| | 3.4 MHz mode | | 0.01 | — | — | μs | 2.7V – 5.5V |
| 92 | STOP Condition Setup Time: | TSU:STO | | | | | |
| | 100 kHz mode | | 4.0 | — | — | μs | 1.8V – 5.5V |
| | 400 kHz mode | | 0.6 | — | — | μs | 2.7V – 5.5V |
| | 3.4 MHz mode | | 0.16 | — | — | μs | 4.5V – 5.5V |

Note 1: This parameter is characterized, not 100% tested.

2: C_B is specified from 10 to 400 (pF).

3: This parameter is not applicable in high-speed mode (3.4 MHz).

MCP23009/MCP23S09

TABLE 2-4: I²C BUS DATA REQUIREMENTS (SLAVE MODE) (CONTINUED)

| I ² C™ AC Characteristics | | Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C RPU (SCL, SDA) = 1 kΩ, CL (SCL, SDA) = 135 pF. | | | | | |
|--------------------------------------|---|--|-----|------|------|-------------|-------------|
| Param No. | Characteristic | Sym | Min | Typ | Max | Units | Conditions |
| 109 | Output Valid From Clock: | TAA | | | | | |
| | 100 kHz mode | | — | — | 3.45 | μs | 1.8V – 5.5V |
| | 400 kHz mode | | — | — | 0.9 | μs | 1.8V – 5.5V |
| | 3.4 MHz mode | — | — | 0.18 | μs | 2.7V – 5.5V | |
| 110 | Bus Free Time: | TBUF (NOTE 3) | | | | | |
| | 100 kHz mode | | 4.7 | — | — | μs | 1.8V – 5.5V |
| | 400 kHz mode | | 1.3 | — | — | μs | 1.8V – 5.5V |
| | 3.4 MHz mode | N/A | — | N/A | μs | 2.7V – 5.5V | |
| | Bus Capacitive Loading: | Cb (NOTE 2) | | | | | |
| | 100 kHz and 400 kHz | | — | — | 400 | pF | (Note 1) |
| | 3.4 MHz | — | — | 100 | pF | (Note 1) | |
| | Input Filter Spike Suppression: (SDA and SCL) | TSP | | | | | |
| | 100 kHz and 400 kHz | | — | — | 50 | ns | (Note 1) |
| | 3.4 MHz | | — | — | 10 | ns | (Note 1) |

- Note 1:** This parameter is characterized, not 100% tested.
Note 2: Cb is specified from 10 to 400 (pF).
Note 3: This parameter is not applicable in high-speed mode (3.4 MHz).

FIGURE 2-7: SPI INPUT TIMING

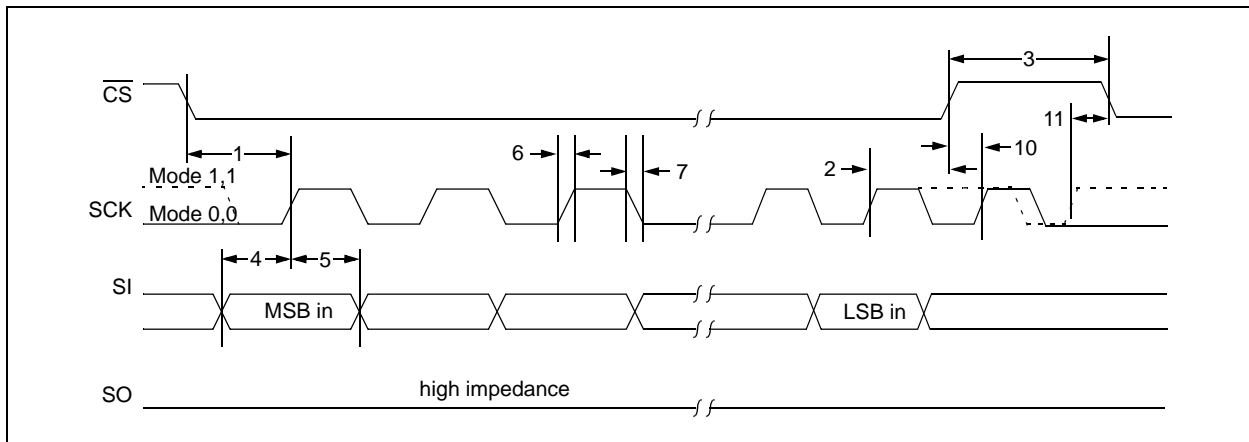
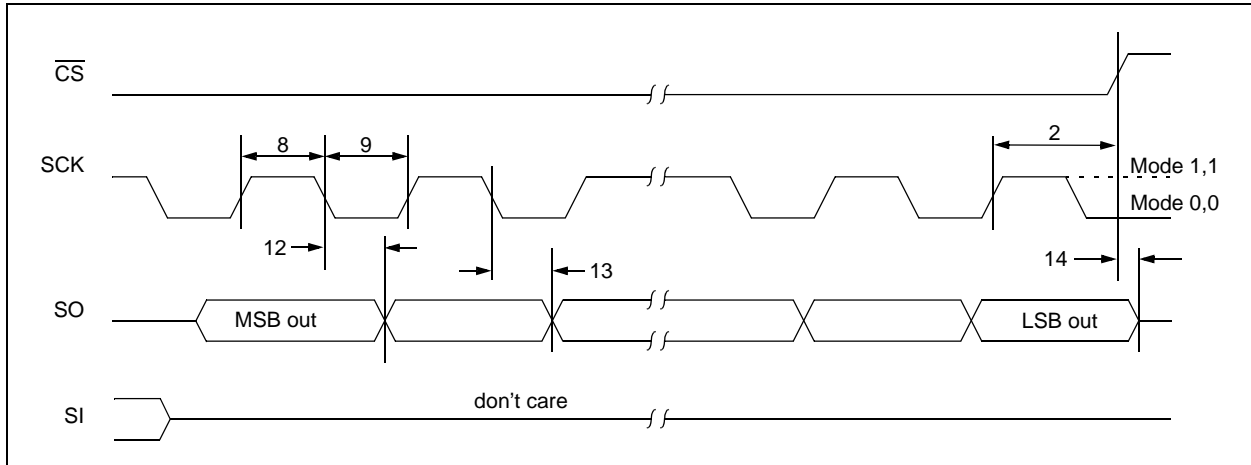


FIGURE 2-8: SPI OUTPUT TIMING



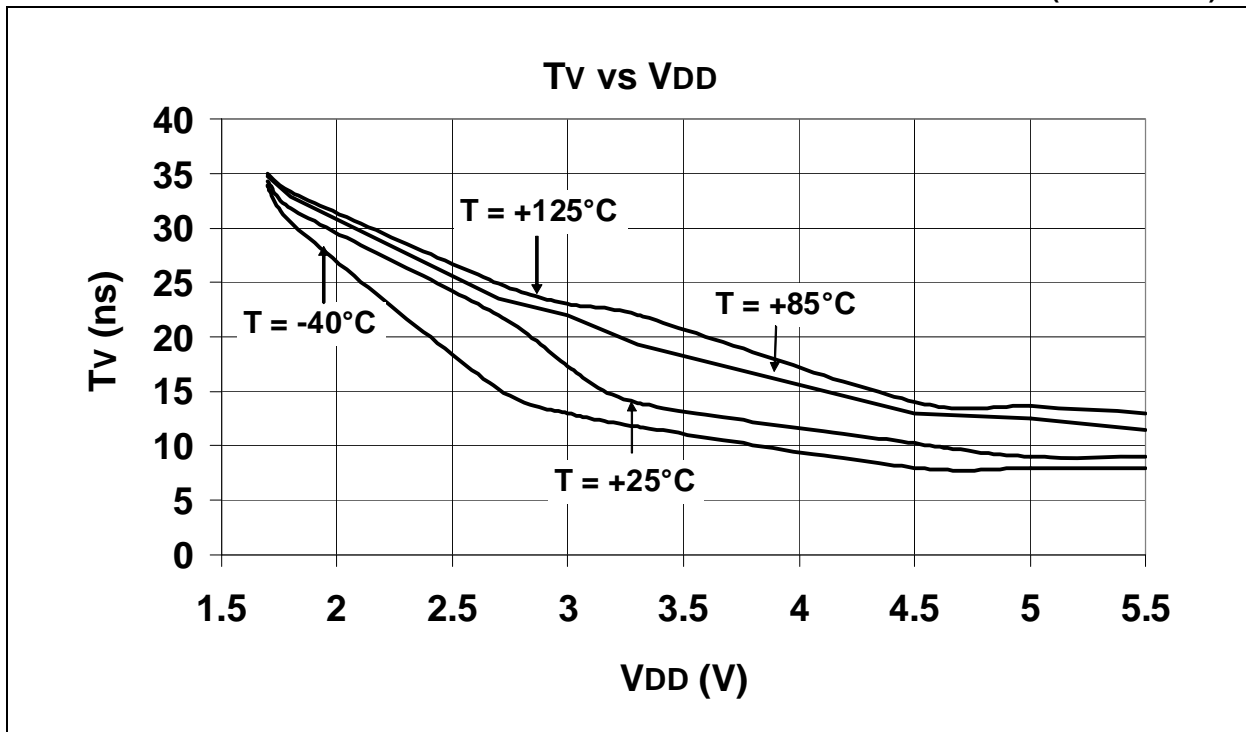
MCP23009/MCP23S09

TABLE 2-5: SPI INTERFACE AC CHARACTERISTICS

| SPI Interface AC Characteristics | | Operating Conditions (unless otherwise indicated): 1.8V ≤ VDD ≤ 5.5V at -40°C ≤ TA ≤ +125°C. | | | | | |
|----------------------------------|-----------------------------|---|-----|-----|-----|-------|---------------|
| Param No. | Characteristic | Sym | Min | Typ | Max | Units | Conditions |
| | Clock Frequency | FCLK | — | — | 10 | MHz | 1.8V – 5.5V |
| 1 | CS Setup Time | T _{CSS} | 50 | — | — | ns | |
| 2 | CS Hold Time | T _{CSH} | 50 | — | — | ns | 1.8V – 5.5V |
| 3 | CS Disable Time | T _{CSD} | 50 | — | — | ns | 1.8V – 5.5V |
| 4 | Data Setup Time | T _{SU} | 10 | — | — | ns | 1.8V – 5.5V |
| 5 | Data Hold Time | T _{HD} | 10 | — | — | ns | 1.8V – 5.5V |
| 6 | CLK Rise Time | T _R | — | — | 2 | μs | Note 1 |
| 7 | CLK Fall Time | T _F | — | — | 2 | μs | Note 1 |
| 8 | Clock High Time | T _{HI} | 45 | — | — | ns | 1.8V – 5.5V |
| 9 | Clock Low Time | T _{LO} | 45 | — | — | ns | 1.8V – 5.5V |
| 10 | Clock Delay Time | T _{C_{LD}} | 50 | — | — | ns | |
| 11 | Clock Enable Time | T _{CLE} | 50 | — | — | ns | |
| 12 | Output Valid from Clock Low | T _V | — | — | 45 | ns | 1.8V – 5.5V |
| 13 | Output Hold Time | T _{HO} | 0 | — | — | ns | |
| 14 | Output Disable Time | T _{DIS} | — | — | 100 | ns | |

Note 1: This parameter is characterized, not 100% tested.

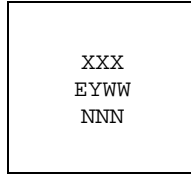
FIGURE 2-9: TYPICAL PERFORMANCE CURVE FOR SPI TV SPECIFICATION (PARAM #12)



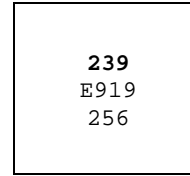
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

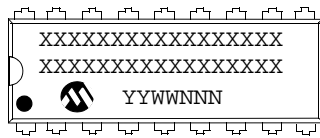
16-Lead QFN (3x3 mm)



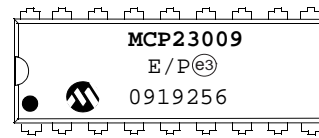
Example



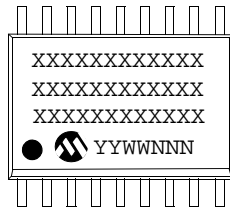
18-Lead PDIP (300 mil)



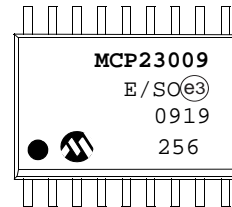
Example:



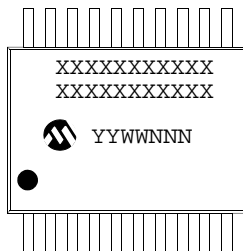
18-Lead SOIC (300 mil)



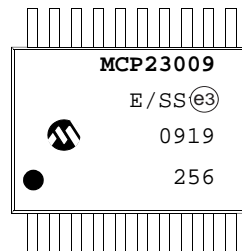
Example:



20-Lead SSOP (300 mil)



Example:



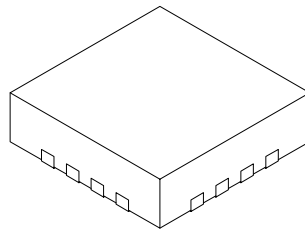
| | | |
|----------------|--------|--|
| Legend: | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | ⓔ3 | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package. |

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

MCP23009/MCP23S09

16-Lead Plastic Quad Flat, No Lead Package (MG) - 3x3x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|------------------------|-------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 16 | | |
| Pitch | e | 0.50 BSC | | |
| Overall Height | A | 0.80 | 0.85 | 0.90 |
| Standoff | A1 | 0.00 | 0.02 | 0.05 |
| Contact Thickness | A3 | 0.20 REF | | |
| Overall Width | E | 3.00 BSC | | |
| Exposed Pad Width | E2 | 1.00 | 1.10 | 1.50 |
| Overall Length | D | 3.00 BSC | | |
| Exposed Pad Length | D2 | 1.00 | 1.10 | 1.50 |
| Contact Width | b | 0.18 | 0.25 | 0.30 |
| Contact Length | L | 0.25 | 0.35 | 0.45 |
| Contact-to-Exposed Pad | K | 0.20 | - | - |

Notes:

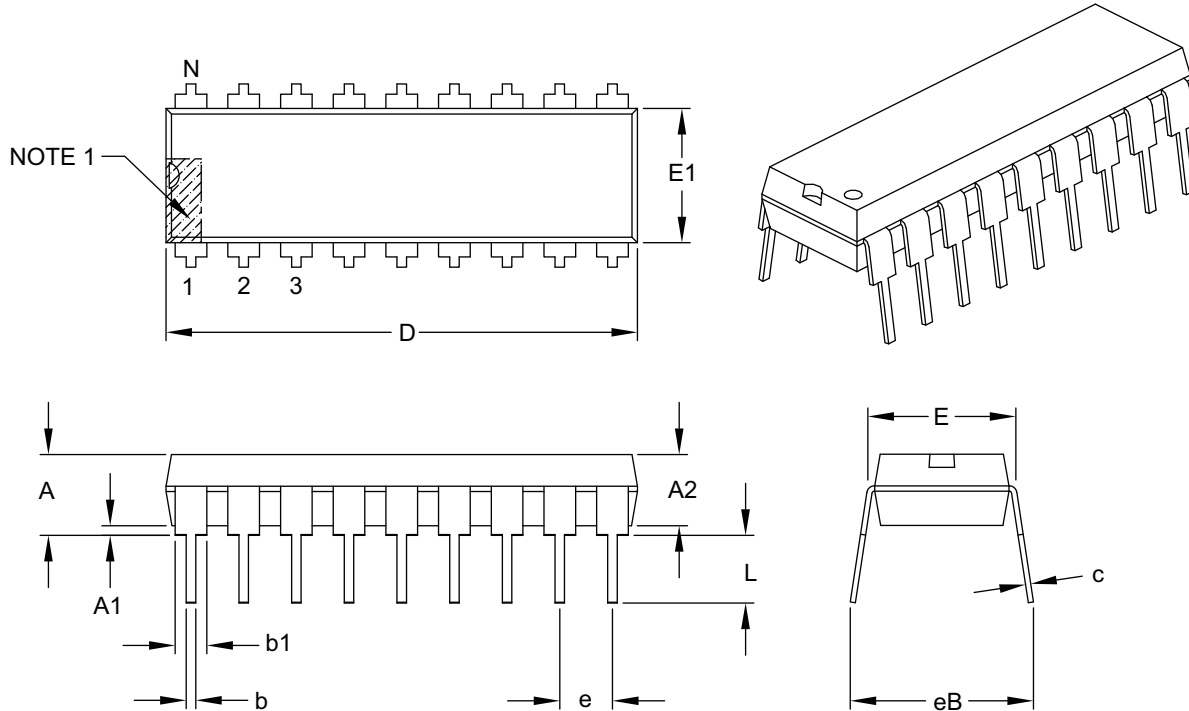
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-142A Sheet 2 of 2

MCP23009/MCP23S09

18-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | INCHES | | |
|----------------------------|-------|----------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 18 | | |
| Pitch | e | .100 BSC | | |
| Top to Seating Plane | A | – | – | .210 |
| Molded Package Thickness | A2 | .115 | .130 | .195 |
| Base to Seating Plane | A1 | .015 | – | – |
| Shoulder to Shoulder Width | E | .300 | .310 | .325 |
| Molded Package Width | E1 | .240 | .250 | .280 |
| Overall Length | D | .880 | .900 | .920 |
| Tip to Seating Plane | L | .115 | .130 | .150 |
| Lead Thickness | c | .008 | .010 | .014 |
| Upper Lead Width | b1 | .045 | .060 | .070 |
| Lower Lead Width | b | .014 | .018 | .022 |
| Overall Row Spacing § | eB | – | – | .430 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.

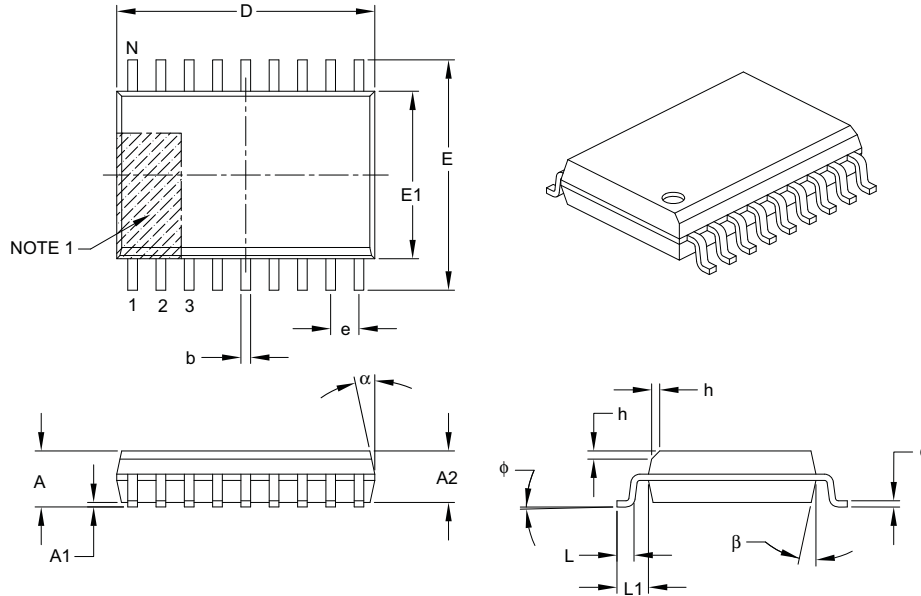
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-007B

MCP23009/MCP23S09

18-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|----------|-------------|-----|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 18 | | |
| Pitch | e | 1.27 BSC | | |
| Overall Height | A | – | – | 2.65 |
| Molded Package Thickness | A2 | 2.05 | – | – |
| Standoff § | A1 | 0.10 | – | 0.30 |
| Overall Width | E | 10.30 BSC | | |
| Molded Package Width | E1 | 7.50 BSC | | |
| Overall Length | D | 11.55 BSC | | |
| Chamfer (optional) | h | 0.25 | – | 0.75 |
| Foot Length | L | 0.40 | – | 1.27 |
| Footprint | L1 | 1.40 REF | | |
| Foot Angle | ϕ | 0° | – | 8° |
| Lead Thickness | c | 0.20 | – | 0.33 |
| Lead Width | b | 0.31 | – | 0.51 |
| Mold Draft Angle Top | α | 5° | – | 15° |
| Mold Draft Angle Bottom | β | 5° | – | 15° |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

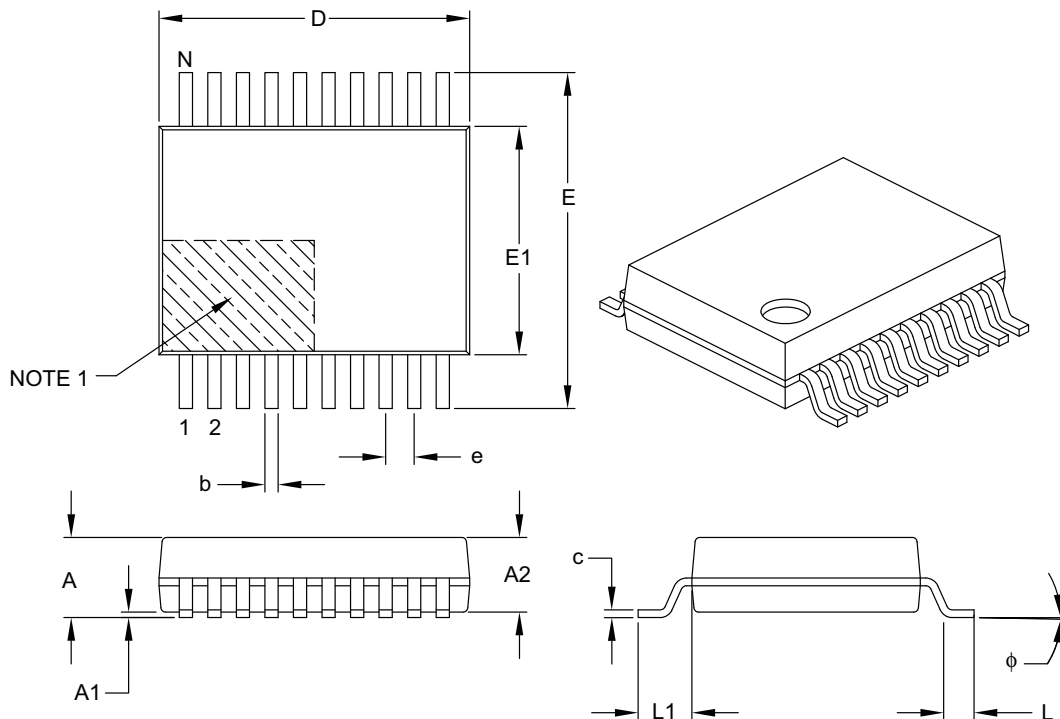
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-051B

MCP23009/MCP23S09

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits | Units | MILLIMETERS | | |
|--------------------------|--------|-------------|------|------|
| | | MIN | NOM | MAX |
| Number of Pins | N | 20 | | |
| Pitch | e | 0.65 BSC | | |
| Overall Height | A | – | – | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | – | – |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 6.90 | 7.20 | 7.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | 1.25 REF | | |
| Lead Thickness | c | 0.09 | – | 0.25 |
| Foot Angle | ϕ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | – | 0.38 |

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

APPENDIX A: REVISION HISTORY

Revision B (May 2009)

The following is the list of modifications:

1. Added the 3x3 QFN package (MG package marking).
2. Updated Revision History.

Revision A (December 2008)

- Original Release of this Document.

MCP23009/MCP23S09

NOTES:

MCP23009/MCP23S09

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

| <u>PART NO.</u> | <u>X</u> | <u>/XX</u> | |
|-------------------|-------------------|--|--|
| Device | Temperature Range | Package | |
| Device | MCP23009: | 8-Bit I/O Expander w/ I ² C™ Interface | |
| | MCP23009T: | 8-Bit I/O Expander w/ I ² C Interface (Tape and Reel) | |
| | MCP23S09: | 8-Bit I/O Expander w/ SPI Interface | |
| | MCP23S09T: | 8-Bit I/O Expander w/ SPI Interface (Tape and Reel) | |
| Temperature Range | E | = -40°C to +125°C (Extended) * | |
| Package | MG | = Plastic Quad Flat, No Lead Package (3x3x0.9 mm Body), 16-Lead | |
| | P | = Plastic DIP (300 mil Body), 18-Lead | |
| | SO | = Plastic SOIC (300 mil Body), 18-Lead | |
| | SS | = Plastic SSOP (5.3 mm), 20-Lead | |

| Examples: | |
|--------------------|---|
| a) MCP23009-E/P: | Extended Temp., 18LD PDIP package. |
| b) MCP23009-E/SO: | Extended Temp., 18LD SOIC package. |
| c) MCP23009T-E/SO: | Tape and Reel, Extended Temp., 18LD SOIC package. |
| d) MCP23009-E/SS: | Extended Temp., 20LD SSOP package. |
| e) MCP23009T-E/SS: | Tape and Reel, Extended Temp., 20LD SSOP package. |
| f) MCP23009-E/MG: | Extended Temp., 16LD QFN package. |
| | |
| a) MCP23S09-E/P: | Extended Temp., 18LD PDIP package. |
| b) MCP23S09-E/SO: | Extended Temp., 18LD SOIC package. |
| c) MCP23S09T-E/SO: | Tape and Reel, Extended Temp., 18LD SOIC package. |
| d) MCP23S09T-E/MG: | Tape and Reel, Extended Temp., 16LD QFN package. |

MCP23009/MCP23S09

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, rfPIC, SmartShunt and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, nanoWatt XLP, PICkit, PICDEM, PICDEM.net, PICtail, PIC³² logo, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2009, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949:2002 ==

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
<http://support.microchip.com>
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4080

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкуренспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru