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# EFM32ZG110 DATASHEET

## *F32/F16/F8/F4*

## Preliminary

- **ARM Cortex-M0+ CPU platform**
  - High Performance 32-bit processor @ up to 24 MHz
  - Wake-up Interrupt Controller
- **Flexible Energy Management System**
  - 20 nA @ 3 V Shutoff Mode
  - 0.5 µA @ 3 V Stop Mode, including Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 0.9 µA @ 3 V Deep Sleep Mode, including RTC with 32.768 kHz oscillator, Power-on Reset, Brown-out Detector, RAM and CPU retention
  - 46 µA/MHz @ 3 V Sleep Mode
  - 114 µA/MHz @ 3 V Run Mode, with code executed from flash
- **32/16/8/4 KB Flash**
- **4/4/2/2 KB RAM**
- **17 General Purpose I/O pins**
  - Configurable push-pull, open-drain, pull-up/down, input filter, drive strength
  - Configurable peripheral I/O locations
  - 11 asynchronous external interrupts
  - Output state retention and wake-up from Shutoff Mode
- **4 Channel DMA Controller**
- **4 Channel Peripheral Reflex System (PRS) for autonomous inter-peripheral signaling**
- **Hardware AES with 128-bit keys in 54 cycles**
- **Timers/Counters**
  - 2× 16-bit Timer/Counter
    - 2×3 Compare/Capture/PWM channels
  - 1× 24-bit Real-Time Counter
  - 1× 16-bit Pulse Counter
  - Watchdog Timer with dedicated RC oscillator @ 50 nA
- **Communication interfaces**
  - 1× Universal Synchronous/Asynchronous Receiver/Transmitter
    - UART/SPI/SmartCard (ISO 7816)/IrDA/I2S
    - Triple buffered full/half-duplex operation
  - Low Energy UART
    - Autonomous operation with DMA in Deep Sleep Mode
  - $I^2C$ Interface with SMBus support
    - Address recognition in Stop Mode
- **Ultra low power precision analog peripherals**
  - 12-bit 1 Msamples/s Analog to Digital Converter
    - 2 single ended channels/ differential channels
    - On-chip temperature sensor
  - Current Digital to Analog Converter
    - Selectable current range between 0.05 and 64 uA
  - 1× Analog Comparator
    - Capacitive sensing with up to 2 inputs
  - Supply Voltage Comparator
- **Ultra efficient Power-on Reset and Brown-Out Detector**
- **2-pin Serial Wire Debug interface**
- **Pre-Programmed UART Bootloader**
- **Temperature range -40 to 85 ºC**
- **Single power supply 1.85 to 3.8 V**
- **QFN24 package**

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# 1 Ordering Information

Table 1.1 (p. 2) shows the available EFM32ZG110 devices.

***Table 1.1. Ordering Information***

| Ordering Code | Flash (kB) | RAM (kB) | Max Speed (MHz) | Supply Voltage (V) | Temperature (ºC) | Package |
|---|---|---|---|---|---|---|
| EFM32ZG110F4-QFN24 | 4 | 2 | 24 | 1.85 - 3.8 | -40 - 85 | QFN24 |
| EFM32ZG110F8-QFN24 | 8 | 2 | 24 | 1.85 - 3.8 | -40 - 85 | QFN24 |
| EFM32ZG110F16-QFN24 | 16 | 4 | 24 | 1.85 - 3.8 | -40 - 85 | QFN24 |
| EFM32ZG110F32-QFN24 | 32 | 4 | 24 | 1.85 - 3.8 | -40 - 85 | QFN24 |

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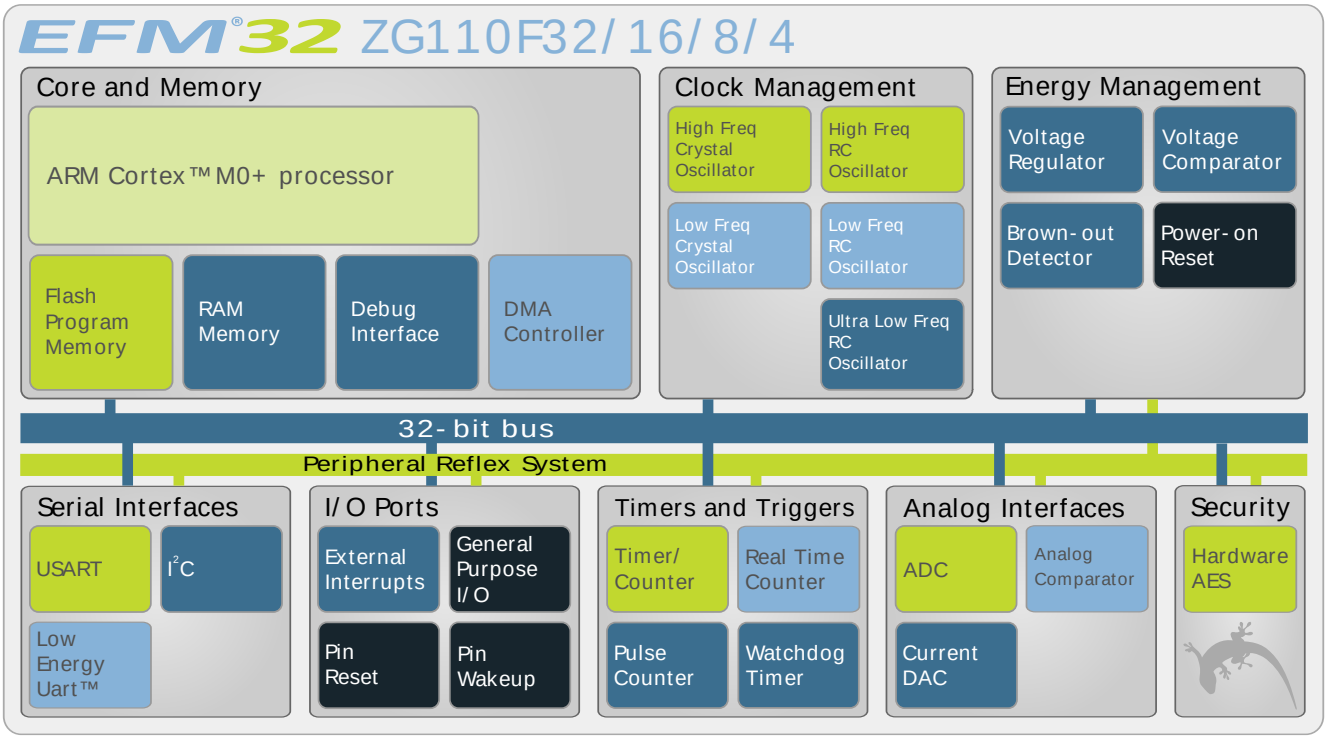
# 2 System Summary

## 2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M0+, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32ZG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32ZG110 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32ZG Reference Manual*.

A block diagram of the EFM32ZG110 is shown in Figure 2.1 (p. 3) .

***Figure 2.1. Block Diagram***




### 2.1.1 ARM Cortex-M0+ Core

The ARM Cortex-M0+ includes a 32-bit RISC processor which can achieve as much as 0.9 Dhrystone MIPS/MHz. A Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep is included as well. The EFM32 implementation of the Cortex-M0+ is described in detail in *ARM Cortex-M0+ Devices Generic User Guide*.

### 2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface.

### 2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32ZG microcontroller. The flash memory is readable and writable from both the Cortex-M0+ and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

### 2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

### 2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32ZG.

### 2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32ZG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

### 2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32ZG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

### 2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

### 2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

### 2.1.10 Inter-Integrated Circuit Interface (I2C)

The $I^2C$ module provides an interface between the MCU and a serial $I^2C$-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fast-mode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the $I^2C$ module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

### 2.1.11 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 SmartCards, IrDA and I2S devices.

### 2.1.12 Pre-Programmed UART Bootloader

The bootloader presented in application note AN0003 is pre-programmed in the device at factory. Auto-baud and destructive write are supported. The autobaud feature, interface and commands are described further in the application note.

### 2.1.13 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUART™, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

### 2.1.14 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse-Width Modulation (PWM) output.

### 2.1.15 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

### 2.1.16 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 – EM3.

### 2.1.17 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.18 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

### 2.1.19 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 2 external pins and 6 internal signals.

### 2.1.20 Current Digital to Analog Converter (IDAC)

The current digital to analog converter can source or sink a configurable constant current, which can be output on, or sinked from pin or ADC. The current is configurable with several ranges of various step sizes.

### 2.1.21 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

### 2.1.22 General Purpose Input/Output (GPIO)

In the EFM32ZG110, there are 17 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

## 2.2 Configuration Summary

The features of the EFM32ZG110 is a subset of the feature set described in the EFM32ZG Reference Manual. Table 2.1 (p. 6) describes device specific implementation of the features.

***Table 2.1. Configuration Summary***

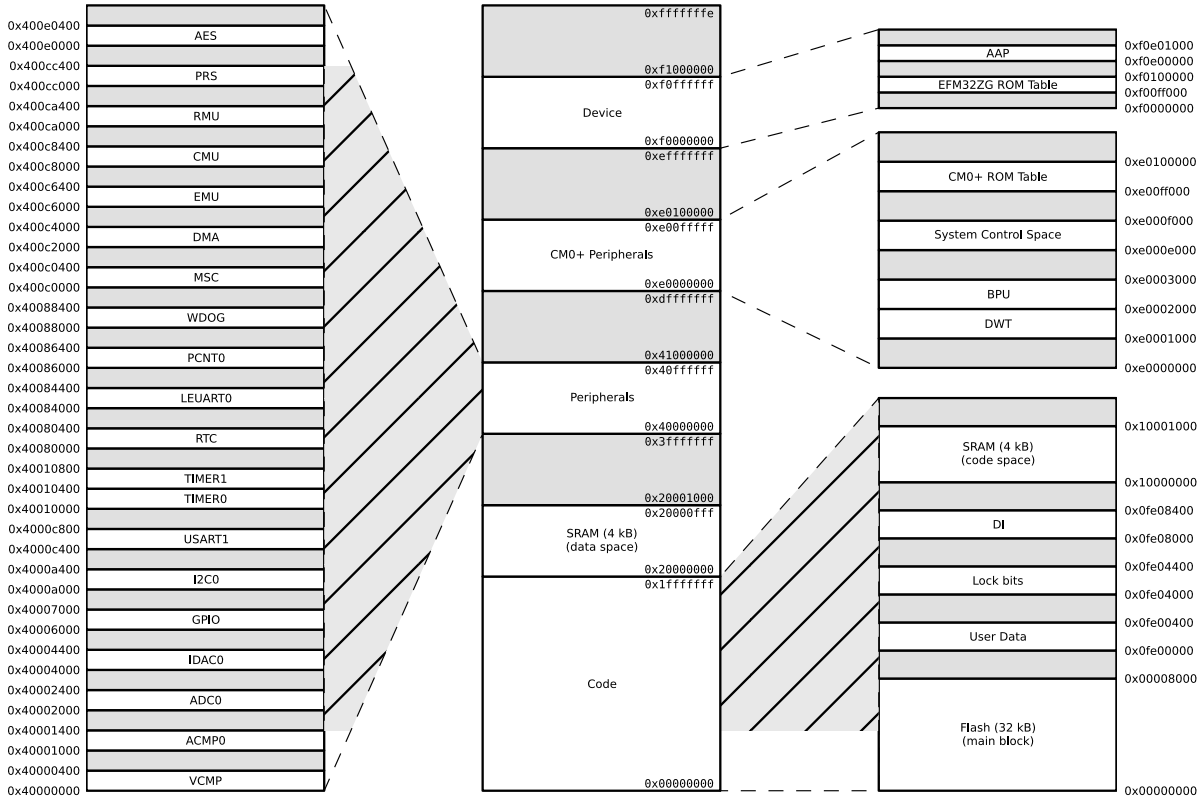
| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M0+ | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| USART0 | Full configuration with IrDA and I2S | US0_TX, US0_RX. US0_CLK, US0_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| TIMER0 | Full configuration | TIM0_CC[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| RTC | Full configuration | NA |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[1:0], ACMP0_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[1:0] |
| IDAC0 | Full configuration | IDAC0_OUT |
| AES | Full configuration | NA |

| Module | Configuration | Pin Connections |
|---|---|---|
| GPIO | 17 pins | Available pins are shown in Table 4.3 (p. 51) |

## 2.3 Memory Map

The *EFM32ZG110* memory map is shown in Figure 2.2 (p. 7), with RAM and Flash sizes for the largest memory configuration.

***Figure 2.2. EFM32ZG110 Memory Map with largest RAM and Flash sizes***



# 3 Electrical Characteristics

## 3.1 Test Conditions

### 3.1.1 Typical Values

The typical data are based on $T_{AMB}$=25°C and $V_{DD}$=3.0 V, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

### 3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 8), by simulation and/or technology characterisation unless otherwise specified.

## 3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 8) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 8) .

***Table 3.1. Absolute Maximum Ratings***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{STG}$ | Storage temperature range | | -40 | | 150[1] | °C |
| $T_S$ | Maximum soldering temperature | Latest IPC/JEDEC J-STD-020 Standard | | | 260 | °C |
| $V_{DDMAX}$ | External main supply voltage | | 0 | | 3.8 | V |
| $V_{IOPIN}$ | Voltage on any I/O pin | | -0.3 | | $V_{DD}$+0.3 | V |

[1]Based on programmed devices tested for 10000 hours at 150ºC. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

## 3.3 General Operating Conditions

### 3.3.1 General Operating Conditions

***Table 3.2. General Operating Conditions***

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_{AMB}$ | Ambient temperature range | -40 | | 85 | °C |
| $V_{DDOP}$ | Operating supply voltage | 1.85 | | 3.8 | V |
| $f_{APB}$ | Internal APB clock frequency | | | 24 | MHz |
| $f_{AHB}$ | Internal AHB clock frequency | | | 24 | MHz |

# 3.4 Current Consumption

***Table 3.3. Current Consumption***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{EM0}$ | EM0 current. No prescaling. Running prime number calculation code from Flash. | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 114.9 | | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 114.4 | | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 116.6 | | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 118.2 | | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 123.5 | | µA/MHz |
| | | 1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 155.1 | | µA/MHz |
| $I_{EM1}$ | EM1 current | 24 MHz HFXO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 48.0 | | µA/MHz |
| | | 21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 48.1 | | µA/MHz |
| | | 14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 50.1 | | µA/MHz |
| | | 11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 51.8 | | µA/MHz |
| | | 6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 57.1 | | µA/MHz |
| | | 1.2 MHz HFRCO. all peripheral clocks disabled, $V_{DD}$= 3.0 V | | 89.1 | | µA/MHz |
| $I_{EM2}$ | EM2 current | EM2 current with RTC at 1 Hz, RTC prescaled to 1kHz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.86 | | µA |
| | | EM2 current with RTC at 1 Hz, RTC prescaled to 1kHz, 32.768 kHz LFRCO, $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 1.66 | | µA |
| $I_{EM3}$ | EM3 current | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.49 | | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 1.26 | | µA |
| $I_{EM4}$ | EM4 current | $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 0.02 | | µA |
| | | $V_{DD}$= 3.0 V, $T_{AMB}$=85°C | | 0.29 | | µA |

## 3.4.1 EM0 Current Consumption

***Figure 3.1. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 24MHz***

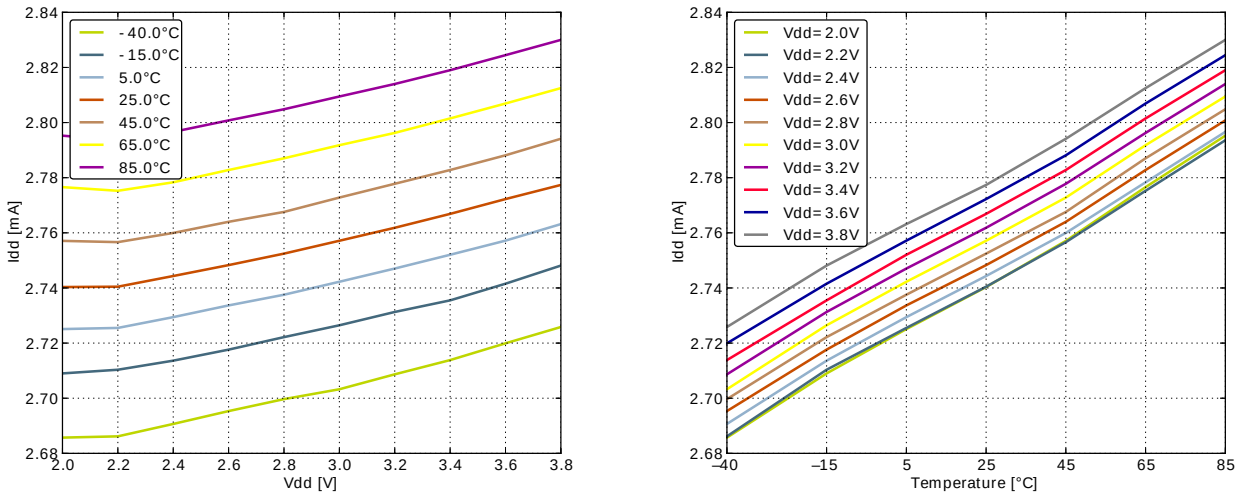



***Figure 3.2. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 21MHz***

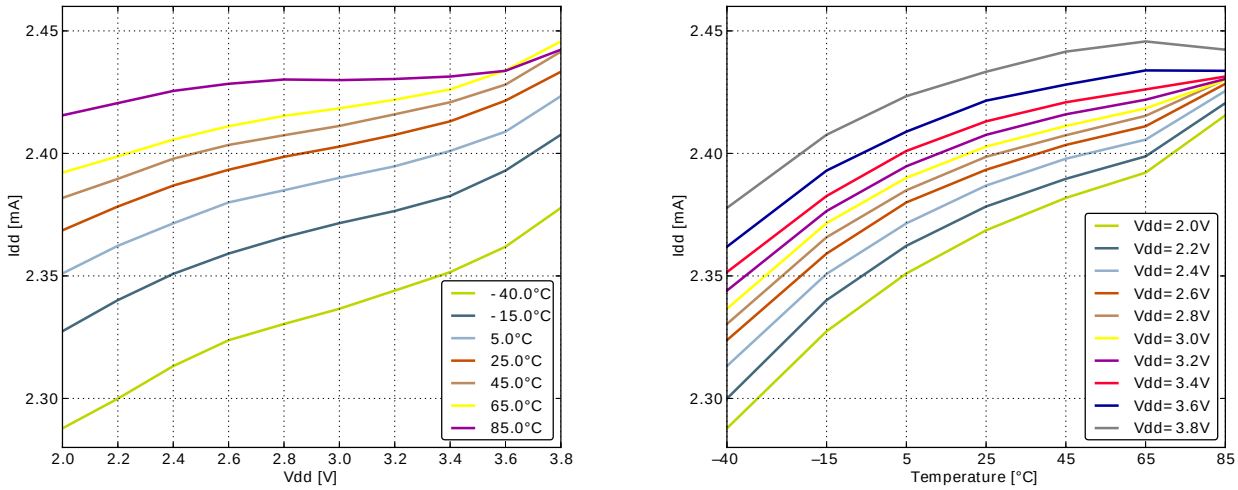


***Figure 3.3. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 14MHz***

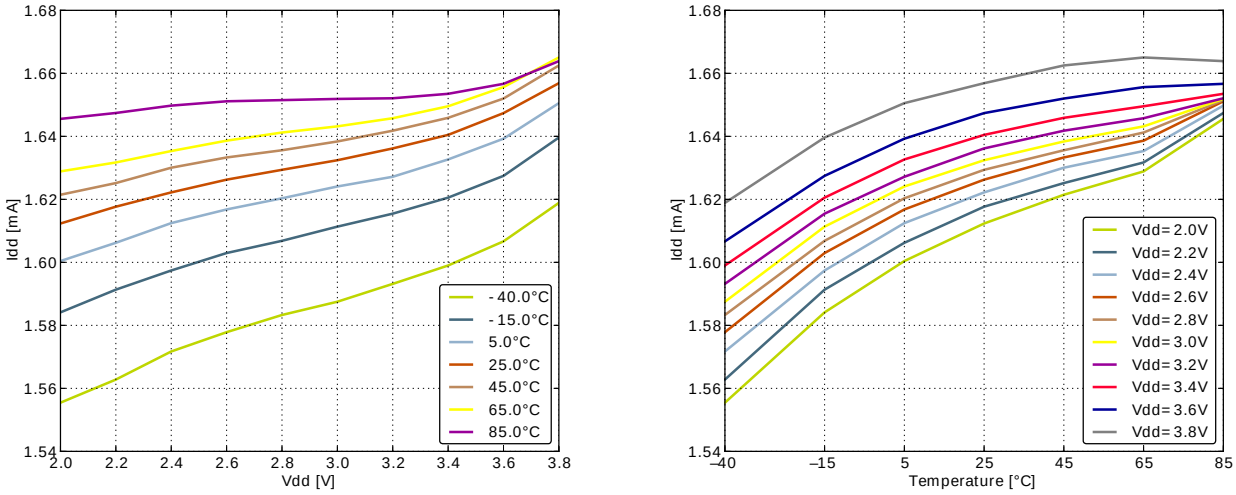



***Figure 3.4. EM0 Current consumption while executing prime number calculation code from flash with HFRCO running at 11MHz***

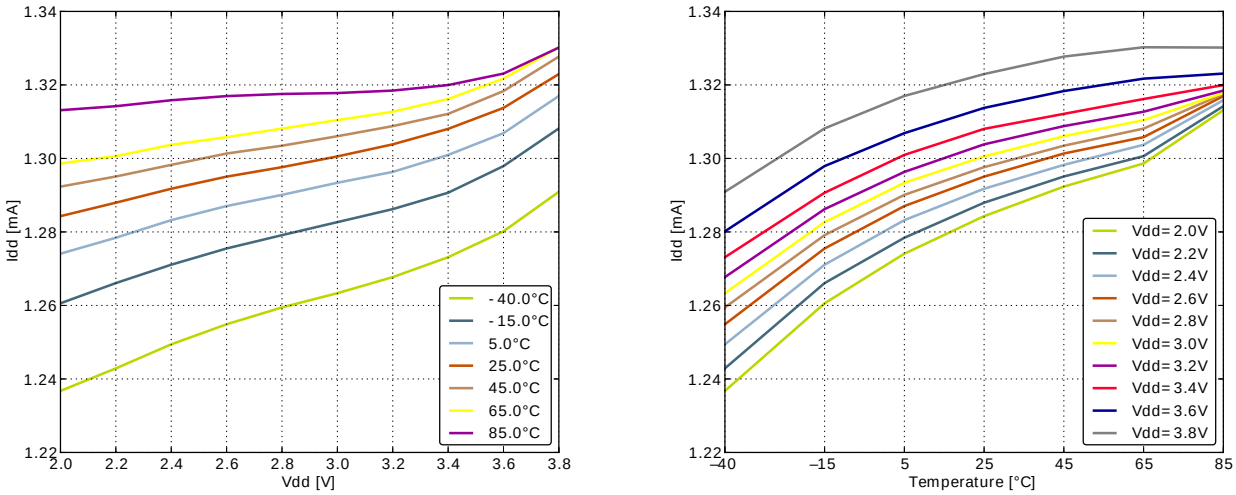
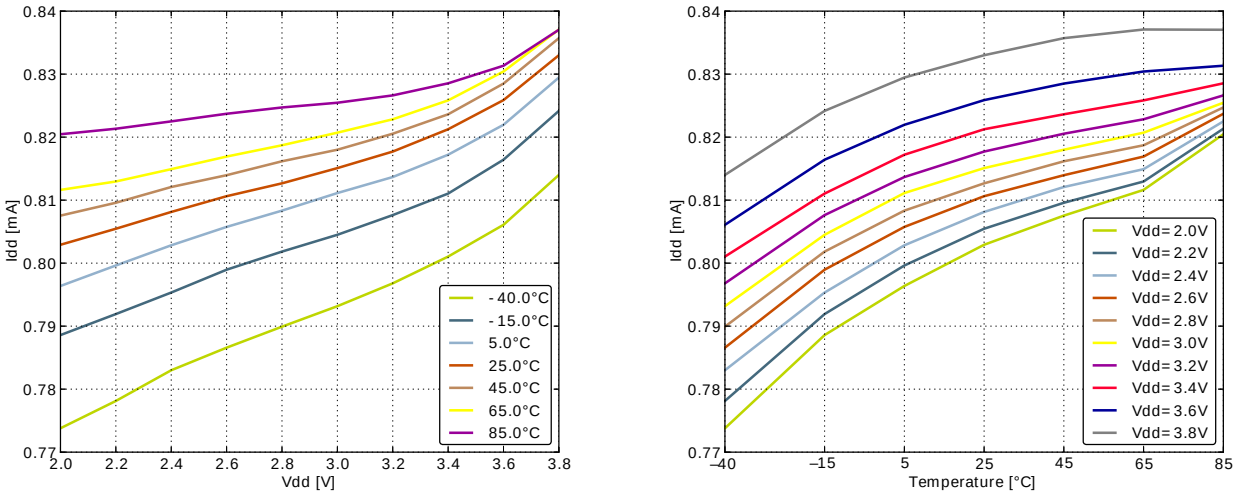


***Figure 3.5.***




## 3.4.2 EM1 Current Consumption

***Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 24MHz***

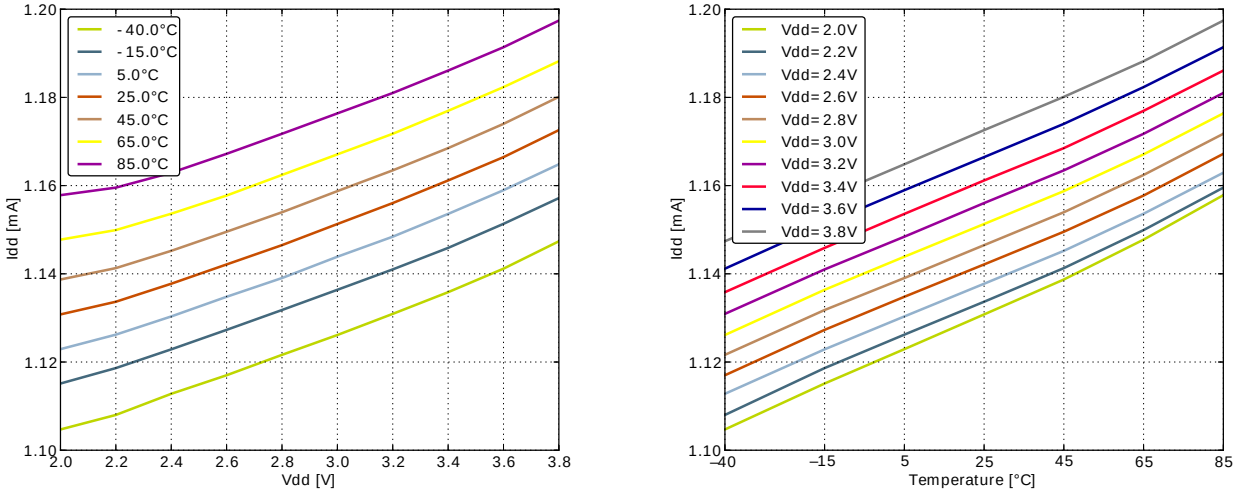


***Figure 3.7. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 21MHz***

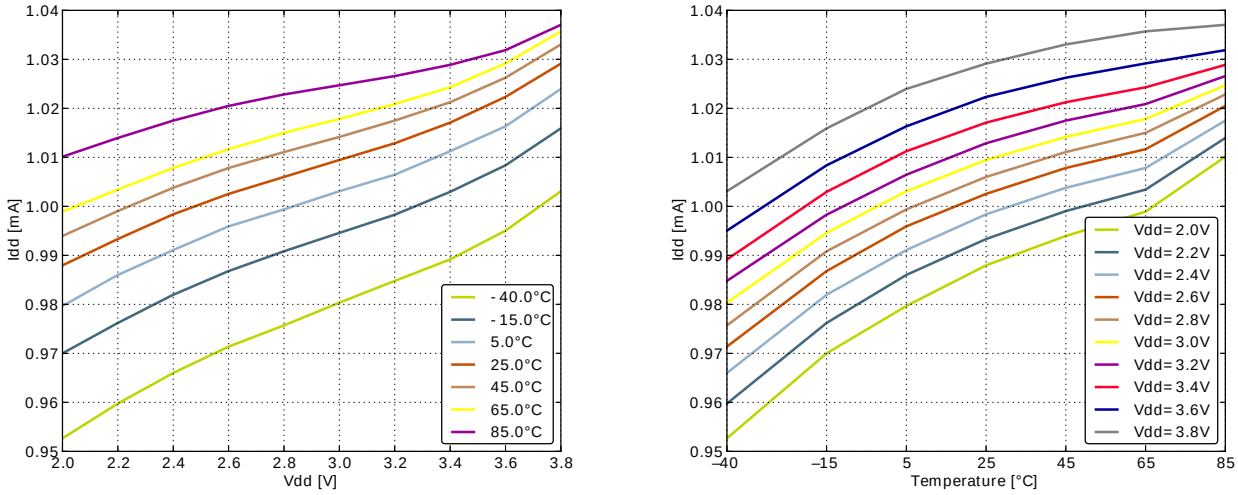



***Figure 3.8. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 14MHz***

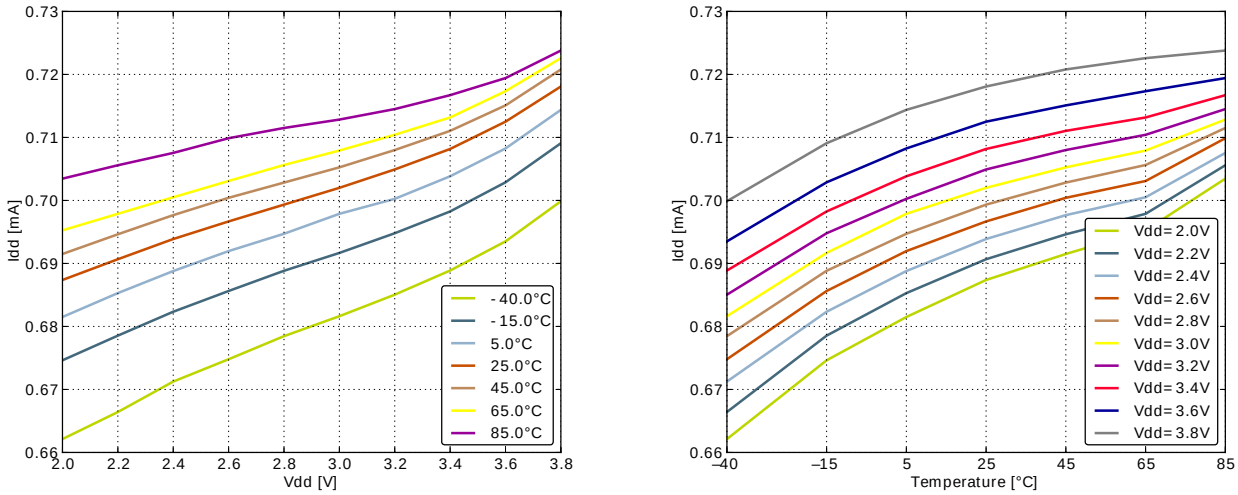


***Figure 3.9. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz***

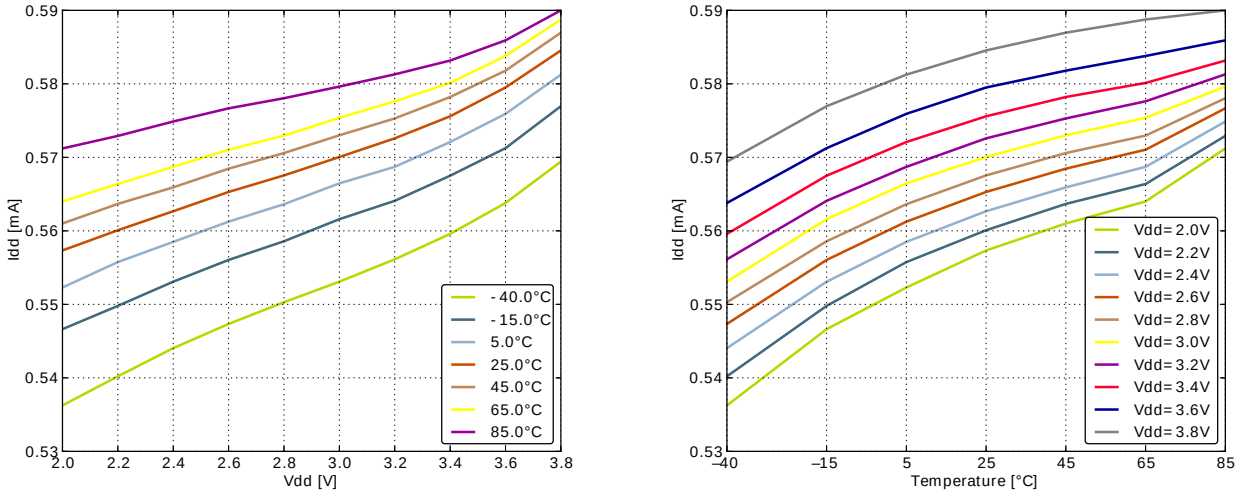
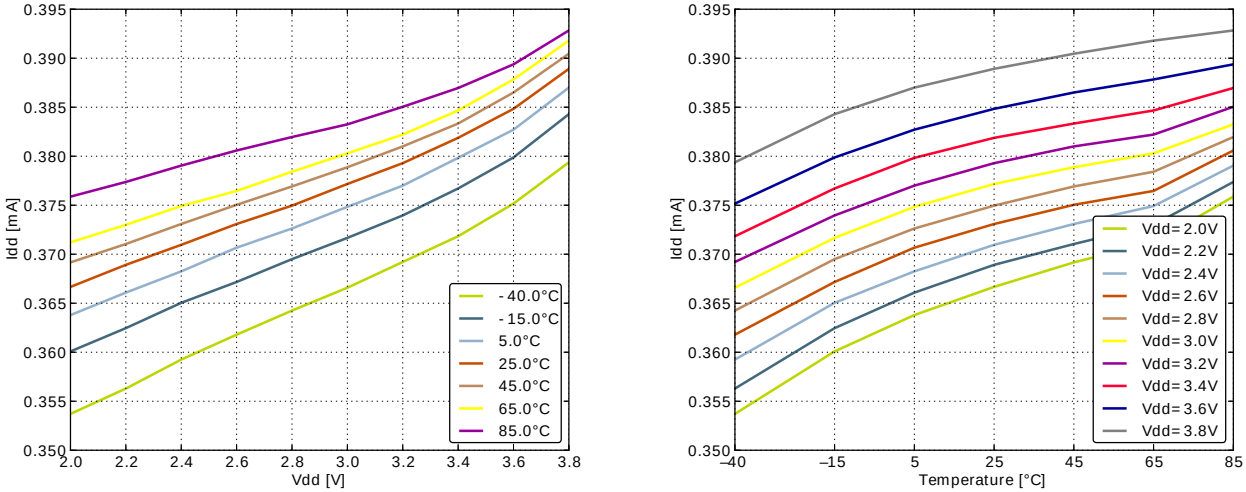
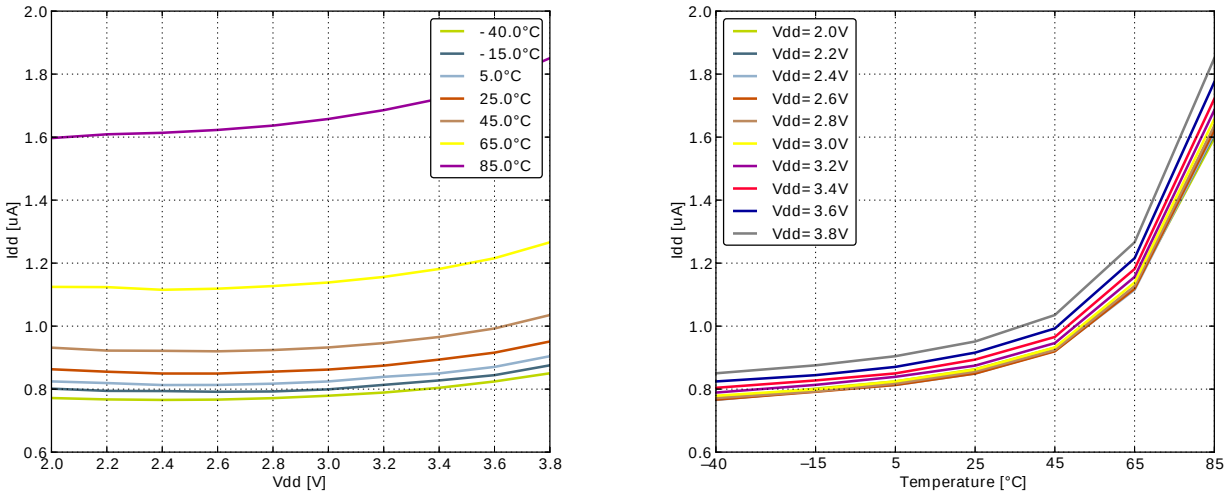



***Figure 3.10.***



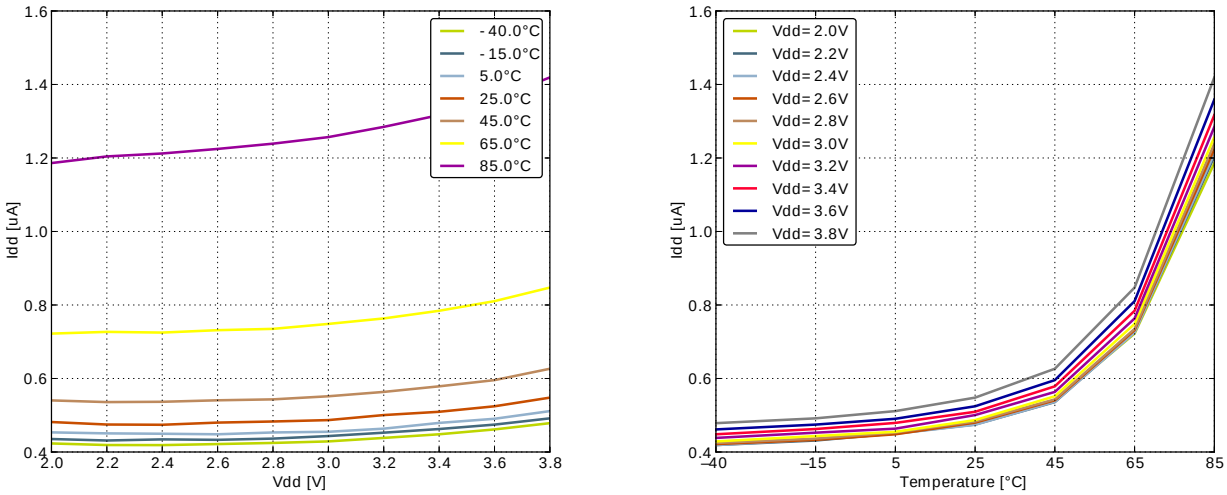
## 3.4.3 EM2 Current Consumption

***Figure 3.11. EM2 current consumption. RTC prescaled to 1kHz, 32.768 kHz LFRCO.***



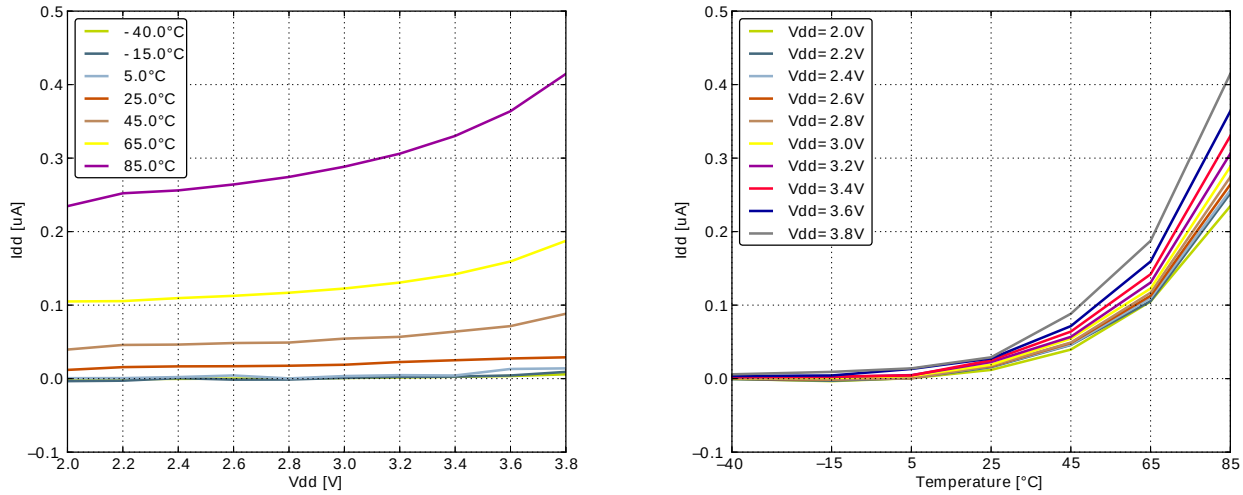

## 3.4.4 EM3 Current Consumption

***Figure 3.12. EM3 current consumption.***



### 3.4.5 EM4 Current Consumption

***Figure 3.13. EM4 current consumption.***




## 3.5 Transition between Energy Modes

***Table 3.4. Energy Modes Transitions***

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{EM10}$ | Transition time from EM1 to EM0 | | 0[1] | | HF core CLK cycles |
| $t_{EM20}$ | Transition time from EM2 to EM0 | | 2 | | µs |
| $t_{EM30}$ | Transition time from EM3 to EM0 | | 2 | | µs |
| $t_{EM40}$ | Transition time from EM4 to EM0 | | 163 | | µs |

[1]Core wakeup time only.

## 3.6 Power Management

The EFM32ZG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

### Table 3.5. Power Management

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BODextthr-}$ | BOD threshold on falling external supply voltage | | 1.82 | | 1.85 | V |
| $V_{BODintthr-}$ | BOD threshold on falling internally regulated supply voltage | | 1.62 | | 1.68 | V |
| $V_{BODextthr+}$ | BOD threshold on rising external supply voltage | | | 1.85 | | V |
| $t_{RESET}$ | Delay from reset is released until program execution starts | Applies to Power-on Reset, Brown-out Reset and pin reset. | | 163 | | µs |
| $C_{DECOUPLE}$ | Voltage regulator decoupling capacitor. | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | | 1 | | µF |

## 3.7 Flash

### Table 3.6. Flash

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $EC_{FLASH}$ | Flash erase cycles before failure | | 20000 | | | cycles |
| $RET_{FLASH}$ | Flash data retention | $T_{AMB}$<150°C | 10000 | | | h |
| | | $T_{AMB}$<85°C | 10 | | | years |
| | | $T_{AMB}$<70°C | 20 | | | years |
| $t_{W_PROG}$ | Word (32-bit) programming time | | 20 | | | µs |
| $t_{P_ERASE}$ | Page erase time | | 20 | 20.4 | 20.8 | ms |
| $t_{D_ERASE}$ | Device erase time | | 40 | 40.8 | 41.6 | ms |
| $I_{ERASE}$ | Erase current | | | | 7[1] | mA |
| $I_{WRITE}$ | Write current | | | | 7[1] | mA |
| $V_{FLASH}$ | Supply voltage during flash erase and write | | 1.8 | | 3.8 | V |

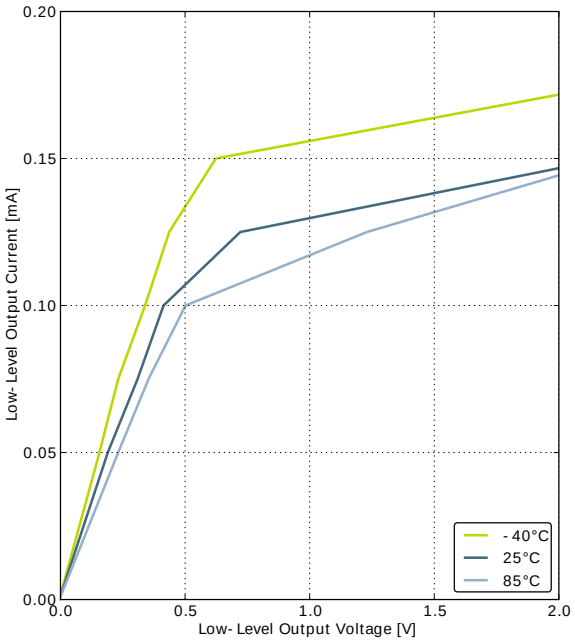
[1]Measured at 25°C

# 3.8 General Purpose Input Output

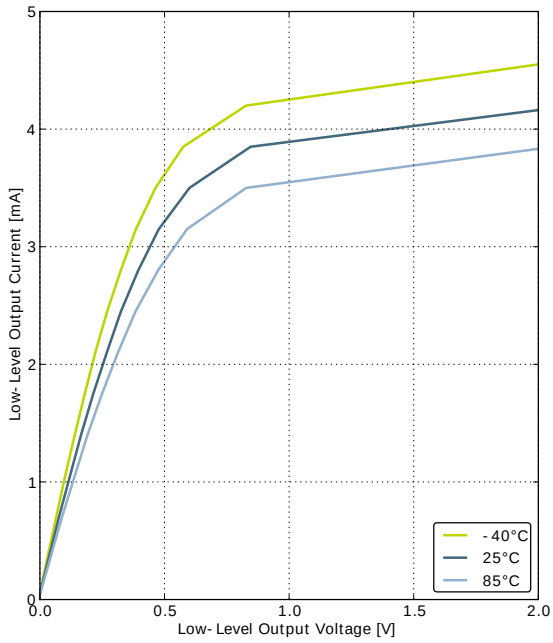
***Table 3.7. GPIO***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IOIL}$ | Input low voltage | | | | 0.3$V_{DD}$ | V |
| $V_{IOIH}$ | Input high voltage | | 0.7$V_{DD}$ | | | V |
| $V_{IOOH}$ | Output high voltage | Sourcing 6 mA, $V_{DD}$=1.85 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | 0.75$V_{DD}$ | | | V |
| | | Sourcing 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | 0.95$V_{DD}$ | | | V |
| | | Sourcing 20 mA, $V_{DD}$=1.85 V, GPIO_Px_CTRL DRIVEMODE = HIGH | 0.7$V_{DD}$ | | | V |
| | | Sourcing 20 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH | 0.9$V_{DD}$ | | | V |
| $V_{IOOL}$ | Output low voltage | Sinking 6 mA, $V_{DD}$=1.85 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | | | 0.25$V_{DD}$ | V |
| | | Sinking 6 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = STANDARD | | | 0.05$V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}$=1.85 V, GPIO_Px_CTRL DRIVEMODE = HIGH | | | 0.3$V_{DD}$ | V |
| | | Sinking 20 mA, $V_{DD}$=3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH | | | 0.1$V_{DD}$ | V |
| $I_{IOLEAK}$ | Input leakage current | High Impedance IO connected to GROUND or Vdd | | | +/-25 | nA |
| $R_{PU}$ | I/O pin pull-up resistor | | | 40 | | kOhm |
| $R_{PD}$ | I/O pin pull-down resistor | | | 40 | | kOhm |
| $R_{IOESD}$ | Internal ESD series resistor | | | 200 | | Ohm |
| $t_{IOGLITCH}$ | Pulse width of pulses to be removed by the glitch suppression filter | | 10 | | 50 | ns |
| $t_{IOOF}$ | Output fall time | 0.5 mA drive strength and load capacitance $C_L$=12.5-25pF. | 20+0.1$C_L$ | | 250 | ns |
| | | 2mA drive strength and load capacitance $C_L$=350-600pF | 20+0.1$C_L$ | | 250 | ns |
| $V_{IOHYST}$ | I/O pin hysteresis ($V_{IOTHR+}$ - $V_{IOTHR-}$) | $V_{DD}$ = 1.85 - 3.8 V | 0.1$V_{DD}$ | | | V |

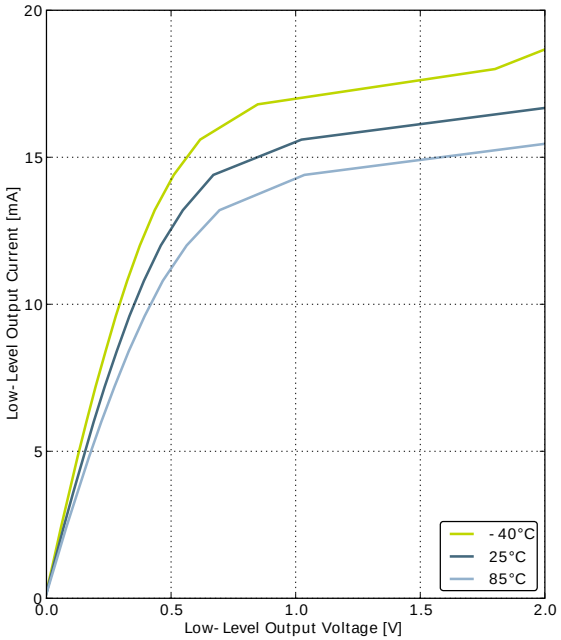
***Figure 3.14. Typical Low-Level Output Current, 2V Supply Voltage***



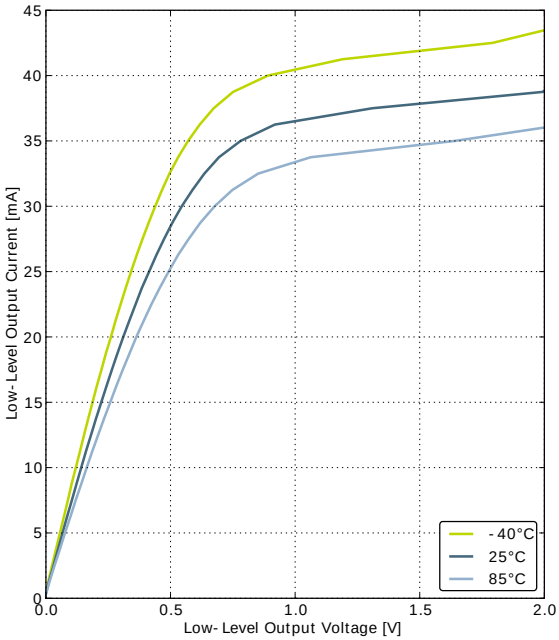

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

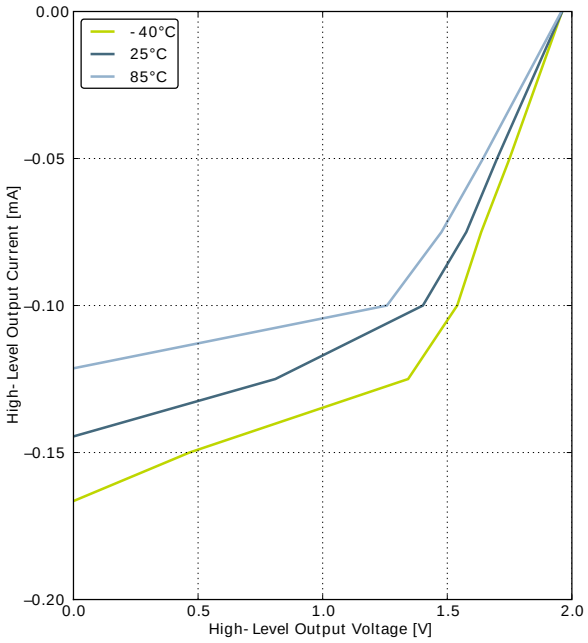



GPIO_Px_CTRL DRIVEMODE = STANDARD

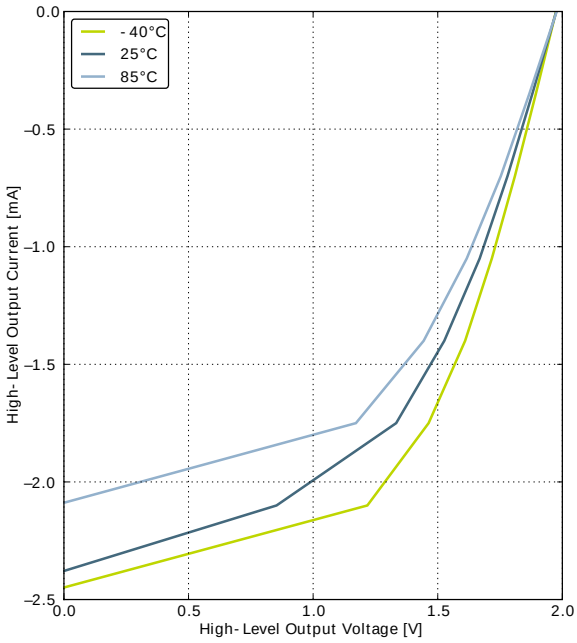



GPIO_Px_CTRL DRIVEMODE = HIGH

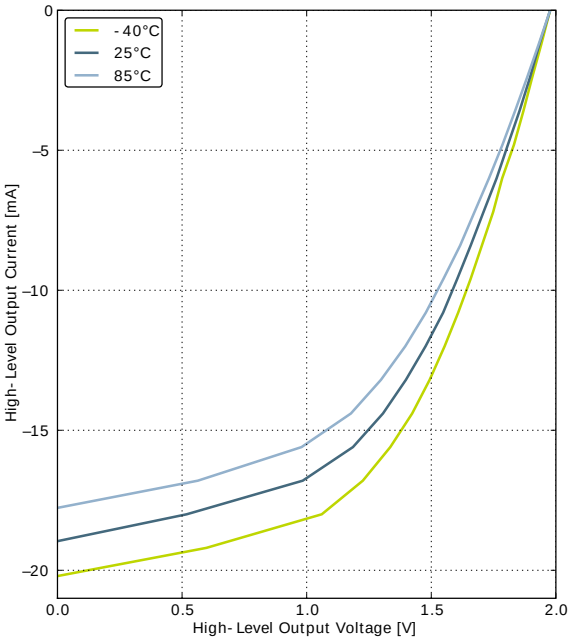
***Figure 3.15. Typical High-Level Output Current, 2V Supply Voltage***



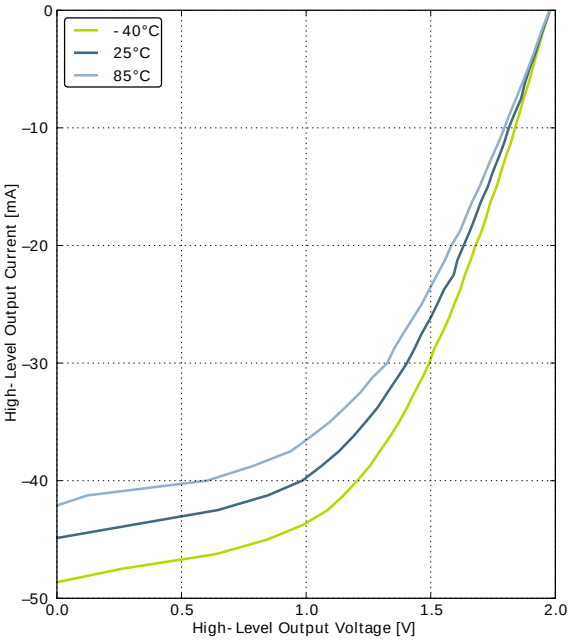

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

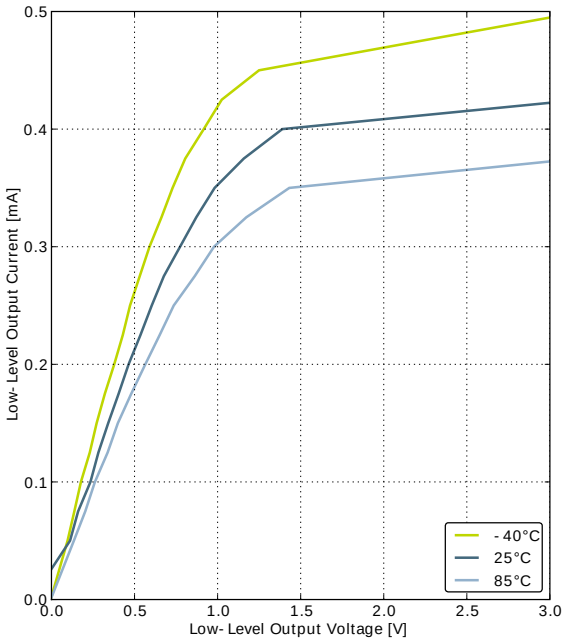



GPIO_Px_CTRL DRIVEMODE = STANDARD

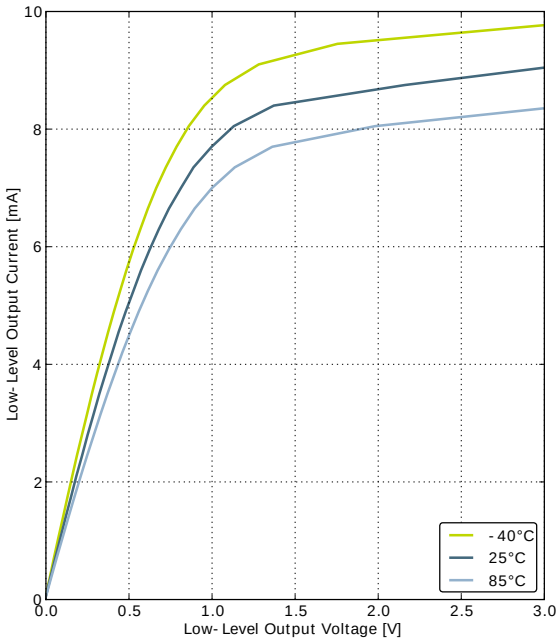



GPIO_Px_CTRL DRIVEMODE = HIGH

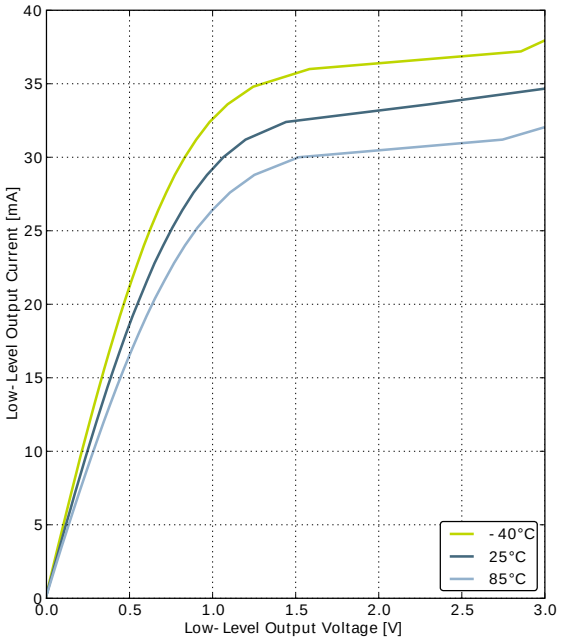
***Figure 3.16. Typical Low-Level Output Current, 3V Supply Voltage***



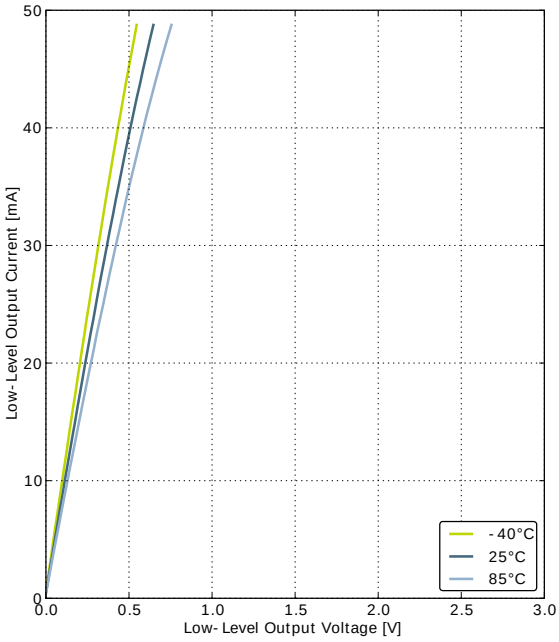

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

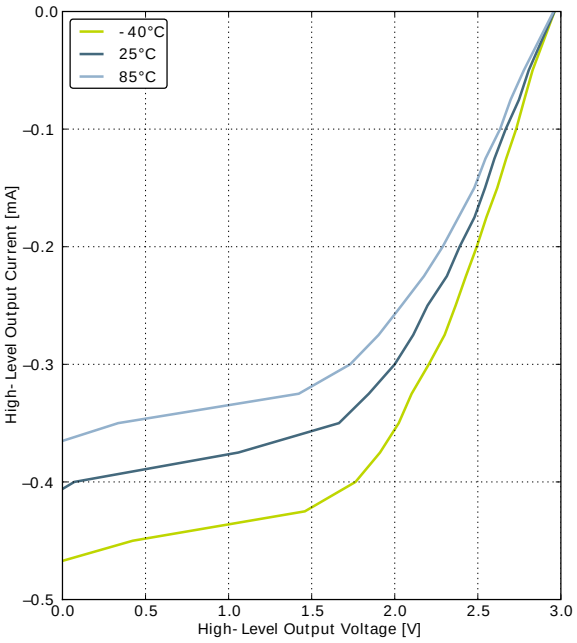



GPIO_Px_CTRL DRIVEMODE = STANDARD

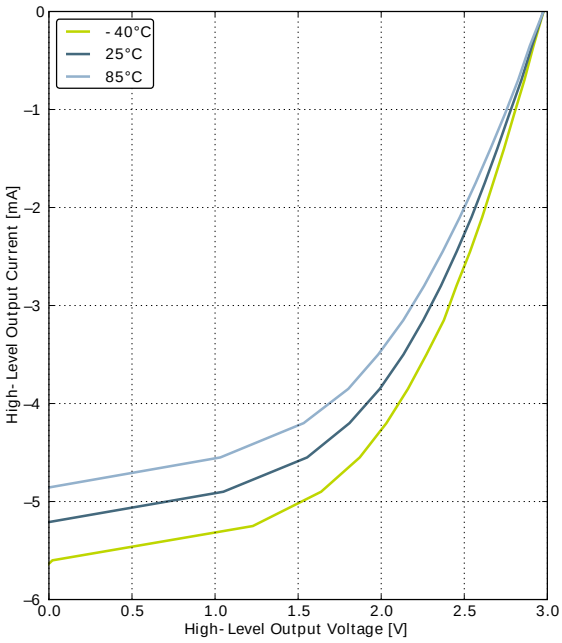



GPIO_Px_CTRL DRIVEMODE = HIGH

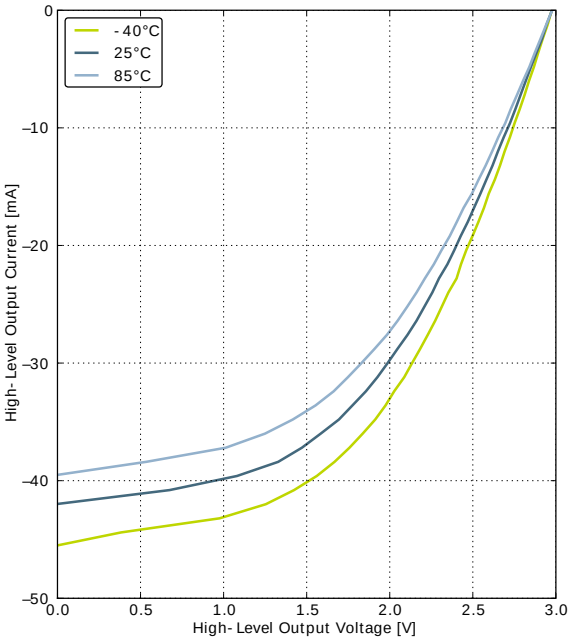
***Figure 3.17. Typical High-Level Output Current, 3V Supply Voltage***



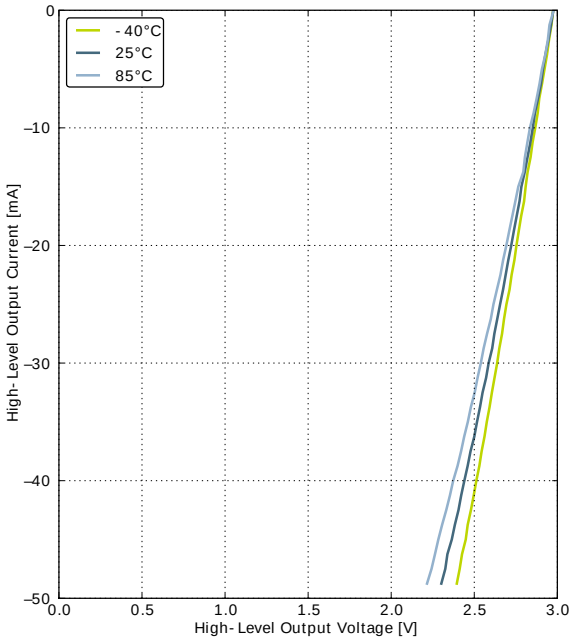

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

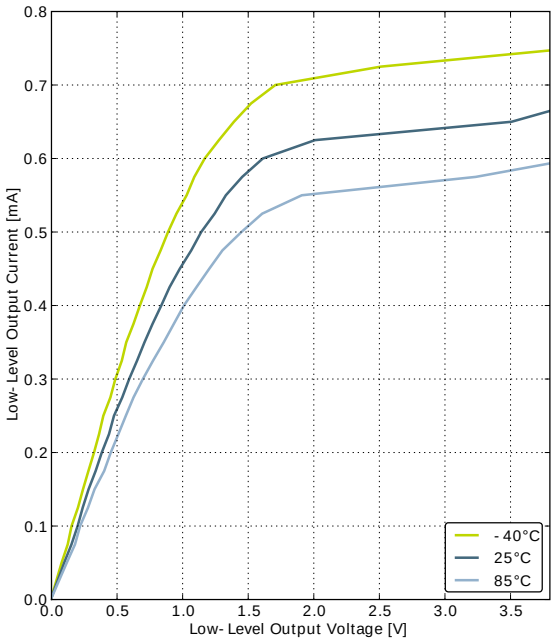



GPIO_Px_CTRL DRIVEMODE = STANDARD

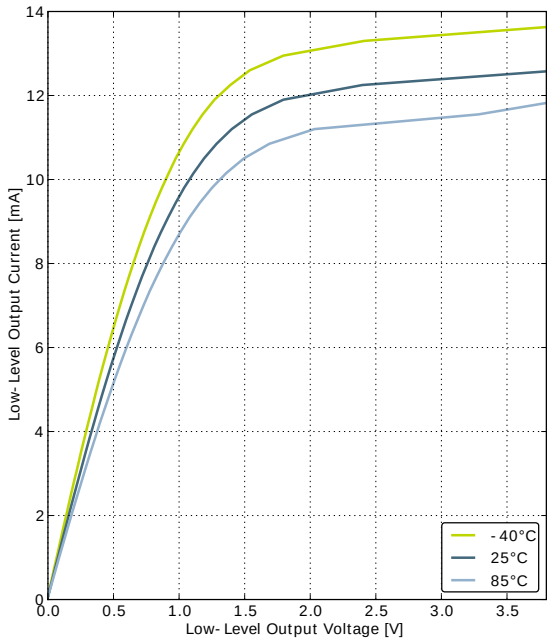



GPIO_Px_CTRL DRIVEMODE = HIGH

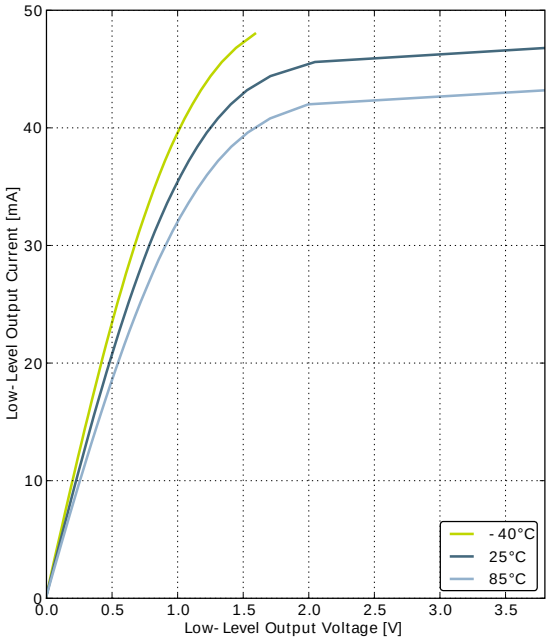
***Figure 3.18. Typical Low-Level Output Current, 3.8V Supply Voltage***



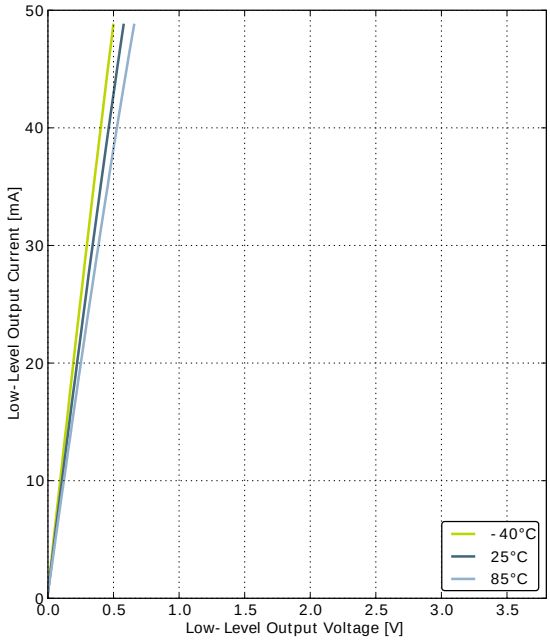

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW

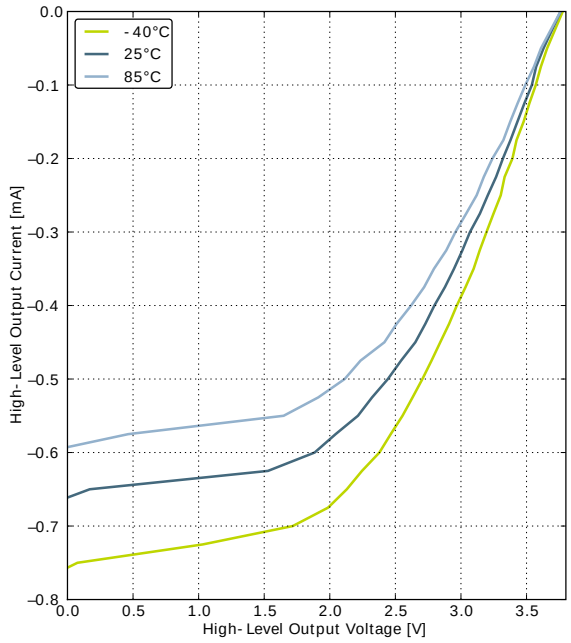



GPIO_Px_CTRL DRIVEMODE = STANDARD

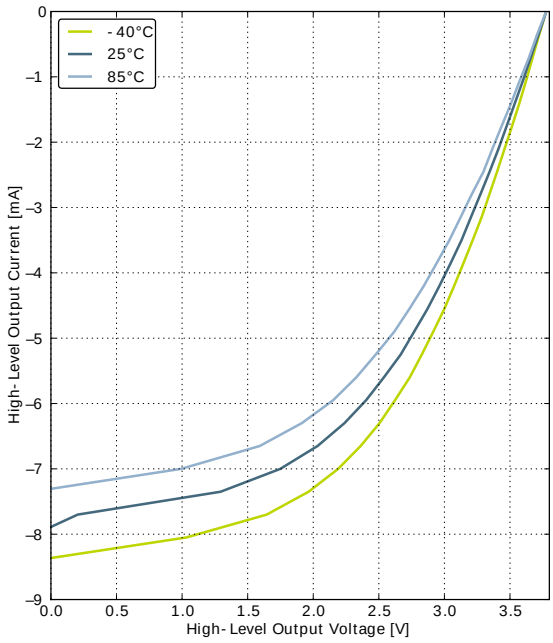



GPIO_Px_CTRL DRIVEMODE = HIGH

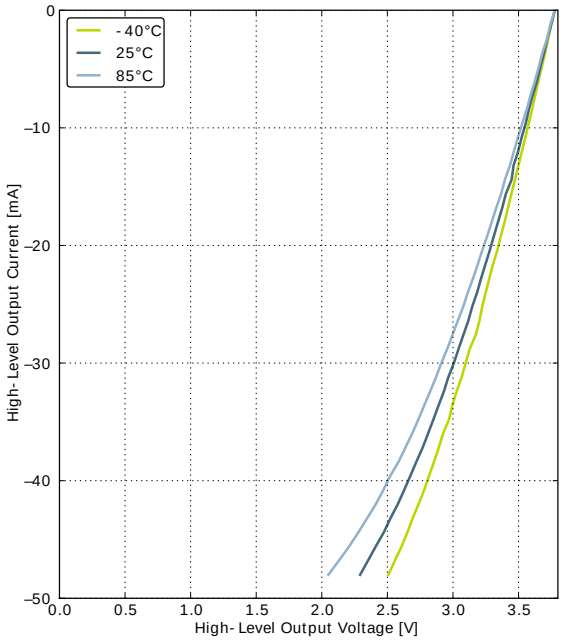
***Figure 3.19. Typical High-Level Output Current, 3.8V Supply Voltage***



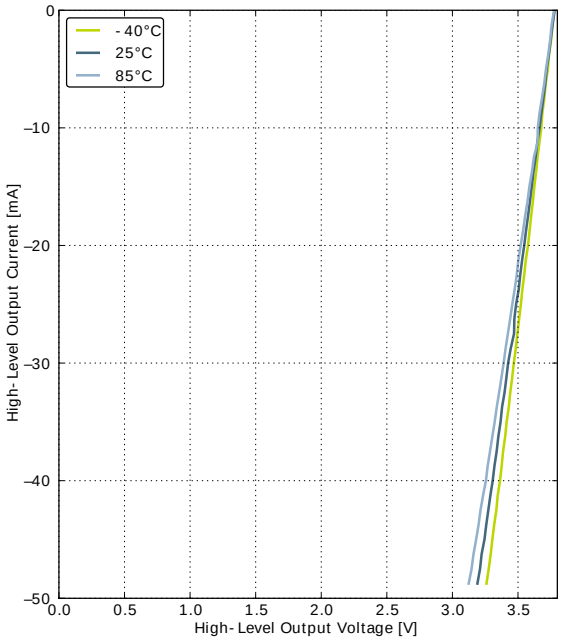

GPIO_Px_CTRL DRIVEMODE = LOWEST




GPIO_Px_CTRL DRIVEMODE = LOW




GPIO_Px_CTRL DRIVEMODE = STANDARD




GPIO_Px_CTRL DRIVEMODE = HIGH

# 3.9 Oscillators

## 3.9.1 LFXO

***Table 3.8. LFXO***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LFXO}$ | Supported nominal crystal frequency | | | 32.768 | | kHz |
| $ESR_{LFXO}$ | Supported crystal equivalent series resistance (ESR) | | | 30 | 120 | kOhm |
| $C_{LFXOL}$ | Supported crystal external load range | | 5 | | 25 | pF |
| $DC_{LFXO}$ | Duty cycle | | 48 | 50 | 53.5 | % |
| $I_{LFXO}$ | Current consumption for core and buffer after startup. | ESR=30 kOhm, $C_L$=10 pF, LFXOBOOST in CMU_CTRL is 1 | | 190 | | nA |
| $t_{LFXO}$ | Start- up time. | ESR=30 kOhm, $C_L$=10 pF, 40% - 60% duty cycle has been reached, LFXOBOOST in CMU_CTRL is 1 | | 400 | | ms |

For safe startup of a given crystal, the energyAware Designer in Simplicity Studio contains a tool to help users configure both load capacitance and software settings for using the LFXO. For details regarding the crystal configuration, the reader is referred to application note "AN0016 EFM32 Oscillator Design Consideration".

## 3.9.2 HFXO

***Table 3.9. HFXO***

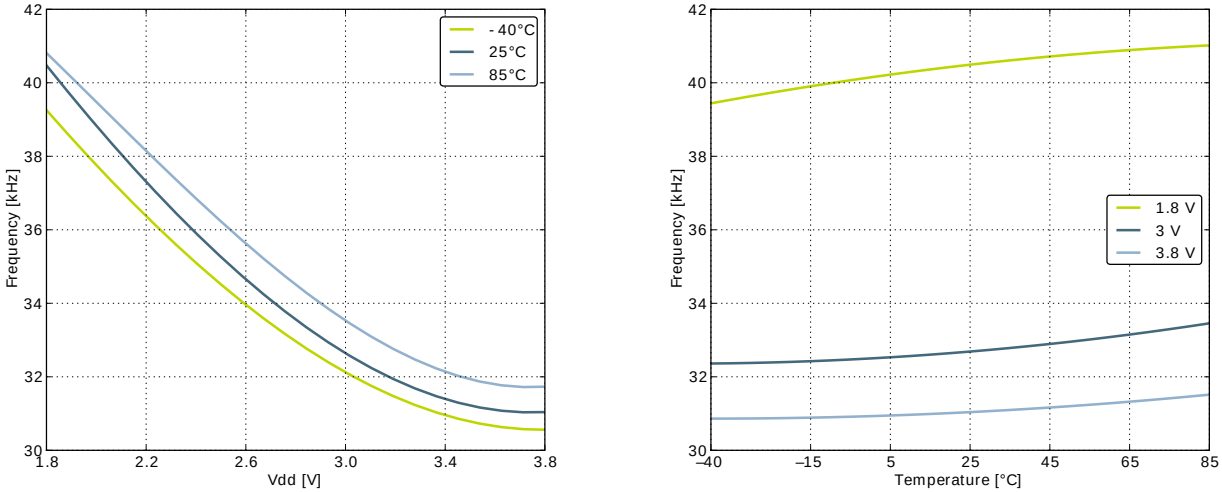
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HFXO}$ | Supported nominal crystal Frequency | | 4 | | 24 | MHz |
| $ESR_{HFXO}$ | Supported crystal equivalent series resistance (ESR) | Crystal frequency 24 MHz | | 30 | 60 | Ohm |
| | | Crystal frequency 4 MHz | | 400 | 1500 | Ohm |
| $g_{mHFXO}$ | The transconductance of the HFXO input transistor at crystal startup | HFXOBOOST in CMU_CTRL equals 0b11 | 20 | | | mS |
| $C_{HFXOL}$ | Supported crystal external load range | | 5 | | 25 | pF |
| $DC_{HFXO}$ | Duty cycle | | 46 | 50 | 54 | % |
| $I_{HFXO}$ | Current consumption for HFXO after startup | 4 MHz: ESR=400 Ohm, $C_L$=20 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 85 | | µA |
| | | 24 MHz: ESR=30 Ohm, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 165 | | µA |
| $t_{HFXO}$ | Startup time | 24 MHz: ESR=30 Ohm, $C_L$=10 pF, HFXOBOOST in CMU_CTRL equals 0b11 | | 400 | | µs |

## 3.9.3 LFRCO

***Table 3.10. LFRCO***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LFRCO}$ | Oscillation frequency , $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | | 32.768 | | kHz |
| $t_{LFRCO}$ | Startup time not including software calibration | | | 150 | | µs |
| $I_{LFRCO}$ | Current consumption | | | 190 | | nA |
| $TUNESTEP_{LFRCO}$ | Frequency step for LSB change in TUNING value | | | 1.5 | | % |

***Figure 3.20. Calibrated LFRCO Frequency vs Temperature and Supply Voltage***



## 3.9.4 HFRCO

***Table 3.11. HFRCO***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 21 MHz frequency band | | 21 | | MHz |
| | | 14 MHz frequency band | | 14 | | MHz |
| | | 11 MHz frequency band | | 11 | | MHz |
| | | 7 MHz frequency band | | 6.6 | | MHz |
| | | 1 MHz frequency band | | 1.2 | | MHz |
| $t_{HFRCO_settling}$ | Settling time after start-up | $f_{HFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $I_{HFRCO}$ | Current consumption | $f_{HFRCO}$ = 21 MHz | | 93 | | µA |
| | | $f_{HFRCO}$ = 14 MHz | | 77 | | µA |
| | | $f_{HFRCO}$ = 11 MHz | | 72 | | µA |
| | | $f_{HFRCO}$ = 6.6 MHz | | 63 | | µA |
| | | $f_{HFRCO}$ = 1.2 MHz | | 22 | | µA |
| $DC_{HFRCO}$ | Duty cycle | $f_{HFRCO}$ = 14 MHz | 48.5 | 50 | 51 | % |
| $TUNESTEP_{H-FRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3 | | % |

***Figure 3.21. Calibrated HFRCO 11 MHz Band Frequency vs Supply Voltage and Temperature***

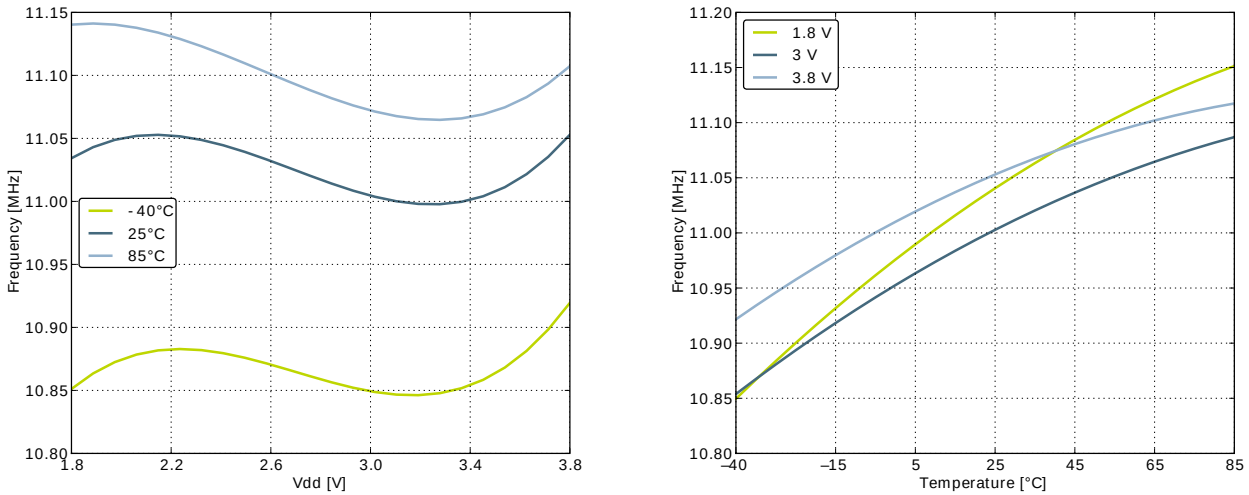


*Figure 3.22. Calibrated HFRCO 14 MHz Band Frequency vs Supply Voltage and Temperature*

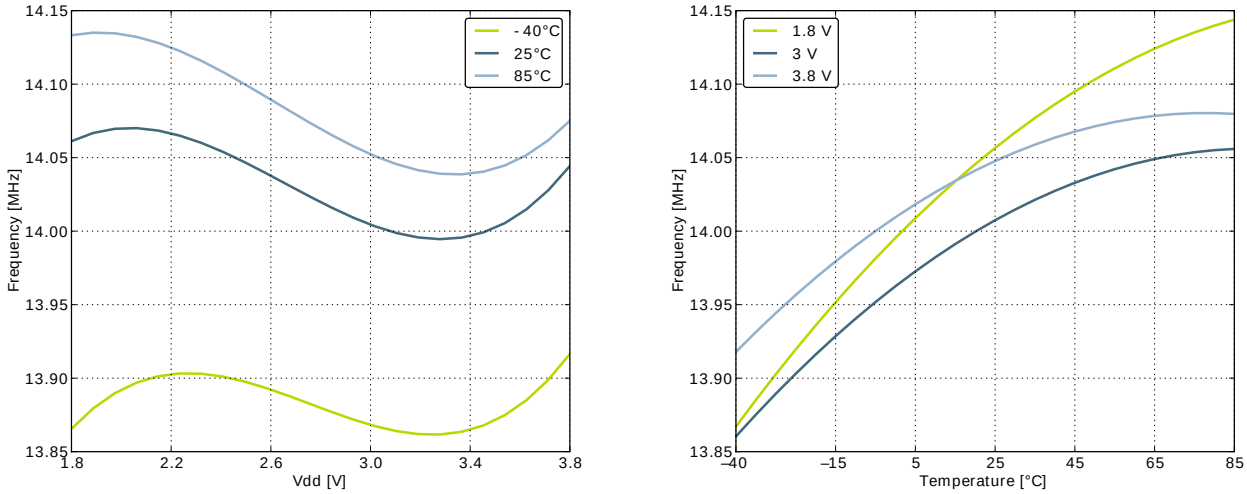
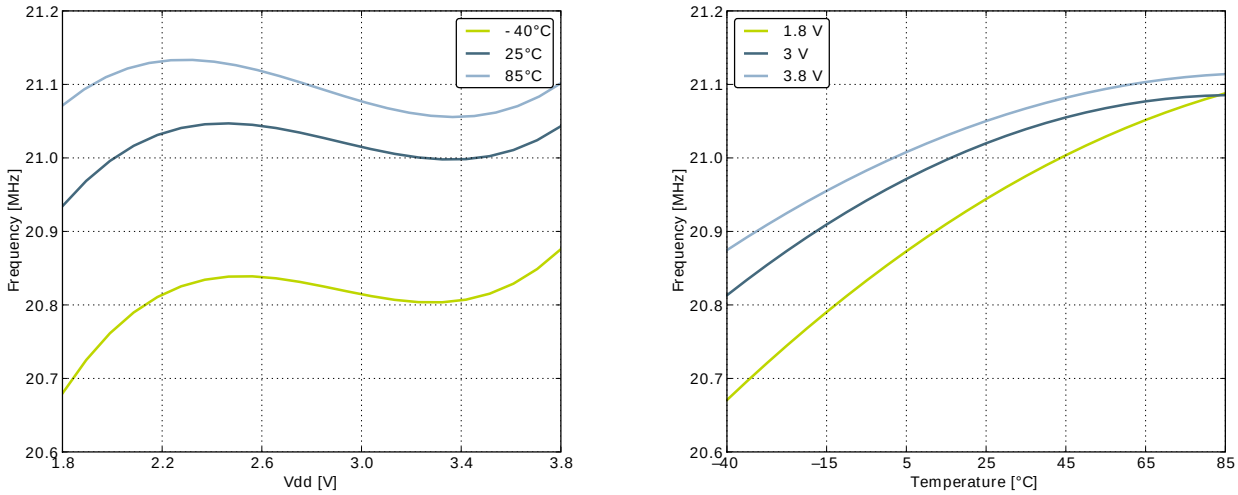



*Figure 3.23. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature*




## 3.9.5 ULFRCO

*Table 3.12. ULFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ULFRCO}$ | Oscillation frequency | 25°C, 3V | 0.8 | | 1.5 | kHz |
| $TC_{ULFRCO}$ | Temperature coefficient | | | 0.05 | | %/°C |
| $VC_{ULFRCO}$ | Supply voltage coefficient | | | -18.2 | | %/V |

# 3.10 Analog Digital Converter (ADC)

*Table 3.13. ADC*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCIN}$ | Input voltage range | Single ended | 0 | | $V_{REF}$ | V |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | Differential | $-V_{REF}/2$ | | $V_{REF}/2$ | V |
| $V_{ADCREFIN}$ | Input range of external reference voltage, single ended and differential | | 1.25 | | $V_{DD}$ | V |
| $V_{ADCREFIN_CH7}$ | Input range of external negative reference voltage on channel 7 | See $V_{ADCREFIN}$ | 0 | | $V_{DD}$ - 1.1 | V |
| $V_{ADCREFIN_CH6}$ | Input range of external positive reference voltage on channel 6 | See $V_{ADCREFIN}$ | 0.625 | | $V_{DD}$ | V |
| $V_{ADCCMIN}$ | Common mode input range | | 0 | | $V_{DD}$ | V |
| $I_{ADCIN}$ | Input current | 2pF sampling capacitors | | <100 | | nA |
| $CMRR_{ADC}$ | Analog input common mode rejection ratio | | | 65 | | dB |
| $I_{ADC}$ | Average active current | 1 MSamples/s, 12 bit, external reference | | 351 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b00 | | 67 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b01 | | 63 | | µA |
| | | 10 kSamples/s 12 bit, internal 1.25 V reference, WARMUPMODE in ADCn_CTRL set to 0b10 | | 64 | | µA |
| $I_{ADCREF}$ | Current consumption of internal voltage reference | Internal voltage reference | | 65 | | µA |
| $C_{ADCIN}$ | Input capacitance | | | 2 | | pF |
| $R_{ADCIN}$ | Input ON resistance | | 1 | | | MOhm |
| $R_{ADCFILT}$ | Input RC filter resistance | | | 10 | | kOhm |
| $C_{ADCFILT}$ | Input RC filter/decoupling capacitance | | | 250 | | fF |
| $f_{ADCCLK}$ | ADC Clock Frequency | | | | 13 | MHz |
| $t_{ADCCONV}$ | Conversion time | 6 bit | 7 | | | ADCCLK Cycles |
| | | 8 bit | 11 | | | ADCCLK Cycles |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 12 bit | 13 | | | ADC-CLK Cycles |
| $t_{ADCACQ}$ | Acquisition time | Programmable | 1 | | 256 | ADC-CLK Cycles |
| $t_{ADCACQVDD3}$ | Required acquisition time for VDD/3 reference | | 2 | | | µs |
| $t_{ADCSTART}$ | Startup time of reference generator and ADC core in NORMAL mode | | | 5 | | µs |
| | Startup time of reference generator and ADC core in KEEPADCWARM mode | | | 1 | | µs |
| $SNR_{ADC}$ | Signal to Noise Ratio (SNR) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 59 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 63 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 65 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 60 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 65 | | dB |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 54 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 67 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $2xV_{DD}$ reference | | 69 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 62 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 67 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 69 | | dB |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 70 | | dB |
| $SINAD_{ADC}$ | SIgnal-to-Noise And Distortion-ratio (SINAD) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 58 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 62 | | dB |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 64 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 60 | | dB |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 64 | | dB |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 54 | | dB |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 66 | | dB |
| | | 1 MSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 68 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 61 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 65 | | dB |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 63 | | dB |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 66 | | dB |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 68 | | dB |
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 69 | | dB |
| $SFDR_{ADC}$ | Spurious-Free Dynamic Range (SFDR) | 1 MSamples/s, 12 bit, single ended, internal 1.25V reference | | 64 | | dBc |
| | | 1 MSamples/s, 12 bit, single ended, internal 2.5V reference | | 76 | | dBc |
| | | 1 MSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 73 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 1.25V reference | | 66 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, internal 2.5V reference | | 77 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, $V_{DD}$ reference | | 76 | | dBc |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | 1 MSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 75 | | dBc |
| | | 1 MSamples/s, 12 bit, differential, 5V reference | | 69 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 75 | | dBc |
| | | 200 kSamples/s, 12 bit, single ended, $V_{DD}$ reference | | 76 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 1.25V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, internal 2.5V reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 5V reference | | 78 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, $V_{DD}$ reference | | 79 | | dBc |
| | | 200 kSamples/s, 12 bit, differential, 2x$V_{DD}$ reference | | 79 | | dBc |
| $V_{ADCOFFSET}$ | Offset voltage | After calibration, single ended | | 0.3 | | mV |
| | | After calibration, differential | | 0.3 | | mV |
| $TGRAD_{ADCTH}$ | Thermometer output gradient | | | -1.92 | | mV/°C |
| | | | | -6.3 | | ADC Codes/°C |
| $DNL_{ADC}$ | Differential non-linearity (DNL) | | | ±0.7 | | LSB |
| $INL_{ADC}$ | Integral non-linearity (INL), End point method | | | ±1.2 | | LSB |
| $MC_{ADC}$ | No missing codes | | 11.999[1] | 12 | | bits |

[1]On the average every ADC will have one missing code, most likely to appear around 2048 +/- n*512 where n can be a value in the set {-3, -2, -1, 1, 2, 3}. There will be no missing code around 2048, and in spite of the missing code the ADC will be monotonic at all times so that a response to a slowly increasing input will always be a slowly increasing output. Around the one code that is missing, the neighbour codes will look wider in the DNL plot. The spectra will show spurs on the level of -78dBc for a full scale input for chips that have the missing code issue.

The integral non-linearity (INL) and differential non-linearity parameters are explained in Figure 3.24 (p. 33) and Figure 3.25 (p. 33) , respectively.

***Figure 3.24. Integral Non-Linearity (INL)***

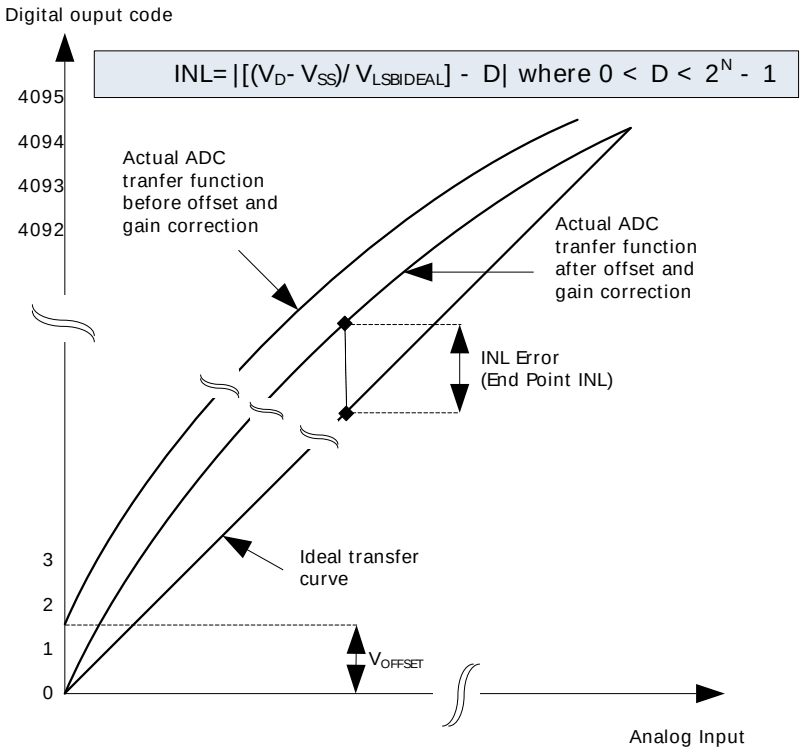
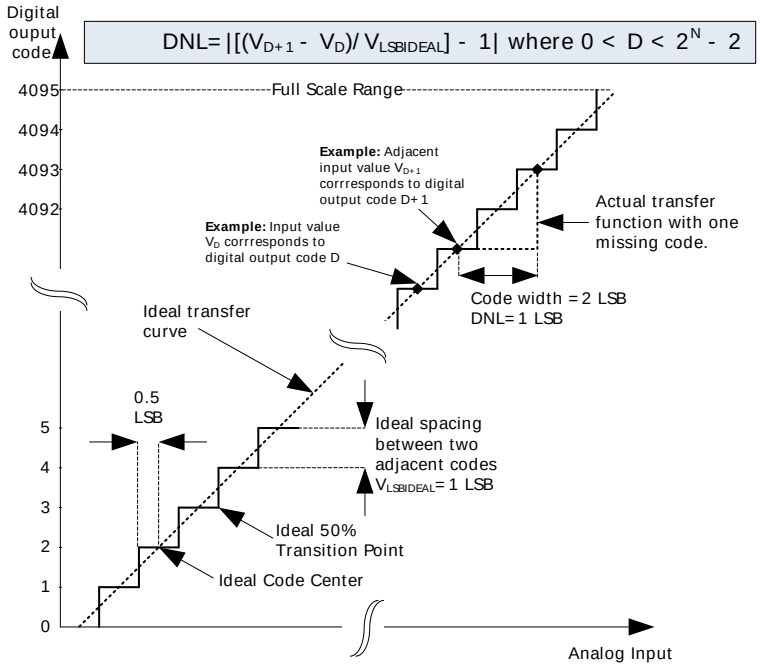
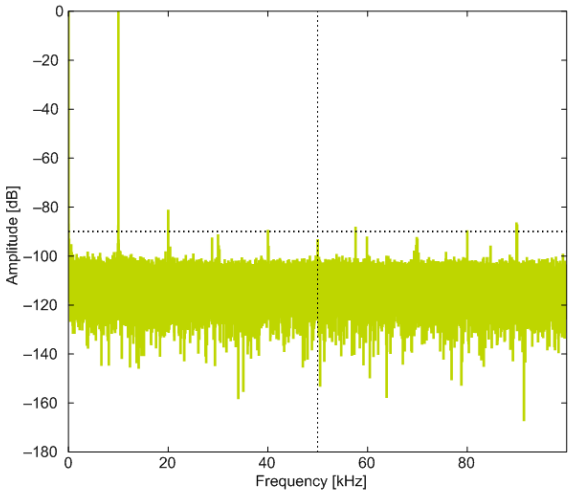



***Figure 3.25. Differential Non-Linearity (DNL)***

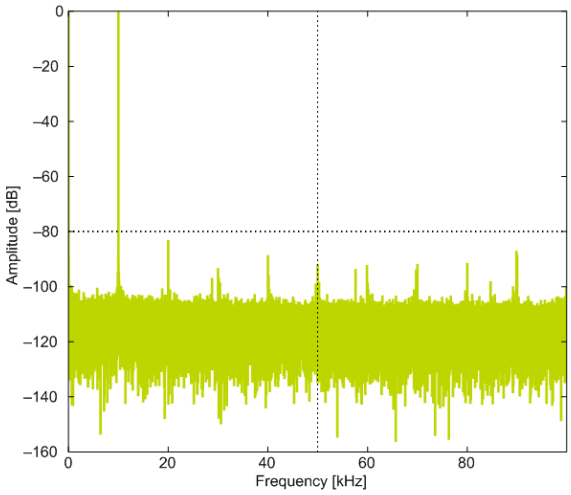


## 3.10.1 Typical performance

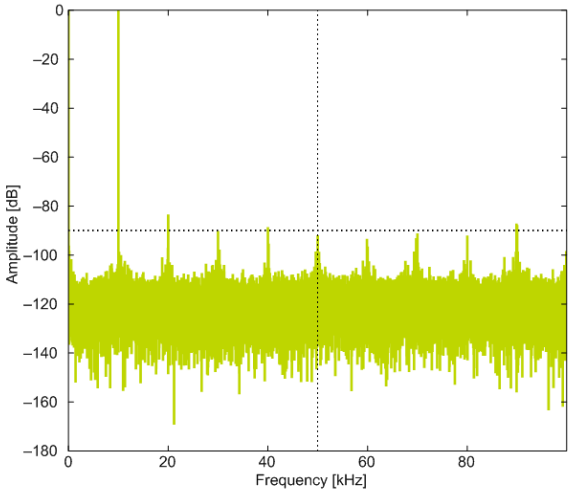
***Figure 3.26. ADC Frequency Spectrum, Vdd = 3V, Temp = 25°C***



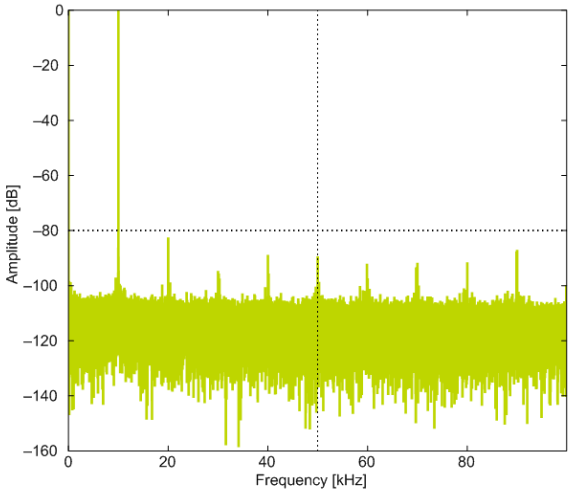

1.25V Reference



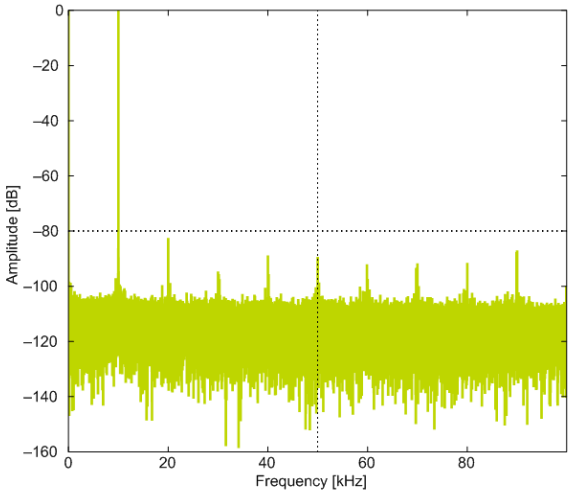

2.5V Reference




2XVDDVSS Reference

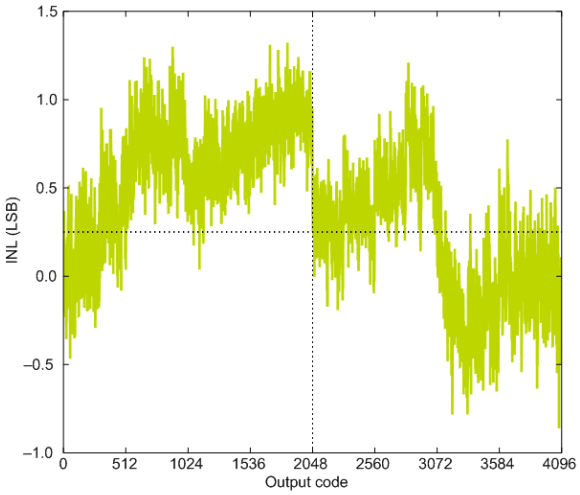



5VDIFF Reference

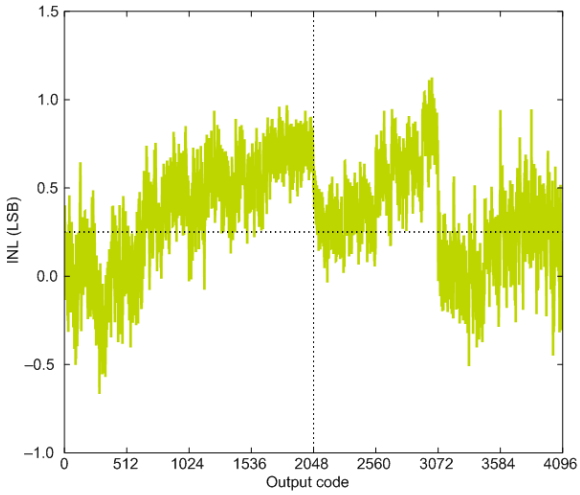



VDD Reference

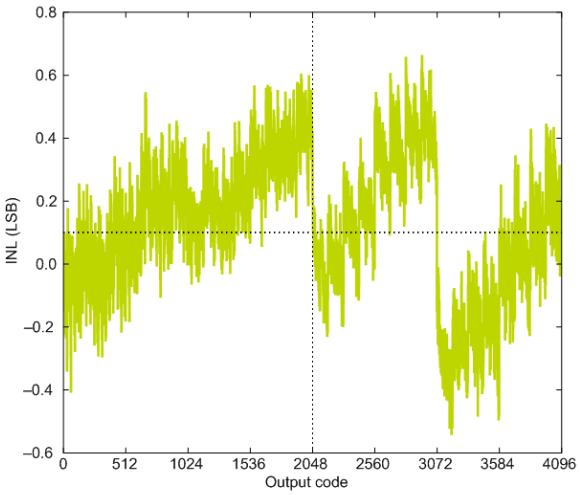
***Figure 3.27. ADC Integral Linearity Error vs Code, Vdd = 3V, Temp = 25°C***



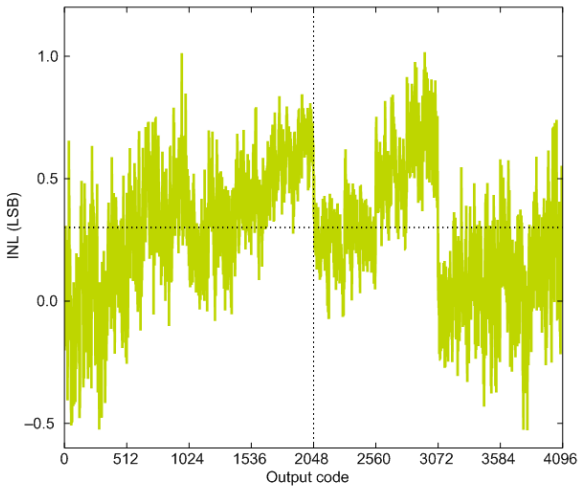

1.25V Reference



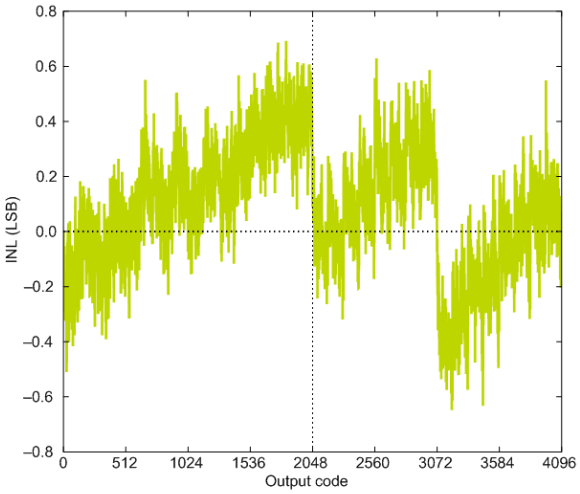

2.5V Reference




2XVDDVSS Reference

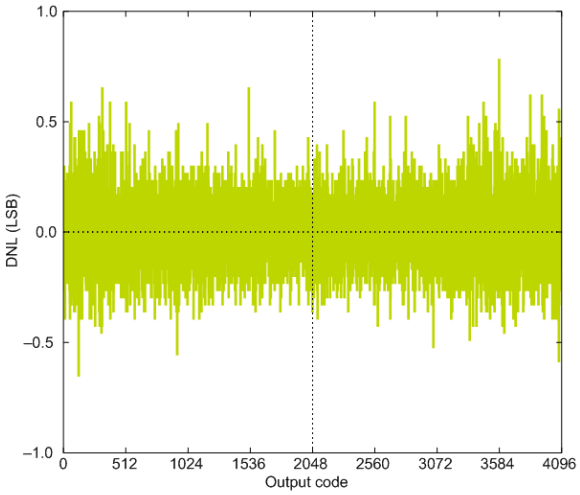



5VDIFF Reference

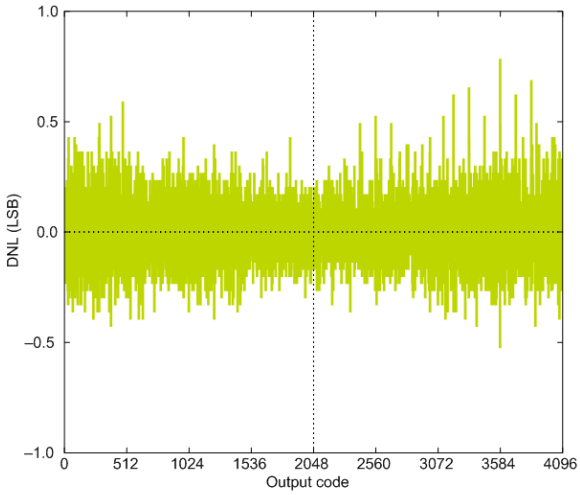



VDD Reference

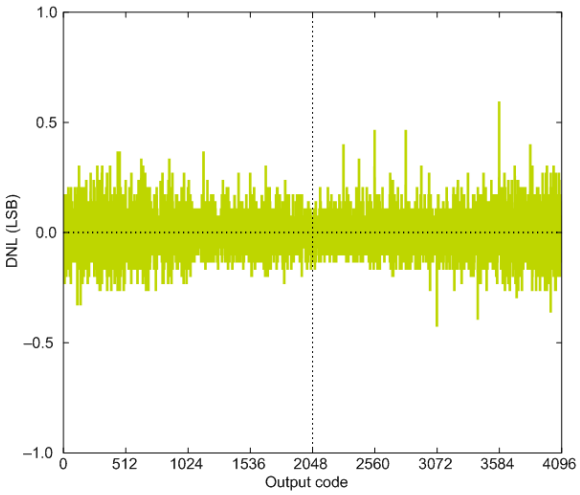
***Figure 3.28. ADC Differential Linearity Error vs Code, Vdd = 3V, Temp = 25°C***



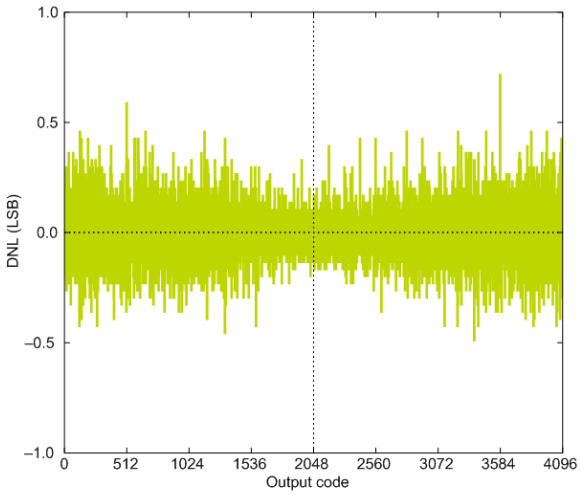

1.25V Reference



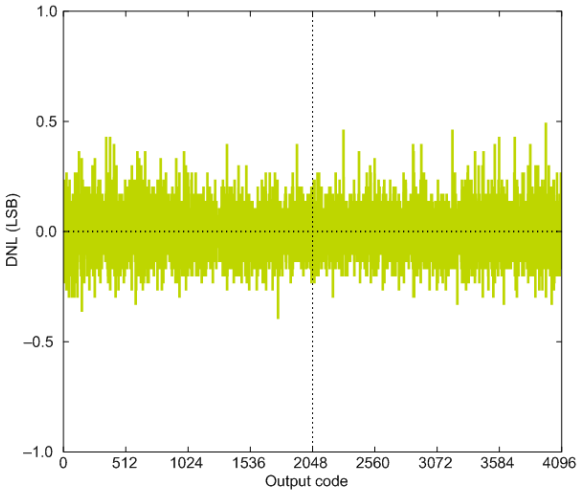

2.5V Reference




2XVDDVSS Reference

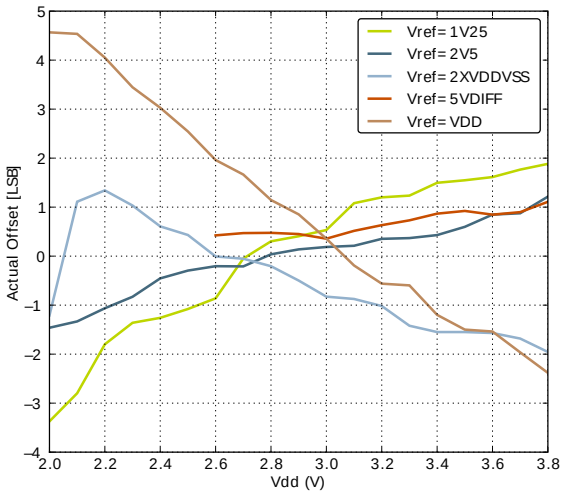



5VDIFF Reference

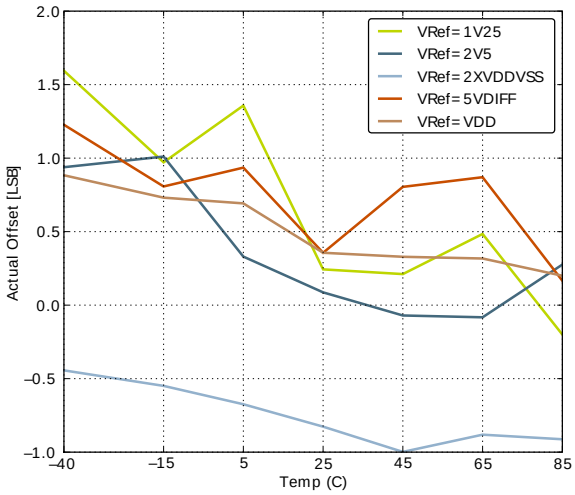



VDD Reference

***Figure 3.29. ADC Absolute Offset, Common Mode = Vdd /2***

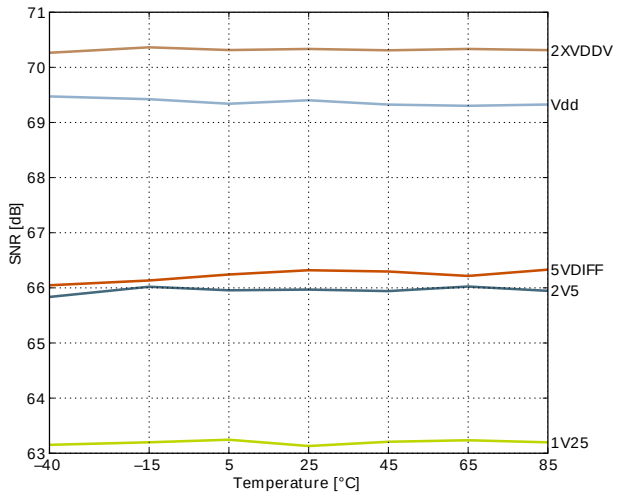



Offset vs Supply Voltage, Temp = 25°C

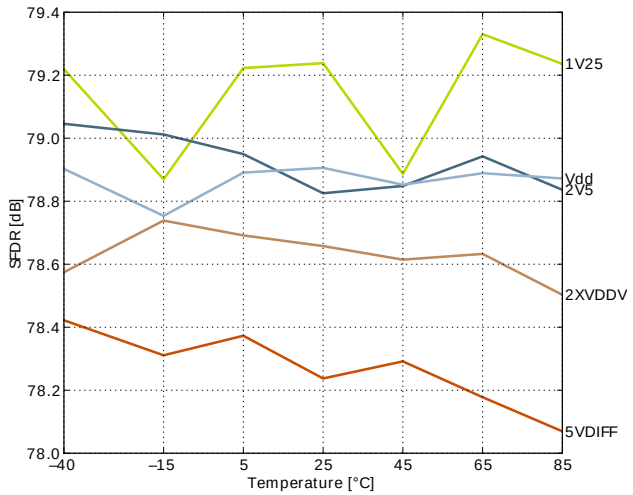



Offset vs Temperature, Vdd = 3V

***Figure 3.30. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V***

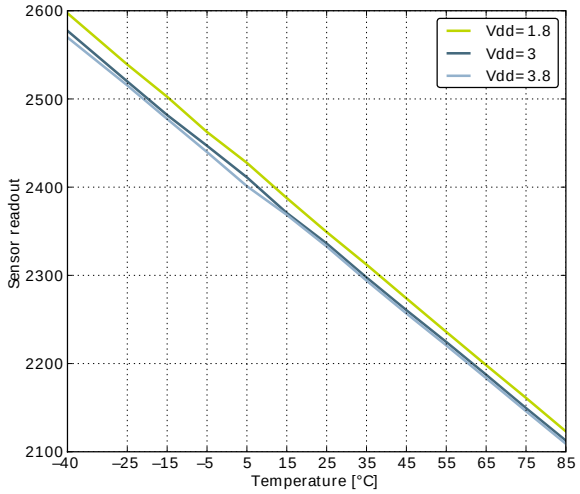



Signal to Noise Ratio (SNR)




Spurious-Free Dynamic Range (SFDR)

***Figure 3.31. ADC Temperature sensor readout***




# 3.11 Current Digital Analog Converter (IDAC)

***Table 3.14. IDAC Range 0 Source***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 11.7 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 0.84 | | µA |
| $I_{STEP}$ | Step size | | | 0.049 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC_OUT}$ = $V_{DD}$ - 100mV | | 0.73 | | % |
| $TC_{IDAC}$ | Temperature coefficient | V=3.0V, STEPSEL=0x10 | | 0.3 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 11.7 | | nA/V |

***Table 3.15. IDAC Range 0 Sink***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 13.7 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 0.84 | | µA |
| $I_{STEP}$ | Step size | | | 0.050 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC_OUT}$ = 200 mV | | 0.16 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.2 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 12.5 | | nA/V |

### Table 3.16. IDAC Range 1 Source

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 13.0 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 3.17 | | µA |
| $I_{STEP}$ | Step size | | | 0.097 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC_OUT}$ = $V_{DD}$ - 100mV | | 0.79 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.7 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 38.4 | | nA/V |

### Table 3.17. IDAC Range 1 Sink

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 17.9 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 3.18 | | µA |
| $I_{STEP}$ | Step size | | | 0.098 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC_OUT}$ = 200 mV | | 0.20 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 0.7 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 40.9 | | nA/V |

### Table 3.18. IDAC Range 2 Source

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 16.2 | | µA |
| | | Duty-cycled | | TBD | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | TBD | | µA |
| $I_{STEP}$ | Step size | | | 0.493 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC_OUT}$ = $V_{DD}$ - 100mV | | 1.26 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 2.8 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 96.6 | | nA/V |

### Table 3.19. IDAC Range 2 Sink

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 28.4 | | µA |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 8.44 | | µA |
| $I_{STEP}$ | Step size | | | 0.495 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC_OUT}$ = 200 mV | | 0.55 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 2.8 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 94.4 | | nA/V |

***Table 3.20. IDAC Range 3 Source***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 18.3 | | µA |
| | | Duty-cycled | | 10 | | nA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 34.03 | | µA |
| $I_{STEP}$ | Step size | | | 1.996 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC_OUT}$ = $V_{DD}$ - 100 mV | | 3.18 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 10.9 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 159.5 | | nA/V |

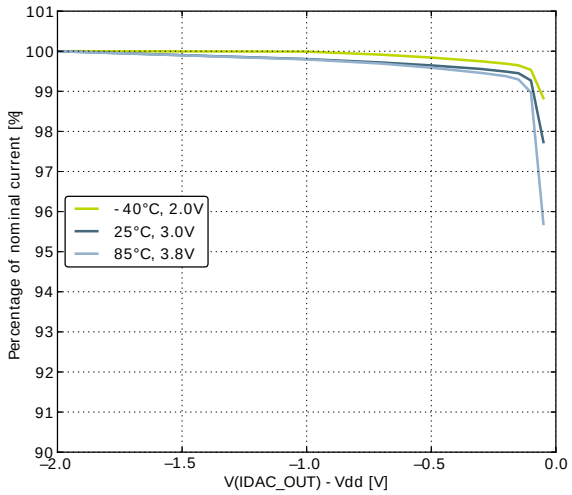
***Table 3.21. IDAC Range 3 Sink***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{IDAC}$ | Active current with STEPSEL=0x10 | EM0, default settings | | 62.9 | | µA |
| $I_{0x10}$ | Nominal IDAC output current with STEPSEL=0x10 | | | 34.16 | | µA |
| $I_{STEP}$ | Step size | | | 2.003 | | µA |
| $I_D$ | Current drop at high impedance load | $V_{IDAC_OUT}$ = 200 mV | | 1.65 | | % |
| $TC_{IDAC}$ | Temperature coefficient | $V_{DD}$ = 3.0 V, STEPSEL=0x10 | | 10.9 | | nA/°C |
| $VC_{IDAC}$ | Voltage coefficient | T = 25 °C, STEPSEL=0x10 | | 148.6 | | nA/V |

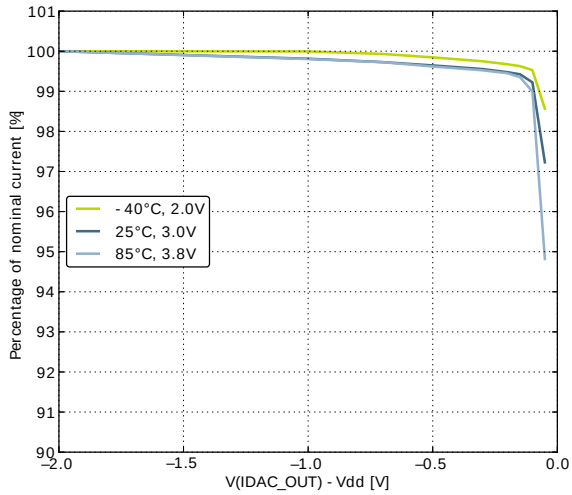
***Table 3.22. IDAC***

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{IDACSTART}$ | Start-up time, from enabled to output settled | | 40 | | µS |

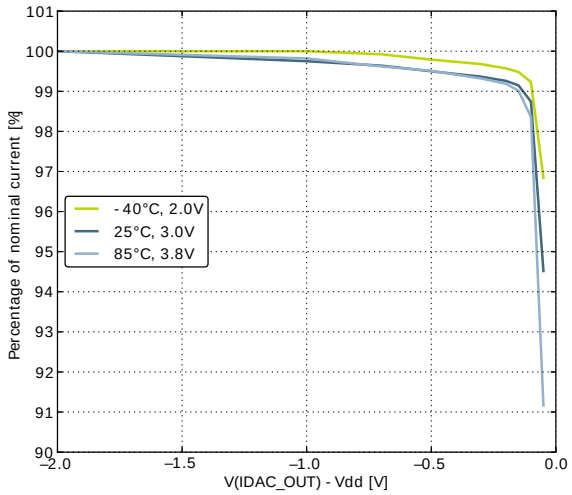
***Figure 3.32. IDAC Source Current as a function of voltage on IDAC_OUT***



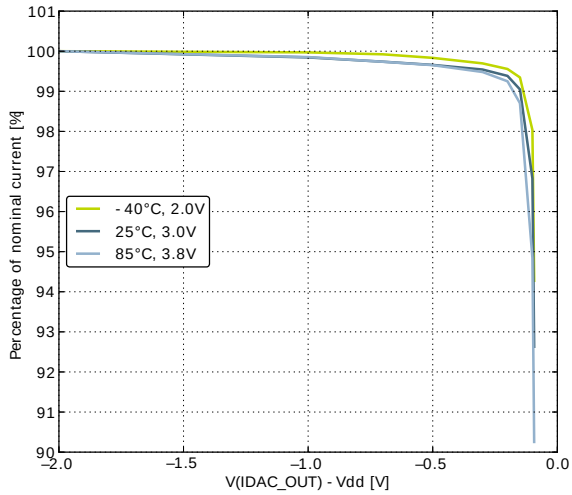

Range 0




Range 1

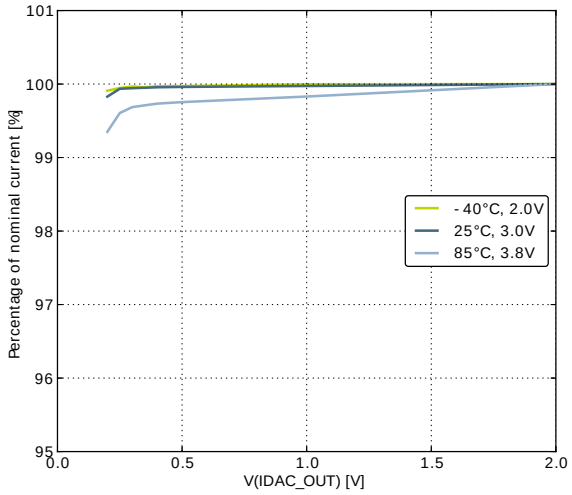



Range 2

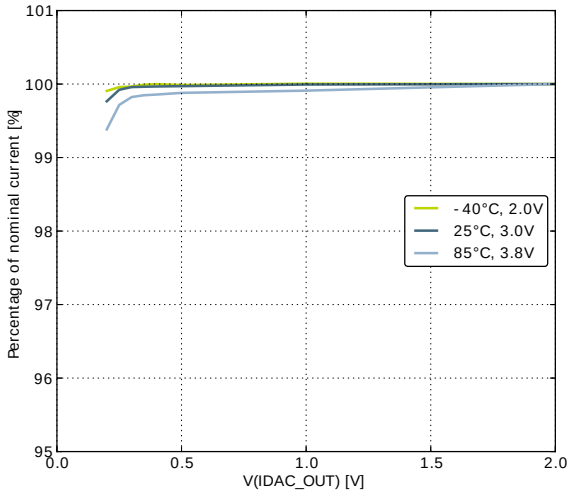



Range 3

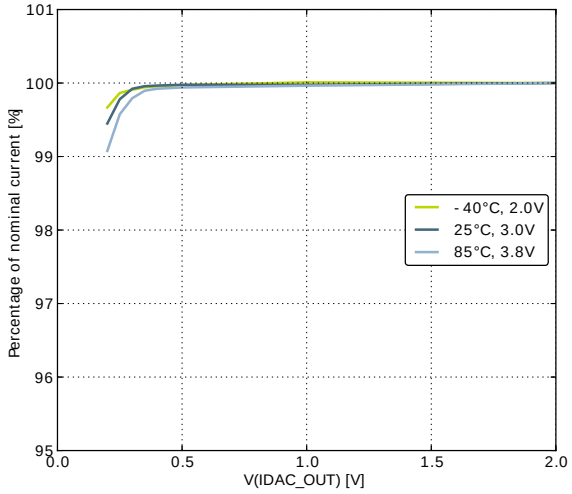
***Figure 3.33. IDAC Sink Current as a function of voltage from IDAC_OUT***



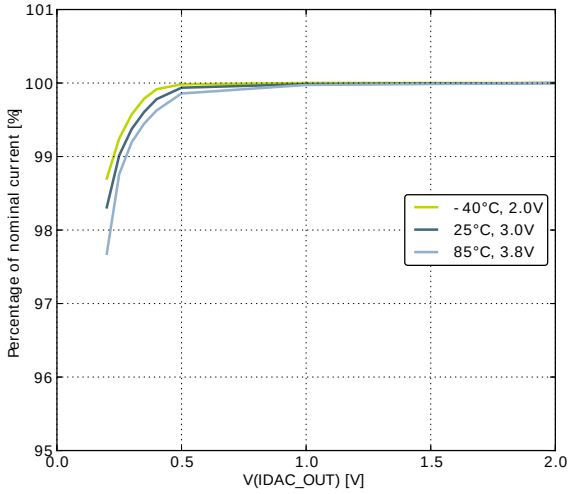

Range 0




Range 1

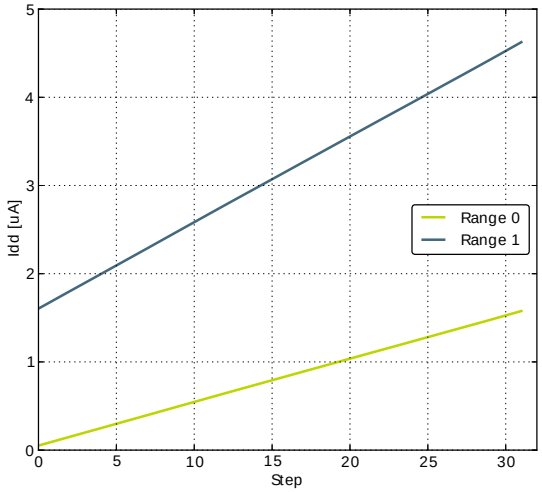


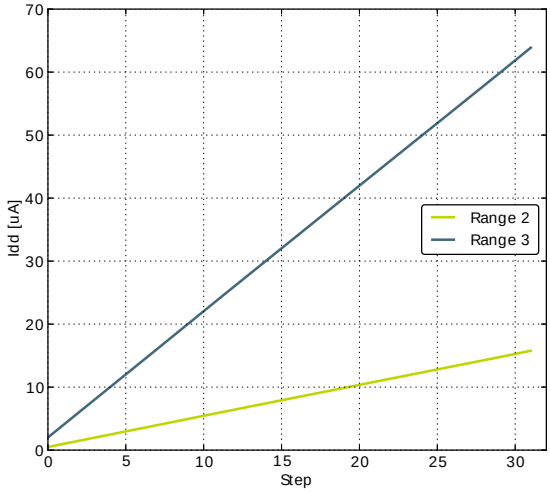

Range 2




Range 3

***Figure 3.34. IDAC linearity***



# 3.12 Analog Comparator (ACMP)

***Table 3.23. ACMP***

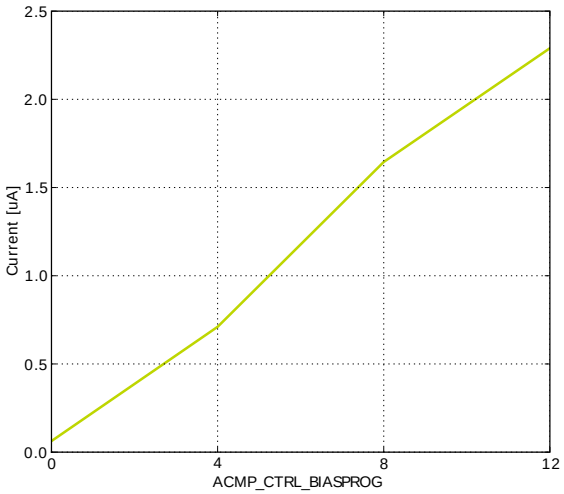
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ACMPIN}$ | Input voltage range | | 0 | | $V_{DD}$ | V |
| $V_{ACMPCM}$ | ACMP Common Mode voltage range | | 0 | | $V_{DD}$ | V |
| $I_{ACMP}$ | Active current | BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register | | 0.1 | | µA |
| | | BIASPROG=0b1111, FULLBIAS=0 and HALFBIAS=0 in ACMPn_CTRL register | | 2.87 | | µA |
| | | BIASPROG=0b1111, FULLBIAS=1 and HALFBIAS=0 in ACMPn_CTRL register | | 195 | | µA |
| $I_{ACMPREF}$ | Current consumption of internal voltage reference | Internal voltage reference off. Using external voltage reference | | 0 | | µA |
| | | Internal voltage reference | | 5 | | µA |
| $V_{ACMPOFFSET}$ | Offset voltage | Single ended | | 10 | | mV |
| | | Differential | | 10 | | mV |
| $V_{ACMPHYST}$ | ACMP hysteresis | Programmable | | 17 | | mV |
| $R_{CSRES}$ | Capacitive Sense Internal Resistance | CSRESSEL=0b00 in ACMPn_INPUTSEL | | 39 | | kOhm |
| | | CSRESSEL=0b01 in ACMPn_INPUTSEL | | 71 | | kOhm |
| | | CSRESSEL=0b10 in ACMPn_INPUTSEL | | 104 | | kOhm |
| | | CSRESSEL=0b11 in ACMPn_INPUTSEL | | 136 | | kOhm |
| $t_{ACMPSTART}$ | Startup time | | | | 10 | µs |

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in Equation 3.1 (p. 43) . $I_{ACMPREF}$ is zero if an external voltage reference is used.

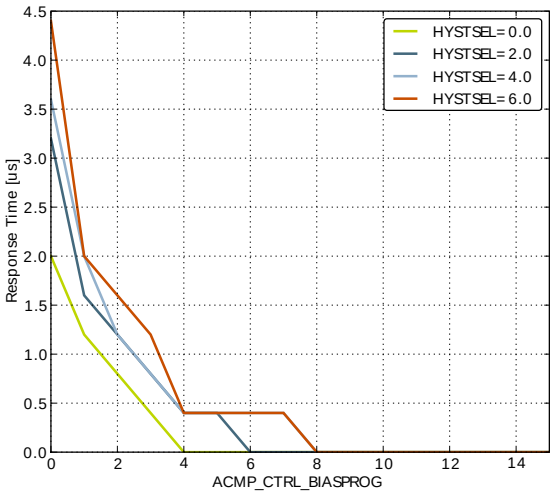
***Total ACMP Active Current***

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF} \quad (3.1)$$

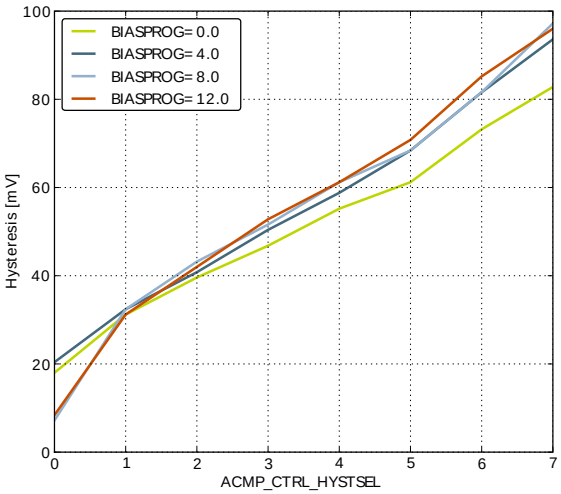
***Figure 3.35. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1***




Current consumption, HYSTSEL = 4




Response time




Hysteresis

# 3.13 Voltage Comparator (VCMP)

***Table 3.24. VCMP***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{VCMPIN}$ | Input voltage range | | | $V_{DD}$ | | V |
| $V_{VCMPCM}$ | VCMP Common Mode voltage range | | | $V_{DD}$ | | V |
| $I_{VCMP}$ | Active current | BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register | | 0.1 | | µA |
| | | BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0. | | 14.7 | | µA |
| $t_{VCMPREF}$ | Startup time reference generator | NORMAL | | 10 | | µs |
| $V_{VCMPOFFSET}$ | Offset voltage | Single ended | | 10 | | mV |
| | | Differential | | 10 | | mV |
| $V_{VCMPHYST}$ | VCMP hysteresis | | | 17 | | mV |
| $t_{VCMPSTART}$ | Startup time | | | | 10 | µs |

The $V_{DD}$ trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

***VCMP Trigger Level as a Function of Level Setting***

$$V_{DD\ Trigger\ Level}=1.667V+0.034 \times TRIGLEVEL \quad (3.2)$$

# 3.14 I2C

***Table 3.25. I2C Standard-mode (Sm)***

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 100[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 4.7 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 4.0 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 250 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | 3450[2,3] | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 4.7 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 4.0 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 4.0 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | | | µs |

[1]For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32ZG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 5).

### Table 3.26. I2C Fast-mode (Fm)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 400[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 1.3 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 0.6 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 100 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | 900[2,3] | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 0.6 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 0.6 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 0.6 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 1.3 | | | µs |

[1]For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32ZG Reference Manual.
[2]The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL ($t_{LOW}$).
[3]When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*$10^{-9}$ [s] * $f_{HFPERCLK}$ [Hz]) - 5).

### Table 3.27. I2C Fast-mode Plus (Fm+)

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCL}$ | SCL clock frequency | 0 | | 1000[1] | kHz |
| $t_{LOW}$ | SCL clock low time | 0.5 | | | µs |
| $t_{HIGH}$ | SCL clock high time | 0.26 | | | µs |
| $t_{SU,DAT}$ | SDA set-up time | 50 | | | ns |
| $t_{HD,DAT}$ | SDA hold time | 8 | | | ns |
| $t_{SU,STA}$ | Repeated START condition set-up time | 0.26 | | | µs |
| $t_{HD,STA}$ | (Repeated) START condition hold time | 0.26 | | | µs |
| $t_{SU,STO}$ | STOP condition set-up time | 0.26 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 0.5 | | | µs |

[1]For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32ZG Reference Manual.

## 3.15 Digital Peripherals

### Table 3.28. Digital Peripherals

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{USART}$ | USART current | USART idle current, clock enabled | | 7.5 | | µA/MHz |
| $I_{I2C}$ | I2C current | I2C idle current, clock enabled | | 6.25 | | µA/MHz |
| $I_{TIMER}$ | TIMER current | TIMER_0 idle current, clock enabled | | 8.75 | | µA/MHz |
| $I_{PCNT}$ | PCNT current | PCNT idle current, clock enabled | | 100 | | nA |
| $I_{RTC}$ | RTC current | RTC idle current, clock enabled | | 100 | | nA |
| $I_{AES}$ | AES current | AES idle current, clock enabled | | 2.5 | | µA/MHz |

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{GPIO}$ | GPIO current | GPIO idle current, clock enabled | | 5.31 | | µA/MHz |
| $I_{PRS}$ | PRS current | PRS idle current | | 2,81 | | µA/MHz |

# 4 Pinout and Package

***Note***

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32ZG110.

## 4.1 Pinout

The *EFM32ZG110* pinout is shown in Figure 4.1 (p. 48) and Table 4.1 (p. 48). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

***Figure 4.1. EFM32ZG110 Pinout (top view, not to scale)***

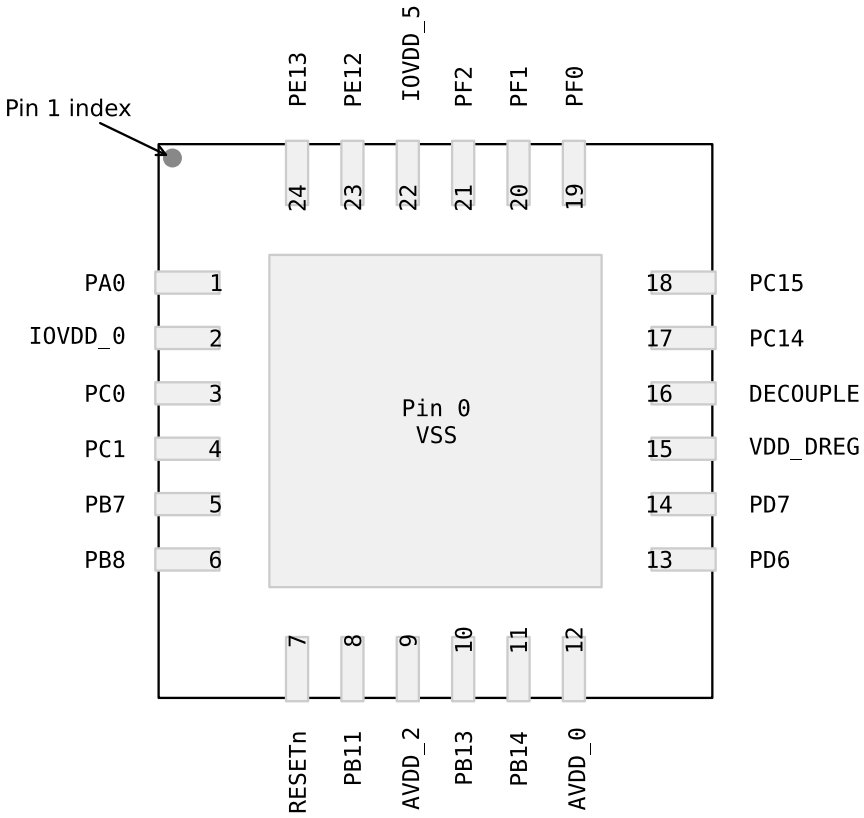



***Table 4.1. Device Pinout***

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground | | | |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 | PRS_CH0 #0 |

| QFN24 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| | | | | I2C0_SDA #0 | GPIO_EM4WU0 |
| 2 | IOVDD_0 | Digital IO power supply 0. | | | |
| 3 | PC0 | ACMP0_CH0 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US1_TX #0<br>I2C0_SDA #4 | PRS_CH2 #0 |
| 4 | PC1 | ACMP0_CH1 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US1_RX #0<br>I2C0_SCL #4 | PRS_CH3 #0 |
| 5 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US1_CLK #0 | |
| 6 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US1_CS #0 | |
| 7 | RESETn | Reset input, active low.<br>To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 8 | PB11 | IDAC0_OUT | TIM1_CC2 #3 | | |
| 9 | AVDD_2 | Analog power supply 2. | | | |
| 10 | PB13 | HFXTAL_P | | LEU0_TX #1 | |
| 11 | PB14 | HFXTAL_N | | LEU0_RX #1 | |
| 12 | AVDD_0 | Analog power supply 0. | | | |
| 13 | PD6 | ADC0_CH6 | TIM1_CC0 #4<br>PCNT0_S0IN #3 | US1_RX #2/3<br>I2C0_SDA #1 | ACMP0_O #2 |
| 14 | PD7 | ADC0_CH7 | TIM1_CC1 #4<br>PCNT0_S1IN #3 | US1_TX #2/3<br>I2C0_SCL #1 | CMU_CLK0 #2 |
| 15 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 16 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 17 | PC14 | | TIM1_CC1 #0<br>PCNT0_S1IN #0 | US1_CS #3 | PRS_CH0 #2 |
| 18 | PC15 | | TIM1_CC2 #0 | US1_CLK #3 | PRS_CH1 #2 |
| 19 | PF0 | | TIM0_CC0 #5 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0<br>BOOT_TX |
| 20 | PF1 | | TIM0_CC1 #5 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0<br>GPIO_EM4WU3<br>BOOT_RX |
| 21 | PF2 | | TIM0_CC2 #5 | LEU0_TX #4 | GPIO_EM4WU4 |
| 22 | IOVDD_5 | Digital IO power supply 5. | | | |
| 23 | PE12 | | TIM1_CC2 #1 | I2C0_SDA #6 | CMU_CLK1 #2 |
| 24 | PE13 | | | I2C0_SCL #6 | ACMP0_O #0<br>GPIO_EM4WU5 |

## 4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in Table 4.2 (p. 50). The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

***Note***

Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

### Table 4.2. Alternate functionality overview

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PF1 | | | | | | | Bootloader RX |
| BOOT_TX | PF0 | | | | | | | Bootloader TX |
| CMU_CLK0 | | | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | | | PE12 | | | | | Clock Management Unit, clock output number 1. |
| DBG_SWCLK | PF0 | | | | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | | | | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | | PD7 | | | PC1 | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | | | PC0 | PF0 | PE12 | I2C0 Serial Data input / output. |
| IDAC0_OUT | PB11 | | | | | | | IDAC0 output |
| LEU0_RX | | PB14 | | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | | PB13 | | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | | | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PRS_CH0 | PA0 | | PC14 | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | | | PC15 | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | | | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | | | | | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | | | | | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM1_CC0 | | | | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | | | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | | PB11 | | | | Timer 1 Capture Compare input / output channel 2. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US1_CLK | PB7 | | PF0 | PC15 | | | | USART1 clock input / output. |
| US1_CS | PB8 | | PF1 | PC14 | | | | USART1 chip select input / output. |
| US1_RX | PC1 | | PD6 | PD6 | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | | PD7 | PD7 | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |

## 4.3 GPIO Pinout Overview

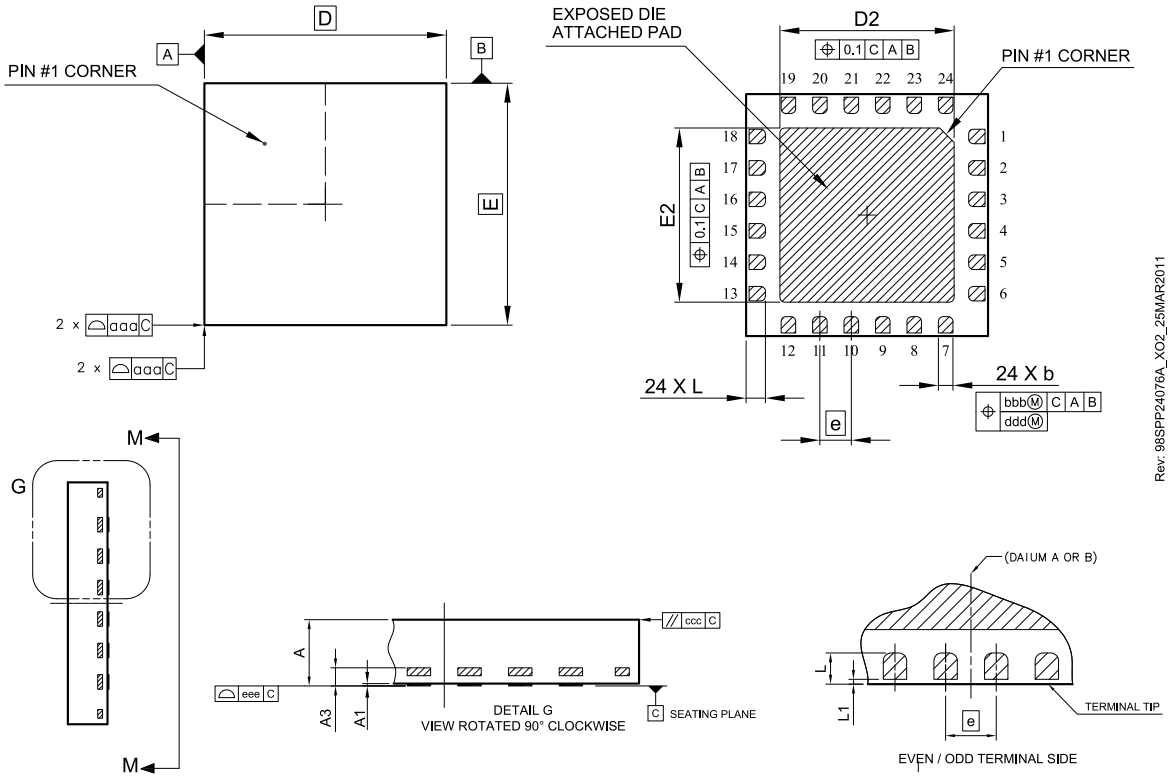
The specific GPIO pins available in *EFM32ZG110* is shown in Table 4.3 (p. 51). Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port in indicated by a number from 15 down to 0.

***Table 4.3. GPIO Pinout***

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | PA0 |
| Port B | - | PB14 | PB13 | - | PB11 | - | - | PB8 | PB7 | - | - | - | - | - | - | - |
| Port C | PC15 | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | PC1 | PC0 |
| Port D | - | - | - | - | - | - | - | - | PD7 | PD6 | - | - | - | - | - | - |
| Port E | - | - | PE13 | PE12 | - | - | - | - | - | - | - | - | - | - | - | - |
| Port F | - | - | - | - | - | - | - | - | - | - | - | - | - | PF2 | PF1 | PF0 |

# 4.4 QFN24 Package

***Figure 4.2. QFN24 (Preliminary)***




Note:

1. Dimensioning & tolerancing confirm to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension 'b' applies to metallized terminal and is measured between 0.25 mm and 0.30 mm from the terminal tip. Dimension L1 represents terminal full back from package edge up to 0.1 mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional

***Table 4.4. QFN24 (Preliminary) (Dimensions in mm)***

| Symbol | A | A1 | A3 | b | D | E | D2 | E2 | e | L | L1 | aaa | bbb | ccc | ddd | eee |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Min | 0.80 | 0.00 | 0.203 REF | 0.25 | 5.00 BSC | 5.00 BSC | 3.50 | 3.50 | 0.65 BSC | 0.35 | 0.00 | 0.10 | 0.10 | 0.10 | 0.05 | 0.08 |
| Nom | 0.85 | - | | 0.30 | | | 3.60 | 3.60 | | 0.40 | | | | | | |
| Max | 0.90 | 0.05 | | 0.35 | | | 3.70 | 3.70 | | 0.46 | 0.10 | | | | | |

The QFN24 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

# 5 PCB Layout and Soldering

## 5.1 Recommended PCB Layout

***Figure 5.1. QFN24 PCB Land Pattern***

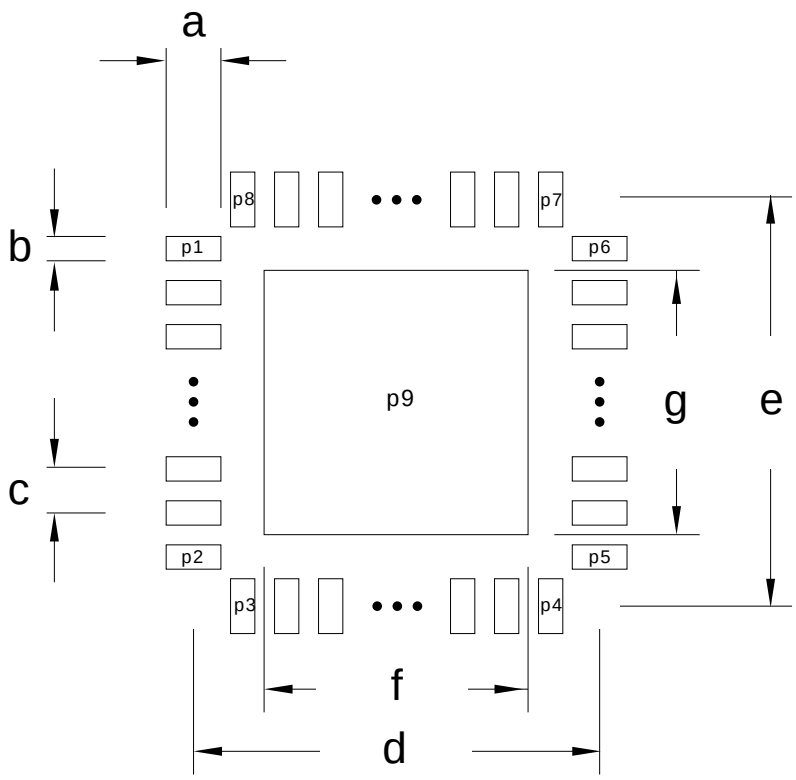



***Table 5.1. QFN24 PCB Land Pattern Dimensions (Dimensions in mm)***

| Symbol | Dim. (mm) | Symbol | Pin number | Symbol | Pin number |
|---|---|---|---|---|---|
| a | 0.80 | P1 | 1 | P8 | 24 |
| b | 0.30 | P2 | 6 | P9 | 25 |
| c | 0.65 | P3 | 7 | - | - |
| d | 5.00 | P4 | 12 | - | - |
| e | 5.00 | P5 | 13 | - | - |
| f | 3.60 | P6 | 18 | - | - |
| g | 3.60 | P7 | 19 | - | - |

*Figure 5.2. QFN24 PCB Solder Mask*

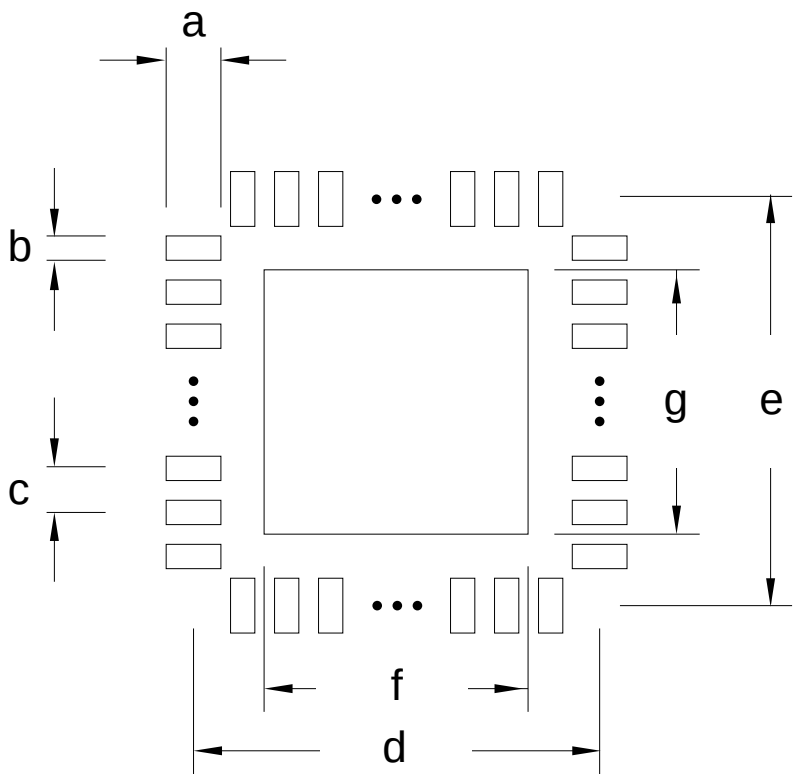



*Table 5.2. QFN24 PCB Solder Mask Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|---|---|---|---|
| a | 0.92 | e | 5.00 |
| b | 0.42 | f | 3.72 |
| c | 0.65 | g | 3.72 |
| d | 5.00 | - | - |

*Figure 5.3. QFN24 PCB Stencil Design*

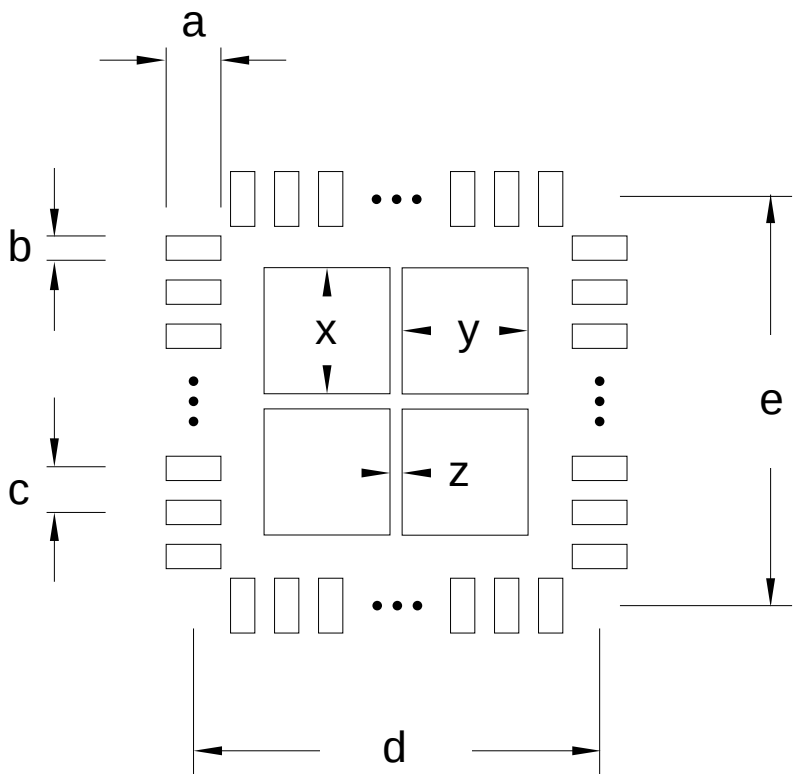



*Table 5.3. QFN24 PCB Stencil Design Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) | Symbol | Dim. (mm) |
|---|---|---|---|
| a | 0.60 | e | 5.00 |
| b | 0.25 | x | 1.00 |
| c | 0.65 | y | 1.00 |
| d | 5.00 | z | 0.50 |

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Figure 4.2 (p. 52) .

## 5.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

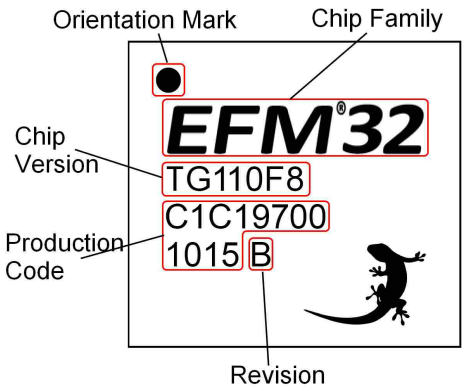
The packages have a Moisture Sensitivity Level rating of 3, please see the latest IPC/JEDEC J-STD-033 standard for MSL description and level 3 bake conditions. Place as many and as small as possible vias underneath each of the solder patches under the ground pad.

# 6 Chip Marking, Revision and Errata

## 6.1 Chip Marking

In the illustration below package fields and position are shown.

***Figure 6.1. Example Chip Marking***




## 6.2 Revision

The revision of a chip can be determined from the "Revision" field in Figure 6.1 (p. 56). If the revision says "ES" (Engineering Sample), the revision must be read out electronically as specified in the reference manual.

## 6.3 Errata

No known errata for EFM32ZG110.

# 7 Revision History

## 7.1 Revision 0.60

October 9th, 2013

Added I2C characterization data.

Added IDAC characterization data.

Updated current consumption table and figures in Electrical characteristics section.

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

Removed Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

## 7.2 Revision 0.50

April 22nd, 2013

Updated HFCORE max frequency from 32 MHz to 24 MHz.

Updated pinout.

Other minor corrections.

## 7.3 Revision 0.40

September 11th, 2012

Updated CPU core from Cortex M0 to Cortex M0+.

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Corrected operating voltage from 1.8 V to 1.85 V.

Other minor corrections.

## 7.4 Revision 0.30

July 16th, 2011

Updated the Electrical Characteristics section.

## 7.5 Revision 0.20

June 8th, 2011

Corrected all current values in Electrical Characteristics section.

Updated Cortex M0 related items in the memory map.

## 7.6 Revision 0.10

June 7th, 2011

Initial preliminary release.

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ARM Cortex-M0+
TINY
ARM Cortex-M3
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