



KSZ8091RNA/KSZ8091RND

10Base-T/100Base-TX Physical Layer Transceiver

Description

The KSZ8091RNA is a single-supply 10Base-T/100Base-TX Ethernet physical-layer transceiver for transmission and reception of data over standard CAT-5 unshielded twisted pair (UTP) cable.

The KSZ8091RNA is a highly-integrated PHY solution. It reduces board cost and simplifies board layout by using on-chip termination resistors for the differential pairs and by integrating a low-noise regulator to supply the 1.2V core, and by offering a flexible 1.8/2.5/3.3V digital I/O interface.

The KSZ8091RNA offers the Reduced Media Independent Interface (RMII) for direct connection with RMII-compliant Ethernet MAC processors and switches.

As the power-up default, the KSZ8091RNA uses a 25MHz crystal to generate all required clocks, including the 50MHz RMII reference clock output for the MAC. The KSZ8091RND takes in the 50MHz RMII reference clock as the power-up default.

Energy Efficient Ethernet (EEE) provides further power saving during idle traffic periods and Wake-on-LAN (WOL) provides a mechanism for the KSZ8091RNA to wake up a system that is in standby power mode.

The KSZ8091RNA and KSZ8091RND are available in 24-pin, lead-free QFN packages.

Applications

- Game console
- IP phone
- IP set-top box
- IP TV
- LOM
- Printer

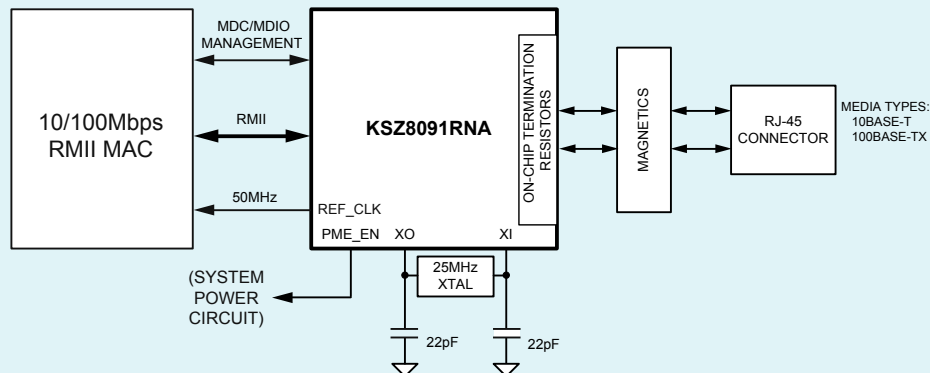
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Functional Diagram



KSZ8091RNA/KSZ8091RND - 10Base-T/100Base-TX PHYSICAL LAYER TRANSCEIVER

Key Features	Benefits
Single-chip 10Base-T/100Base-TX IEEE 802.3-compliant Ethernet transceiver	Standard compliance ensures that the device will work with other standard-compliant, already deployed devices
RMII v1.2 Interface support, with a 50MHz reference clock output to MAC and an option to input a 50MHz reference clock	Provides flexible options for the 50MHz RMII reference clock as the input or output
RMII back-to-back mode support	Allows creation of low-cost 100Mbps copper repeater using only two KSZ8091 PHYs
MDC/MDIO management interface	Allows the MAC processor complete access to the KSZ8091 control and status registers
On-chip termination resistors for the differential pairs	On-chip termination (eliminating four external resistors) simplifies PCB design, reduces system BOM, and improves overall signal integrity and EMI emission
On-chip regulator	Reduces BOM cost by eliminating external regulator for 1.2V core
HP Auto MDI/MDI-X to reliably detect and correct straight-through and crossover cable connections with disable and enable option	Easy-to-use feature eliminates the need for crossover cable, which reduces installation costs
Energy Efficient Ethernet (EEE) support with low-power idle (LPI) mode for 100Base-TX and transmit amplitude reduction with 10Base-Te option	Saves greater than 50% power in idle mode
Wake-on-LAN (WOL) support with either magic packet, link status change, or robust custom-packet detection	Provides a mechanism to wake up a system that is in standby power mode, saving total system power consumption
Multiple loopback options	Allows diagnostic testing for RMII and line side data paths
Single 3.3V power supply with VDD I/O options for 1.8V, 2.5V, or 3.3V	Enables low-power and flexible I/O design
Power-down and power-saving modes	Optimizes power consumption based on the status of the link or the device
LinkMD TDR-based cable diagnostics	Identifies common cable faults in production testing and in deployment

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