260-Ball BGA
Commercial Temp
Industrial Temp

# 72Mb SigmaQuad-IIIe™ Burst of 4 ECCRAM™

675 MHz–500 MHz
1.35V $V_{DD}$
1.2V to 1.5V $V_{DDQ}$

## Features

- On-Chip ECC with virtually zero SER
- Configurable Read Latency (3.0 or 2.0 cycles)
- Simultaneous Read and Write SigmaQuad-IIIe™ Interface
- Separate I/O Bus
- Double Data Rate interface
- Burst of 4 Read and Write
- Pipelined read operation
- Fully coherent Read and Write pipelines
- 1.35V nominal $V_{DD}$
- 1.2V JESD8-16A BIC-3 Compliant Interface
- 1.5V HSTL Interface
- ZQ pin for programmable output drive impedance
- ZT pin for programmable input termination impedance
- Configurable Input Termination
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 260-ball, 14 mm x 22 mm, 1 mm ball pitch BGA package
  - –K: 5/6 RoHS-compliant package

## SigmaQuad-IIIe™ Family Overview

SigmaQuad-IIIe ECCRAMs are the Separate I/O half of the SigmaQuad-IIIe/SigmaDDR-IIIe family of high performance ECCRAMs. Although very similar to GSI's second generation of networking SRAMs (the SigmaQuad-II/SigmaDDR-II family), these third generation devices offer several new features that help enable significantly higher performance.

## Clocking and Addressing Schemes

The GS8673ED18/36BK SigmaQuad-IIIe ECCRAMs are synchronous devices. They employ dual, single-ended master clocks, CK and $\overline{CK}$. These clocks are single-ended clock inputs, not differential inputs to a single differential clock input buffer. CK and $\overline{CK}$ are used to control the address and control input registers, as well as all output timing.

The KD and $\overline{KD}$ clocks are dual mesochronous (with respect to CK and $\overline{CK}$) input clocks that are used to control the data input registers. Consequently, data input setup and hold windows can be optimized independently of address and control input setup and hold windows.

Each internal read and write operation in a SigmaQuad-IIIe B4 ECCRAM is four times wider than the device I/O bus. An input data bus de-multiplexer is used to accumulate incoming data before it is simultaneously written to the memory array. An output data multiplexer is used to capture the data produced from a single memory array read and then route it to the appropriate output drivers as needed. Therefore, the address field of a SigmaQuad-IIIe B4 ECCRAM is always two address pins less than the advertised index depth (e.g. the 4M x 18 has 1M addressable index).

## On-Chip Error Correction Code

GSI's ECCRAMs implement an ECC algorithm that detects and corrects all single-bit memory errors, including those induced by Soft Error Rate (SER) events such as cosmic rays, alpha particles, etc. The resulting SER of these devices is anticipated to be <0.002 FITs/Mb — a 5-order-of-magnitude improvement over comparable SRAMs with no On-Chip ECC, which typically have an SER of 200 FITs/Mb or more. SER quoted above is based on reading taken at sea level.

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### Parameter Synopsis

| Speed Bin | Operating Frequency | Data Rate (per pin) | Read Latency | $V_{DD}$ |
|---|---|---|---|---|
| -675 | 675 / 450 MHz | 1350 / 900 Mbps | 3.0 / 2.0 | 1.3V to 1.4V |
| -625 | 625 / 400 MHz | 1250 / 800 Mbps | 3.0 / 2.0 | 1.3V to 1.4V |
| -550 | 550 / 375 MHz | 1100 / 750 Mbps | 3.0 / 2.0 | 1.25V to 1.4V |
| -500 | 500 / 333 MHz | 1000 / 666 Mbps | 3.0 / 2.0 | 1.25V to 1.4V |

Note: Please contact GSI for availability of 714 MHz devices.


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## 4M x 18 (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | MCL | MCH (CFG) | MCL | ZQ | PZT1 | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ |
| **B** | $V_{SS}$ | $NU_O$ | $V_{SS}$ | $NU_I$ | MVQ | MCH (B4M) | NC (RSVD) | MCH (SIOM) | PZT0 | D0 | $V_{SS}$ | Q0 | $V_{SS}$ |
| **C** | Q17 | $V_{DDQ}$ | D17 | $V_{DDQ}$ | $V_{SS}$ | SA | $V_{DD}$ | SA | $V_{SS}$ | $V_{DDQ}$ | $NU_I$ | $V_{DDQ}$ | $NU_O$ |
| **D** | $V_{SS}$ | $NU_O$ | $V_{SS}$ | $NU_I$ | SA | $V_{DDQ}$ | NC (288 Mb) | $V_{DDQ}$ | NC (144 Mb) | D1 | $V_{SS}$ | Q1 | $V_{SS}$ |
| **E** | Q16 | $V_{DDQ}$ | D16 | $V_{DD}$ | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | $V_{DD}$ | $NU_I$ | $V_{DDQ}$ | $NU_O$ |
| **F** | $V_{SS}$ | $NU_O$ | $V_{SS}$ | $NU_I$ | SA | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | SA | D2 | $V_{SS}$ | Q2 | $V_{SS}$ |
| **G** | Q15 | $NU_O$ | D15 | $NU_I$ | $V_{SS}$ | SA | MZT1 | SA | $V_{SS}$ | D3 | $NU_I$ | Q3 | $NU_O$ |
| **H** | Q14 | $V_{DDQ}$ | D14 | $V_{DDQ}$ | SA | $V_{DDQ}$ | $\overline{W}$ | $V_{DDQ}$ | SA | $V_{DDQ}$ | $NU_I$ | $V_{DDQ}$ | $NU_O$ |
| **J** | $V_{SS}$ | $NU_O$ | $V_{SS}$ | $NU_I$ | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | D4 | $V_{SS}$ | Q4 | $V_{SS}$ |
| **K** | CQ1 | $V_{DDQ}$ | $V_{REF}$ | $V_{DD}$ | KD1 | $V_{DD}$ | CK | $V_{DD}$ | KD0 | $V_{DD}$ | $V_{REF}$ | $V_{DDQ}$ | CQ0 |
| **L** | $\overline{CQ1}$ | $V_{SS}$ | QVLD1 | $V_{ss}$ | $\overline{KD1}$ | $V_{DDQ}$ | $\overline{CK}$ | $V_{DDQ}$ | $\overline{KD0}$ | $V_{SS}$ | QVLD0 | $V_{SS}$ | $\overline{CQ0}$ |
| **M** | $V_{SS}$ | Q13 | $V_{SS}$ | D13 | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | $NU_I$ | $V_{SS}$ | $NU_O$ | $V_{SS}$ |
| **N** | $NU_O$ | $V_{DDQ}$ | $NU_I$ | $V_{DDQ}$ | DLL | $V_{DDQ}$ | $\overline{R}$ | $V_{DDQ}$ | MCH | $V_{DDQ}$ | D5 | $V_{DDQ}$ | Q5 |
| **P** | $NU_O$ | Q12 | $NU_I$ | D12 | $V_{SS}$ | SA | MZT0 | SA | $V_{SS}$ | $NU_I$ | D6 | $NU_O$ | Q6 |
| **R** | $V_{SS}$ | Q11 | $V_{SS}$ | D11 | MCH | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | RST | $NU_I$ | $V_{SS}$ | $NU_O$ | $V_{SS}$ |
| **T** | $NU_O$ | $V_{DDQ}$ | $NU_I$ | $V_{DD}$ | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | $V_{DD}$ | D7 | $V_{DDQ}$ | Q7 |
| **U** | $V_{SS}$ | Q10 | $V_{SS}$ | D10 | $NU_I$ | $V_{DDQ}$ | $\overline{ADZT1}$ | $V_{DDQ}$ | $NU_I$ | $NU_I$ | $V_{SS}$ | $NU_O$ | $V_{SS}$ |
| **V** | $NU_O$ | $V_{DDQ}$ | $NU_I$ | $V_{DDQ}$ | $V_{SS}$ | SA (x18) | $V_{DD}$ | $NU_I$ (B2) | $V_{SS}$ | $V_{DDQ}$ | D8 | $V_{DDQ}$ | Q8 |
| **W** | $V_{SS}$ | Q9 | $V_{SS}$ | D9 | TCK | RLM0 | NC (RSVD) | MCL | TMS | $NU_I$ | $V_{SS}$ | $NU_O$ | $V_{SS}$ |
| **Y** | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | TDO | ZT | RLM1 | MCL | TDI | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ |

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**Notes:**

1. Pins 5A and 7A are reserved for future use. They must be tied Low in this device.
2. Pins 5R and 9N are reserved for future use. They must be tied High in this device.
3. Pin 6A is defined as mode pin CFG in the pinout standard. It must be tied High in this device to select x18 configuration.
4. Pin 8B is defined as mode pin SIOM in the pinout standard. It must be tied High in this device to select Separate I/O configuration.
5. Pin 6B is defined as mode pin B4M in the pinout standard. It must be tied High in this device to select Burst-of-4 configuration.
6. Pin 6V is defined as address pin SA for x18 devices. It is used in this device.
7. Pin 8V is defined as address pin SA for B2 devices. It is unused in this device, and must be left unconnected or driven Low.
8. Pin 9D is reserved as address pin SA for 144 Mb devices. It is a true no connect in this device.
9. Pin 7D is reserved as address pin SA for 288 Mb devices. It is a true no connect in this device.
10. Pins 5U and 9U are unused in this device. They must be left unconnected or driven Low.
11. Pins 8W and 8Y are reserved for internal use only. They must be tied Low.
12. Pins 7B and 7W are reserved for future use. They are true no connects in this device.

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## 2M x 36 (Top View)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | MCL | MCL (CFG) | MCL | ZQ | PZT1 | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ |
| **B** | $V_{SS}$ | Q35 | $V_{SS}$ | D35 | MVQ | MCH (B4M) | NC (RSVD) | MCH (SIOM) | PZT0 | D0 | $V_{SS}$ | Q0 | $V_{SS}$ |
| **C** | Q26 | $V_{DDQ}$ | D26 | $V_{DDQ}$ | $V_{SS}$ | SA | $V_{DD}$ | SA | $V_{SS}$ | $V_{DDQ}$ | D9 | $V_{DDQ}$ | Q9 |
| **D** | $V_{SS}$ | Q34 | $V_{SS}$ | D34 | SA | $V_{DDQ}$ | NC (288 Mb) | $V_{DDQ}$ | NC (144 Mb) | D1 | $V_{SS}$ | Q1 | $V_{SS}$ |
| **E** | Q25 | $V_{DDQ}$ | D25 | $V_{DD}$ | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | $V_{DD}$ | D10 | $V_{DDQ}$ | Q10 |
| **F** | $V_{SS}$ | Q33 | $V_{SS}$ | D33 | SA | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | SA | D2 | $V_{SS}$ | Q2 | $V_{SS}$ |
| **G** | Q24 | Q32 | D24 | D32 | $V_{SS}$ | SA | MZT1 | SA | $V_{SS}$ | D3 | D11 | Q3 | Q11 |
| **H** | Q23 | $V_{DDQ}$ | D23 | $V_{DDQ}$ | SA | $V_{DDQ}$ | $\overline{W}$ | $V_{DDQ}$ | SA | $V_{DDQ}$ | D12 | $V_{DDQ}$ | Q12 |
| **J** | $V_{SS}$ | Q31 | $V_{SS}$ | D31 | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | D4 | $V_{SS}$ | Q4 | $V_{SS}$ |
| **K** | CQ1 | $V_{DDQ}$ | $V_{REF}$ | $V_{DD}$ | KD1 | $V_{DD}$ | CK | $V_{DD}$ | KD0 | $V_{DD}$ | $V_{REF}$ | $V_{DDQ}$ | CQ0 |
| **L** | $\overline{CQ}$1 | $V_{SS}$ | QVLD1 | $V_{SS}$ | $\overline{KD}$1 | $V_{DDQ}$ | $\overline{CK}$ | $V_{DDQ}$ | $\overline{KD}$0 | $V_{SS}$ | QVLD0 | $V_{SS}$ | $\overline{CQ}$0 |
| **M** | $V_{SS}$ | Q22 | $V_{SS}$ | D22 | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | D13 | $V_{SS}$ | Q13 | $V_{SS}$ |
| **N** | Q30 | $V_{DDQ}$ | D30 | $V_{DDQ}$ | DLL | $V_{DDQ}$ | $\overline{R}$ | $V_{DDQ}$ | MCH | $V_{DDQ}$ | D5 | $V_{DDQ}$ | Q5 |
| **P** | Q29 | Q21 | D29 | D21 | $V_{SS}$ | SA | MZT0 | SA | $V_{SS}$ | D14 | D6 | Q14 | Q6 |
| **R** | $V_{SS}$ | Q20 | $V_{SS}$ | D20 | MCH | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | RST | D15 | $V_{SS}$ | Q15 | $V_{SS}$ |
| **T** | Q28 | $V_{DDQ}$ | D28 | $V_{DD}$ | $V_{SS}$ | SA | $V_{SS}$ | SA | $V_{SS}$ | $V_{DD}$ | D7 | $V_{DDQ}$ | Q7 |
| **U** | $V_{SS}$ | Q19 | $V_{SS}$ | D19 | $NU_I$ | $V_{DDQ}$ | $\overline{ADZT1}$ | $V_{DDQ}$ | $NU_I$ | D16 | $V_{SS}$ | Q16 | $V_{SS}$ |
| **V** | Q27 | $V_{DDQ}$ | D27 | $V_{DDQ}$ | $V_{SS}$ | $NU_I$ (x18) | $V_{DD}$ | $NU_I$ (B2) | $V_{SS}$ | $V_{DDQ}$ | D8 | $V_{DDQ}$ | Q8 |
| **W** | $V_{SS}$ | Q18 | $V_{SS}$ | D18 | TCK | RLM0 | NC (RSVD) | MCL | TMS | D17 | $V_{SS}$ | Q17 | $V_{SS}$ |
| **Y** | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | TDO | ZT | RLM1 | MCL | TDI | $V_{DDQ}$ | $V_{DD}$ | $V_{DDQ}$ | $V_{DD}$ |

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**Notes:**

1. Pins 5A and 7A are reserved for future use. They must be tied Low in this device.
2. Pins 5R and 9N are reserved for future use. They must be tied High in this device.
3. Pin 6A is defined as mode pin CFG in the pinout standard. It must be tied Low in this device to select x36 configuration.
4. Pin 8B is defined as mode pin SIOM in the pinout standard. It must be tied High in this device to select Separate I/O configuration.
5. Pin 6B is defined as mode pin B4M in the pinout standard. It must be tied High in this device to select Burst-of-4 configuration.
6. Pin 6V is defined as address pin SA for x18 devices. It is unused in this device, and must be left unconnected or driven Low.
7. Pin 8V is defined as address pin SA for B2 devices. It is unused in this device, and must be left unconnected or driven Low.
8. Pin 9D is reserved as address pin SA for 144 Mb devices. It is a true no connect in this device.
9. Pin 7D is reserved as address pin SA for 288 Mb devices. It is a true no connect in this device.
10. Pins 5U and 9U are unused in this device. They must be left unconnected or driven Low.
11. Pins 8W and 8Y are reserved for internal use only. They must be tied Low.
12. Pins 7B and 7W are reserved for future use. They are true no connects in this device.

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## Pin Description

| Symbol | Description | Type |
|---|---|---|
| SA | **Address**—Read or Write Address is registered on ↑CK. | Input |
| D[35:0] | **Write Data**—Registered on ↑KD and ↑$\overline{KD}$ during Write operations.<br>D[17:0]—x18 and x36.<br>D[35:18]—x36 only. | Input |
| Q[35:0] | **Read Data**—Driven by ↑CK and ↑$\overline{CK}$, and synchronized with ↑CQ and ↑$\overline{CQ}$ during Read operations.<br>Q[17:0]—x18 and x36.<br>Q[35:18]—x36 only. | Output |
| QVLD[1:0] | **Read Data Valid**—Driven high one half cycle before valid Read Data. | Output |
| CK, $\overline{CK}$ | **Primary Input Clocks**—Dual single-ended. For Address and Control input latching, internal timing control, and Read Data and Echo Clock output timing control. | Input |
| $\overline{KD}$[1:0], KD[1:0] | **Write Data Input Clocks**—Dual single-ended. For Write Data input latching.<br>KD0, $\overline{KD}$0—latch Write Data (D[17:0] in x36, D[8:0] in x18).<br>KD1, $\overline{KD}$1—latch Write Data (D[35:18] in x36, D[17:9] in x18). | Input |
| $\overline{CQ}$[1:0], CQ[1:0] | **Echo Clocks**—Free running source synchronous output clocks. | Output |
| $\overline{R}$ | **Read Enable**—Registered on ↑CK. $\overline{R}$ = 0 initiates a Read operation. | Input |
| $\overline{W}$ | **Write Enable**—Registered on ↑CK. $\overline{W}$ = 0 initiates a Write operation. | Input |
| $\overline{ADZT1}$ | **Address and Write Data Input Termination Pull-Up Enable**—Registered on↑CK.<br>$\overline{ADZT1}$ = 0: enables termination pull-up on Address (SA), Write Data (D) inputs.<br>$\overline{ADZT1}$ = 1: disables termination pull-up on Address (SA), Write Data (D) inputs. | Input |
| DLL | **DLL Enable**—Weakly pulled High internally.<br>DLL = 0: disables internal DLL.<br>DLL = 1: enables internal DLL. | Input |
| RST | **Reset**—Holds the device inactive and resets the device to its initial power-on state when asserted High. Weakly pulled Low internally. | Input |
| RLM[1:0] | **Read Latency Select 1:0**—Must be tied High or Low.<br>RLM[1:0] = 00: reserved.<br>RLM[1:0] = 01: selects 2.0 cycle Read Latency.<br>RLM[1:0] = 10: selects 3.0 cycle Read Latency.<br>RLM[1:0] = 11: reserved. | Input |
| ZQ | **Output Driver Impedance Control Resistor Input**—Must be connected to $V_{SS}$ through an external resistor RQ to program output driver impedance. | Input |
| ZT | **Input Termination Impedance Control Resistor Input**—Must be connected to $V_{SS}$ through an external resistor RT to program input termination impedance. | Input |

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## Pin Description (Continued)

| Symbol | Description | Type |
|---|---|---|
| MZT[1:0] | **Input Termination Mode Select**—Selects the termination mode used for all terminated inputs. Must be tied High or Low.<br>MZT[1:0] = 00: disabled.<br>MZT[1:0] = 01: RT/2 Thevenin-equivalent (pull-up = RT, pull-down = RT).<br>MZT[1:0] = 10: RT Thevenin-equivalent (pull-up = 2*RT, pull-down = 2*RT).<br>MZT[1:0] = 11: reserved. | Input |
| PZT[1:0] | **Input Termination Configuration Select**—Selects which inputs are terminated. Must be tied High or Low.<br>PZT[1:0] = 00: Write Data only.<br>PZT[1:0] = 01: Write Data, Input Clocks.<br>PZT[1:0] = 10: Write Data, Address, Control.<br>PZT[1:0] = 11: Write Data, Address, Control, Input Clocks. | Input |
| MVQ | **I/O Voltage Select**—Indicates what voltage is supplied to the $V_{DDQ}$ pins. Must be tied High or Low.<br>MVQ = 0: Configure for 1.2V to 1.35V nominal $V_{DDQ}$.<br>MVQ = 1: Configure for 1.5V nominal $V_{DDQ}$. | Input |
| $V_{DD}$ | **Core Power Supply**—1.35V nominal core supply voltage. | — |
| $V_{DDQ}$ | **I/O Power Supply**—1.2V to 1.5V nominal I/O supply voltage. Configurable via MVQ pin. | — |
| $V_{REF}$ | **Input Reference Voltage**—Input buffer reference voltage. | — |
| $V_{SS}$ | **Ground** | — |
| TCK | **JTAG Clock** | Input |
| TMS | **JTAG Mode Select**—Weakly pulled High internally. | Input |
| TDI | **JTAG Data Input**—Weakly pulled High internally. | Input |
| TDO | **JTAG Data Output** | Output |
| MCH | **Must Connect High**—May be tied to $V_{DDQ}$ directly or via a 1kΩ resistor. | Input |
| MCL | **Must Connect Low**—May be tied to $V_{SS}$ directly or via a 1kΩ resistor. | Input |
| NC | **No Connect**—There is no internal chip connection to these pins. They may be left unconnected, or tied High or Low. | — |
| $NU_I$ | **Not Used, Input**—There is an internal chip connection to these input pins, but they are unused by the device. They are pulled Low internally. They may be left unconnected or tied Low. They should not be tied High. | Input |
| $NU_O$ | **Not Used, Output**—There is an internal chip connection to these output pins, but they are unused by the device. Unused output pins are tri-stated internally. They should be left unconnected. | Output |

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## Power Up Requirements

For reliability purposes, power supplies must power up simultaneously, or in the following sequence:
$V_{SS}$, $V_{DD}$, $V_{DDQ}$, $V_{REF}$ and inputs.
Power supplies must power down simultaneously, or in the reverse sequence.

After power supplies power up, the following start-up sequence must be followed.

**Step 1 (Recommended, but not required)**: Assert RST High for at least 1ms.
While RST is asserted high:
• The DLL is disabled, regardless of the state of the DLL pin.
• Read and Write operations are ignored.

**Note**: If possible, RST should be asserted High before input clocks (CK, $\overline{CK}$, KD, $\overline{KD}$) begin toggling, and remain asserted High until input clocks are stable and toggling within specification, in order to prevent unstable, out-of-spec input clocks from causing trouble in the SRAM.

**Step 2:** Begin toggling input clocks.
After input clocks begin toggling, but not necessarily within specification:
• Q are placed in the non-Read state, and remain so until the first Read operation.
• QVLD are driven Low, and remain so until the first Read operation.
• CQ, $\overline{CQ}$ begin toggling, but not necessarily within specification.

**Step 3**: Wait until input clocks are stable and toggling within specification.

**Step 4**: De-assert RST Low (if asserted High).

**Step 5**: Wait at least 160K (163,840) cycles.
During this time:
• Output driver and input termination impedances are calibrated (i.e. set to the programmed values).

**Note**: The DLL pin may be asserted High or de-asserted Low during this time. If asserted High, DLL synchronization begins immediately after output driver and input termination impedance calibration has completed. If de-asserted Low, DLL synchronization begins after the DLL pin is asserted High (see Step 6). In either case, Step 7 must follow thereafter.

**Step 6**: Assert DLL pin High (if de-asserted Low).

**Step 7**: Wait at least 64K (65,536) cycles.
During this time:
• The DLL is enabled and synchronized properly.

After DLL synchronization has completed:
• CQ, $\overline{CQ}$ begin toggling within specification.

**Step 8**: Begin initiating Read and Write operations.

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## Reset (RST) Requirements

Although not generally recommended, RST may be asserted High at any time after completion of the initial power-up sequence described previously, to reset the SRAM control logic to its initial power-on state. However, whenever RST is subsequently de-asserted Low (as in Step 4 in the power up sequence), Steps 5~7 in the power-up sequence must be followed before Read and Write operations are initiated.

**Note**: Memory array content may be perturbed/corrupted when RST is asserted High.

## DLL Operation

An on-chip DLL is used to align output timing with input clocks. The DLL uses the CK input clock as a source, and is enabled when all of the following conditions are met:

1. The DLL pin is asserted High, and
2. The RST pin is de-asserted Low, and
3. The input clock $t_{KHKH} \leq 6.0$ns.

Once enabled, the DLL requires 64K (65,536) stable clock cycles in order to synchronize properly.

The DLL can tolerate changes in input clock frequency due to clock jitter (i.e. such jitter will not cause the DLL to lose lock/ synchronization), provided the cycle-to-cycle jitter does not exceed 200ps (see the $t_{KJITcc}$ specification in the AC Electrical Characteristics section for more information). However, the DLL must be resynchronized (i.e. disabled and then re-enabled) whenever the nominal input clock frequency is changed.

When the DLL is enabled, read latency is determined by the RLM mode pins, as defined in the Read Latency section. Output timing is aligned with the input clocks.

The DLL is disabled when any of the following conditions are met:

1. The DLL pin is de-asserted Low, or
2. The RST pin is asserted High, or
3. The input clock is stopped for at least 30ns, or $t_{KHKH} \geq 30$ns.

## On-Chip Error Correction

SigmaQuad-IIIe ECCRAMs implement a single-bit error detection and correction algorithm (specifically, a Hamming Code) on each DDR data word (comprising two 9-bit data bytes) transmitted on each 9-bit data bus (i.e., transmitted on D/Q[8:0], D/Q[17:9], D/Q[26:18], or D/Q[35:27]). To accomplish this, 5 ECC parity bits (invisible to the user) are utilized per every 18 data bits (visible to the user).

The ECC algorithm neither corrects nor detects multi-bit errors. However, GSI ECCRAMs are architected in such a way that a single SER event very rarely causes a multi-bit error across any given “transmitted data unit”, where a “transmitted data unit” represents the data transmitted as the result of a single read or write operation to a particular address. The extreme rarity of multi-bit errors results in the SER mentioned previously (i.e., <0.002 FITs/Mb (measured at sea level)).

Not only does the on-chip ECC significantly improve SER performance, but it also frees up the entire memory array for data storage. Very often SRAM applications allocate 1/9th of the memory array (i.e., one “error bit” per eight “data bits”, in any 9-bit “data byte”) for error detection (either simple parity error detection, or system-level ECC error detection and correction). Such error-bit allocation is unnecessary with ECCRAMs the entire memory array can be utilized for data storage, effectively providing 12.5% greater storage capacity compared to SRAMs of the same density not equipped with on-chip ECC.

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## Read Latency (RL)

Read Latency is the Read pipeline length, and directly impacts the maximum operating frequency of the device. It is user-programmable through mode pins RLM [1:0].

### GS8673ED18/36BK-675 Read Latency

| Read Latency (RL) | RLM1 | RLM0 | Frequency |
|---|---|---|---|
| 3.0 cycles | 1 | 0 | 167 MHz–675 MHz |
| 2.0 cycles | 0 | 1 | 167 MHz–450 MHz |

### GS8673ED18/36BK-625 Read Latency

| Read Latency (RL) | RLM1 | RLM0 | Frequency |
|---|---|---|---|
| 3.0 cycles | 1 | 0 | 167 MHz–625 MHz |
| 2.0 cycles | 0 | 1 | 167 MHz–400 MHz |

### GS8673ED18/36BK-550 Read Latency

| Read Latency (RL) | RLM1 | RLM0 | Frequency |
|---|---|---|---|
| 3.0 cycles | 1 | 0 | 167 MHz–550 MHz |
| 2.0 cycles | 0 | 1 | 167 MHz–375 MHz |

### GS8673ED18/36BK-500 Read Latency

| Read Latency (RL) | RLM1 | RLM0 | Frequency |
|---|---|---|---|
| 3.0 cycles | 1 | 0 | 167 MHz–500 MHz |
| 2.0 cycles | 0 | 1 | 167 MHz–333 MHz |

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## Functional Description

Separate I/O ECCRAMs, from a system architecture point of view, are attractive in applications that execute continuous back-to-back alternating Reads and Writes. Therefore, the SigmaQuad-IIIe ECCRAM interface and truth table are optimized for continuously alternating Reads and Writes. Separate I/O ECCRAMs are unpopular in applications where block transfers of Reads or Writes are needed because half of the data pins will go unused during the block transfer, potentially cutting Separate I/O ECCRAM data bandwidth in half. Applications of this sort are better served by Common I/O ECCRAMs such as the SigmaDDR-IIIe series.

## Truth Table

| Previous Operation | SA | $\overline{R}$ | $\overline{W}$ | Current Operation | D | | | | Q | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ($t_{n-1}$) | ↑CK ($t_n$) | ↑CK ($t_n$) | ↑CK ($t_n$) | ($t_n$) | ↑KD ($t_{n+1}$) | ↑$\overline{KD}$ ($t_{n+1½}$) | ↑KD ($t_{n+2}$) | ↑$\overline{KD}$ ($t_{n+2½}$) | ↑CK ($t_m$) | ↑CK ($t_{m+180°}$) | ↑CK ($t_{m+1}$) | ↑CK ($t_{m+1+180°}$) |
| NOP | X | 1 | 1 | NOP | X | X | — | — | Hi-Z/0 | Hi-Z/0 | — | — |
| Write | X | 1 | X | NOP | D3 | D4 | — | — | Hi-Z/0 | Hi-Z/0 | — | — |
| Read | X | X | 1 | NOP | X | X | — | — | Q3 | Q4 | — | — |
| NOP | V | 1 | 0 | Write | D1 | D2 | D3 | D4 | Hi-Z/0 | Hi-Z/0 | — | — |
| Read | V | X | 0 | Write | D1 | D2 | D3 | D4 | Q3 | Q4 | — | — |
| NOP | V | 0 | X | Read | X | X | — | — | Q1 | Q2 | Q3 | Q4 |
| Write | V | 0 | X | Read | D3 | D4 | — | — | Q1 | Q2 | Q3 | Q4 |

**Notes:**

1. 1 = input High; 0 = input Low; V = input valid; X = input don't care.
2. $t_m = t_{n + RL}$, where RL = Read Latency of the device.
3. D1, D2, D3, and D4 indicate the first, second, third, and fourth pieces of Write Data transferred during Write operations.
4. Q1, Q2, Q3, and Q4 indicate the first, second, third, and fourth pieces of Read Data transferred during Read operations.
5. When D input termination is disabled (MZT[1:0] = 00), Q drivers are disabled (i.e. Q pins are tri-stated) for one cycle in response to NOP and Write commands, RL cycles after the command is sampled, except when preceded by a Read command.
6. When D input termination is enabled (MZT[1:0] = 01 or 10), Q drivers are enabled Low (i.e. Q pins are driven Low) for one cycle in response to NOP and Write commands, RL cycles after the command is sampled, except when preceded by a Read command. This is done so the Memory Controller can enable On-Die Termination on its data inputs without having to cope with the termination pulling tri-stated data inputs to $V_{DDQ}/2$ (i.e., to the switch point of the data input receivers).

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## Low Power NOP Mode

When input termination is enabled on the Address (SA) and Write Data (D) inputs, those inputs can be placed in Low Power NOP (LP NOP) mode via the synchronous $\overline{\text{ADZT1}}$ input. When NOP operations are initiated with $\overline{\text{ADZT1}}$ High, the termination pull-ups on the SA and D inputs are disabled, thereby reducing the DC power associated with those inputs.

## LP NOP Truth Table

| $\overline{\text{R}}$ | $\overline{\text{W}}$ | $\overline{\text{ADZT1}}$ | Current Operation | SA, D Pull-Up |
|---|---|---|---|---|
| ↑CK ($t_n$) | ↑CK ($t_n$) | ↑CK ($t_n$) | ($t_n$) | ↑CK ($t_{n+2}$) |
| X | X | 0 | Any | Enabled |
| X | X | 1 | Any | Disabled |

**Notes:**

1. 1 = input High; 0 = input Low; X = input don't care.
2. $\overline{\text{ADZT1}}$ should only be driven High during NOP operations; SA, D input timing is not guaranteed in LP NOP Mode.
3. SA, D should be driven Low (or tri-stated) during LP NOP Mode, to take advantage of the power-saving feature.

## LP NOP Timing Specifications

| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| CK Clock High to SA Pull-up Enable / Disable | $t_{KHAZTV}$ | 0 | 2.0 | ns |
| CK Clock High to D Pull-Up Enable / Disable | $t_{KHDZTV}$ | –0.4 | 0.4 | ns |

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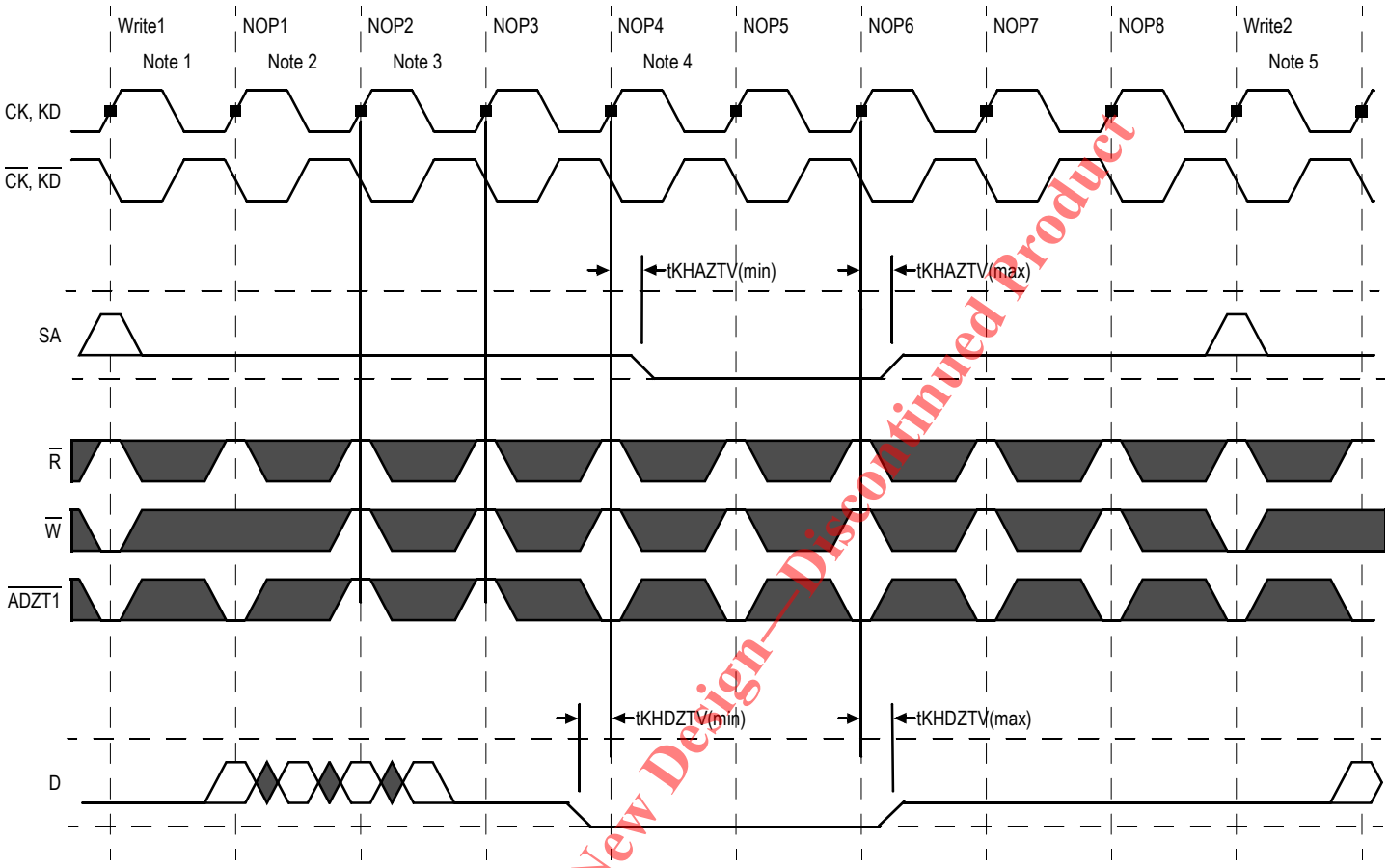
## LP NOP Timing Diagram

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**Notes:**

1. The Controller initiates Write1. The ECCRAM is enabling SA and D termination.
2. The Controller initiates one NOP (NOP1) with ADZT1 Low, to allow time for Write1 to complete.
   The Controller drives SA, D Low during NOP1 ~ NOP8.
3. The Controller initiates two more NOPs (NOP2 ~ NOP3) with ADZT1 High, to cause the ECCRAM to enter LP NOP mode for 2 cycles.
   The ECCRAM disables SA and D termination pull ups at ↑CK in NOP4, 2 cycles after sampling ADZT1 = 1 at ↑CK in NOP2.
4. The Controller initiates five more NOPs (NOP4 ~ NOP8) with ADZT1 Low, to allow time for the ECCRAM to exit LP NOP Mode.
   The ECCRAM enables SA and D termination pull ups at ↑CK in NOP6, 2 cycles after sampling ADZT1 = 0 at ↑CK in NOP4.
5. The Controller initiates Write2. The ECCRAM is enabling SA and D termination.

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## Input Timing

Address (SA) inputs are latched with CK.
Address input timing is clock-centered; that is, CK edges must be driven such that adequate setup and hold time is provided to the address input registers, as specified by the ECCRAM.

Control ($\overline{R}$, $\overline{W}$, $\overline{ADZT1}$) inputs are latched with CK.
Control input timing is clock-centered; that is, CK edges must be driven such that adequate setup and hold time is provided to the control input registers, as specified by the ECCRAM.

Write Data (D) inputs are latched with KD[1:0] and $\overline{KD}$[1:0].

1. KD0 and $\overline{KD}$0 are used to latch D[17:0] in x36, and D[8:0] in x18.
2. KD1 and $\overline{KD}$1 are used to latch D[35:18] in x36, and D[17:9] in x18.

Write Data input timing is clock-centered; that is, KD and $\overline{KD}$ edges must be driven such that adequate setup and hold time is provided to the data input registers, as specified by the ECCRAM.

## Output Timing

The SigmaQuad-IIIe ECCRAMs feature source-synchronous output clocks, also known as echo clocks. These outputs, CQ0, $\overline{CQ0}$, CQ1, and $\overline{CQ1}$ are designed to be electrically identical to data output pins. They are designed to behave just like data output pins. They are designed to track variances demonstrated by the data outputs due to influences of temperature, voltage, process, or other factors. As a result, the specifications that describe the relationship between the CQ clock edges and the data output edges are much tighter than those that describe the relationship between the data outputs and the incoming CK clock.

Note that the CQ clock-to-data output specifications apply to specific combinations of clocks and data, as follows:

1. CQ0 and $\overline{CQ0}$ are associated with Q[17:0] in x36, and with Q[8:0] in x18. They are also associated with QVLD0.
2. CQ1 and $\overline{CQ1}$ are associated with Q[35:18] in x36, and with Q[17:9] in x18. They are also associated with QVLD1.

As can be seen, the echo clock pairs are, in each case, associated with data output pins on the nearest side of the chip. The left vs. right side groupings prevent skew across the device and pinout from degrading the data output valid window.

## Output Alignment

| Q1 Active | Q2 Inactive | ↑CQ | ↓$\overline{CQ}$ | Q1 Inactive | Q2 Active | QVLD Active/Inactive | ↑$\overline{CQ}$ | ↓CQ |
|---|---|---|---|---|---|---|---|---|
| Generated from ↑CK | | | | Generated from ↑$\overline{CK}$ | | | | |

**Notes:**

1. Q1 and Q2 indicate the first and second pieces of read data transferred in any given cycle.
2. Output timing is aligned with input clocks.
3. Output timing is clock-aligned. That is, CQ, $\overline{CQ}$ edges are aligned with Q edges.

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## Output Driver Impedance Control

Programmable output drivers have been implemented on Read Data (Q), Read Data Valid (QVLD), and Echo Clocks (CQ, $\overline{CQ}$). The output driver impedance can be programmed via the ZQ pin. When an external impedance-matching resistor (RQ) is connected between ZQ and $V_{SS}$, output driver impedance is set to RQ/5 nominally.

Output driver impedance is set to the programmed value within 160K cycles after input clocks are operating within specification, and RST is de-asserted Low. It is updated periodically thereafter, to compensate for temperature and voltage fluctuations in the system.

## Input Termination Impedance Control

On-die input termination can be enabled on Write Data (D), Address (SA), Control ($\overline{R}$, $\overline{W}$, $\overline{ADZT1}$), and Input Clocks (CK, $\overline{CK}$, KD, $\overline{KD}$) via the MZT[1:0] and PZT[1:0] pins. The termination impedance can be programmed via the ZT pin. When an external impedance-matching resistor (RT) is connected between ZT and $V_{SS}$, termination impedance is set according to the table below.

Termination impedance is set to the programmed value within 160K cycles after input clocks are operating within specification, and RST is de-asserted Low. It is updated periodically thereafter, to compensate for temperature and voltage fluctuations in the system.

**Note:** When termination impedance is enabled on a particular input, that input should always be driven High or Low; it should never be tri-stated (i.e., in a High-Z state). If the input is tri-stated, the termination will pull the signal to $V_{DDQ}$ / 2 (i.e., to the switch point of the diff-amp receiver), which could cause the receiver to enter a meta-stable state and consume more power than it normally would. This could result in the device's operating currents being higher.

The following table specifies the pull-up and pull-down termination impedances for each terminated input:

## Pull-up and Pull-Down Termination Impedance

| Terminated Inputs | PZT[1:0] | MZT[1:0] | Pull-Down Impedance | Pull-Up Impedance |
|---|---|---|---|---|
| CK, $\overline{CK}$, KD, $\overline{KD}$ | X0 | XX | disabled | disabled |
| | X1 | 01 | RT | RT |
| | | 10 | 2 * RT | 2 * RT |
| SA, $\overline{R}$, $\overline{W}$, $\overline{ADZT1}$ | 0X | XX | disabled | disabled |
| | 1X | 01 | RT | RT |
| | | 10 | 2 * RT | 2 * RT |
| D | XX | 01 | RT | RT |
| | | 10 | 2 * RT | 2 * RT |

**Notes:**

1. When MZT[1:0] = 00, input termination is disabled on all inputs.
2. When MZT[1:0] = 11, input termination state is not specified; it is reserved for future use.
3. During JTAG EXTEST and SAMPLE-Z instructions, input termination is disabled on all inputs.

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## Electrical Specifications

### Absolute Maximum Ratings

| Parameter | Symbol | Rating | Units |
|---|---|---|---|
| Core Supply Voltage | $V_{DD}$ | -0.3 to +1.6 | V |
| I/O Supply Voltage when MVQ = 0 | $V_{DDQ}$ | -0.3 to $V_{DD}$ | V |
| I/O Supply Voltage when MVQ = 1 | $V_{DDQ}$ | -0.3 to $V_{DD}$ + 0.3 | V |
| Input Voltage when MVQ = 0 | $V_{IN}$ | -0.3 to $V_{DDQ}$ + 0.3 (1.7 max) | V |
| Input Voltage when MVQ = 1 | $V_{IN}$ | -0.3 to $V_{DDQ}$ + 0.3 (2.0 max) | V |
| Maximum Junction Temperature | $T_J$ | 125 | °C |
| Storage Temperature | $T_{STG}$ | -55 to 125 | °C |

**Note:**

Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions for an extended period of time may affect reliability of this component.

### Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Core Supply Voltage: -675 and -625 speed bins | $V_{DD}$ | 1.3 | 1.35 | 1.4 | V |
| Core Supply Voltage: -550 and -500 speed bins | $V_{DD}$ | 1.25 | 1.3 ~ 1.35 | 1.4 | V |
| I/O Supply Voltage when MVQ = 0 | $V_{DDQ}$ | 1.15 | 1.2 ~ 1.35 | $V_{DD}$ | V |
| I/O Supply Voltage when MVQ = 1 | $V_{DDQ}$ | 1.4 | 1.5 | 1.6 | V |
| Commercial Junction Temperature | $T_{JC}$ | 0 | — | 85 | °C |
| Industrial Junction Temperature | $T_{JI}$ | –40 | — | 100 | °C |

**Note:**

For reliability purposes, power supplies must power up simultaneously, or in the following sequence:

$V_{SS}$, $V_{DD}$, $V_{DDQ}$, $V_{REF}$, and Inputs.

Power supplies must power down simultaneously, or in the reverse sequence.

### Thermal Impedance

| Package | θ JA (C°/W) Airflow = 0 m/s | θ JA (C°/W) Airflow = 1 m/s | θ JA (C°/W) Airflow = 2 m/s | θ JB (C°/W) | θ JC (C°/W) |
|---|---|---|---|---|---|
| FBGA | 15.5 | 13.1 | 12.1 | 4.4 | 0.2 |

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## I/O Capacitance

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | — | 5.0 | pF | 1, 3 |
| Output Capacitance | $C_{OUT}$ | — | 5.5 | pF | 2, 3 |

**Notes:**
1. $V_{IN} = V_{DDQ}/2$.
2. $V_{OUT} = V_{DDQ}/2$.
3. $T_A = 25°C$, f = 1 MHz.

## Input Electrical Characteristics when MVQ = 0

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| DC Input Reference Voltage | $V_{REFdc}$ | 0.48 * $V_{DDQ}$ | 0.52 * $V_{DDQ}$ | V | — |
| DC Input High Voltage | $V_{IH1dc}$ | $V_{REF}$ + 0.08 | $V_{DDQ}$ + 0.15 | V | 4 |
| DC Input Low Voltage | $V_{IL1dc}$ | –0.15 | $V_{REF}$ – 0.08 | V | 4 |
| DC Input High Voltage | $V_{IH2dc}$ | 0.75 * $V_{DDQ}$ | $V_{DDQ}$ + 0.15 | V | 5 |
| DC Input Low Voltage | $V_{IL2dc}$ | –0.15 | 0.25 * $V_{DDQ}$ | V | 5 |
| AC Input Reference Voltage | $V_{REFac}$ | 0.47 * $V_{DDQ}$ | 0.53 * $V_{DDQ}$ | V | 1 |
| AC Input High Voltage | $V_{IH1ac}$ | $V_{REF}$ + 0.15 | $V_{DDQ}$ + 0.25 | V | 2, 3, 4 |
| AC Input Low Voltage | $V_{IL1ac}$ | –0.25 | $V_{REF}$ – 0.15 | V | 2, 3, 4 |
| AC Input High Voltage | $V_{IH2ac}$ | $V_{DDQ}$ – 0.2 | $V_{DDQ}$ + 0.25 | V | 2, 5 |
| AC Input Low Voltage | $V_{IL2ac}$ | – 0.25 | 0.2 | V | 2, 5 |

**Notes:**
1. $V_{REFac}$ is equal to $V_{REFdc}$ plus noise.
2. $V_{IH}$ max and $V_{IL}$ min apply for pulse widths less than one-quarter of the cycle time.
3. Input rise and fall times must be a minimum of 1 V/ns, and within 10% of each other.
4. Applies to: CK, $\overline{CK}$, KD[1.0], $\overline{KD}$[1.0], SA, D[35:0], $\overline{R}$, $\overline{W}$, $\overline{ADZT1}$.
5. Applies to: DLL, RST, RLM[1:0], MZT[1:0], PZT[1:0].

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## Input Electrical Characteristics when MVQ = 1

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| DC Input Reference Voltage | $V_{REFdc}$ | 0.47 * $V_{DDQ}$ | 0.53 * $V_{DDQ}$ | V | — |
| DC Input High Voltage | $V_{IH1dc}$ | $V_{REF}$ + 0.1 | $V_{DDQ}$ + 0.15 | V | 4 |
| DC Input Low Voltage | $V_{IL1dc}$ | –0.15 | $V_{REF}$ – 0.1 | V | 4 |
| DC Input High Voltage | $V_{IH2dc}$ | 0.75 * $V_{DDQ}$ | $V_{DDQ}$ + 0.15 | V | 5 |
| DC Input Low Voltage | $V_{IL2dc}$ | –0.15 | 0.25 * $V_{DDQ}$ | V | 5 |
| AC Input Reference Voltage | $V_{REFac}$ | 0.46 * $V_{DDQ}$ | 0.54 * $V_{DDQ}$ | V | 1 |
| AC Input High Voltage | $V_{IH1ac}$ | $V_{REF}$ + 0.2 | $V_{DDQ}$ + 0.25 | V | 2, 3, 4 |
| AC Input Low Voltage | $V_{IL1ac}$ | –0.25 | $V_{REF}$ – 0.2 | V | 2, 3, 4 |
| AC Input High Voltage | $V_{IH2ac}$ | $V_{DDQ}$ – 0.2 | $V_{DDQ}$ + 0.25 | V | 2, 5 |
| AC Input Low Voltage | $V_{IL2ac}$ | –0.25 | 0.2 | V | 2, 5 |

**Notes:**

1. $V_{REFac}$ is equal to $V_{REFdc}$ plus noise.
2. $V_{IH}$ max and $V_{IL}$ min apply for pulse widths less than one-quarter of the cycle time.
3. Input rise and fall times must be a minimum of 1V/ns, and within 10% of each other.
4. Applies to: CK, $\overline{CK}$, KD[1.0], $\overline{KD}$[1.0], SA, D[35:0], $\overline{R}$, $\overline{W}$, $\overline{ADZT}$1.
5. Applies to: DLL, RST, RLM[1:0], MZT[1:0], PZT[1:0].

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## Input Termination Impedance

| Parameter | Symbol | MZT[1:0] | Min | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Input Termination Impedance when MVQ = 0 | $R_{IN}$ | 01 | RT * 0.85 | RT * 1.15 | Ω | 1, 2, 3 |
| | | 10 | (2*RT) * 0.8 | (2*RT) * 1.2 | | |
| Input Termination Impedance when MVQ = 1 | $R_{IN}$ | 01 | RT * 0.8 | RT * 1.2 | Ω | 1, 2, 3 |
| | | 10 | (2*RT) * 0.75 | (2*RT) * 1.25 | | |

**Notes:**
1. Applies to pull-up and pull-down individually.
2. Parameter applies when 105 ≤ RT ≤ 135.
3. Tested at $V_{IN} = V_{DDQ} * 0.2$ and $V_{DDQ} * 0.8$.

## Output Electrical Characteristics

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| DC Output High Voltage | $V_{OHdc}$ | — | $V_{DDQ}$ + 0.15 | V | 1 |
| DC Output Low Voltage | $V_{OLdc}$ | -0.15 | — | V | 1 |
| AC Output High Voltage | $V_{OHac}$ | — | $V_{DDQ}$ + 0.25 | V | 1 |
| AC Output Low Voltage | $V_{OLac}$ | -0.25 | — | V | 1 |

**Notes:**
1. Parameters apply to: CQ, $\overline{CQ}$, Q, QVLD.

## Output Driver Impedance

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Output Driver Impedance when MVQ = 0 | $R_{OUT}$ | (RQ/5) * 0.9 | (RQ/5) * 1.1 | Ω | 1, 2 |
| Output Driver Impedance when MVQ = 1 | $R_{OUT}$ | (RQ/5) * 0.85 | (RQ/5) * 1.15 | Ω | 1, 2 |

**Notes:**
1. Parameter applies when 175Ω ≤ RQ ≤ 225Ω
2. Tested at $V_{OUT} = V_{DDQ} * 0.2$ and $V_{DDQ} * 0.8$.

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## Leakage Currents

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| Input Leakage Current | $I_{LI1}$ | –2 | 2 | uA | 1, 2 |
| | $I_{LI2}$ | –20 | 2 | uA | 1, 3 |
| | $I_{LI3}$ | –2 | 20 | uA | 1, 4 |
| Output Leakage Current | $I_{LO}$ | –2 | 2 | uA | 5, 6 |

**Notes:**
1. $V_{IN} = V_{SS}$ to $V_{DDQ}$.
2. Parameters apply to CK, $\overline{CK}$, KD, $\overline{KD}$, SA, D, $\overline{R}$, $\overline{W}$, $\overline{ADZT1}$ when input termination is disabled. Parameters apply to RLM, MZT, PZT, MVQ, TCK.
3. Parameters apply to DLL, TMS, TDI (weakly pulled up).
4. Parameters apply to RST (weakly pulled down).
5. $V_{OUT} = V_{SS}$ to $V_{DDQ}$.
6. Parameters apply to Q, CQ, $\overline{CQ}$, QVLD, TDO.

## Operating Currents

| P/N | RL | Operating Frequency | $I_{DD}$ ($V_{DD}$ = 1.25V) | | $I_{DD}$ ($V_{DD}$ = 1.3V) | | $I_{DD}$ ($V_{DD}$ = 1.35V) | | $I_{DD}$ ($V_{DD}$ = 1.4V) | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | x18 | x36 | x18 | x36 | x18 | x36 | x18 | x36 | |
| **GS8673ED18/36BK-675** | 3 | 675 MHz | n/a | n/a | 2030 | 2870 | 2140 | 3010 | 2260 | 3170 | mA |
| | 2 | 450 MHz | | | 1460 | 2020 | 1540 | 2130 | 1630 | 2240 | |
| **GS8673ED18/36BK-625** | 3 | 625 MHz | n/a | n/a | 1900 | 2680 | 2000 | 2820 | 2110 | 2970 | mA |
| | 2 | 400 MHz | | | 1330 | 1830 | 1410 | 1930 | 1490 | 2030 | |
| **GS8673ED18/36BK-550** | 3 | 550 MHz | 1630 | 2290 | 1720 | 2410 | 1820 | 2540 | 1930 | 2670 | mA |
| | 2 | 375 MHz | 1190 | 1640 | 1270 | 1730 | 1340 | 1830 | 1420 | 1930 | |
| **GS8673ED18/36BK-500** | 3 | 500 MHz | 1490 | 2090 | 1580 | 2200 | 1670 | 2320 | 1770 | 2440 | mA |
| | 2 | 333 MHz | 1090 | 1490 | 1160 | 1570 | 1230 | 1670 | 1300 | 1750 | |

**Notes:**
1. $I_{OUT}$ = 0 mA; $V_{IN} = V_{IH}$ or $V_{IL}$.
2. Applies at 50% Reads + 50% Writes.

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## AC Test Conditions for 1.2V nominal $V_{DDQ}$ (MVQ = 0)

| Parameter | Symbol | Conditions | Units |
|---|---|---|---|
| Core Supply Voltage: -675 and -625 speed bins | $V_{DD}$ | 1.3 to 1.4 | V |
| Core Supply Voltage: -550 and -500 speed bins | $V_{DD}$ | 1.25 to 1.4 | V |
| I/O Supply Voltage | $V_{DDQ}$ | 1.15 to 1.25 | V |
| Input Reference Voltage | $V_{REF}$ | 0.6 | V |
| Input High Level | $V_{IH}$ | 0.9 | V |
| Input Low Level | $V_{IL}$ | 0.3 | V |
| Input Rise and Fall Time | — | 2.0 | V/ns |
| Input and Output Reference Level | — | 0.6 | V |

**Note:**
Output Load Conditions RQ = 200Ω. Refer to figure below.

## AC Test Conditions for 1.5V nominal $V_{DDQ}$ (MVQ = 1)

| Parameter | Symbol | Conditions | Units |
|---|---|---|---|
| Core Supply Voltage: -675 and -625 speed bins | $V_{DD}$ | 1.3 to 1.4 | V |
| Core Supply Voltage: -550 and -500 speed bins | $V_{DD}$ | 1.25 to 1.4 | V |
| I/O Supply Voltage | $V_{DDQ}$ | 1.4 to 1.6 | V |
| Input Reference Voltage | $V_{REF}$ | 0.75 | V |
| Input High Level | $V_{IH}$ | 1.25 | V |
| Input Low Level | $V_{IL}$ | 0.25 | V |
| Input Rise and Fall Time | — | 2.0 | V/ns |
| Input and Output Reference Level | — | 0.75 | V |

**Note:**
Output Load Conditions RQ = 200Ω. Refer to figure below.

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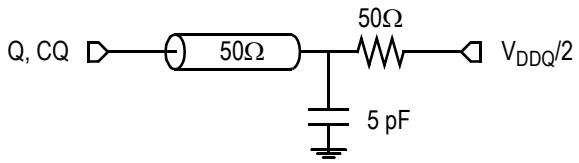
### AC Test Output Load

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## AC Electrical Characteristics (independent of device speed grade)

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| **Input Clock Timing** | | | | | |
| Clk High Pulse Width | $t_{KHKL}$ | 0.45 | — | cycles | 1 |
| Clk Low Pulse Width | $t_{KLKH}$ | 0.45 | — | cycles | 1 |
| Clk High to $\overline{\text{Clk}}$ High | $t_{KH\overline{K}H}$ | 0.45 | 0.55 | cycles | 2 |
| Clk High to Write Data Clk High | $t_{KHKDH}$ | -200 | 200 | ps | 3 |
| DLL Lock Time | $t_{Klock}$ | 65,536 | — | cycles | 4 |
| Clk Static to DLL Reset | $t_{Kreset}$ | 30 | — | ns | 5,11 |
| **Output Timing** | | | | | |
| Clk High to Data Output Valid | $t_{KHQV}$ | — | 400 | ps | 6 |
| Clk High to Data Output Hold | $t_{KHQX}$ | -400 | — | ps | 6 |
| Clk High to Data Output High-Z | $t_{KHQHZ}$ | — | 400 | ps | 7 |
| Clk High to Data Output Low-Z | $t_{KHQLZ}$ | -400 | — | ps | 7 |
| Clk High to Echo Clock High | $t_{KHCQH}$ | -400 | 400 | ps | 8 |
| Echo Clk High to $\overline{\text{Echo Clock}}$ High | $t_{CQH\overline{CQ}H}$ | $t_{KH\overline{K}H}$ (min) - 50 | $t_{KH\overline{K}H}$ (max) + 50 | ps | 9,11 |
| $\overline{\text{Echo Clk}}$ High to Echo Clock High | $t_{\overline{CQ}HCQH}$ | $t_{\overline{K}HKH}$ (min) - 50 | $t_{\overline{K}HKH}$ (max) + 50 | ps | 10,11 |

**Notes:**

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal unless otherwise noted.

1. Parameters apply to CK, $\overline{\text{CK}}$, KD, $\overline{\text{KD}}$.
2. Parameter specifies ↑CK → ↑$\overline{\text{CK}}$ and ↑KD → ↑$\overline{\text{KD}}$ requirements.
3. Parameter specifies ↑CK → ↑KD and ↑$\overline{\text{CK}}$ → ↑$\overline{\text{KD}}$ requirements.
4. $V_{DD}$ slew rate must be < 0.1V DC per 50ns for DLL lock retention. DLL lock time begins once $V_{DD}$ and input clock are stable.
5. Parameter applies to CK.
6. Parameters apply to Q, and are referenced to ↑CK.
7. Parameters apply to Q when MZT[1:0] = 00, and are referenced to ↑CK. They are measured at ± 50 mV from steady state voltage.
8. Parameter specifies ↑CK → ↑CQ timing.
9. Parameter specifies ↑CQ → ↑$\overline{\text{CQ}}$ timing. $t_{KH\overline{K}H}$ (min) and $t_{KH\overline{K}H}$ (max) are the minimum and maximum input delays from ↑CK to ↑$\overline{\text{CK}}$ applied to the device, as determined by the Absolute Jitter associated with those clock edges.
10. Parameter specifies ↑$\overline{\text{CQ}}$ → ↑CQ timing. $t_{\overline{K}HKH}$ (min) and $t_{\overline{K}HKH}$ (max) are the minimum and maximum input delays from ↑$\overline{\text{CK}}$ to ↑CK applied to the device, as determined by the Absolute Jitter associated with those clock edges.
11. Parameters are not tested. They are guaranteed by design, and verified through extensive corner-lot characterization.

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## AC Electrical Characteristics (variable with device speed grade)

| Parameter | Symbol | –675 | | –625 | | –550 | | –500 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| **Input Clock Timing** | | | | | | | | | | | |
| Clk Cycle Time | $t_{KHKH}$ | 1.48 | 6.0 | 1.6 | 6.0 | 1.8 | 6.0 | 2.0 | 6.0 | ns | 1,2 |
| | | 2.2 | 6.0 | 2.5 | 6.0 | 2.66 | 6.0 | 3.0 | 6.0 | ns | 1,3 |
| Clk Cycle-to-Cycle Jitter | $t_{KJITcc}$ | — | 60 | — | 60 | — | 60 | — | 60 | ps | 1,4,5 |
| **Input Setup and Hold Timing** | | | | | | | | | | | |
| Address Input Valid to Clk High | $t_{AVKH}$ | 190 | — | 210 | — | 230 | — | 250 | — | ps | 6 |
| Control Input Valid to Clk High | $t_{IVKH}$ | 190 | — | 210 | — | 230 | — | 250 | — | ps | 7 |
| Data Input Valid to Clk High | $t_{DVKH}$ | 150 | — | 160 | — | 180 | — | 200 | — | ps | 8 |
| Clk High to Address Input Hold | $t_{KHAX}$ | 190 | — | 210 | — | 230 | — | 250 | — | ps | 6 |
| Clk High to Control Input Hold | $t_{KHIX}$ | 190 | — | 210 | — | 230 | — | 250 | — | ps | 7 |
| Clk High to Data Input Hold | $t_{KHDX}$ | 150 | — | 160 | — | 180 | — | 200 | — | ps | 8 |
| **Output Timing** | | | | | | | | | | | |
| Echo Clk High to Data Output Valid | $t_{CQHQV}$ | — | 150 | — | 150 | — | 150 | — | 150 | ps | 9,10 |
| Echo Clk High to Data Output Hold | $t_{CQHQX}$ | -150 | — | -150 | — | -150 | — | -150 | — | ps | 9,10 |

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**Notes:**

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal.

1. Parameters apply to CK, $\overline{CK}$, KD, $\overline{KD}$.
2. Parameter applies when RL=3.
3. Parameter applies when RL=2.
4. Parameter specifies *Cycle-to-Cycle (C2C) Jitter* (i.e. the maximum variation from clock rising edge to the next clock rising edge). As such, it limits *Period Jitter* (i.e. the maximum variation in clock cycle time from nominal) to ± 30ps. And as such, it limits *Absolute Jitter* (i.e. the maximum variation in clock rising edge from its nominal position) to ± 15ps.
5. The device can tolerated C2C Jitter greater than 60ps, up to a maximum of 200ps. However, when using a device from a particular speed bin, $t_{KHKH}$ (min) of that speed bin must be derated (increased) by half the difference between the actual C2C Jitter and 60ps. For example, if the actual C2C Jitter is 100ps, then $t_{KHKH}$ (min) for the -675 speed bin (RL=3) is derated to 1.5ns (1.48ns + 0.5*(100ps - 60ps)).
6. Parameters apply to SA, and are referenced to ↑CK.
7. Parameters apply to $\overline{R}$, $\overline{W}$, $\overline{ADZT1}$, and are referenced to ↑CK.
8. Parameters apply to D, and are referenced to ↑KD & ↑$\overline{KD}$.
9. Parameters apply to Q, QVLD and are referenced to ↑CQ & ↑$\overline{CQ}$.
10. Parameters are not tested. They are guaranteed by design, and verified through extensive corner-lot characterization.

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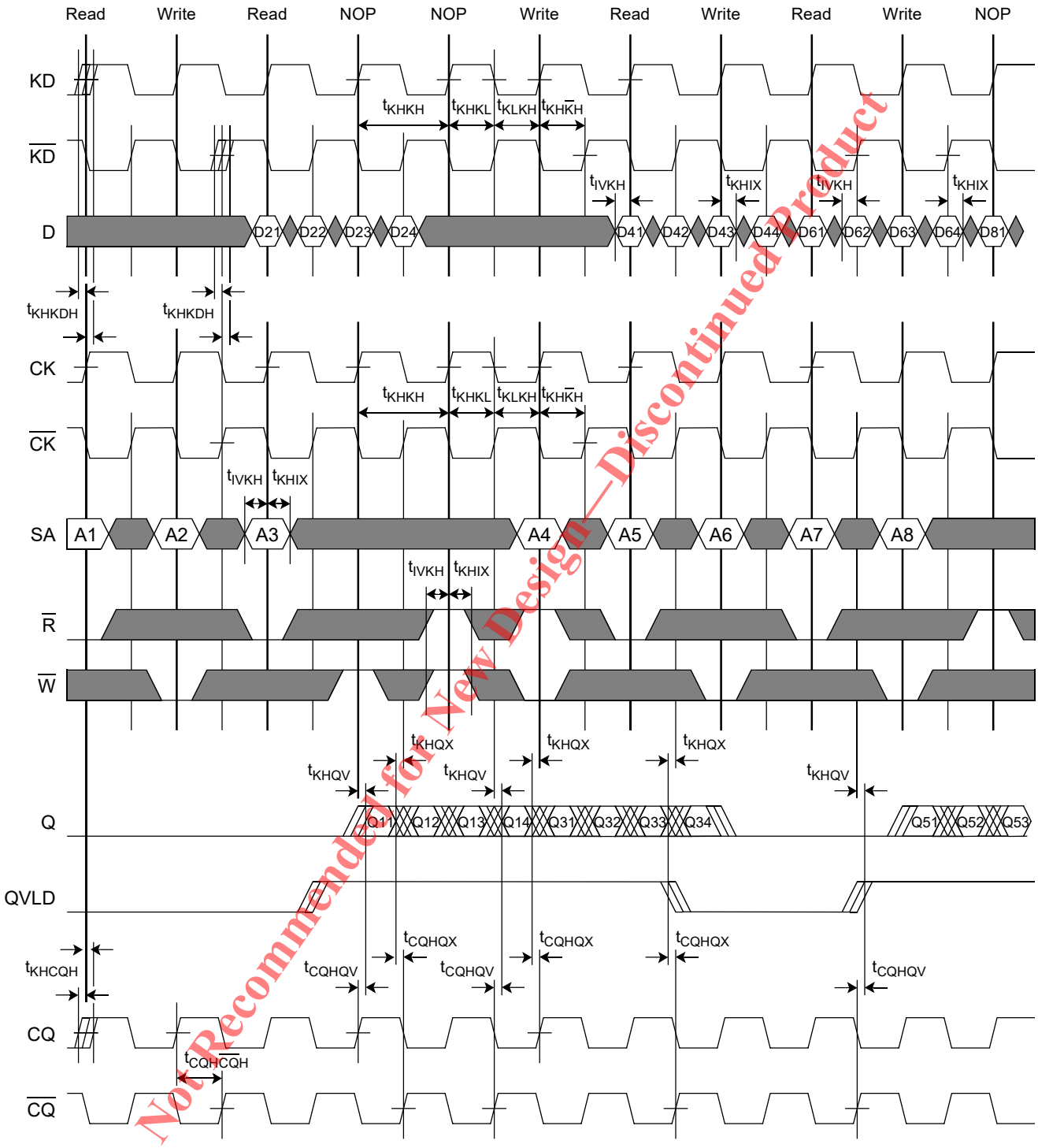
## SigmaQuad-IIIe Burst of 4, RL = 3

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**Note: The Q state during non-Reads depicted in this diagram (Q=Low) applies when D input termination is enabled (MZT=01 or 10). When D input termination is disabled (MZT=00), the Q state during non-Reads is High-Z.**

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## JTAG Test Mode Description

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), ECCRAM, other components, and the printed circuit board. In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and multiple TAP Registers. The TAP Registers consist of one Instruction Register and multiple Data Registers.

The TAP consists of the following four signals:

| Pin | Pin Name | I/O | Description |
|---|---|---|---|
| TCK | Test Clock | I | Induces (clocks) TAP Controller state transitions. |
| TMS | Test Mode Select | I | Inputs commands to the TAP Controller. Sampled on the rising edge of TCK. |
| TDI | Test Data In | I | Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK. |
| TDO | Test Data Out | O | Outputs data serially from the TAP Registers. Driven from the falling edge of TCK. |

### Concurrent TAP and Normal ECCRAM Operation

According to IEEE std. 1149.1, most public TAP Instructions do not disrupt normal device operation. In these devices, the only exceptions are EXTEST and SAMPLE-Z. See the Tap Registers section for more information.

### Disabling the TAP

When JTAG is not used, TCK should be tied Low to prevent clocking the ECCRAM. TMS and TDI should either be tied High through a pull-up resistor or left unconnected. TDO should be left unconnected.

## JTAG DC Operating Conditions

| Parameter | Symbol | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| JTAG Input High Voltage | $V_{TIH}$ | 0.75 * $V_{DDQ}$ | $V_{DDQ}$ + 0.15 | V | 1 |
| JTAG Input Low Voltage | $V_{TIL}$ | –0.15 | 0.25 * $V_{DDQ}$ | V | 1 |
| JTAG Output High Voltage | $V_{TOH}$ | $V_{DDQ}$ – 0.2 | — | V | 2, 3 |
| JTAG Output Low Voltage | $V_{TOL}$ | — | 0.2 | V | 2, 4 |

**Notes:**

1. Parameters apply to TCK, TMS, and TDI during JTAG Testing.
2. Parameters apply to TDO during JTAG testing.
3. $I_{TOH}$ = –2.0 mA.
4. $I_{TOL}$ = 2.0 mA.

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## JTAG AC Timing Specifications

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| TCK Cycle Time | $t_{THTH}$ | 50 | — | ns |
| TCK High Pulse Width | $t_{THTL}$ | 20 | — | ns |
| TCK Low Pulse Width | $t_{TLTH}$ | 20 | — | ns |
| TMS Setup Time | $t_{MVTH}$ | 10 | — | ns |
| TMS Hold Time | $t_{THMX}$ | 10 | — | ns |
| TDI Setup Time | $t_{DVTH}$ | 10 | — | ns |
| TDI Hold Time | $t_{THDX}$ | 10 | — | ns |
| Capture Setup Time (Address, Control, Data, Clock) | $t_{CS}$ | 10 | — | ns |
| Capture Hold Time (Address, Control, Data, Clock) | $t_{CH}$ | 10 | — | ns |
| TCK Low to TDO Valid | $t_{TLQV}$ | — | 10 | ns |
| TCK Low to TDO Hold | $t_{TLQX}$ | 0 | — | ns |

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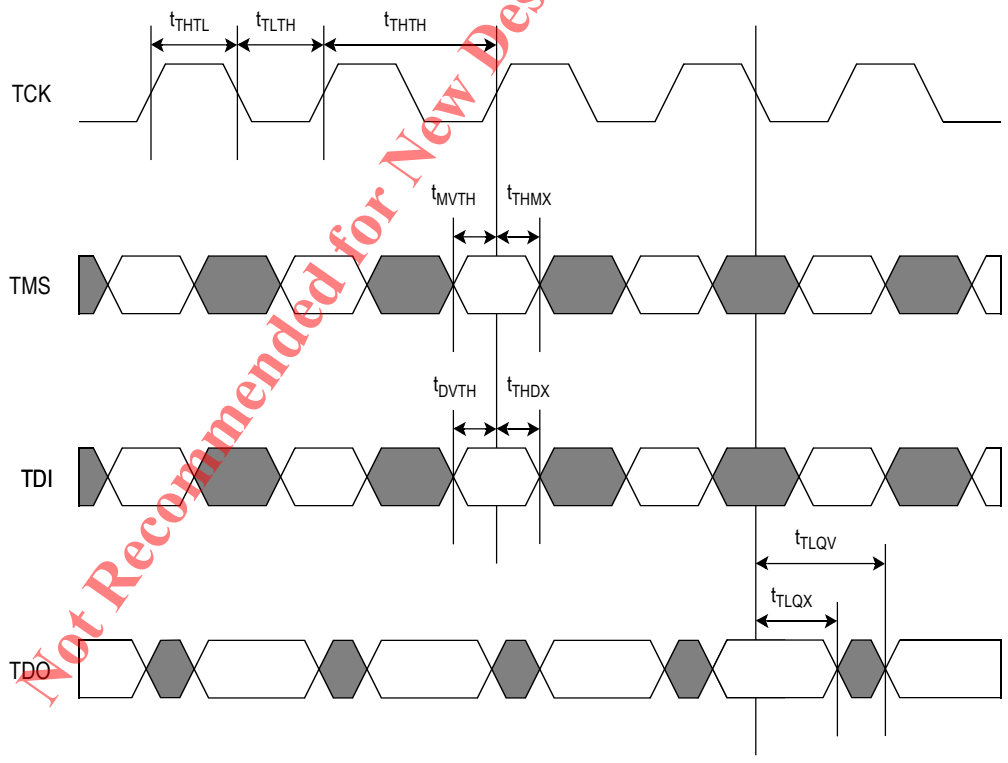
### JTAG Timing Diagram

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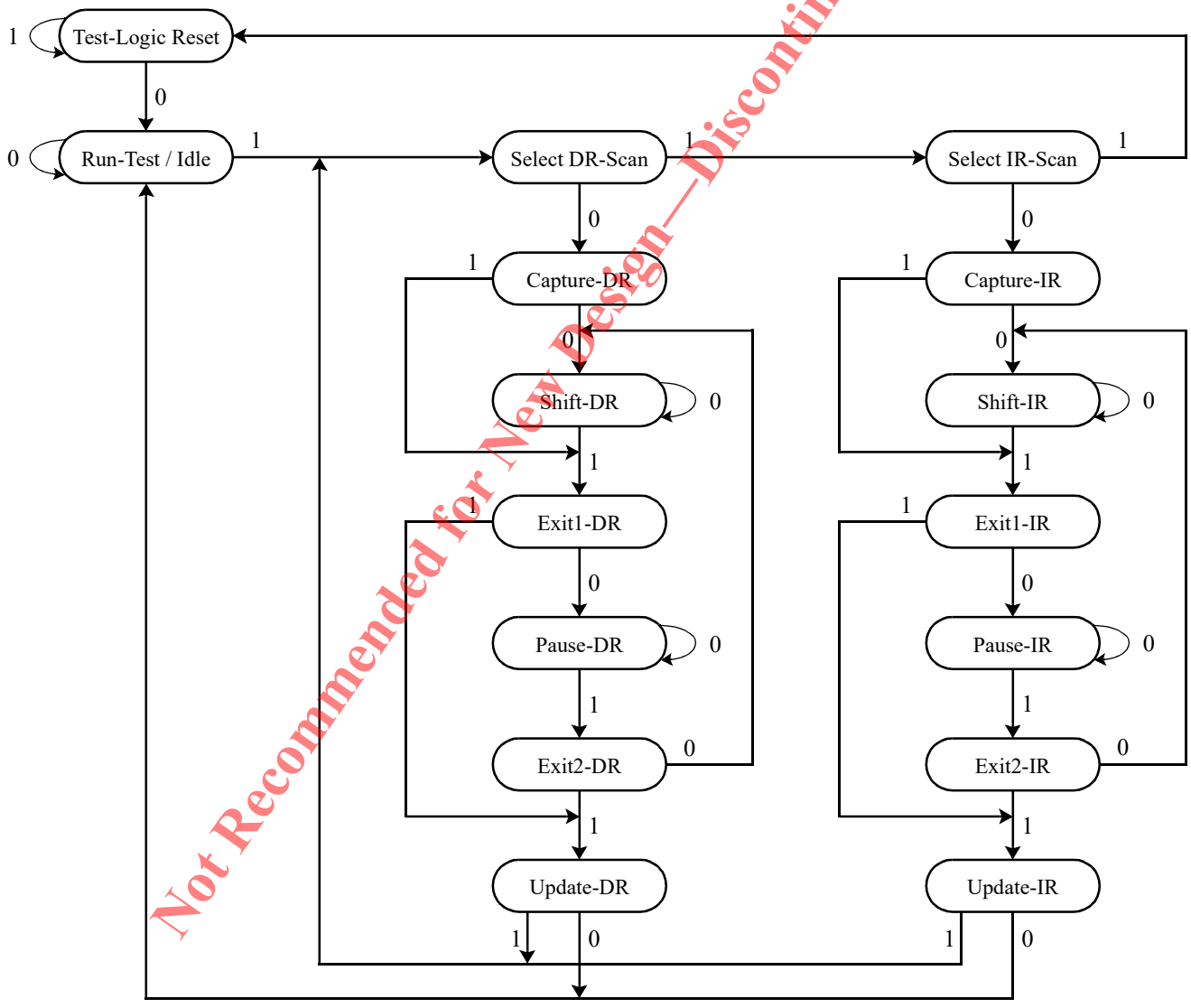
## TAP Controller

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction. State transitions are controlled by TMS and occur on the rising edge of TCK.
The TAP Controller enters the Test-Logic Reset state in one of two ways:

1. At power up.
2. When a logic 1 is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state.
The TDO output driver is enabled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state.

### TAP Controller State Diagram

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## TAP Registers

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) on the subsequent falling edge of TCK. They are divided into two groups: Instruction Registers (IR), which are manipulated via the IR states in the TAP Controller, and Data Registers (DR), which are manipulated via the DR states in the TAP Controller.

### Instruction Register (IR—3 bits)

The Instruction Register stores the various TAP Instructions supported by ECCRAM. It is loaded with the IDCODE instruction (logic 001) at power-up, and when the TAP Controller is in the Test-Logic Reset and Capture-IR states. It is inserted between TDI and TDO when the TAP Controller is in the Shift-IR state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed until the TAP Controller has reached the Update-IR state.

The Instruction Register is 3 bits wide, and is encoded as follows:

| Code (2:0) | Instruction | Description |
|---|---|---|
| 000 | EXTEST | Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>Also transfers the contents of the Boundary Scan Register associated with all output signals (Q, QVLD, CQ, $\overline{CQ}$) directly to their corresponding output pins. However, newly loaded Boundary Scan Register contents do not appear at the output pins until the TAP Controller has reached the Update-DR state.<br>Also disables all input termination.<br>See the Boundary Scan Register description for more information. |
| 001 | IDCODE | Loads a predefined device- and manufacturer-specific identification code into the ID Register when the TAP Controller is in the Capture-DR state, and inserts the ID Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>See the ID Register description for more information. |
| 010 | SAMPLE-Z | Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>Also disables all input termination.<br>See the Boundary Scan Register description for more information. |
| 011 | PRIVATE | Reserved for manufacturer use only. |
| 100 | SAMPLE | Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>See the Boundary Scan Register description for more information. |
| 101 | PRIVATE | Reserved for manufacturer use only. |
| 110 | PRIVATE | Reserved for manufacturer use only. |
| 111 | BYPASS | Loads a logic 0 into the Bypass Register when the TAP Controller is in the Capture-DR state, and inserts the Bypass Register between TDI and TDO when the TAP Controller is in the Shift-DR state.<br>See the Bypass Register description for more information. |

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### Bypass Register (DR—1 bit)

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic 0 when the BYPASS instruction has been loaded in the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

### ID Register (DR—32 bits)

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

The ID Register is 32 bits wide, and is encoded as follows:

| See BSDL Model (31:12) | GSI ID (11:1) | Start Bit (0) |
|---|---|---|
| XXXX XXXX XXXX XXXX XXXX | 0001 1011 001 | 1 |

Bit 0 is the LSB of the ID Register, and Bit 31 is the MSB. When the ID Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

### Boundary Scan Register (DR—127 bits)

The Boundary Scan Register is equal in length to the number of active signal connections to the ECCRAM (excluding the TAP pins) plus a number of place holder locations reserved for functional and/or density upgrades. It is loaded with the logic states of all signals composing the ECCRAM's I/O ring when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

Additionally, the contents of the Boundary Scan Register associated with the ECCRAM outputs (Q, QVLD, CQ, $\overline{CQ}$) are driven directly to the corresponding ECCRAM output pins when the EXTEST instruction is selected. However, after the EXTEST instruction has been selected, any new data loaded into Boundary Scan Register when the TAP Controller is in the Shift-DR state does not appear at the output pins until the TAP Controller has reached the Update-DR state.

The value captured in the boundary scan register for NU pins is determined by the external pin state while the NC pins are 0 regardless of the external pin state. The value captured in the internal cells is 1.

### Output Driver State During EXTEST

EXTEST allows the Internal Cell (Bit 127) in the Boundary Scan Register to control the state of Q drivers. That is, when Bit 127 = 1, Q drivers are enabled (i.e., driving High or Low), and when Bit 127 = 0, Q drivers are disabled (i.e., forced to High-Z state). See the Boundary Scan Register section for more information.

### Input Termination State During EXTEST and SAMPLE-Z

Input termination on all inputs is disabled during EXTEST and SAMPLE-Z.

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**Boundary Scan Register Bit Order Assignment**

The table below depicts the order in which the bits are arranged in the Boundary Scan Register. Bit 1 is the LSB and Bit 127 is the MSB. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

| Bit | Pad | Bit | Pad | Bit | Pad | Bit | Pad | Bit | Pad |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 7L | 29 | 11G | 57 | 10W | 85 | 4R | 113 | 3C |
| 2 | 7K | 30 | 13G | 58 | 8V | 86 | 2R | 114 | 2B |
| 3 | 9L | 31 | 10G | 59 | 9U | 87 | 3P | 115 | 4B |
| 4 | 9K | 32 | 12G | 60 | 8T | 88 | 1P | 116 | 6A |
| 5 | 8J | 33 | 11H | 61 | 9R | 89 | 4P | 117 | 6B |
| 6 | 7H | 34 | 13H | 62 | 8P | 90 | 2P | 118 | 6C |
| 7 | 9H | 35 | 10J | 63 | 9N | 91 | 3N | 119 | 5D |
| 8 | 7G | 36 | 12J | 64 | 8M | 92 | 1N | 120 | 6E |
| 9 | 8G | 37 | 13K | 65 | 6M | 93 | 4M | 121 | 5F |
| 10 | 9F | 38 | 13L | 66 | 7N | 94 | 2M | 122 | 6G |
| 11 | 8E | 39 | 11L | 67 | 5N | 95 | 3L | 123 | 5H |
| 12 | 7D | 40 | 12M | 68 | 7P | 96 | 1L | 124 | 6J |
| 13 | 9D | 41 | 10M | 69 | 6P | 97 | 1K | 125 | 5K |
| 14 | 8C | 42 | 13N | 70 | 5R | 98 | 2J | 126 | 5L |
| 15 | 8B | 43 | 11N | 71 | 6T | 99 | 4J | 127 | Internal |
| 16 | 9B | 44 | 12P | 72 | 7U | 100 | 1H | | |
| 17 | 7A | 45 | 10P | 73 | 5U | 101 | 3H | | |
| 18 | 9A | 46 | 13P | 74 | 6V | 102 | 2G | | |
| 19 | 10B | 47 | 11P | 75 | 6W | 103 | 4G | | |
| 20 | 12B | 48 | 12R | 76 | 7Y | 104 | 1G | | |
| 21 | 11C | 49 | 10R | 77 | 4W | 105 | 3G | | |
| 22 | 13C | 50 | 13T | 78 | 2W | 106 | 2F | | |
| 23 | 10D | 51 | 11T | 79 | 3V | 107 | 4F | | |
| 24 | 12D | 52 | 12U | 80 | 1V | 108 | 1E | | |
| 25 | 11E | 53 | 10U | 81 | 4U | 109 | 3E | | |
| 26 | 13E | 54 | 13V | 82 | 2U | 110 | 2D | | |
| 27 | 10F | 55 | 11V | 83 | 3T | 111 | 4D | | |
| 28 | 12F | 56 | 12W | 84 | 1T | 112 | 1C | | |

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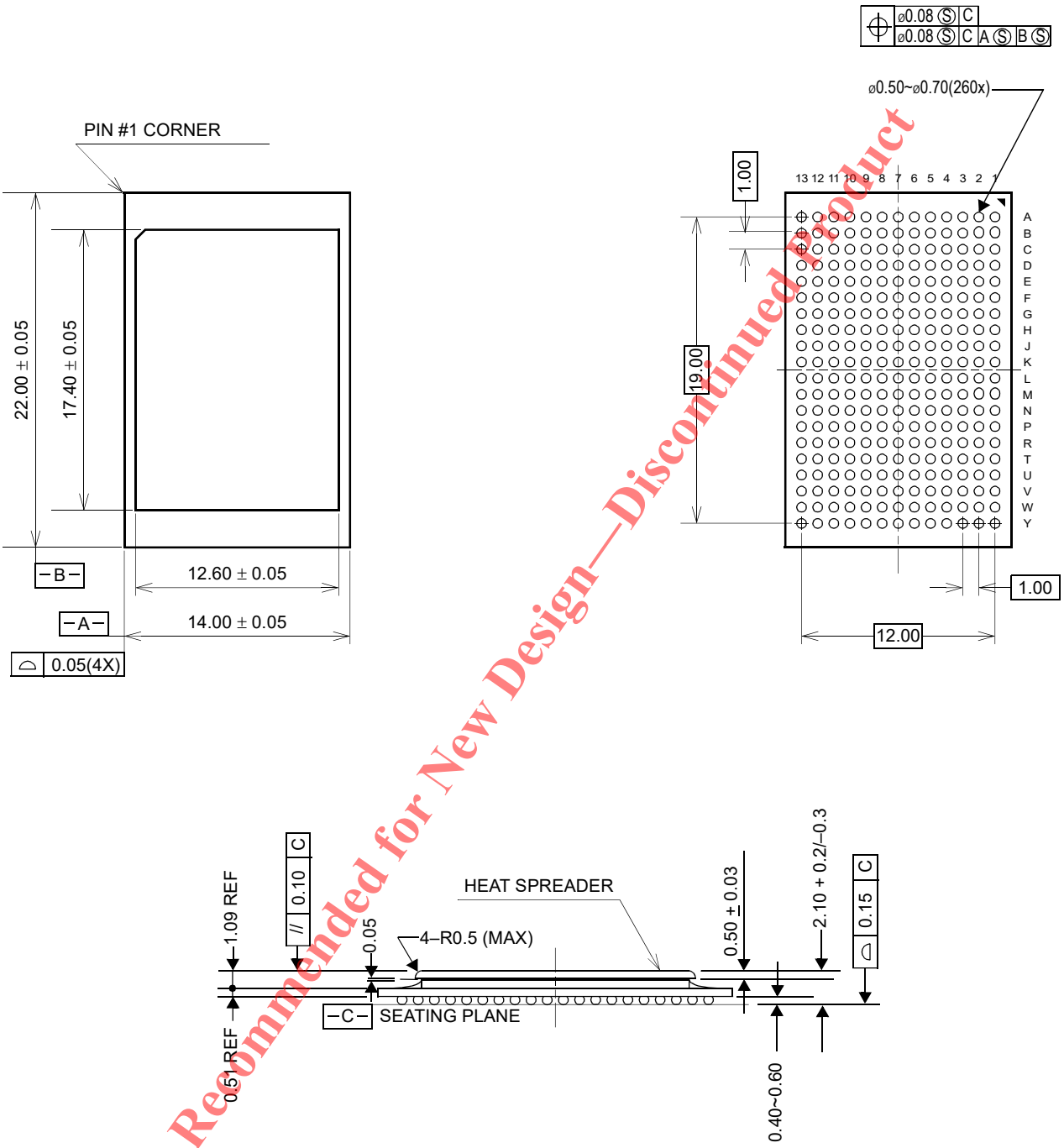
## 260-Pin BGA Package Drawing (Package K)

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| | | | |
|---|---|---|---|
| Ball Pitch: | 1.00 | Substrate Thickness: | 0.51 |
| Ball Diameter: | 0.60 | Mold Thickness: | — |

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## Ordering Information—GSI SigmaQuad-IIIe ECCRAM

| Org | Part Number | Type | Package | Status | Speed (MHz) | $T_A$ |
|---|---|---|---|---|---|---|
| 4M x 18 | GS8673ED18BK-675 | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 675 | C |
| 4M x 18 | GS8673ED18BK-625 | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 625 | C |
| 4M x 18 | GS8673ED18BK-550 | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 550 | C |
| 4M x 18 | GS8673ED18BK-500 | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 500 | C |
| 4M x 18 | GS8673ED18BK-675I | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 675 | I |
| 4M x 18 | GS8673ED18BK-625I | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 625 | I |
| 4M x 18 | GS8673ED18BK-550I | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 550 | I |
| 4M x 18 | GS8673ED18BK-500I | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 500 | I |
| 2M x 36 | GS8673ED36BK-675 | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 675 | C |
| 2M x 36 | GS8673ED36BK-625 | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 625 | C |
| 2M x 36 | GS8673ED36BK-550 | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 550 | C |
| 2M x 36 | GS8673ED36BK-500 | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 500 | C |
| 2M x 36 | GS8673ED36BK-675I | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 675 | I |
| 2M x 36 | GS8673ED36BK-625I | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 625 | I |
| 2M x 36 | GS8673ED36BK-550I | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 550 | I |
| 2M x 36 | GS8673ED36BK-500I | SigmaQuad-IIIe B4 ECCRAM | 260-ball BGA | Qual | 500 | I |

**Notes:** C = Commercial Temperature Range. I = Industrial Temperature Range.

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## Revision History

| Rev. Code | Types of Changes Format or Content | Revisions |
|---|---|---|
| GS8673ED1836BK_r1 | | • Creation of new datasheet |
| GS8673ED1836BK_r1_01 | Content | • Changed speed bins to 625, 550, & 500 MHz.<br>• Increased $V_{DD}$ (min) spec from 1.25V to 1.3V for 625 MHz speed bin.<br>• Improved $t_{KHQV}$ / $t_{KHQX}$ specs from +/-500ps to +/-400ps.<br>• Updated the Low Power NOP Mode section. |
| GS8673ED1836BK_r1_02 | Content | • Added 675 MHz speed bin.<br>• Updated to MP status. |

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## Revision History

| Rev. Code | Types of Changes Format or Content | Revisions |
|---|---|---|
| GS8673ED1836BK_r1_02a | Content | • Re-added $t_{KHKH}$ (max) specs (previously inadvertently deleted).<br>• Updated $I_{DD}$ specs. |
| GS8673ED1836BK_r1_03 | Content | • Added part numbers for lead-free RoHS-compliant BGA package. |
| GS8673ED1836BK_r1_04 | Content | • Updated Addressing Schemes section, and moved to p.1.<br>• Updated Absolute Maximum Ratings.<br>• Updated Input Electrical Characteristics.<br>• Corrected JTAG BScan Register bit order. |
| GS8673ED1836BK_r1_05 | Content | • Updated status of lead-free RoHS-compliant BGA pkg to “Qual”. |
| GS8673ED1836BK_r1_06 | Content | • Updated Absolute Maximum Ratings.<br>• Updated Recommended Operating Conditions.<br>• Updated AC Electrical Specifications:<br>Updated $t_{CQHC\overline{Q}H}$ spec, and associated note.<br>Added $t_{\overline{C}QHCQH}$ and $t_{KJITcc}$ specs, and associated notes.<br>Removed $t_{Kvar}$ and $t_{CQvar}$ specs. |
| GS8673ED1836BK_r1_07 | Content | • Changed Junction Temp to Max Junction Temp in AbsMax table |
| GS8673ED1836BK_r1_08 | Content | • Separated non-RoHS and RoHS-compliant into two datasheets |

Not Recommended for New Design–Discontinued Product

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Живое партнерство

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