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performance
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design.**

Datasheet: AS8222 Enhanced FlexRay Standard Transceiver

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AS8222

Enhanced FlexRay Standard Transceiver

1 General Description

The AS8222 is a high-speed fault tolerant device operating as interface between a generic FlexRay Communication Controller and the copper wiring.

This device is the first FlexRay certified Transceiver for temperature ranges up to 150°C ambient temperature. For bare-die deliveries please contact ams for more information.

The AS8222 is designed to extend the application range for high speed and safety critical time triggered bus systems in an automotive environment. The bus driver is protected against short circuits to the supply and GND. The AS8222 operates at baudrates up to 10 Mbps and is fully conforming to the FlexRay Electrical Physical Layer Specification V2.1 Rev B.

The AS8222 provides a host controller interface consisting of Enable (EN) and Standby (STBN) input pins for mode handling by the microcontroller and the Error (ERRN) output pin, signalling failures and status information.

The device supports the NORMAL mode with activated FlexRay bus transmitter and receiver, the RECEIVE_ONLY mode with activated receiver only to avoid unwanted disturbances while listening to the communication and the low-power modes STANDBY and SLEEP with very low power consumption.

In case of undervoltage at one of the supply voltages (VBAT, VCC, and VIO) the device will change its mode to a low-power mode (either STANDBY or SLEEP mode) and the device will signal an error accordingly. In case of low voltage is detected on both VBAT and VCC the device will enter the POWER-OFF mode.

Ensuring application in safety critical environments a two wire bus-guardian interface is implemented where additional redundant circuitries on the electronic-control-unit can monitor the communication on the receive enable output (RxEN) and can activate and deactivate through the bus guardian enable input (BGE) the transmitter. Additionally in low-power modes the wake conditions at the RxEN pin can be monitored.

A thermal sensor circuit with an integral shutdown mechanism prevents damage to the device in extreme temperature conditions.

2 Key Features

- Data transfer up to 10 Mbps
- Compliant with FlexRay Electrical Physical Layer Specification V2.1 Rev. B
- **Wide operating ambient temperature range -40°C to +150°C**
- Excellent EMC performance
- High common mode range insures excellent EMI immunity

- Interface with optional bus guardian for bus supervision
- Automatic thermal shutdown protection
- Supports 12, 24V systems with low sleep current consumption
- Integrated power management system
- Two INH pins for the external voltage regulators control
- Local wake-up input
- Remote wake-up capability via FlexRay bus in sleep mode
- Supports 2.5, 3, 3.3, 5 V microcontrollers and automatically adapts to interface levels
- Does not disturb the bus line if not powered
- Protected against damage due to short circuit conditions on the bus (positive and negative battery voltage)
- Small Pb-free package: SSOP-20
- Automotive qualified to AEC-Q100, grade 0
- For bare-die deliveries please contact us.

3 Applications

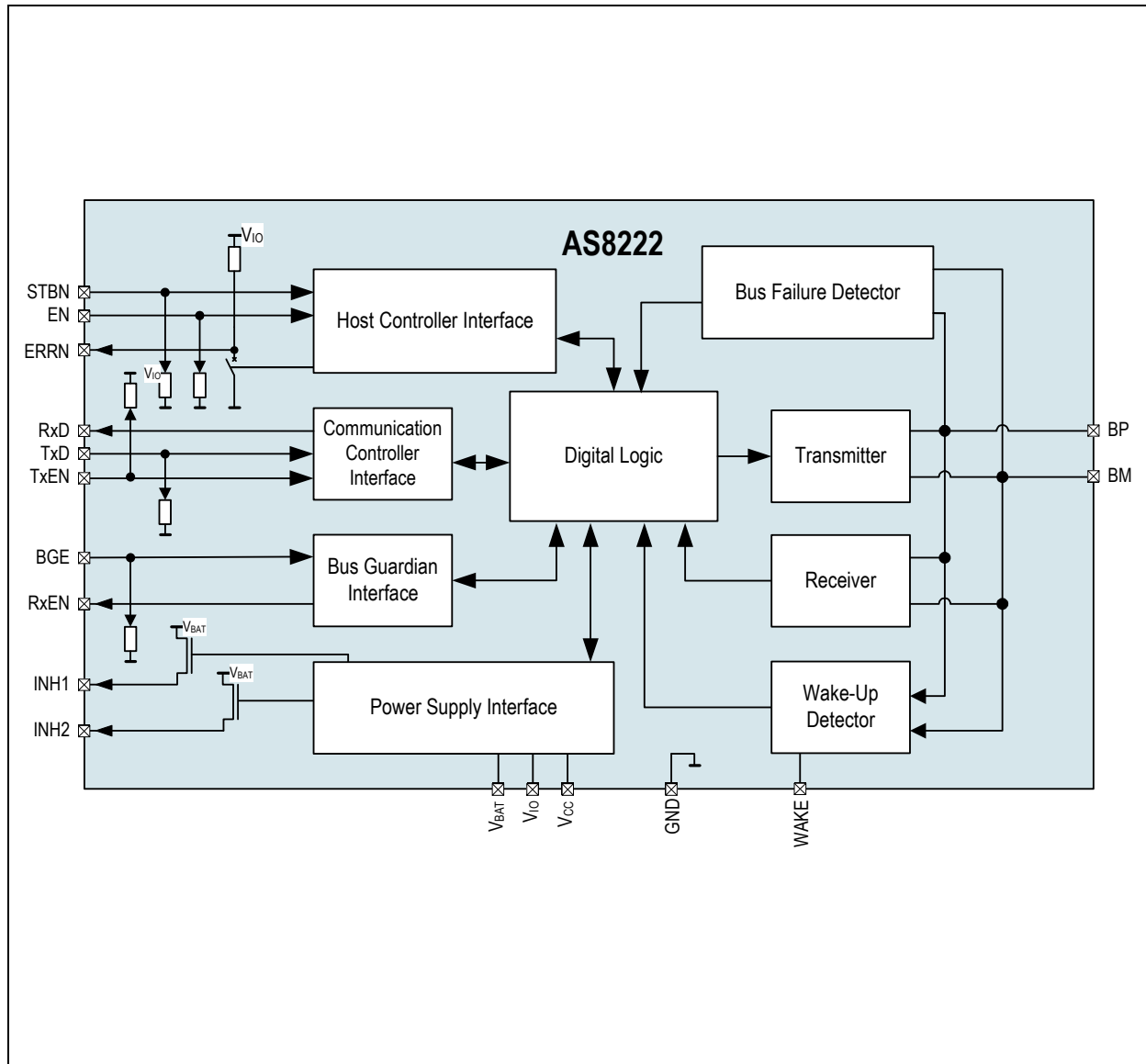
The AS8222 FlexRay Standard Transceiver is best fitting for automotive FlexRay nodes where bus wake-up and voltage regulator control for voltage supplies is needed.

The device addresses all ECUs connected to the permanent battery supply (terminal 30).

The device is best suited for high temperature applications with up to 150°C.



Figure 1. AS8222 Enhanced FlexRay Standard Transceiver Block Diagram





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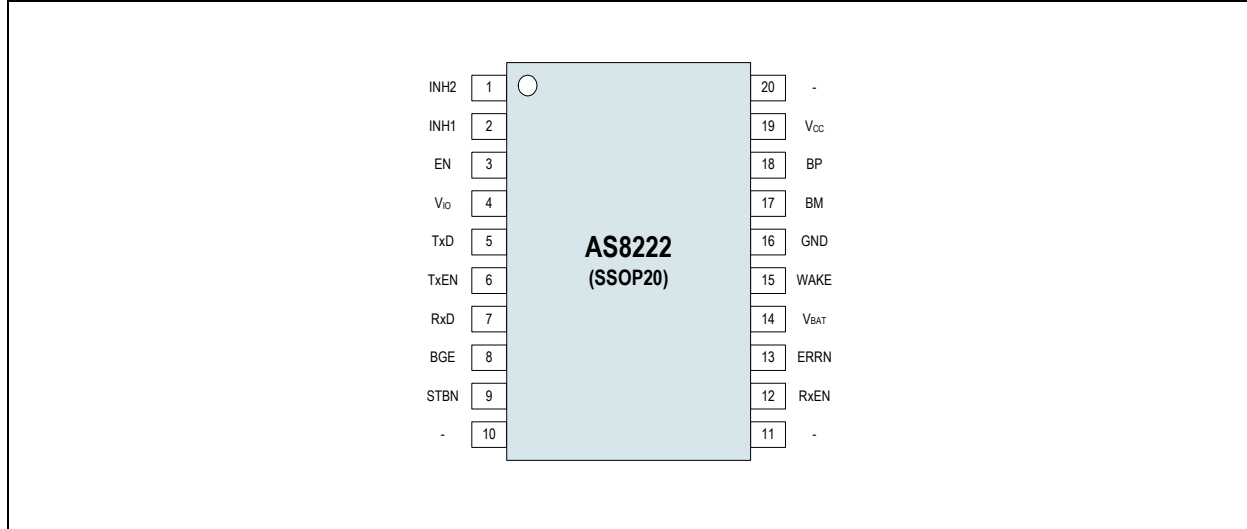
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4 Pin Assignments

The AS8222 is available in SSOP-20 5.3mm.

Figure 2. Pin Assignments (Top View)



4.1 Pin Descriptions

Table 1. SSOP-20 Pin Descriptions

| Pin Name | Pin Number | Pin Type | Description |
|-----------------|------------|--|--|
| INH2 | 1 | Analog I/O | Analog Output. Inhibit 2 output for switching external voltage regulator |
| INH1 | 2 | | Analog Output. Inhibit 1 output for switching external voltage regulator |
| EN | 3 | Digital Input with Pull-down | Digital Input. Enable input |
| V _{io} | 4 | Supply | Supply Voltage. I/O supply voltage |
| TxD | 5 | Digital Input with Pull-down | Digital Input. Transmit data input |
| TxEN | 6 | Digital Input with Pull-up | Digital Input. Transmitter enable input |
| RxD | 7 | Digital Output | Digital Output. Receive data output |
| BGE | 8 | Digital Input with Pull-down | Digital Input. Bus guardian enable input |
| STBN | 9 | | Digital Input. Standby input |
| Reserved | 10 | Analog/digital Input/output with Pull-down | To be connected to GND or to be unconnected |
| Not used | 11 | - | - |
| RxEN | 12 | Digital Output | Digital Output. Receive data enable output |
| ERRN | 13 | | Digital Output. Error diagnosis output and wake status output |
| VBAT | 14 | Supply | Supply Voltage. Battery supply voltage |
| WAKE | 15 | Analog I/O | Analog Input. Local wake-up input |
| GND | 16 | Supply | Ground |
| BM | 17 | Analog I/O | Analog Input/Output. Bus line Minus |
| BP | 18 | | Analog Input/Output. Bus line Plus |
| V _{cc} | 19 | Supply | Supply voltage. |
| Not used | 20 | - | - |



5 Absolute Maximum Ratings

Stresses beyond those listed in [Table 2](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in [Absolute Maximum Ratings](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: All voltages are referred to pin GND.

Table 2. Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | Note |
|--------------------------------|---|------|-----------------------|-------|--|
| Electrical Parameters | | | | | |
| V _{BAT} | Battery Supply Voltage | -0.3 | +50 | V | |
| V _{CC} | Supply Voltage | -0.3 | +7.0 | V | |
| V _{IO} | | -0.3 | +7.0 | V | V _{IO} < V _{CC} |
| | DC Voltage at EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN | -0.3 | V _{IO} +0.3 | V | |
| | DC Voltage on pin WAKE, INH1, INH2 | -0.3 | V _{BAT} +0.3 | | |
| | DC Voltage at BP and BM | -40 | +40 | V | |
| | Input current (latchup immunity) | -100 | 100 | mA | According to JEDEC 78 |
| Electrostatic Discharge | | | | | |
| ESD | Electrostatic Discharge | ±2 | | kV | All pins AEC-Q100-002 (HBM) |
| | uESDI_{Int} | 2 | | kV | ESD on all other pins |
| | Electrostatic Discharge | ±4 | | kV | For V _{BAT} , GND, WAKE AEC-Q100-002 (HBM) |
| | uESD_{Ext} | 4 | | kV | ESD protection on pins that lead to ECU external terminals |
| | Electrostatic Discharge | ±6 | | kV | BP, BM AEC-Q100-002 (HBM) |
| | uESD_{Ext} | 4 | | kV | ESD protection on pins that lead to ECU external terminals |
| | Electrostatic Discharge | ±6 | | kV | BP, BM FlexRay Physical Layer EMC Measurement Specification Version 3.0 |
| | Electrostatic Discharge | ±500 | | V | On all pins AEC-Q100-011 (Charge Device Model) |
| | | ±750 | | V | At the corner pins AEC-Q100-011 (Charge Device Model) |
| | | ±100 | | V | On all pins AEC-Q100-003 (Machine Model) |



Table 2. Absolute Maximum Ratings

| Symbol | Parameter | Min | Max | Units | Note |
|--|---|------|------|-------|--|
| Damage Tests | | | | | |
| U _s | Transient voltage on VBAT, Bus and Wake pins (damage tests) | -100 | | V | ISO7637-2 test pulse 1; class D (see Figure 14) |
| | | | +75 | V | ISO7637-2 test pulses 2a; class D (see Figure 14) |
| | | -150 | | V | ISO7637-2 test pulses 3a; class D (see Figure 14) |
| | | | +100 | V | ISO7637-2 test pulses 3b; class D (see Figure 14) |
| Power Dissipation | | | | | |
| P _t | Total power dissipation (all supplies and outputs) | | 150 | mW | |
| Temperature Ranges and Storage Conditions | | | | | |
| T _{strg} | Storage temperature | -55 | +150 | °C | |
| T _{BODY} | Package body temperature ¹ | | 260 | °C | |
| H | Humidity non-condensing | 5 | 85 | % | |
| MSL | Moisture Sensitivity Level ² | 3 | | | |

1. The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices". The lead finish for Pb-free leaded packages is matte tin (100% Sn).

2. Represents a maximum floor life time of 168h.



6 Electrical Characteristics

In this specification, all the defined tolerances for external components are assured over the whole operation conditions range as well as over lifetime.

Operation Range:

$T_{AMB} = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{CC} = +4.75\text{V}$ to $+5.25\text{V}$, $V_{BAT} = 5.5\text{V}$ to $+40\text{V}$, $V_{IO} = +2.2$ to V_{CC} , $R_L = 40\Omega$, $C_L = 100\text{pF}$ unless otherwise specified.

6.1 Supply Voltage

Table 3. Supply Voltage

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------|--|---|------|------|------|--------------------|
| T_{AMB} | Ambient temperature | | -40 | +25 | +150 | $^{\circ}\text{C}$ |
| T | Ambient temperature | | -40 | | +125 | $^{\circ}\text{C}$ |
| V_{CC-VIO} | Difference of supplies | | -0.1 | | 3.05 | V |
| I_{BAT} | VBAT current consumption (standard transceiver only) | VBAT=12V; SLEEP mode; $T_{AMB} < 125^{\circ}\text{C}$ ¹ | 0 | 30 | 50 | μA |
| | | VBAT=12V; SLEEP mode ¹ | 0 | 80 | 170 | μA |
| | | Non-low-power modes | 0 | 0.24 | 1 | mA |
| I_{CC} | VCC current consumption | Low-power modes; $V_{CC} = 0\text{V}$ to $+5.25\text{V}$ ¹ | -5 | 10 | 20 | μA |
| | | Non-low-power mode: NORMAL, driver enabled | 15 | 25 | 45 | mA |
| | | Non-low-power mode: NORMAL, driver enabled; $R_{BUS} = \infty\Omega$ | 3 | 7 | 15 | mA |
| | | Non-low-power mode: RECEIVE-ONLY | 1 | 2 | 10 | mA |
| I_{IO} | VIO current consumption | Low-power Modes; $V_{IO} = 0\text{V}$ to $+5.25\text{V}$ ¹ | -5 | 2 | 20 | μA |
| | | Non-low-power Modes | 0 | 0.02 | 1 | mA |

1. EN, STBN, ERRN, TxD, RxD, TxEN, BGE, RxEN, WAKE, INH1, INH2: open.



6.2 State Transitions

Table 4. State Transitions

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------------------|---|-----------------------|-----|-----|-----|---------------|
| $t_{\text{STBN_RXD}}$ | Delay STBN high to RxD high with wake flag set | | 1 | 10 | 50 | μs |
| $t_{\text{STBN_RXEN}}$ | Delay STBN high to RxEN high with wake flag set | | 1 | 10 | 50 | μs |
| $t_{\text{SLEEP_INH1}}$ | Delay STBN high to INH1 high | INH1 high = 80 % VBAT | 1 | 10 | 50 | μs |
| $t_{\text{STANDBY_INH2}}$ | Delay STBN high to INH2 high | INH2 high = 80 % VBAT | 1 | 10 | 50 | μs |
| t_{SLEEP} | go-to-sleep hold time | INH1 low = 20 % VBAT | 10 | 25 | 70 | μs |

6.3 Transmitter

The following parameters are applicable to all the branch transmitters.

Table 5. Transmitter

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|--|--|-----------------------|-----------------------|-----------------------|-------|
| $V_{\text{BUS_DIFF_D0}}$ | Differential bus voltage low in NORMAL mode (Data_0) | $V_{\text{BPdata0}} - V_{\text{BMdata0}}$; $40 \Omega < R_L < 55 \Omega$ | -2 | -1 | -0.6 | V |
| $u_{\text{BDT}x_{\text{active}}}$ | Absolute value of uBus, while sending | Load on BP/BM: $40 \Omega \parallel 100\text{pF}$ | 2000 | | 600 | mV |
| $V_{\text{BUS_DIFF_D1}}$ | Differential bus voltage high in NORMAL mode (Data_1) | $V_{\text{BPdata1}} - V_{\text{BMdata1}}$; $40 \Omega < R_L < 55 \Omega$ | 0.6 | 1 | 2 | V |
| $u_{\text{BDT}x_{\text{active}}}$ | Absolute value of uBus, while sending | Load on BP/BM: $40 \Omega \parallel 100\text{pF}$ | 600 | | 2000 | mV |
| $\Delta V_{\text{BUS_DIFF}}$ | Matching between Data_0 and Data_1 differential bus voltage in NORMAL mode | $V_{\text{BUS_DIFF_D0}} - V_{\text{BUS_DIFF_D1}}$; $40 \Omega < R_L < 55 \Omega$ | -200 | 0 | 200 | mV |
| $V_{\text{BUS_COM_D0}}$ | Common mode bus voltage in case of Data_0 in non-low-power mode | $V_{\text{BPdata0}}/2 + V_{\text{BMdata0}}/2$; $40 \Omega < R_L < 55 \Omega$ | $0.4 * V_{\text{CC}}$ | $0.5 * V_{\text{CC}}$ | $0.6 * V_{\text{CC}}$ | V |
| $V_{\text{BUS_COM_D1}}$ | Common mode bus voltage in case of Data_1 in non-low-power mode | $V_{\text{BPdata1}}/2 + V_{\text{BMdata1}}/2$; $40 \Omega < R_L < 55 \Omega$ | $0.4 * V_{\text{CC}}$ | $0.5 * V_{\text{CC}}$ | $0.6 * V_{\text{CC}}$ | V |
| $\Delta V_{\text{BUS_COM}}$ | Matching between Data_0 and Data_1 common mode voltage | $V_{\text{BUS_COM_D0}} - V_{\text{BUS_COM_D1}}$; $40 \Omega < R_L < 55 \Omega$ | -200 | 0 | 200 | mV |
| $V_{\text{BUS_DIFF_Idle}}$ | Absolute differential bus voltage in idle mode | $40 \Omega < R_L < 55 \Omega$ | | 0 | 30 | mV |
| $u_{\text{BDT}x_{\text{idle}}}$ | Absolute value of uBus, while Idle | | 0 | | 30 | mV |
| $IBP_{\text{BMShortMax}}$ $IBM_{\text{BPShortMax}}$ | Absolute max current when BP shorted to BM | $V_{\text{BP}} = V_{\text{BM}}$ | | 25 | +100 | mA |
| $IBP_{\text{BMShortMax}}$ $IBM_{\text{BPShortMax}}$ | Absolute maximum output current when BP shorted to BM | | | | 100 | mA |
| $IBP_{\text{GNDShortMax}}$ | Absolute max current when BP is shorted to GND | $V_{\text{BP}} = 0 \text{ V}$ | | 50 | +100 | mA |
| $IBP_{\text{GNDShortMax}}$ | Absolute maximum output current when shorted to GND | | | | 100 | mA |



Table 5. Transmitter

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------------|---|--|------|-----|-------|-------|
| IBM _{GNDShortMax} | Absolute max current when BM is shorted to GND | $V_{BM}=0\text{ V}$ | | 50 | +100 | mA |
| IBM _{GNDShortMax} | Absolute maximum output current when shorted to GND | | | | 100 | mA |
| IBP _{-5VShortMax} | Absolute max current when BP is shorted to -5 V | $V_{BP}=-5\text{ V}$ | | 50 | +100 | mA |
| IBP _{-5VShortMax} | Absolute maximum output current when shorted to -5V | | | | 100 | mA |
| IBM _{-5VShortMax} | Absolute max current when BM is shorted to -5 V | $V_{BM}=-5\text{ V}$ | | 50 | +100 | mA |
| IBM _{-5VShortMax} | Absolute maximum output current when shorted to -5V | | | | 100 | mA |
| IBP _{27VShortMax} | Absolute max current when BP is shorted to 27 V | $V_{BP}=27\text{ V}$ | | 60 | +100 | mA |
| IBP _{BAT27ShortMax} | Absolute maximum output current when shorted to 27V | | | | 100 | mA |
| IBM _{27VShortMax} | Absolute max current when BM is shorted to 27 V | $V_{BM}=27\text{ V}$ | | 60 | +100 | mA |
| IBM _{BAT27ShortMax} | Absolute maximum output current when shorted to 27V | | | | 100 | mA |
| IBP _{40VShortMax} | Absolute max current when BP is shorted to 40 V | $V_{BP}=40\text{ V}$ | | 75 | +100 | mA |
| IBM _{40VShortMax} | Absolute max current when BM is shorted to 40 V | $V_{BM}=40\text{ V}$ | | 75 | +100 | mA |
| t _{TXD_BUS01} | Delay time from TxD to BUS positive edge | $t_{\text{riseTxD}} = 5\text{ ns}$ | | 25 | 50 | ns |
| dBDTx01 | Transmitter delay, positive edge | | | | 100 | ns |
| t _{TXD_BUS10} | Delay time from TxD to BUS negative edge | $t_{\text{fall TxD}} = 5\text{ ns}$ | | 25 | 50 | ns |
| dBDTx10 | Transmitter delay, negative edge | | | | 100 | ns |
| t _{TXD_MISMATCH} | Delay time from TxD to BUS mismatch | $t_{\text{TXD_BUS10}} - t_{\text{TXD_BUS01}}$ | -4 | 0 | 4 | ns |
| dTxAsym | Transmitter delay mismatch dBDTx10 - dBDTx01 | | | | 4 | ns |
| t _{BUS_TX10} | Fall time differential bus voltage | 80 % - 20 % of V_{BUS} ; $R_L=45\ \Omega$; $C_L=100\ \text{pF}$ | 3.75 | 13 | 18.75 | ns |
| dBusTx10 | Fall time differential bus voltage (80% → 20%) | | 3.75 | | 18.75 | ns |
| t _{BUS_TX01} | Rise time differential bus voltage | 20 % - 80 % of V_{BUS} ; $R_L=45\ \Omega$; $C_L=100\ \text{pF}$ | 3.75 | 13 | 18.75 | ns |
| dBusTx01 | Rise time differential bus voltage (20% → 80%) | | 3.75 | | 18.75 | ns |
| t _{TXEN_BUS_Idle_Active} | Delay time from TxEN to bus active | $R_L=45\ \Omega$; $C_L=100\ \text{pF}$ | | 18 | 50 | ns |
| dBDTxia | Propagation delay idle → active | | | | 100 | ns |



Table 5. Transmitter

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|--|---|-----|-----|-----------|----------|
| $t_{\text{TXEN_BUS_Active_Idle}}$ dBDTxai | Delay time from TxEN to bus idle Propagation delay active → idle | $R_L=45 \Omega$; $C_L=100 \text{ pF}$ | | 18 | 50 100 | ns ns |
| $t_{\text{TXEN_MISMATCH}}$ dBDTxDM | Delay time from TxEN to BUS mismatch $ \text{dBDTxia} - \text{dBDTxai} $ | $ t_{\text{TXEN_BUS_Idle_Active}} - t_{\text{TXEN_BUS_Active_Idle}} $; $R_L=45 \Omega$; $C_L=100 \text{ pF}$ | | 0 | 50 50 | ns ns |
| $t_{\text{BGE_BUS_IdleActive}}$ dBDTxia | Delay time from BGE to bus active Propagation delay idle → active | | | 18 | 50 100 | ns ns |
| $t_{\text{BGE_BUS_Active_Idle}}$ dBDTxai | Delay time from BGE to bus idle Propagation delay active → idle | | | 18 | 50 100 | ns ns |
| $t_{\text{BUS_Idle_Active}}$ dBusTxia | Differential bus voltage transition time: idle to active Transition time idle → active | $R_L=45 \Omega$; $C_L=100 \text{ pF}$ | | 5 | 30 30 | ns ns |
| $t_{\text{BUS_Active_Idle}}$ dBusTxai | Differential bus voltage transition time: active to idle Transition time active → idle | $R_L=45 \Omega$; $C_L=100 \text{ pF}$ | | 2 | 30 30 | ns ns |
| $t_{\text{TXEN_timeout}}$ | TxEN timeout | | 3 | 5 | 10 | ms |

6.4 Receiver

The following parameters are applicable to all the branch receivers.

Table 6. Receiver

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|-----------------------------------|---------------------------|-----------------------------------|--------------------------|
| $R_{\text{BP}}, R_{\text{BM}}$ RCM1, RCM2 | BP, BM input resistance Receiver common mode input resistance | Idle mode; $R_{\text{BUS}} = \infty$ | 10 10 | 25 | 40 40 | k Ω k Ω |
| R_{DIFF} | BP, BM differential input resistance | Idle mode; $R_{\text{BUS}} = \infty$ | 20 | 50 | 80 | k Ω |
| $V_{\text{BP}}, V_{\text{BM}}$ uCM | Common mode voltage range Common mode voltage range (with respect to GND) that does not disturb the receive function | | -10 -10 | | +15 +15 | V V |
| $V_{\text{BPidle}}, V_{\text{BMidle}}$ uBias | Idle voltage in non-low-power modes on pin BP, BM Bus bias voltage during BD_Normal mode | Non-low-power modes; $V_{\text{TXEN}}=V_{\text{IO}}$ $40 \Omega < R_L < 55 \Omega$ | $0.4 \cdot V_{\text{CC}}$ 1800 | $0.5 \cdot V_{\text{CC}}$ | $0.6 \cdot V_{\text{CC}}$ 3200 | V mV |



Table 6. Receiver

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|---|---|------------------|------|------------------|------------------------|
| V_{BPIdle_low} , $V_{BMiddle_low}$ $uBias$ | Idle voltage in low-power modes on pin BP, BM Bus bias voltage during low-power modes | Low-power modes $40 \Omega < R_L < 55 \Omega$ | -0.2 -200 | 0 | +0.2 +200 | V mV |
| I_{BPIdle} | Absolute idle output current on pin BP | $-40 V < V_{BP} < 40 V$ | 0 | 2 | 7.5 | mA |
| $I_{BMiddle}$ | Absolute idle output current on pin BM | $-40 V < V_{BM} < 40 V$ | 0 | 2 | 7.5 | mA |
| I_{BPLeak_ST} , I_{BMLeak_ST} $iBPLeak$, $iBMLeak$ | Absolute leakage current, when not powered Absolute leakage current, when not powered | $V_{BP}=V_{BM}=5 V$, $V_{DD}=0 V$, $V_{BAT}=0 V$; $V_{IO}=0 V$; $T_{amb} < 125^\circ C$ | | 6 | 25 25 | μA μA |
| I_{BPLeak_HT} , I_{BMLeak_HT} | Absolute leakage current, when not powered | $V_{BP}=V_{BM}=5 V$, $V_{DD}=0 V$, $V_{BAT}=0 V$; $V_{IO}=0 V$; $125^\circ C < T_{amb} < 150^\circ C$ | | 35 | 150 | μA |
| $V_{BUSActiveHigh}$ $uBusActiveHigh$ | Activity detection differential input voltage high Upper receiver threshold for detecting activity | Normal power modes $-10 V < (V_{BP}, V_{BM}) < 15 V$ | 150 150 | 260 | 400 425 | mV mV |
| $V_{BUSActiveLow}$ $uBusActiveLow$ | Activity detection differential input voltage low Lower receiver threshold for detecting activity | Normal power modes $-10 V < (V_{BP}, V_{BM}) < 15 V$ | -400 -425 | -260 | -150 -150 | mV mV |
| V_{Data1} $uData1$ | Data1 detection differential input voltage Receiver threshold for detecting Data_1 | Pre-condition: activity already detected. Normal power mode. $-10 V < (V_{BP}, V_{BM}) < 15 V$ | 150 150 | 225 | 300 300 | mV mV |
| V_{Data0} $uData0$ | Data0 detection differential input voltage Receiver threshold for detecting Data_0 | Pre-condition: activity already detected. Normal power mode. $-10 V < (V_{BP}, V_{BM}) < 15 V$ | -300 -300 | 225 | -150 -150 | mV mV |
| $V_{DataErr}$ $\Delta uData$ | Mismatch between Data0 and Data1 differential input voltage Mismatch of receiver thresholds | $2 \times (V_{Data0} - V_{Data1}) / (V_{Data0} + V_{Data1})^1$ | | 0 | 10 10 | % % |
| t_{BUS_RxD10} $dBDRx10$ | Delay from BUS to RxD negative edge Receiver delay, negative edge | $C_{RXD}=15 pF^2$ | | 34 | 80 100 | ns ns |
| t_{BUS_RxD01} $dBDRx01$ | Delay from BUS to RxD positive edge Receiver delay, positive edge | $C_{RXD}=15 pF^2$ | | 34 | 80 100 | ns ns |



Table 6. Receiver

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--|---|---|-----|-----|-----|-------|
| t_{bit} | Bit time | $C_{RXD}=15\text{ pF}^2$ | 60 | | | ns |
| t_{RXD_ASYM} $dRxAsym$ | Delay time from BUS to RxD mismatch Receiver delay mismatch $ dBDRx10 - dBDRx01 $ | $C_{RXD}=15\text{ pF}$, $ t_{BUS_RXD10} - t_{BUS_RXD01} ^2$ | | 0 | 5 | ns |
| $t_{RXDfall}$ $dRxSlope$ | Fall time RxD voltage Fall and rise time 20%-80%, 15pF load | 80 % - 20 % of V_{RXDL} ; $C_{RXD}=15\text{ pF}^2$ | | 2 | 5 | ns |
| $t_{RXDrise}$ $dRxSlope$ | Rise time RxD voltage Fall and rise time 20%-80%, 15pF load | 20 % - 80 % of V_{RXDL} ; $C_{RXD}=15\text{ pF}^2$ | | 2 | 5 | ns |
| $t_{BUSIdleDetection}$ $dIdleDetection$ | Idle detection time Filter-time for idle detection | $V_{BUS}: 400\text{mV} \rightarrow 0$ | 50 | 150 | 250 | ns |
| $t_{BUSActivityDetection}$ $dActivityDetection$ | Activity detection time Filter-time for activity detection | $V_{BUS}: 0\text{ V} \rightarrow 400\text{ mV}$ | 100 | 200 | 300 | ns |
| $t_{BUSIdleReaction}$ $dBDRxai$ | Idle reaction time Idle reaction time | $V_{BUS}: 400\text{mV} \rightarrow 0$ | 50 | 160 | 300 | ns |
| $t_{BUSActivityReaction}$ $dBDRxia$ | Activity reaction time Activity reaction time | $V_{BUS}: 0\text{ V} \rightarrow 400\text{ mV}$ | 100 | 210 | 350 | ns |

1. Test condition: $(V_{BP} + V_{BM}) / 2 = 2,5\text{V} \pm 5\%$

2. For test signal see Figure 13

6.5 Wake-up Detector

The following parameters are applicable to all the branch wake-up detectors.

Table 7. Wake-up Detector

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------------|--|---|-----|-----|-----|---------------|
| V_{BAT_BW} | V_{BAT} voltage supply for bus wake-up | | 6.5 | | 40 | V |
| t_{BWU0} $dWU0Detect$ | Data_0 detection time in remote wake-up pattern Acceptance timeout for detection of a Data_0 phase in wake-up pattern | $-10\text{V} < (V_{BP}, V_{BM}) < 15\text{V}$ | 1 | 2 | 4 | μs |

In case a V_{BAT} supply voltage input is implemented, the wake-up detector shall be operable when uV_{BAT} is equal to or greater than 7V even if other supplies are not present.



Table 7. Wake-up Detector

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------------|---|---|------|------|------|---------|
| $t_{BWUIdle}$ | Idle or Data_1 detection time in remote wake-up pattern | $-10V < (V_{BP}, V_{BM}) < 15V$ | 1 | 2 | 4 | μs |
| $dWUIdleDetect$ | Acceptance timeout for detection of a Idle phase in wake-up pattern | | 1 | | 4 | μs |
| $t_{BWUDetect}$ | Total remote wake-up detection time | $-10V < (V_{BP}, V_{BM}) < 15V$ | 48 | 75 | 140 | μs |
| $dWUTimeout$ | Acceptance timeout for wake-up pattern recognition | | 48 | | 140 | μs |
| V_{BWU0} | Remote wake-up detector threshold | $-10V < (V_{BP}, V_{BM}) < 15V$ | -300 | -250 | -150 | mV |
| V_{LWUTH} | Wake-up detection threshold | | 2 | 2.8 | 4 | V |
| I_{LWUL} | Low level input current on WAKE pin | $V_{BAT}=12V; V_{LWAKE}=2V$ for $t < t_{LWUFilter}$ | -20 | -10 | -5 | μA |
| I_{LWUH} | High level input current on WAKE pin | $V_{BAT}=12V; V_{LWAKE}=4V$ for $t < t_{LWUFilter}$ | 5 | 10 | 20 | μA |
| $t_{LWUFilter}$ | Local wake filter time | | 1 | 20 | 40 | μs |
| $dWakePulseFilter$ | Wake pulse filter time (spike rejection) | | 1 | | 500 | μs |

6.6 Supply Voltage Monitor

Table 8. Supply Voltage Monitor

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------------|---------------------------------------|------------|------|-----|------|-------|
| V_{BATTHH} | VBAT undervoltage recovery threshold | | 3.5 | 4 | 4.5 | V |
| V_{BATTHL} | VBAT undervoltage detection threshold | | 2.5 | 3 | 3.5 | V |
| uUV_{BAT} | Undervoltage detection threshold | | 2 | | 5.5 | V |
| V_{CCTHH} | VCC undervoltage recovery threshold | | 3.5 | 4 | 4.5 | V |
| V_{CCTHL} | VCC undervoltage detection threshold | | 2.5 | 3 | 3.5 | V |
| uUV_{CC} | Undervoltage detection threshold | | 2 | | | V |
| V_{IOTHH} | VIO undervoltage recovery threshold | | 1.25 | 1.6 | 2.0 | V |
| V_{IOTHL} | VIO undervoltage detection threshold | | 0.75 | 1.1 | 1.5 | V |
| uUV_{IO} | Undervoltage detection threshold | | 0.75 | | | V |
| t_{UV_DETECT} | Undervoltage detection time | | 100 | 300 | 700 | ms |
| $dUV_{BAT}, dUV_{CC}, dUV_{IO}$ | Undervoltage reaction time | | | | 1000 | ms |
| t_{UV_REC} | Undervoltage recovery time | | 0.7 | 2 | 5 | ms |



6.7 Bus Error Detection

The following parameters are applicable to all the branch error detectors.

Table 9. Bus Error Detection

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------|---|---|-----|-----|-----|---------|
| I_{THL} | Absolute bus current for low current detection | NORMAL mode, Transmitter enabled not production tested | | 5 | 20 | mA |
| I_{THH} | Absolute bus current for high current detection | NORMAL mode, Transmitter enabled not production tested | 20 | 40 | | mA |
| V_{SHORT} | Differential voltage on BP and BM for detecting short circuit between bus lines | NORMAL mode, Transmitter enabled | 150 | 260 | 400 | mV |
| t_{BUS_ERROR} | Bus error detection time | Normal mode, Transmitter enabled (**) detection only required while actively transmitting a data frame, error indication to host latest when transmission stops. | | | 500 | ns |
| t_{BUS_INHIB} | Bus short detection inhibit time | Normal mode, Transmitter enabled | 0.5 | 2 | 4 | μ s |

6.8 Over Temperature

Table 10. Over Temperature

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------|---------------------------------|------------|-----|-----|-----|--------------|
| OT_{TH} | Over temperature threshold high | | 175 | 190 | 205 | $^{\circ}$ C |
| OT_{TL} | Over temperature hysteresis low | | 165 | 180 | 195 | $^{\circ}$ C |

6.9 Power Supply Interface

Table 11. Power Supply Interface

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------|---------------------------------------|--|-----|-----|-----|---------|
| ΔV_{OINH} | High level voltage drop on INH1, INH2 | $I_{INH}=0.2\text{mA}$; $V_{BAT}=5.5\text{V}$ | 0 | 0.2 | 0.8 | V |
| $ I_{IL} $ | Leakage current | Sleep mode, $V_{INH}=0\text{V}$ | -5 | 0 | 5 | μ A |

6.10 Communication Controller Interface

Table 12. Communication Controller Interface

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------------------------|---|------------|--|-----------------|--|---------|
| V_{TXDIH} μ VDIG-IN-HIGH | Threshold for detecting TxD as on logical high Threshold for detecting a digital input as on logical high | | | $0.48 * V_{IO}$ | $0.7 * V_{IO}$ $0.7 * \mu$ VDIG | V |
| V_{TXDIL} μ VDIG-IN-LOW | Threshold for detecting TxD as on logical low Threshold for detecting a digital input as on logical low | | $0.3 * V_{IO}$ $0.3 * \mu$ VDIG | | | V |
| I_{TXDIH} | TxD high level input current | | 20 | 50 | 100 | μ A |
| I_{TXDIL} | TxD low level input current | | -5 | 0 | 5 | μ A |
| V_{TXENIH} μ VDIG-IN-HIGH | Threshold for detecting TxEN as on logical high Threshold for detecting a digital input as on logical high | | | | $0.7 * V_{IO}$ $0.7 * \mu$ VDIG | V |



Table 12. Communication Controller Interface

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------|--|---|-----------------------|-----------------------|-----------------------|-------|
| V _{TxENIL} | Threshold for detecting TxEN as on logical low | | 0.3 * V _{IO} | | | V |
| uVDIG-IN-LOW | Threshold for detecting a digital input as on logical low | | 0.3 * uVDIG | | | |
| I _{TxENIH} | TxEN high level input current | | -5 | 0 | 5 | μA |
| I _{TxENIL} | TxEN low level input current | | -100 | -50 | -20 | μA |
| V _{RxD0H} | RxD high level output voltage | I _{RxD} =-4mA, V _{IO} =5V | 0.8 * V _{IO} | 0.9 * V _{IO} | 1.0 * V _{IO} | V |
| uVDIG-OUT-HIGH | Output voltage on a digital output, when in logical high state | | 0.8 * uVDIG | | 1.0 * uVDIG | |
| V _{RxD0L} | RxD low level output voltage | I _{RxD} =4mA, V _{IO} =5V | 0 | 0.1 * V _{IO} | 0.2 * V _{IO} | V |
| uVDIG-OUT-LOW | Output voltage on a digital output, when in logical low state | | | | 0.2 * uVDIG | |



6.11 Host Interface

Table 13. Host Interface

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------------|--|--------------------------------|------------------|-----------------|------------------|---------|
| V_{STBNIH} | Threshold for detecting STBN as on logical high | | | $0.48 * V_{IO}$ | $0.7 * V_{IO}$ | V |
| $\mu VDIG-IN-HIGH$ | Threshold for detecting a digital input as on logical high | | | | $0.7 * \mu VDIG$ | |
| V_{STBNIL} | Threshold for detecting STBN as on logical low | | $0.3 * V_{IO}$ | $0.48 * V_{IO}$ | | V |
| $\mu VDIG-IN-LOW$ | Threshold for detecting a digital input as on logical low | | $0.3 * \mu VDIG$ | | | |
| I_{STBNIH} | STBN high level input current | | 20 | 50 | 100 | μA |
| I_{STBNIL} | STBN low level input current | | -5 | 0 | 5 | μA |
| $t_{STBN_DEB_LP}$ | STBN de-bouncing time low-power modes | | 0.1 | 1 | 40 | μs |
| $t_{STBN_DEB_NLP}$ | STBN de-bouncing time non-low-power modes | | 0.1 | 1 | 2 | μs |
| V_{ENIH} | Threshold for detecting EN as on logical high | | | $0.48 * V_{IO}$ | $0.7 * V_{IO}$ | V |
| $\mu VDIG-IN-HIGH$ | Threshold for detecting a digital input as on logical high | | | | $0.7 * \mu VDIG$ | |
| V_{ENIL} | Threshold for detecting EN as on logical low | | $0.3 * V_{IO}$ | $0.48 * V_{IO}$ | | V |
| $\mu VDIG-IN-LOW$ | Threshold for detecting a digital input as on logical low | | $0.3 * \mu VDIG$ | | | |
| I_{ENIH} | EN high level input current | | 20 | 50 | 100 | μA |
| I_{ENIL} | EN low level input current | | -5 | 0 | 5 | μA |
| $t_{EN_DEB_LP}$ | EN de-bouncing time low-power modes | | 0.1 | 1 | 40 | μs |
| $t_{EN_DEB_NLP}$ | EN de-bouncing time non-low-power modes | | 0.1 | 1 | 2 | μs |
| V_{ERRNOH} | ERRN high level output voltage | $I_{ERRN} = -4mA, V_{IO} = 5V$ | $0.8 * V_{IO}$ | $0.9 * V_{IO}$ | $1.0 * V_{IO}$ | V |
| $\mu VDIG-OUT-HIGH$ | Output voltage on a digital output, when in logical high state | | $0.8 * \mu VDIG$ | | $1.0 * \mu VDIG$ | |
| V_{ERRNOL} | ERRN low level output voltage | $I_{ERRN} = 4mA, V_{IO} = 5V$ | 0 | $0.1 * V_{IO}$ | $0.2 * V_{IO}$ | V |
| $\mu VDIG-OUT-LOW$ | Output voltage on a digital output, when in logical low state | | | | $0.2 * \mu VDIG$ | |



6.12 Bus Guardian Interface

Table 14. Bus Guardian Interface

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------|--|--|-----------------------|------------------------|-----------------------|-------|
| V _{BGEIH} | Threshold for detecting BGE as on logical high | | | 0.48 * V _{IO} | 0.7 * V _{IO} | V |
| uVDIG-IN-HIGH | Threshold for detecting a digital input as on logical high | | | | 0.7 * uVDIG | |
| V _{BGEIL} | Threshold for detecting BGE as on logical low | | 0.3 * V _{IO} | 0.48 * V _{IO} | | V |
| uVDIG-IN-LOW | Threshold for detecting a digital input as on logical low | | 0.3 * uVDIG | | | |
| I _{BGEIH} | BGE high level input current | | 20 | 50 | 100 | μA |
| I _{BGEIL} | BGE low level input current | | -5 | 0 | 5 | μA |
| V _{RxENOH} | RxEN high level output voltage | I _{RxEN} =-4mA, V _{IO} =5V | 0.8 * V _{IO} | 0.9 * V _{IO} | 1.0 * V _{IO} | V |
| uVDIG-OUT-HIGH | Output voltage on a digital output, when in logical high state | | 0.8 * uVDIG | | 1.0 * uVDIG | |
| V _{RxENOL} | RxEN low level output voltage | I _{RxEN} =4mA, V _{IO} =5V | 0 | 0.1 * V _{IO} | 0.2 * V _{IO} | V |
| uVDIG-OUT-LOW | Output voltage on a digital output, when in logical low state | | | | 0.2 * uVDIG | |

6.13 Read Out Interface

Table 15. Read Out Interface

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------------------|---|------------|-----|-----|-----|-------|
| t _{RO_PROP_ERRN} | Propagation delay falling edge EN to ERRN | | | 2 | 4.5 | μs |
| t _{RO_EN_TIMEOUT} | Error read out time out | | 25 | 50 | 100 | μs |



7 Detailed Description

The AS8222 is a FlexRay Transceiver operating as an interface between the Communication Controller and the wired bus lines. The AS8222 is designed to extend the application range for high speed and safety critical time triggered bus systems in an automotive environment. The drivers are short circuit protected against the positive and negative supply voltage to increase the robustness and reliability of automotive systems. The AS8222 operates at baudrates up to 10 Mbps.

7.1 Block Description

The AS8222 consists of 9 functional blocks [Figure 1](#).

Table 16. Functional Blocks

| Symbol | Parameter |
|---|--|
| Host Controller Interface (HCI) | Digital interface between the Transceiver and the host controller (HC) The host interface comprises the read-out handler, which delivers failure and status information via the ERRN pin to the host controller. |
| Communication Controller Interface (CCI) | Digital interface between the Transceiver and the FlexRay communication controller (CC) |
| Bus Guarding Interface (BGI) | Digital interface between the Transceiver and the FlexRay bus guardian (BG) or monitoring circuitry. |
| Power Supply Interface (PSI) | The power supply interface consists of the voltage monitor (VM) with two analog inhibit outputs switching external voltage supplies. |
| Internal Logic (IL) | The digital signals from the functional blocks of the device are fed into the internal logic where the forwarding of FlexRay messages from analog side to digital interfaces and vice versa is done. The state machine is embedded in the Internal Logic and the handling of error, wake, and power-on flags is executed herein. |
| Bus Failure Detector (BFD) Temperature Protection (TP) | The bus failure detector is directly connected to the bus pins, in order to detect several external failure conditions which may occur on the bus. The temperature protection turns off the output driver when reaching the specified internal temperature in order to protect the device. |
| Transmitter | The transmitter provides the differential signaling according the FlexRay standard on the bus pins. |
| Receiver | The Receiver captures FlexRay valid signals at the bus pins and provides the received data streams to the Internal Logic. |
| Wake-Up Detector (WUD) | The wake-up detector recognizes valid wake-up frames on the bus, recognizes a wake signal on the local WAKE pin and signals valid wake-up events to the Internal Logic. |

7.2 Events

Transitions in order to change between the operation modes are possible only if events are detected. The device supports three types of events:

- Events on the host controller interface (STBN, EN),
- Detection of undervoltage or supply voltage recovery and
- Wake events.

Mode changes are only performed upon detected events.

7.3 Operating Modes

The AS8222 provides the following operating modes:

- NORMAL: Non-low-power mode
- RECEIVE-ONLY: Non-low-power mode
- STANDBY: Low-power mode
- GO-TO-SLEEP: Low-power mode
- SLEEP: Low-power mode



7.3.1 NORMAL Mode

In this mode the transceiver is able to send and receive data signals on the bus. TxEN and BGE control the state of the transmitter. INH1 and INH2 outputs are set high. RxD shows the bus data and RxEN the bus state. The error read out mechanism is enabled. In this mode the transmitter state can be selected as shown in Table 17. In case the over-temperature flag is set the transmitter is disabled. The bus wires are terminated to $V_{CC}/2$ via receiver input resistances.

Table 17. Transmitter States

| BGE | TxEN | TxD | Transmitter State | Bus state |
|-----|------|-----|-------------------|--|
| H | L | H | Enabled | Data_1 (BP is driven high, BM is driven low) |
| H | L | L | Enabled | Data_0 (BP is driven low, BM is driven high) |
| X | H | X | Disabled | Idle (BP and BM are not driven) |
| L | X | X | Disabled | Idle (BP and BM are not driven) |

- If the differential bus voltage is higher than $V_{BUSActivehigh}$ or lower than $V_{BUSActivelow}$ for a time longer than $t_{BUSActiveDetection}$, then activity is detected on the bus (Bus = active), RxEN is switched to logical "low" and RxD is released.
- If after the activity detection, the differential bus voltage is higher than V_{Data1} , RxD is high.
- If after the activity detection, the differential bus voltage is lower than V_{Data0} , RxD is low.
- If the absolute differential bus voltage is lower than $V_{BUSActivehigh}$ and higher than $V_{BUSActivelow}$ for a time longer than $t_{BUSIdleDetection}$, then idle is detected on the bus (Bus = idle), RxEN and RxD are switched to logical "high".

7.3.2 RECIEVE-ONLY Mode

In this mode the transceiver has the same behavior as in NORMAL mode but the transmitter is disabled.

7.3.3 STANDBY Mode

In this mode the transceiver is not able to send and receive data signals to and from the bus, but the wake up detector is active. The power consumption is significantly reduced with respect to the non-low-power operation modes. RxD, RxEN signals the negation of the wake-up flag. INH1 is set to high. If wake-up flag is set then INH2 is high, otherwise it is floating. The error read out mechanism is not enabled. The bus wires are terminated to GND (bus state: Idle_LP).

7.3.4 GO-TO-SLEEP Mode

In this mode the transceiver has the same behavior as in STANDBY mode but if this mode is selected for a time longer than t_{SLEEP} and the wake flag is cleared the device enters into the SLEEP mode.

7.3.5 SLEEP Mode

In this mode the transceiver has the same behavior as in standby mode but INH1 and INH2 are floating.

7.4 Non-Operating Modes

The AS8222 provides the following non-operating mode:

- POWER-OFF

7.4.1 POWER-OFF Mode

In this mode the transceiver is not able to operate. RxD, RxEN are set to high and ERRN is set to low. INH1 and INH2 are floating. The bus wires are not connected to GND (bus state: Idle_HZ).

7.5 Undervoltage Events

The device monitors the following three voltage supplies:

- **V_{BAT}**: Battery supply voltage
- **V_{IO}**: Supply voltage for I/O digital level adaptation
- **V_{CC}**: Supply voltage (+5V)



7.5.1 Undervoltage / Voltage Recovery V_{BAT}

If V_{BAT} voltage falls below V_{CCTHL} for a time longer than t_{UV_DETECT} then an undervoltage V_{BAT} event is detected. Undervoltage recovery is detected if V_{BAT} exceeds the voltage threshold V_{BATTHH} for a time longer than t_{UV_REC}.

7.5.2 Undervoltage / Voltage Recovery V_{IO}

If V_{IO} voltage falls below V_{IO_{THL}} for a time longer than t_{UV_DETECT} then an undervoltage V_{IO} event is detected. Undervoltage recovery is detected if V_{IO} exceeds the voltage threshold V_{IO_{THH}} for a time longer than t_{UV_REC}.

7.5.3 Undervoltage / Voltage Recovery V_{CC}

If V_{CC} voltage falls below V_{CCTHL} for a time longer than t_{UV_DETECT} then an undervoltage V_{CC} event is detected. Undervoltage recovery is detected if V_{CC} exceeds the voltage threshold V_{CCTHH} for a time longer than t_{UV_REC}.

7.6 Power On/Off Events

- Starting from POWER-OFF mode a power-on event occurs in case V_{BAT} undervoltage recovery is detected.
- Starting from every operation mode a POWER-OFF event occurs in case V_{BAT} and V_{CC} undervoltage flags are set.

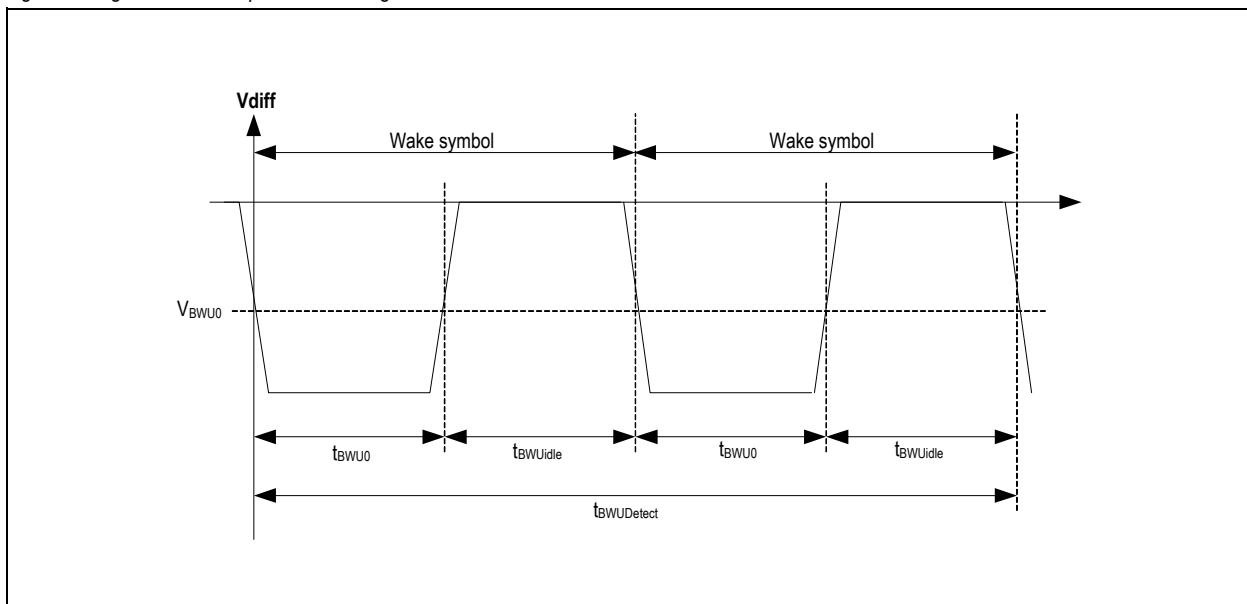
7.7 Wake-Up Events

A wake-up event is only detected in low-power modes.

7.7.1 Remote Wake-Up Event

A remote wake-up event, only possible in low-power modes, is detected if at least two consecutive wake-up symbols via the FlexRay bus within t_{BWUDetect} are received. The wake-up symbol is defined as Data0 longer than t_{BWU0} followed by idle or Data1 longer than t_{BWUidle} shown in Figure 3.

Figure 3. Signal for Wake-up Pattern Recognition



7.7.2 Remote Wake-up with Frames

A valid wake-up event can be generated out of the standard FlexRay communication in 5 Mbps and 10 Mbps network configurations, while the data bits of the FlexRay Frame are set to “low” for a time longer than t_{BWU0} and set to “high” for time longer than t_{BWUidle} represent one wake symbol. A valid wake-up pattern consists of two wake symbols as shown in Figure 3.

In a 10Mbps speed configuration of the network, the payload of the frame is configured as follows:

- 1st wake symbol : 0x00 0x00 0x00 0x00 0x00 0xFF 0xFF 0xFF 0xFF 0xFF
- 2nd wake symbol : 0x00 0x00 0x00 0x00 0x00 0xFF 0xFF 0xFF 0xFF 0xFF

Repetitions of wake symbols might be required if network components are shortening valid Wake symbols (e.g. the time until the device is able to re-send wake symbols after wake-up).



7.7.3 Local Wake-Up Event

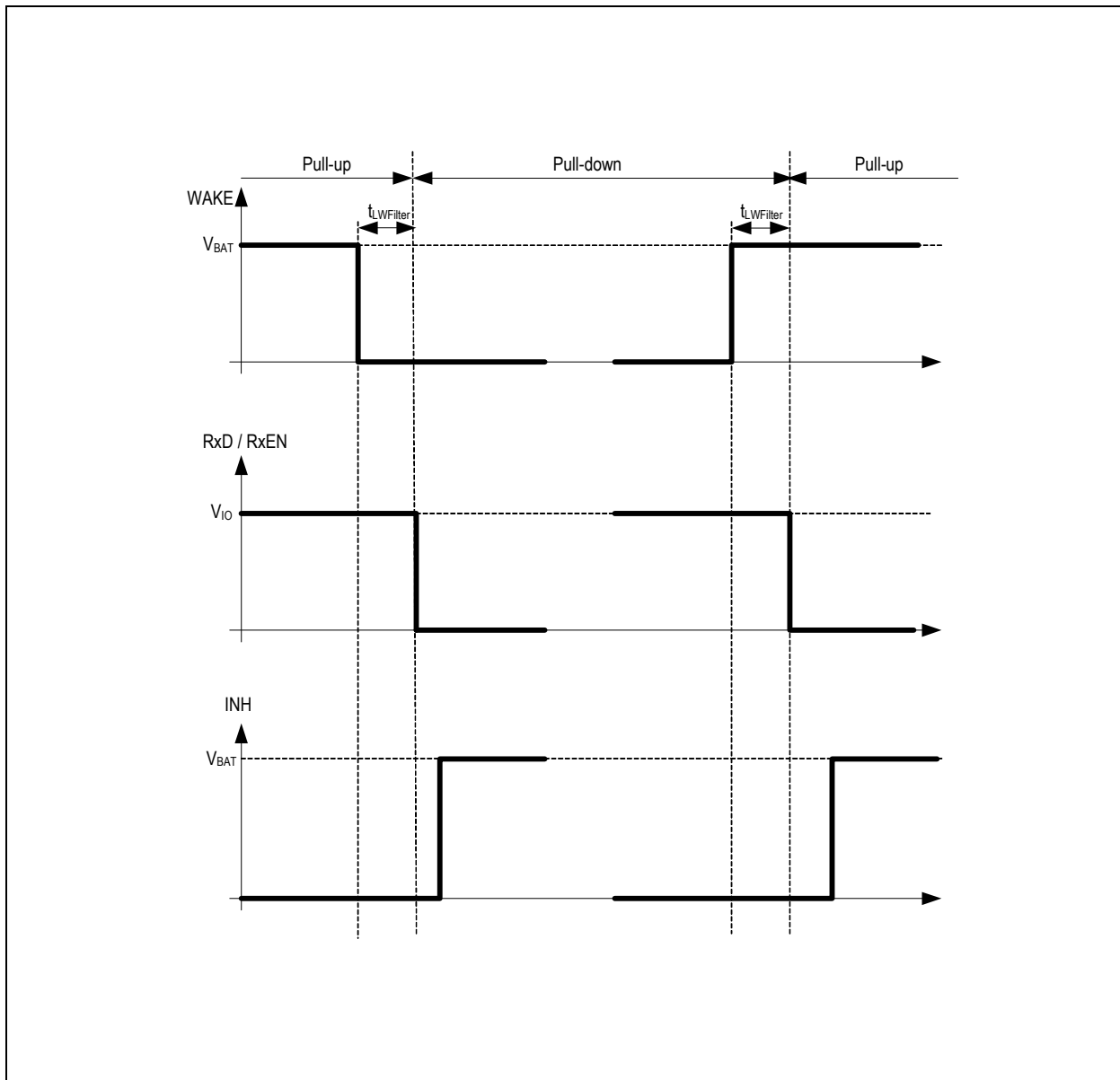
In all low-power modes, if the voltage on the WAKE pin falls below V_{LWUTL} for longer than $t_{LWUFilter}$, a local wake-up event is detected. At the same time the biasing of the pin is switched to pull-down. As well a local wake up event is detected if the voltage on the WAKE pin rises above V_{LWUTH} for longer than $t_{LWUFilter}$, then biasing of the pin is switched to pull-up. The pull-up and -down mechanism is activated in low- and non-low-power modes.

7.8 Over-temperature Events

In NORMAL mode if the temperature exceeds OT_{TH} , the transmitter is deactivated. During this condition the device will remain in NORMAL mode.

The transmitter is activated again, if the temperature falls below OT_{TL} .

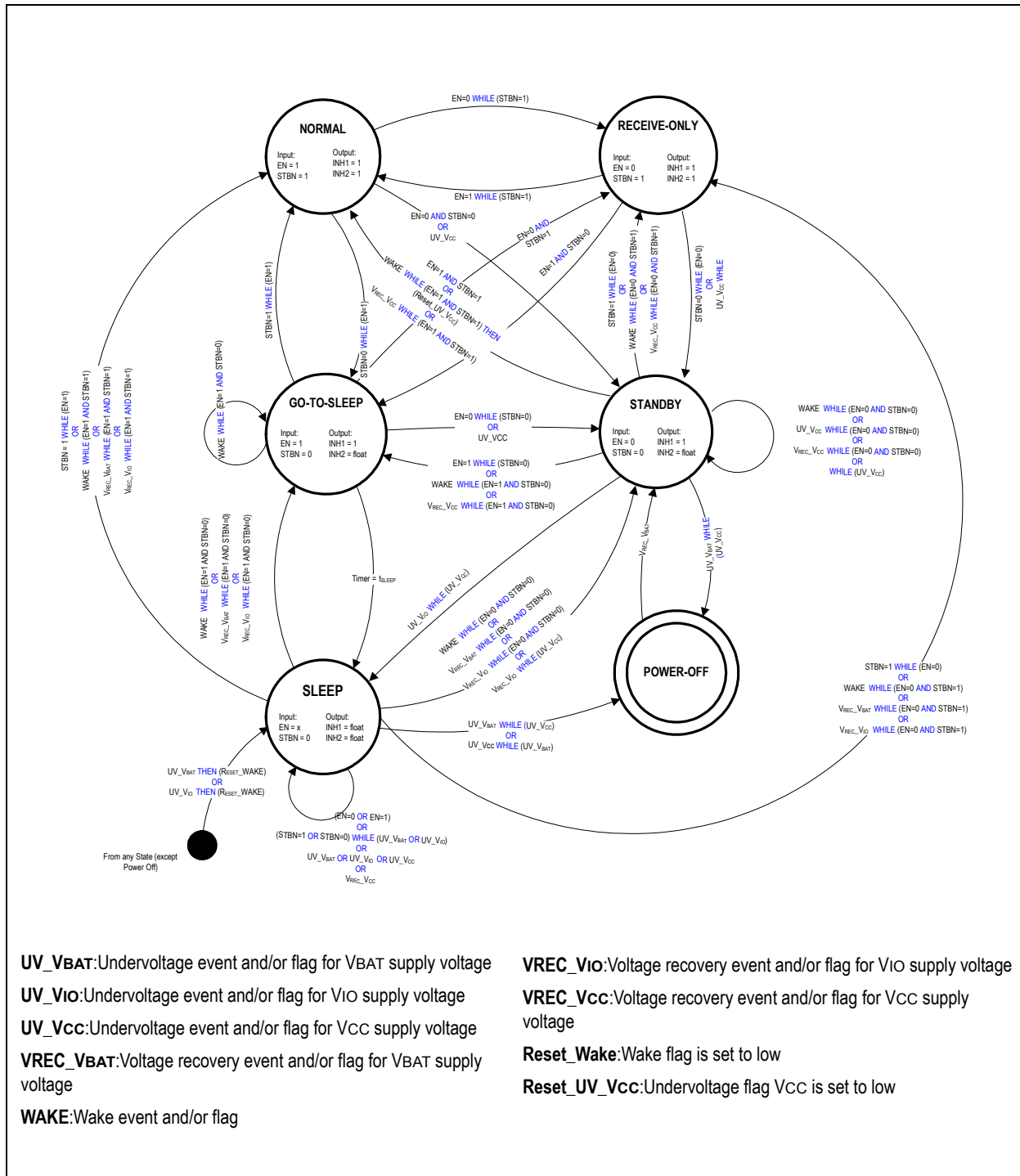
Figure 4. Wake Input Pin Behaviour





7.9 System Description

Figure 5. State Machine Diagram



Notes:

- This state diagram does not include all transitions, which are shown in Table 19.
- Prefix of "WHILE" is an event and suffix in brackets checks the flags or in case of EN and STBN the input condition.
 - **For example:** VREC_VBAT WHILE (EN=0 AND STBN=0)
 - After the event VBAT supply voltage recovery is detected, the transition is performed if EN and STBN are "low".



7.10 Fail Silent Behaviour

7.10.1 RxEN / BGE Timeout

In case no edges on RxEN and BGE are detected within $t_{TxEN_timeout}$, the transmitter will stop transmitting the signals on RxD to the bus pins. Transmission is only possible in case the BGE (Bus Guardian Enable) pin is set to high and if TxEN (Transmit Enable Not) is set to low (see [Table 17](#)).

7.10.2 State Transitions due to Undervoltage Detection

- In case of VBAT or VIO undervoltage is detected, SLEEP mode will be entered regardless the status of EN and STBN.
- In case VCC undervoltage is detected, STANDBY mode will be entered regardless the status of EN and STBN.
- VBAT and VIO undervoltage detection have higher priority than VCC undervoltage detection.
- In case undervoltage at VBAT and VCC is detected, POWER-OFF mode is entered (bus state: Idle_HZ).

7.10.3 State Transitions due to Voltage Recovery Detection

- If the voltage recovers the device will enter the mode selected by the EN and STBN pins, in case no undervoltage is present at the other supply pins.
- Starting from the POWER-OFF, the device enters the state selected by the host input pins (EN, STBN) only if VBAT or VCC recovers ($V_{BAT} \geq V_{BATTHH}$ or $V_{CC} \geq V_{CCTHH}$) while VIO is available (undervoltage flag of VIO flag not set). If the VIO undervoltage flag is set, the STANDBY mode will be entered. In both cases the Power-On flag is set.
- If $V_{BAT} \leq V_{BATTHL}$ and $V_{CC} \leq V_{CCTHL}$ the device will be in POWER-OFF state, thus the bus wires are not terminated (bus state: Idle_HZ).

7.11 Mode Transitions

- Starting from every operation mode the device enters POWER-OFF in case a power-off event occurs regardless the VIO undervoltage flag, the wake-up flag and the host input pins (EN, STBN).
- Starting from the POWER-OFF the device enters STANDBY only in case a power-on event occurs.
- Starting from every operation mode the device enters SLEEP in case VBAT or VIO undervoltage flag is set regardless the VCC undervoltage flag, the wake-up flag and the host input pins (EN, STBN).
- Starting from every operation mode except SLEEP the device enters STANDBY in case VCC undervoltage flag is set and VBAT and VIO undervoltage flags are not set, regardless the wake-up flag indication and the host input pins state.
- Starting from a low-power mode the device enters the operation mode indicated by the host input pins if a wake-up event occurs.
- In case all the undervoltage flags are reset the operation mode is selected by the wake-up flag and the host pins according to [Table 18](#)



Table 18. Pin Signalling in Operating Modes

| Inputs | | Operation Mode | Outputs | | | |
|--------|----|--------------------------|---------------------------|--------------------|----------|-----------------------|
| STBN | EN | | RxD | RxEN | INH1 | INH2 |
| H | H | NORMAL | L Bus = Data_0 | L Bus = Active | H | H |
| | | | H Bus = Idle or Data_1 | H Bus = Idle | | |
| H | L | RECEIVE-ONLY | L Bus = Data_0 | L Bus = Active | H | H |
| | | | H Bus = Idle or Data_1 | H Bus = Idle | | |
| L | H | GO-TO-SLEEP ¹ | NOT [Wake-up flag] | NOT [Wake-up flag] | H | Floating ² |
| L | L | STANDBY | NOT [Wake-up flag] | NOT [Wake-up flag] | H | Floating ² |
| L | X | SLEEP ³ | NOT [Wake-up flag] | NOT [Wake-up flag] | Floating | Floating |

1. If GO-TO-SLEEP is selected for more than t_{SLEEP} then the device will enter SLEEP only if the wake-up flag is not set otherwise it will remain in GO-TO-SLEEP.
2. If wake-up flag is set INH2=H otherwise INH2=floating.
3. Starting from SLEEP, if the wake-up flag is set, the device enters STANDBY regardless of the host pins state and undervoltage flags. Starting from SLEEP, if the wake up flag is not set, the only operating mode that can be entered through host pins are the non-low-power modes.

Note: "H" = Digital level high; "L" = Digital level low; "X" = Don't care; "Floating" = the analog output is not driven.

Table 19. Mode Transitions

| Initial Mode | Supply Undervoltage Flag / Event | | | Wake Flag | Host Event | | Next Mode |
|--------------|----------------------------------|------------------|-----------------|-----------|------------|-----|--------------|
| | V _{IO} | V _{BAT} | V _{CC} | | STBN | EN | |
| NORMAL | L | L | L | X | H | H→L | RECEIVE-ONLY |
| | L | L | L | X | H→L | H→L | STANDBY |
| | L | L | L→H | X | X | X | |
| | L | L | L | X | H→L | H | GO-TO-SLEEP |
| | L→H | L | X | X | X | X | SLEEP |
| | X | L→H | L | X | X | X | |
| RECEIVE-ONLY | L | L | L | X | H | L→H | NORMAL |
| | L | L | L | X | H→L | L | STANDBY |
| | L | L | L→H | X | X | X | |
| | L→H | L | X | X | X | X | SLEEP |
| | X | L→H | L | X | X | X | |



Table 19. Mode Transitions

| Initial Mode | Supply Undervoltage Flag / Event | | | Wake Flag | Host Event | | Next Mode |
|--------------|----------------------------------|------------------|-----------------|-----------|----------------|----------------|--------------|
| | V _{IO} | V _{BAT} | V _{CC} | | STBN | EN | |
| STANDBY | L | L | H → L | X | H | H | NORMAL |
| | L | L | L | X | L → H | L → H | |
| | L | L | (b) H → L | (a) → H | H | H | |
| | L | L | L | X | L → H | L | RECEIVE-ONLY |
| | L | L | H → L | X | H | L | |
| | L | L | (b) H → L | (a) → H | H | L | |
| | L | L | L | X | L | L → H | GO-TO-SLEEP |
| | L | L | H → L | X | L | H | |
| | L | L | H → L | (a) → H | L | H | |
| | L → H | L | X | X | X | X | SLEEP |
| X | L → H | L | X | X | X | | |
| GO-TO-SLEEP | L | L | L | X | LH | H | NORMAL |
| | L | L | L → H | X | X | X | STANDBY |
| | L | L | L | X | L | H → L | |
| | L | L | L | L | L ¹ | H ¹ | SLEEP |
| | L → H | L | X | X | X | X | |
| | X | L → H | L | X | X | X | |
| SLEEP | L | L | L | L | LH | H | NORMAL |
| | H → L | L | L | L | H | H | |
| | L | H → L | L | L | H | H | |
| | L | L | H → L | L | H | H | RECEIVE-ONLY |
| | L | L | L | L | L → H | L | |
| | H → L | L | L | L | H | L | |
| | L | H → L | L | L | H | L | |
| | L | L | H → L | L | H | L | |
| (b) → L | (b) → L | (b) → L | (a) → H | X | X | STANDBY | |
| POWER-OFF | X | H → L | X | X | X | X | STANDBY |
| Any | X | H | L → H | X | X | X | POWER-OFF |
| | X | L → H | H | X | X | X | |

1. If GO-TO-SLEEP is selected for more than t_{SLEEP}

Notes:

1. (a) indicates the event that causes the transition.
2. (b) indicates the consequence of the event (a).
3. "H" = Digital level high; "L" = Digital level low; "X" = Don't care.



7.11.1 Error Pin Signalling

In Table 20 the signaling at the Error Not (ERRN) pin is shown.

Table 20. Error Not (ERRN) Signalling

| Supply undervoltage Flag at VBAT, VIO, VCC | Remote Wake Flag | Local Wake Flag | Host Command | | ERRN |
|--|----------------------|----------------------|--------------|----------------------|----------------------|
| | | | STBN | EN | |
| L | X | X | H | H | NOT [Error flag] |
| L | H | X | H | L | L |
| L | H | X | H | ↑ (positive edge) | L → NOT [Error flag] |
| L | L | X | H | L | H |
| L | L | X | H | ↑ (positive edge) | H → NOT [Error flag] |
| L | L | L | L | X | H |
| L | L | ↑ (positive edge) | L | X | H → L |
| L | ↑ (positive edge) | L | L | X | H → L |
| L | H | ↑ (positive edge) | L | X | L |
| L | ↑ (positive edge) | H | L | X | L |
| H | X | X | X | X | L |

7.12 Loss of Ground

In case the ground of the device is disconnected and the host pins are open the bus lines are switched to Idle_HZ.

7.13 ERROR Flags Description

All error flags are reset after error readout is completed (see Section 7.15) or in POWER-OFF mode.

7.13.1 Undervoltage Detected VBAT Flag

This flag is set if an undervoltage event at VBAT is detected. This flag signals if undervoltage was detected but will not initiate a mode change.

7.13.2 Undervoltage Detected VIO Flag

This flag is set if an undervoltage event at VIO is detected. This flag signals if undervoltage was detected but will not initiate a mode change.

7.13.3 Undervoltage Detected VCC Flag

This flag is set if an undervoltage event at VCC is detected. This flag signals if undervoltage was detected but will not initiate a mode change.

7.13.4 Bus Error

The bus error flag is set, after a time t_{BUS_INHIB} while the driver is enabled and activated until the end of the frame if

- 2 consecutive rising edges at the TxD pin without any rising edge at the RxD pin are detected, or
- 2 consecutive falling edges at the TxD pin without any falling edge at the RxD pin are detected.

The flag is only set in NORMAL mode.

7.13.5 Bus Open Line

BP open line can only be set in NORMAL mode if the driver is enabled. The flag is set if the absolute current through BP or BM is lower than I_{THL} for a time longer than t_{BUS_ERROR} . The flag is meaningful only if no short circuit flag is set.

7.13.6 BP Short Circuit to Vcc

BP short circuit to VCC can only be set in NORMAL mode if the driver is enabled. The flag is set if the absolute current flowing through BP is higher than I_{THH} during transmission of Data0 for a time longer than t_{BUS_ERROR} .



7.13.7 BP Short Circuit to GND

BP short circuit to GND can only be set in NORMAL mode if the driver is enabled. The flag is set if the absolute current flowing through BP is higher than I_{THH} during transmission of Data1 for a time longer than t_{BUS_ERROR} .

7.13.8 BM Short Circuit to Vcc

BM short circuit to VCC can only be set in NORMAL mode if the driver is enabled. The flag is set if the absolute current flowing through BM is higher than I_{THH} during transmission of Data1 for a time longer than t_{BUS_ERROR} .

7.13.9 BM Short Circuit to GND

BM short circuit to GND can only be set in NORMAL mode if the driver is enabled. The flag is set if the absolute current flowing through BM is higher than I_{THH} during transmission of Data0 for a time longer than t_{BUS_ERROR} .

7.13.10 Short Circuit between BP and BM

The flag is set if, after a time t_{BUS_INHIB} while the driver is enabled and active until the end of the current FlexRay frame and the absolute differential bus voltage is lower than V_{SHORT} .

7.13.11 Over-temperature

This flag can only be set and reset in the non-low-power modes. The flag is set if the junction temperature exceeds OT_{TH} and is reset if the junction temperature falls below OT_{TL} .

7.13.12 TxEN_BGE Timeout

This flag can only be set in NORMAL mode if the driver is enabled (TxEN is low and BGE is high) for a time longer than t_{TxEN_max} . It is reset after every status change at TxEN or BGE or if the device exits NORMAL mode. In case the flag is set the driver is disabled.

7.13.13 Error Flag

This flag is set if at least one error flag (as listed below) is set, except undervoltage VBAT, VIO and VCC (refer to sections 7.13.1, 7.13.2 & 7.13.3). The error flag is reset if none of the flags are set.

Table 21. Functional Blocks

| Section No. | Flag Name |
|-------------|---------------------------------|
| 7.13.4 | Bus Error |
| 7.13.5 | Bus Open Line |
| 7.13.6 | BP Short Circuit to VCC |
| 7.13.7 | BP Short Circuit to GND |
| 7.13.8 | BM Short Circuit to VCC |
| 7.13.9 | BM Short Circuit to GND |
| 7.13.10 | Short Circuit between BP and BM |
| 7.13.11 | Over-temperature |
| 7.13.12 | TxEN_BGE Timeout |

Note: The error flag is signalled on ERRN pin according to [Table 20](#).

7.14 STATUS Flags Description

7.14.1 Local and Remote Wake Flag

Local and remote flags and function are described in [Section 7.7 Wake-Up Events](#).

7.14.2 Power on Flag

The power on flag is set leaving the POWER-OFF state and it is reset entering a low-power mode after a non-low-power mode.

7.14.3 BGE Status

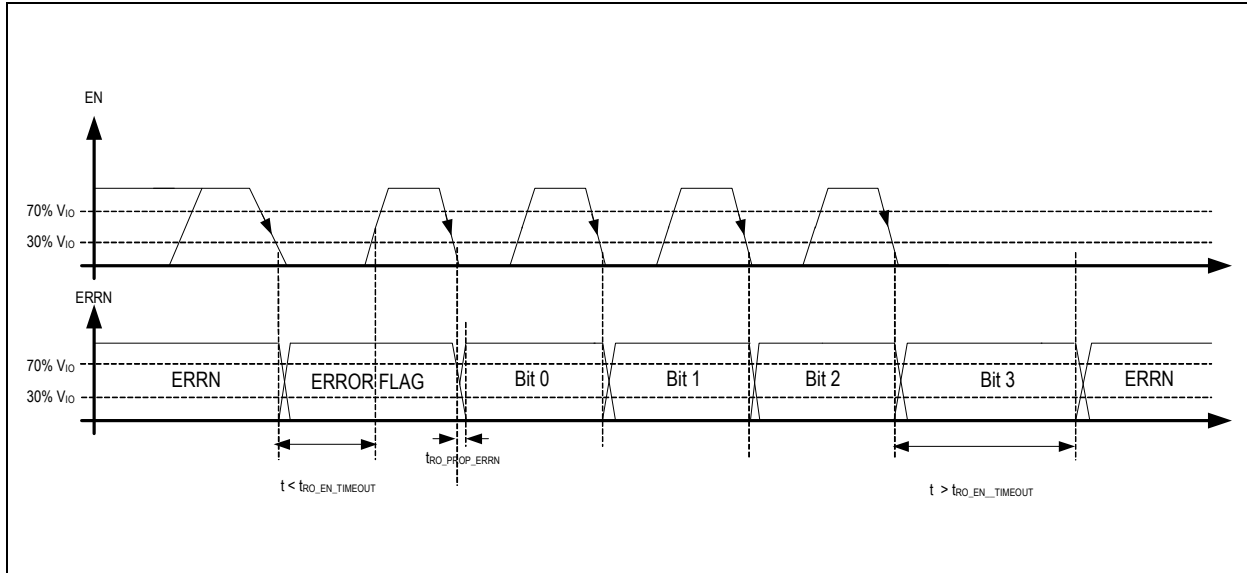
The BGE status flag is set if BGE is high and is reset if BGE is low. The state of the BGE is latched at the beginning of the readout cycle.



7.15 Error and Status Flags Read Out

The error and status flag readout mechanism is a serial transmission which is controlled with the EN pin and the information is submitted on the ERRN pin. The mechanism is only activated in NORMAL and RECEIVE-ONLY mode. In all other operation modes the error and status information cannot be accessed.

Figure 6. Timing of the Readout Mechanism



The error and status flags are read out by applying a clock signal to pin EN. A falling edge on pin EN starts the readout loading the content of the error/status flag into the shift register and signaling the stream of flags on the ERRN pin. On the second falling edge the first flag (Bit 0) will be shifted out. The ERRN data is valid after $t_{RO_PROP_ERRN}$. If EN pin keeps on toggling after last flag (Bit 15) the next flag shifted out is Bit 0. The complete list of bits is shown in Table 22. If no transition is detected on pin EN for longer than $t_{RO_EN_TIMEOUT}$ the device enters the operation mode indicated by the host pins.

Table 22. Bit Order for the Readout Sequence

| BIT | Flag Description |
|--------|--|
| Bit 0 | Undervoltage V _{BAT} detected |
| Bit 1 | Undervoltage V _{IO} detected |
| Bit 2 | Undervoltage V _{CC} detected |
| Bit 3 | Bus error |
| Bit 4 | BGE status |
| Bit 5 | BP short circuit to V _{CC} |
| Bit 6 | BP short circuit to GND |
| Bit 7 | Bus open line |
| Bit 8 | BM short circuit to V _{CC} |
| Bit 9 | BM short circuit to GND |
| Bit 10 | Short circuit between BP and BM |
| Bit 11 | Over temperature |
| Bit 12 | TxEN_BGE timeout |
| Bit 13 | Local wake flag |
| Bit 14 | Remote wake flag |
| Bit 15 | Power on flag |



8 Bus Driver

8.1 AS8222 Bus States

Activity: Differential bus signals as shown in chapter 10.3 Transmitter and 10.4 Receiver applies.

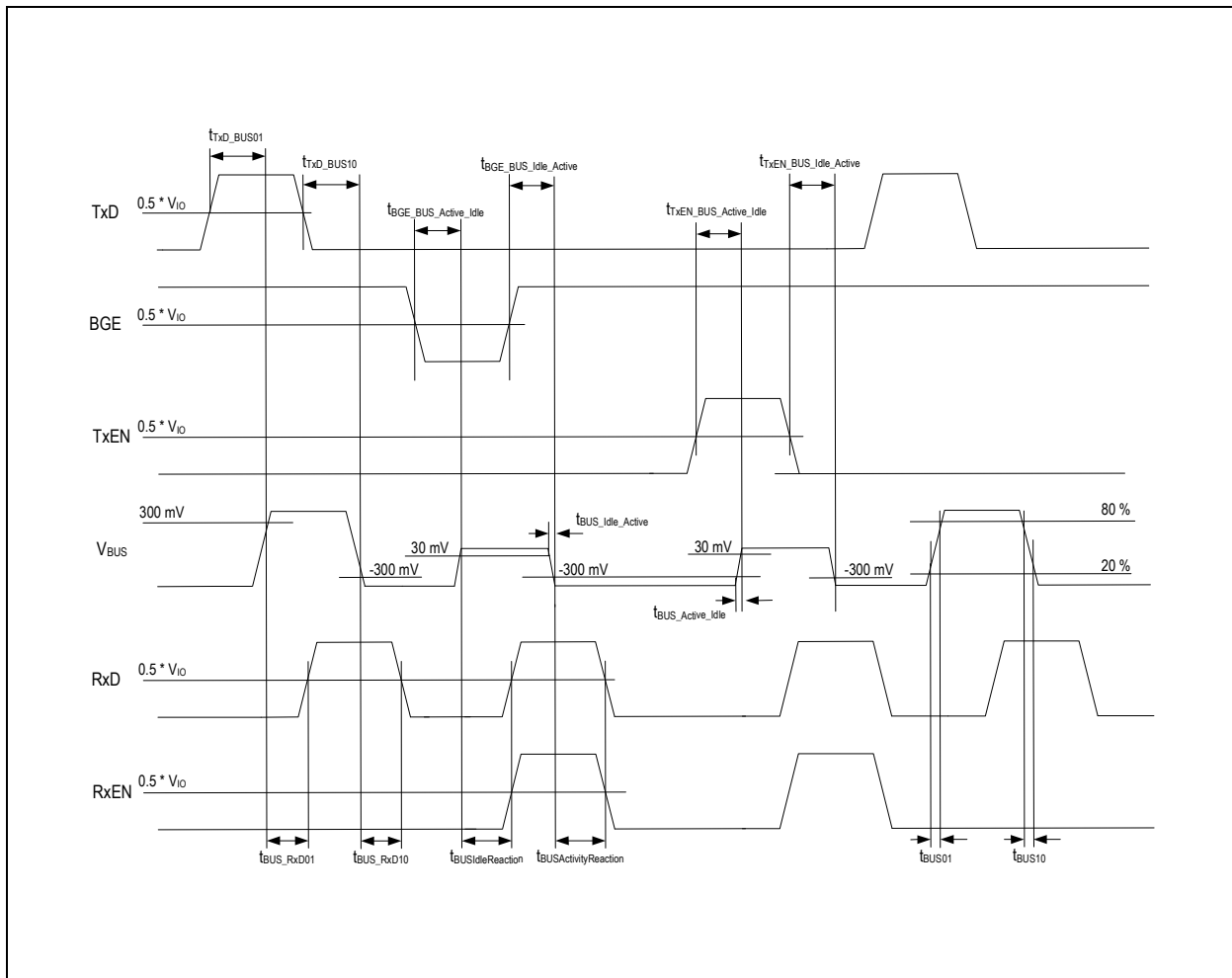
Idle: The bus wires are terminated to $V_{CC} / 2$ through the receiver input resistances.

Idle_LP: The bus wires are terminated to GND through the receiver input resistances.

Idle_HZ: The bus wires are not terminated. The input resistances are about $1 \text{ M}\Omega$.

8.2 Transceiver Timing

Figure 7. Bus Driver Timing Diagram



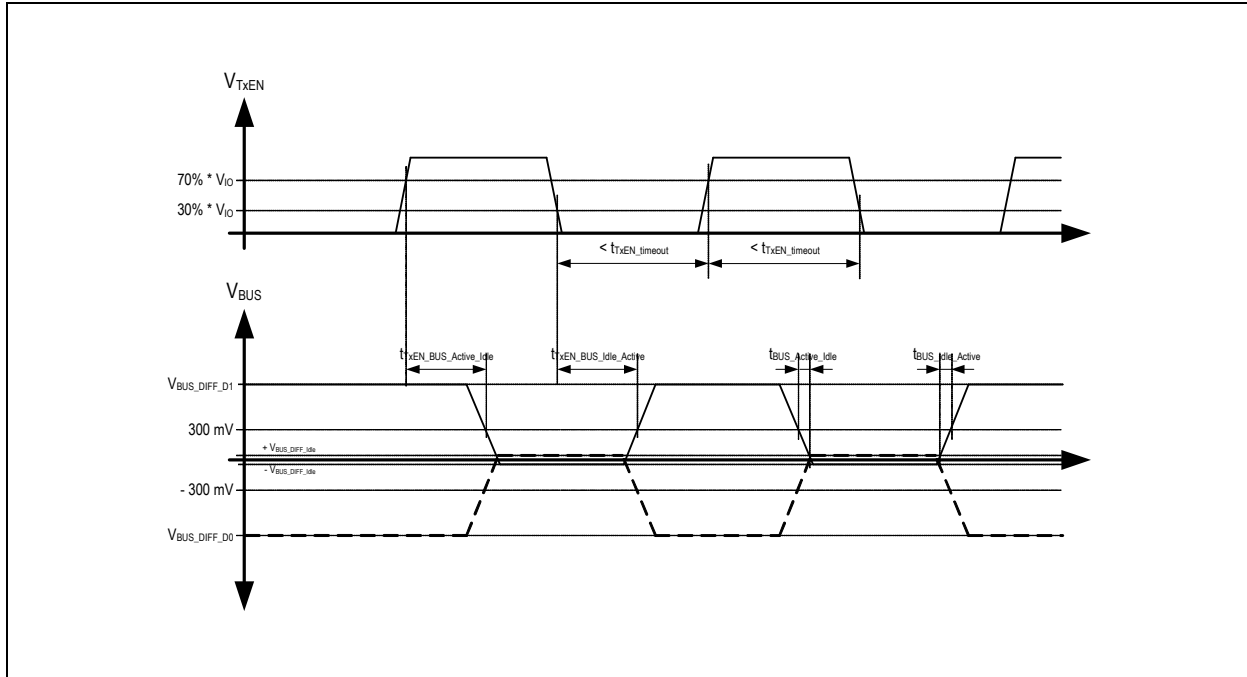


8.3 Transmitter

In NORMAL mode, while BGE is high, the transmitter drives full voltage levels on the bus after $t_{TXEN_BUS_Idle_Active}$ from TxEN falling edge and drives idle after $t_{TXEN_BUS_Active_Idle}$ from TxEN rising edge.

The Transmitter is not permanently enabled. If after the time $t_{TXEN_timeout}$ no edge is detected at TxEN, the transmission will be stopped to avoid unwanted collisions on the FlexRay bus.

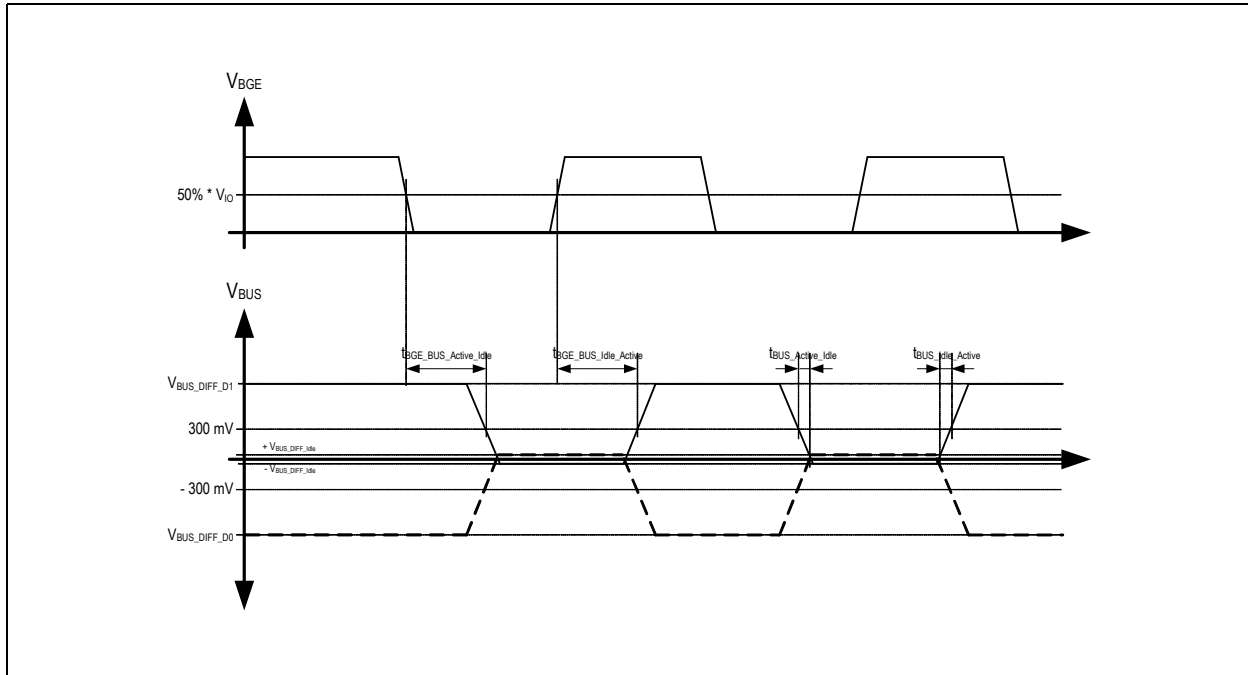
Figure 8. Transmitter Characteristics (TxEN → BUS, while BGE is high)



In NORMAL mode, while TxEN is high, the transmitter drives full voltage levels on the bus after $t_{TXEN_BUS_Idle_Active}$ from BGE rising edge and drives idle after $t_{TXEN_BUS_Active_Idle}$ from BGE falling edge.

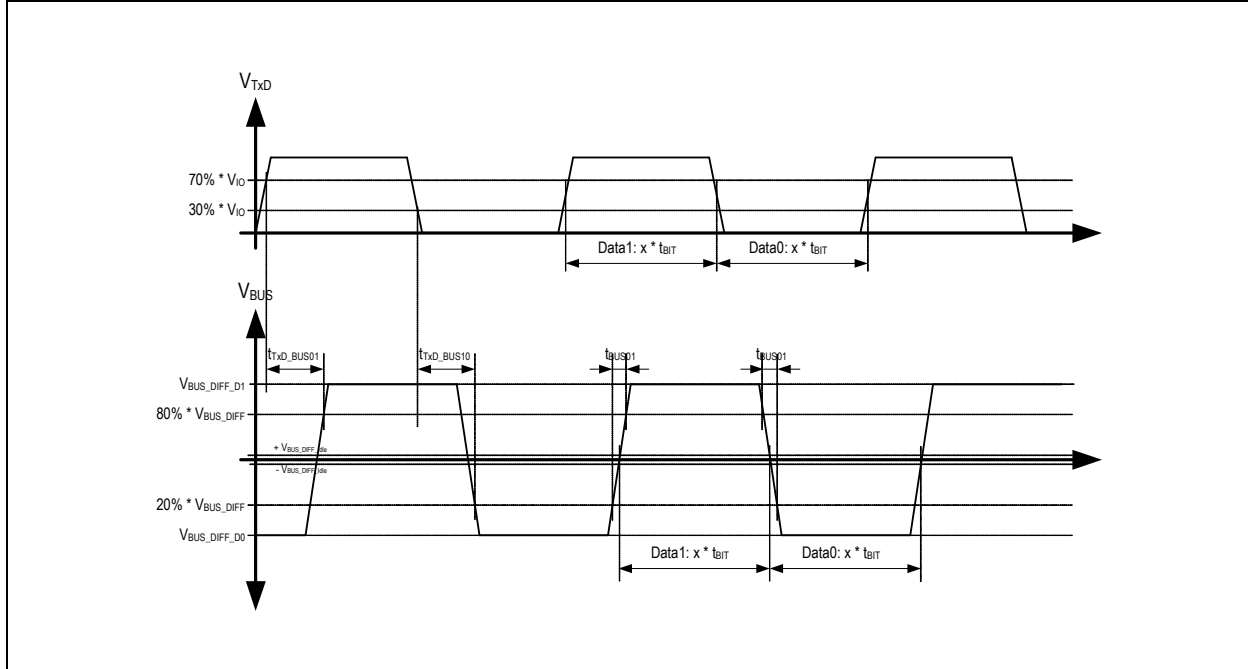


Figure 9. Transmitter Characteristics (BGE → BUS, while TxEN is low)



The transmitter generates the FlexRay differential bus voltage according to input signal on TxD as shown in Figure 10.

Figure 10. Transmitter Characteristics TxD → BUS



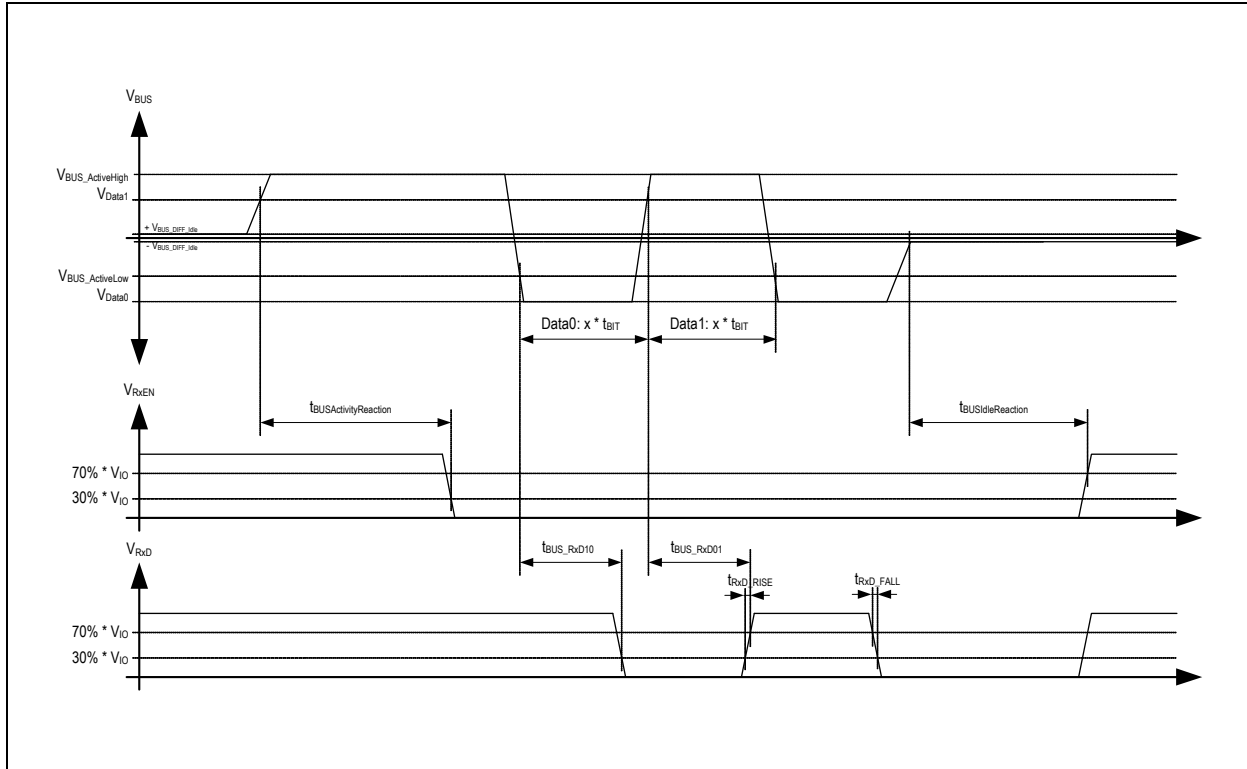
In NORMAL and RECEIVE-ONLY mode the transmitter drives Idle on the bus in case no data are transmitted. In STANDBY, GO-TO-SLEEP and SLEEP mode the transmitter drives Idle_LP (idle low-power) on the bus pins. In POWER_OFF mode the bus pins shows Idle_HZ (idle high impedance).



8.4 Receiver

The receiver generates from the FlexRay differential bus voltage a digital signal on the RxD and RxEN pins. RxD shows the data (Data0 and Data1) and RxEN shows the bus idle and activity status received on the bus pins. The receiver is only active in NORMAL and RECEIVE_ONLY mode.

Figure 11. Timing Characteristics (BUS → RxD and RxEN)



8.4.1 Bus activity and idle detection (only in NORMAL and RECEIVE ONLY mode)

- If the absolute differential bus voltage is higher than $V_{BUSActiveLow}$ and less than $V_{BUSActiveHigh}$ for a time longer than $t_{BUSIdleDetection}$, bus Idle is detected, RxEN and RxD are switched to logical high after with a time $t_{BUSIdleReaction}$.
- If the absolute differential bus voltage is higher than $V_{BUSActiveHigh}$ or lower than $V_{BUSActiveLow}$ for a time longer than $t_{BUSActivityDetection}$, bus Activity is detected, RxEN is switched to logical low and RxD is following the detected bus data states as indicated below with a time $t_{BUSActivityReaction}$.

Table 23. Logic Table for Receiver Bus Signal Detection

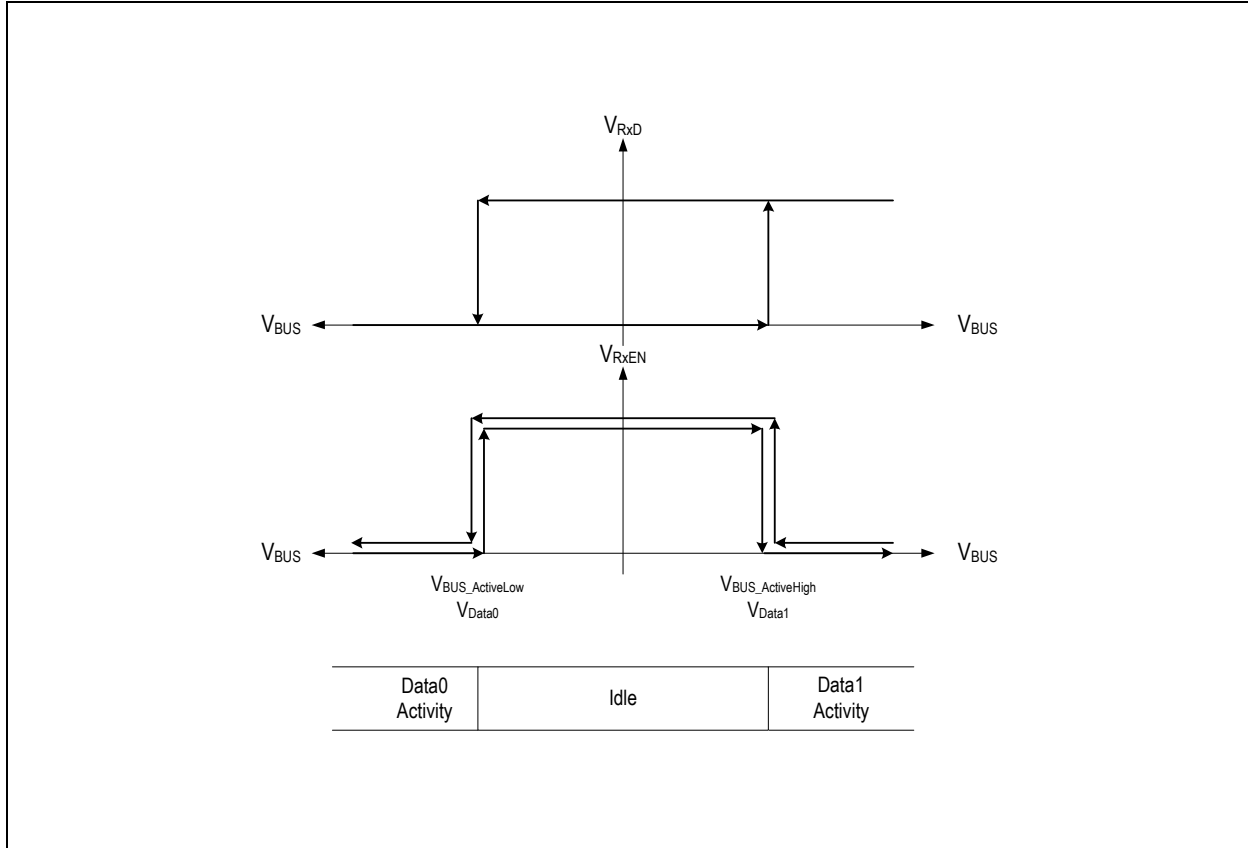
| Receiver Operation Mode | Bus State / Signals | RxEN | RxD |
|---|---------------------|------|-----|
| Normal power modes (NORMAL and RECEIVE-ONLY mode) | Idle | H | H |
| | Data0 | L | L |
| | Data1 | L | H |



8.4.2 Bus Data Detection (Only in NORMAL and RECEIVE ONLY Mode)

- If, after the activity detection the differential bus voltage is higher than V_{Data1} , RxD will be high after a time t_{BUS_RxD01} .
- If, after the activity detection the differential bus voltage is lower than V_{Data0} , RxD will be low after a time t_{BUS_RxD10} .

Figure 12. Receiver Characteristics (BUS → RxD and RxEN)

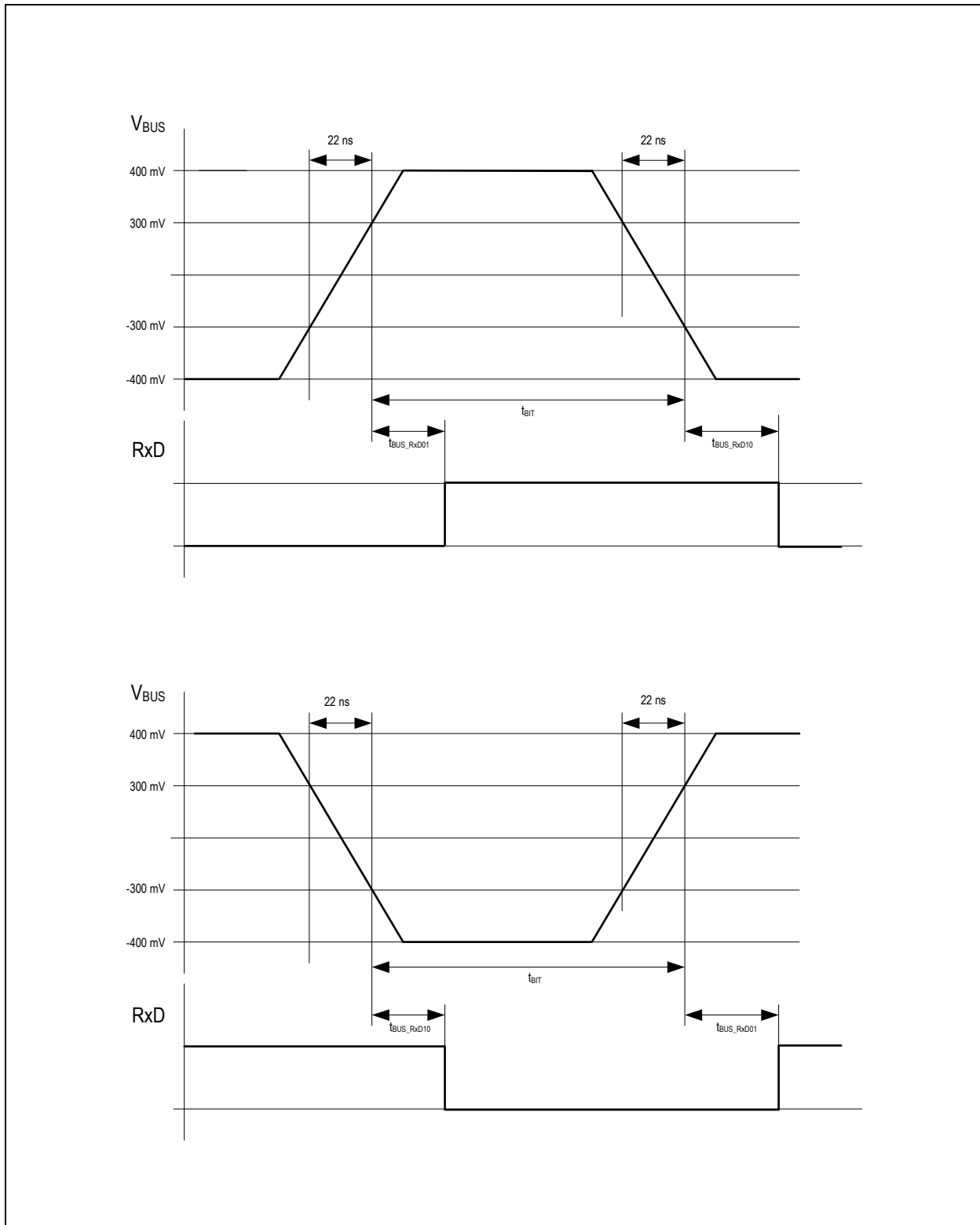




8.4.3 Receiver Test Signal

In Figure 13 the receiver test signal according the FlexRay Electrical Physical Layer specification is shown.

Figure 13. Receiver Test Signal

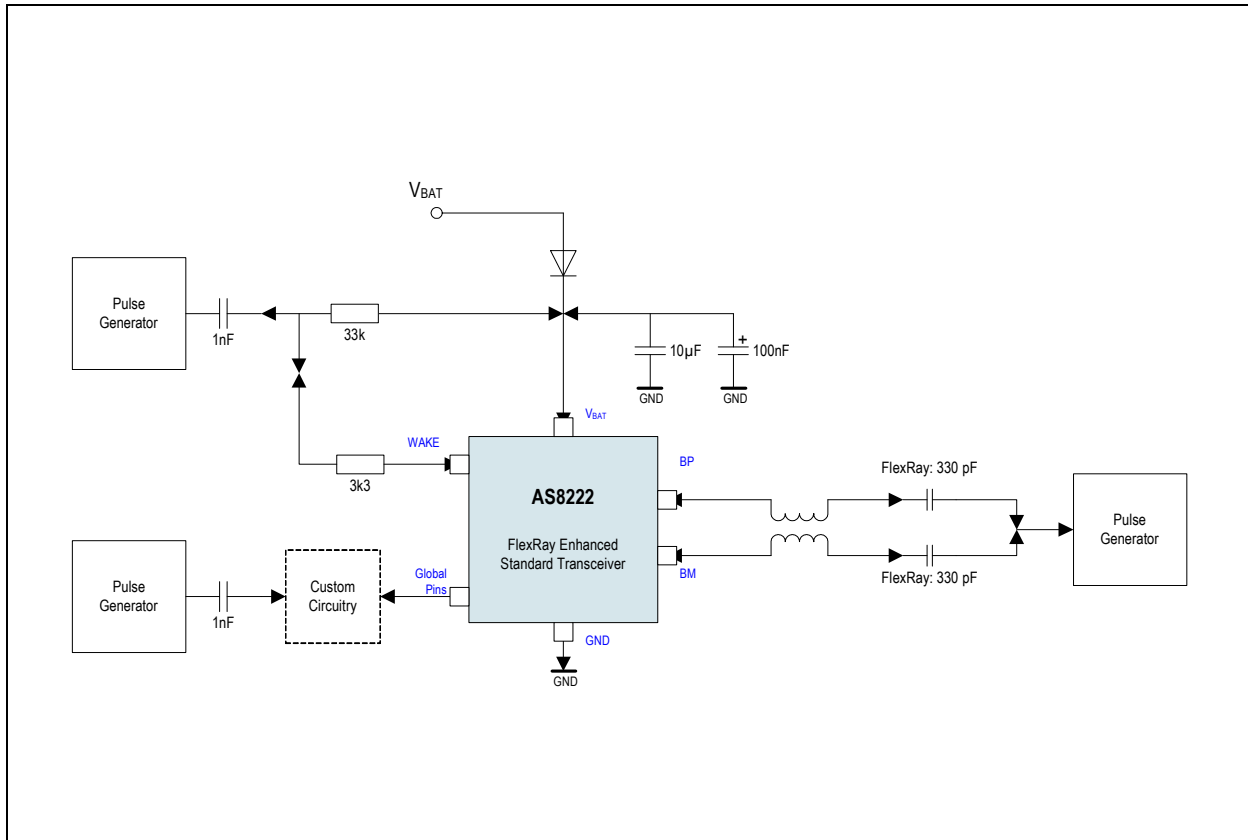




9 Test circuits

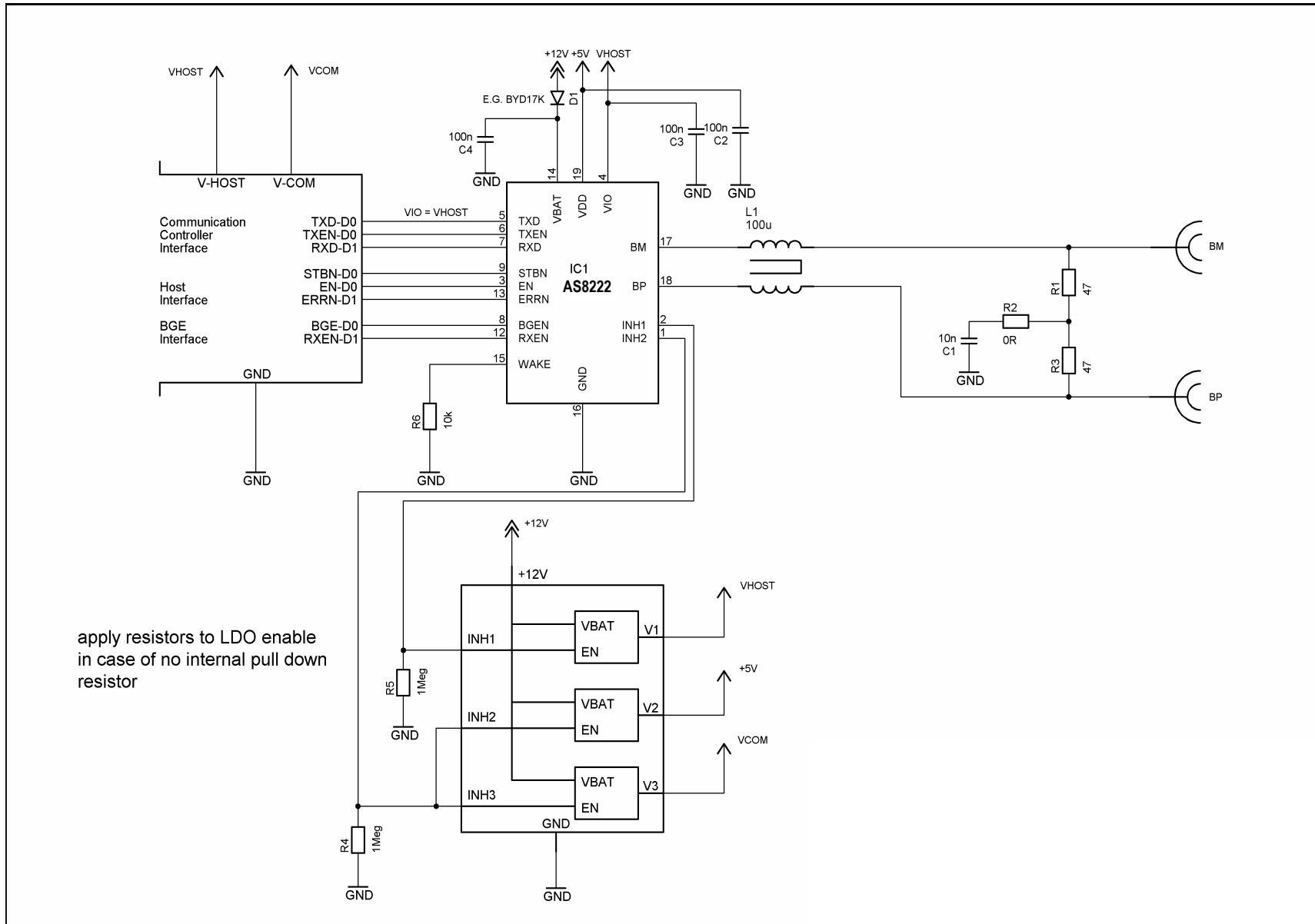
9.1 ISO7637-2 Test Pulses - Class D

Figure 14. Test Circuitry for ISO 7637 - 2 Test Pulses



9.2 Application Circuit

Figure 15. AS8222 Application Schematic





10 Appendix

10.1 FlexRay Functional Classes

The AS8222 FlexRay Enhances Standard Transceiver has the following Bus Driver function classes according the FlexRay Electrical Physical Layer Specification V2.1 Rev B implemented:

- Functional Class: Chapter 8.13.1 “Bus Driver voltage regulator control”
- Functional Class: Chapter 8.13.2 “Bus Driver - Bus Guardian interface”
- Functional Class: Chapter 8.13.4 “Bus Driver logic level adaptation”

10.2 FlexRay Parameter Comparison

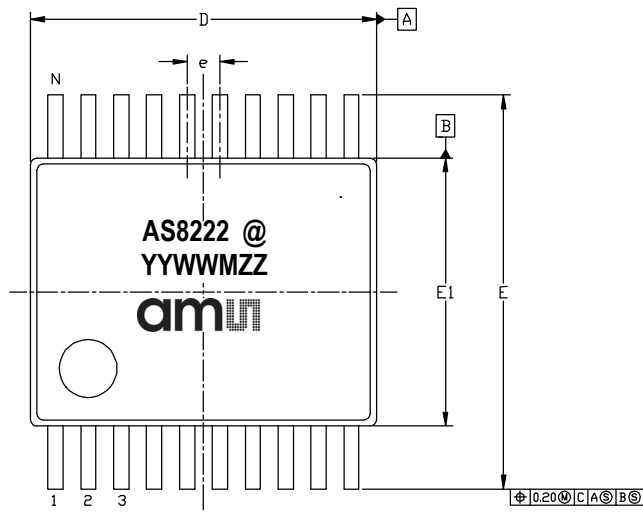
[FlexRay Electrical Physical Layer Specification V2.1 Rev. B](#) parameters are shown in color blue in tables (2 to 15).



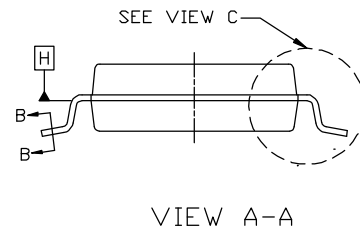
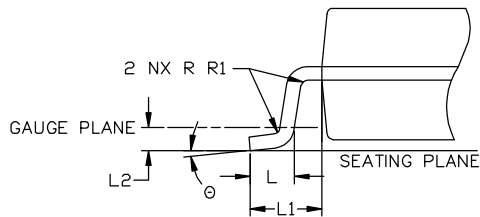
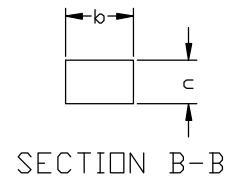
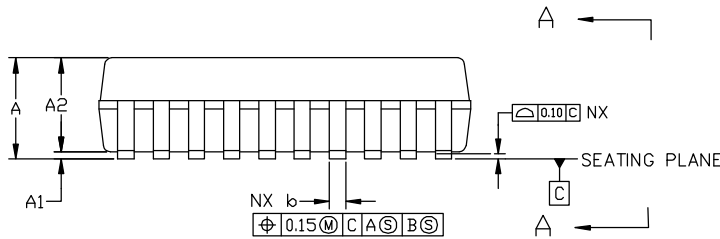
11 Package Drawings and Markings

The product is available in 20-Lead Shrink Small Outline Package SSOP-20.

Figure 16. Drawings and Dimensions



| Symbol | Min | Nom | Max |
|--------|------|----------|------|
| A | 1.73 | 1.86 | 1.99 |
| A1 | 0.05 | 0.13 | 0.21 |
| A2 | 1.68 | 1.73 | 1.78 |
| b | 0.22 | 0.30 | 0.38 |
| c | 0.09 | 0.17 | 0.25 |
| D | 6.90 | 7.20 | 7.50 |
| E | 7.40 | 7.80 | 8.20 |
| E1 | 5.00 | 5.30 | 5.60 |
| e | - | 0.65 BSC | - |
| L | 0.55 | 0.75 | 0.95 |
| L1 | - | 125 REF | - |
| L2 | - | 0.25 BSC | - |
| R | 0.09 | - | - |
| θ | 0° | 4° | 8° |
| N | | 20 | |



VIEW C

Notes:

1. Dimensions & tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. N is the total number of terminals.



Marking: YYWMZZ.

| YY | WW | M | ZZ | @ |
|------|--------------------|---------------------------|----------------------------|-------------------|
| Year | Manufacturing Week | Assembly plant identifier | Assembly traceability code | Sublot identifier |

Note: Package marking is not applied to engineering samples!



12 Ordering Information

Table 24. Ordering Information

| Ordering Code | Marking | Description | Delivery Form | Package |
|---------------|---------|--|--|---------|
| AS8222-HSSP | AS8222 | AS8222 Enhanced FlexRay Standard Transceiver | Tape & Reel in Dry Pack (1 reel = 2000 units) | SSOP-20 |
| AS8222-HSSM | AS8222 | AS8222 Enhanced FlexRay Standard Transceiver | Tape & Reel in Dry Pack (1 reel = 500 units) | SSOP-20 |

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Revision History

| Revision | Date | Owner | Description |
|----------|--------------|-------|-----------------|
| 1.0 | 11 Dec, 2012 | hgl | Initial version |

Note: Typos may not be explicitly mentioned under revision history.



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- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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