

## Dual 10GHz GBW, 1.1nV/ $\sqrt{\text{Hz}}$ Differential Amplifier/ADC Driver

### FEATURES

- 10GHz Gain-Bandwidth Product
- 85dB SFDR at 100MHz, 2V<sub>P-P</sub>
- 1.1nV/ $\sqrt{\text{Hz}}$  Input Noise Density
- Channel Separation 95dB at 100MHz
- Input Range Includes Ground
- External Resistors Set Gain (Min 1V/V)
- 3300V/ $\mu\text{s}$  Differential Slew Rate
- 52mA Supply Current (Per Amplifier)
- 2.7V to 5.25V Supply Voltage Range
- Fully Differential Input and Output
- Adjustable Output Common Mode Voltage
- Low Power Shutdown
- Small 20-Lead 4mm × 3mm × 0.75mm LQFN Package

### APPLICATIONS

- Broadband I/Q Amplifiers
- Dual Differential ADC Driver
- High-Speed Data-Acquisition Cards
- Automated Test Equipment
- Time Domain Reflectometry
- Communications Receivers

### DESCRIPTION

The LTC<sup>®</sup>6419 is a dual very high speed, low distortion, differential amplifier. Its input common mode range includes ground, so that a ground-referenced single-ended or differential input signal can be DC-coupled, level-shifted, and converted to drive an ADC differentially.

The gain and feedback resistors are external, so that the exact gain and frequency response can be tailored to each application. For example, the amplifier could be externally compensated in a no-overshoot configuration, which is desired in certain time-domain applications.

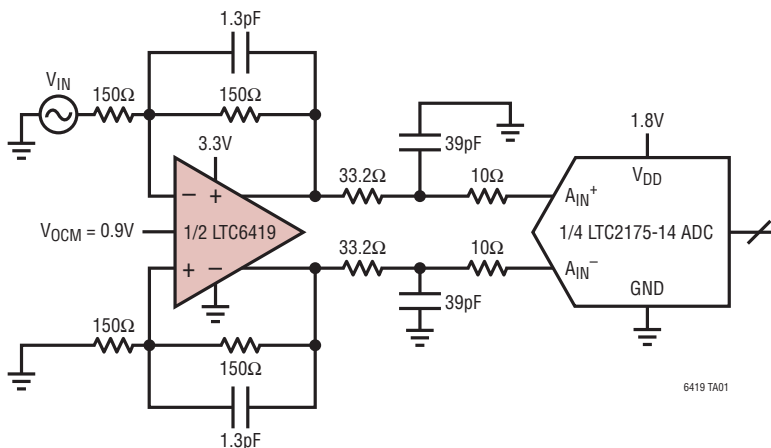
The LTC6419 is stable in a differential gain of 1. This allows for low output noise in applications where gain is not desired. Each amplifier draws 52mA of supply current and has an independent shutdown pin which reduces current consumption to 100 $\mu\text{A}$  per amplifier.

The LTC6419 is available in a compact 4mm × 3mm 20-pin LQFN package and operates over a -40°C to 125°C temperature range.

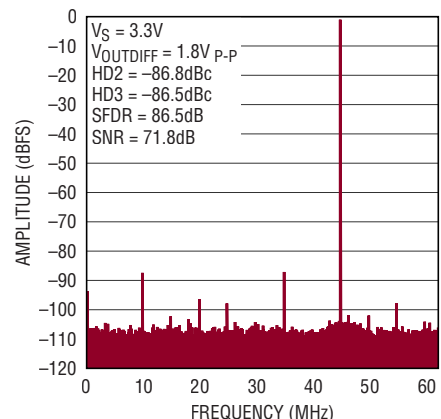
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### TYPICAL APPLICATION

DC-Coupled Interface from a Ground-Referenced Single-Ended Input to an LTC2175-14 ADC



1/2 LTC6419 Driving 1/4 LTC2175-14 ADC,  $f_{\text{IN}} = 45\text{MHz}$ , -1dBFS,  $f_{\text{S}} = 125\text{MHz}$ , 32768-Point FFT



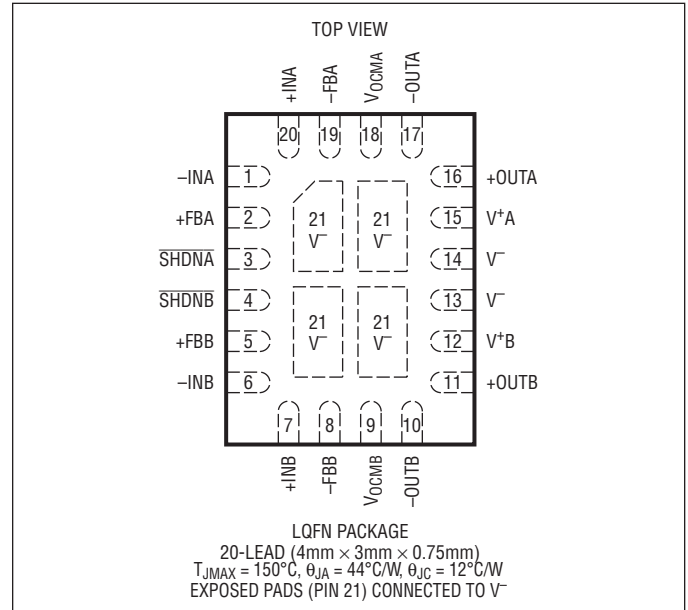
# LTC6419

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage ( $V^+A - V^-$ ), ( $V^+B - V^-$ ) .....	5.5V
Input Current (+INA, -INA, +INB, -INB, $V_{OCMA}$ , $V_{OCMB}$ , $\overline{SHDNA}$ , $\overline{SHDNB}$ ) (Note 2) .....	$\pm 10$ mA
Output Current (Note 13) .....	50mA <sub>RMS</sub>
Output Short-Circuit Duration (Note 3).....	Thermally Limited
Temperature Range (Notes 4, 5)	
LTC6419I .....	-40°C to 85°C
LTC6419H .....	-40°C to 125°C
Maximum Junction Temperature .....	150°C
Storage Temperature Range .....	-65°C to 150°C
Maximum Reflow (Package Body) Temperature .....	260°C

## PIN CONFIGURATION



## ORDER INFORMATION <http://www.linear.com/product/LTC6419#orderinfo>

PART NUMBER	PART MARKING*	FINISH CODE	PAD FINISH	PACKAGE** TYPE	MSL RATING	TEMPERATURE RANGE
LTC6419IV#PBF	6419	e4	Au (RoHS)	LQFN	3	-40°C to 85°C
LTC6419HV#PBF	6419					-40°C to 125°C

- Consult Marketing for parts specified with wider operating temperature ranges. Pad or ball finish code is per IPC/JEDEC J-STD-609. \*The temperature grade is identified by a label on the shipping container.
- Terminal Finish Part Marking: [www.linear.com/leadfree](http://www.linear.com/leadfree)
- Recommended PCB Assembly and Manufacturing Procedures: [www.linear.com/umodule/pcbassembly](http://www.linear.com/umodule/pcbassembly)
- Package and Tray Drawings: [www.linear.com/packaging](http://www.linear.com/packaging)

Parts ending with PBF are RoHS and WEEE compliant. \*\*The LTC6419 is a laminate package with the same dimensions as a standard 4mm × 3mm × 0.75mm QFN package.

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = V^+A = V^+B = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_{\text{ICM}} = V_{\text{OCMA}} = V_{\text{OCMB}} = 1.25\text{V}$ ,  $V_{\text{SHDNA}} = V_{\text{SHDNB}} = \text{open}$ .  $V_S$  is defined as  $(V^+ - V^-)$ .  $V_{\text{OUTCM}}$  is defined as  $(V_{+\text{OUT}} + V_{-\text{OUT}})/2$ .  $V_{\text{ICM}}$  is defined as  $(V_{+\text{IN}} + V_{-\text{IN}})/2$ .  $V_{\text{OUTDIFF}}$  is defined as  $(V_{+\text{OUT}} - V_{-\text{OUT}})$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{\text{OSDIFF}}$	Differential Offset Voltage (Input Referred)	$V_S = 3\text{V}$	●	±300	±1000	μV	
		$V_S = 3\text{V}$	●		±1200	μV	
		$V_S = 5\text{V}$	●	±300	±1100	μV	
		$V_S = 5\text{V}$	●		±1400	μV	
$\frac{\Delta V_{\text{OSDIFF}}}{\Delta T}$	Differential Offset Voltage Drift (Input Referred)	$V_S = 3\text{V}$	●	2		μV/°C	
		$V_S = 5\text{V}$	●	2		μV/°C	
$I_B$	Input Bias Current (Note 6)	$V_S = 3\text{V}$	●	-140	-62	0	μA
		$V_S = 5\text{V}$	●	-160	-70	0	μA
$I_{\text{OS}}$	Input Offset Current (Note 6)	$V_S = 3\text{V}$	●	±2	±10	μA	
		$V_S = 5\text{V}$	●	±2	±10	μA	
$R_{\text{IN}}$	Input Resistance	Common Mode		165		kΩ	
		Differential Mode		860		Ω	
$C_{\text{IN}}$	Input Capacitance	Differential Mode		0.5		pF	
$e_n$	Differential Input Noise Voltage Density	$f = 1\text{MHz}$ , Not Including $R_I/R_F$ Noise		1.1		nV/√Hz	
$i_n$	Input Noise Current Density	$f = 1\text{MHz}$ , Not Including $R_I/R_F$ Noise		8.8		pA/√Hz	
$e_{\text{nVOCM}}$	Common Mode Noise Voltage Density	$f = 10\text{MHz}$		12		nV/√Hz	
$V_{\text{ICMR}}$ (Note 7)	Input Signal Common Mode Range	$V_S = 3\text{V}$	●	0	1.5	V	
		$V_S = 5\text{V}$	●	0	3.5	V	
CMRRI (Note 8)	Input Common Mode Rejection Ratio (Input Referred) $\Delta V_{\text{ICM}}/\Delta V_{\text{OSDIFF}}$	$V_S = 3\text{V}$ , $V_{\text{ICM}}$ from 0V to 1.5V	●	75	90	dB	
		$V_S = 5\text{V}$ , $V_{\text{ICM}}$ from 0V to 3.5V	●	75	90	dB	
CMRRIO (Note 8)	Output Common Mode Rejection Ratio (Input Referred) $\Delta V_{\text{OCM}}/\Delta V_{\text{OSDIFF}}$	$V_S = 3\text{V}$ , $V_{\text{OCM}}$ from 0.5V to 1.5V	●	55	80	dB	
		$V_S = 5\text{V}$ , $V_{\text{OCM}}$ from 0.5V to 3.5V	●	60	85	dB	
PSRR (Note 9)	Differential Power Supply Rejection ( $\Delta V_S/\Delta V_{\text{OSDIFF}}$ )	$V_S = 2.7\text{V}$ to 5.25V	●	60	85	dB	
PSRRCM (Note 9)	Output Common Mode Power Supply Rejection ( $\Delta V_S/\Delta V_{\text{OCM}}$ )	$V_S = 2.7\text{V}$ to 5.25V	●	55	70	dB	
$V_S$	Supply Voltage Range (Note 10)		●	2.7	5.25	V	
$G_{\text{CM}}$	Common Mode Gain ( $\Delta V_{\text{OUTCM}}/\Delta V_{\text{OCM}}$ )	$V_S = 3\text{V}$ , $V_{\text{OCM}}$ from 0.5V to 1.5V	●	1		V/V	
		$V_S = 5\text{V}$ , $V_{\text{OCM}}$ from 0.5V to 3.5V	●	1		V/V	
$\Delta G_{\text{CM}}$	Common Mode Gain Error, $100 \times (G_{\text{CM}} - 1)$	$V_S = 3\text{V}$ , $V_{\text{OCM}}$ from 0.5V to 1.5V	●	±0.1	±0.3	%	
		$V_S = 5\text{V}$ , $V_{\text{OCM}}$ from 0.5V to 3.5V	●	±0.1	±0.3	%	
BAL	Output Balance ( $\Delta V_{\text{OUTCM}}/\Delta V_{\text{OUTDIFF}}$ )	$\Delta V_{\text{OUTDIFF}} = 2\text{V}$ Single-Ended Input	●	-65	-50	dB	
		Differential Input	●	-70	-50	dB	
$V_{\text{OSCM}}$	Common Mode Offset Voltage ( $V_{\text{OUTCM}} - V_{\text{OCM}}$ )	$V_S = 3\text{V}$	●	±1	±5	mV	
		$V_S = 5\text{V}$	●	±1	±6	mV	
$\frac{\Delta V_{\text{OSCM}}}{\Delta T}$	Common Mode Offset Voltage Drift		●	4		μV/°C	
$V_{\text{OUTCMR}}$ (Note 7)	Output Signal Common Mode Range (Voltage Range for the $V_{\text{OCMA}}/V_{\text{OCMB}}$ Pins)	$V_S = 3\text{V}$	●	0.5	1.5	V	
		$V_S = 5\text{V}$	●	0.5	3.5	V	
$R_{\text{INVOCM}}$	Input Resistance, $V_{\text{OCMA}}/V_{\text{OCMB}}$ Pins		●	30	40	50	kΩ
$V_{\text{OCM}}$	Self-Biased Voltage at the $V_{\text{OCMA}}/V_{\text{OCMB}}$ Pins	$V_S = 3\text{V}$ , $V_{\text{OCMA}} = V_{\text{OCMB}} = \text{Open}$	●	0.9	0.85	1.6	V
		$V_S = 5\text{V}$ , $V_{\text{OCMA}} = V_{\text{OCMB}} = \text{Open}$	●	0.9	1.25	1.6	V

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = V^+A = V^+B = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_{\text{ICM}} = V_{\text{OCMA}} = V_{\text{OCMB}} = 1.25\text{V}$ ,  $V_{\text{SHDNA}} = V_{\text{SHDNB}} = \text{open}$ .  $V_S$  is defined as  $(V^+ - V^-)$ .  $V_{\text{OUTCM}}$  is defined as  $(V_{+\text{OUT}} + V_{-\text{OUT}})/2$ .  $V_{\text{ICM}}$  is defined as  $(V_{+\text{IN}} + V_{-\text{IN}})/2$ .  $V_{\text{OUTDIFF}}$  is defined as  $(V_{+\text{OUT}} - V_{-\text{OUT}})$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{\text{OUT}}$	Output Voltage, High, Either Output Pin	$V_S = 3\text{V}$ , $I_L = 0$ $V_S = 3\text{V}$ , $I_L = -20\text{mA}$ $V_S = 5\text{V}$ , $I_L = 0$ $V_S = 5\text{V}$ , $I_L = -20\text{mA}$	● ● ● ●	1.85 1.8 3.85 3.8	2 1.95 4 3.95	V V V V	
	Output Voltage, Low, Either Output Pin	$V_S = 3\text{V}$ , $5\text{V}$ ; $I_L = 0$ $V_S = 3\text{V}$ , $5\text{V}$ ; $I_L = 20\text{mA}$	● ●		0.06 0.2	0.15 0.4	V V
$I_{\text{SC}}$	Output Short-Circuit Current, Either Output Pin (Note 11)	$V_S = 3\text{V}$	●	$\pm 50$	$\pm 70$	mA	
		$V_S = 5\text{V}$	●	$\pm 70$	$\pm 95$	mA	
$A_{\text{VOL}}$	Large-Signal Open Loop Voltage Gain			65		dB	
$I_S$	Supply Current (Per Amplifier)		●	52	56	mA	
					58	mA	
$I_{\text{SHDN}}$	Supply Current in Shutdown (Per Amplifier)	$V_{\text{SHDNA}} = V_{\text{SHDNB}} \leq 0.6\text{V}$	●	100	500	$\mu\text{A}$	
$R_{\text{SHDN}}$	SHDNA/SHDNB Pull-Up Resistor	$V_{\text{SHDNA}} = V_{\text{SHDNB}} = 0\text{V}$ to $0.5\text{V}$	●	115	150	185	$\text{K}\Omega$
$V_{\text{IL}}$	SHDNA/SHDNB Input Logic Low		●		0.6	V	
$V_{\text{IH}}$	SHDNA/SHDNB Input Logic High		●	1.4		V	
$t_{\text{ON}}$	Turn-On Time			160		ns	
$t_{\text{OFF}}$	Turn-Off Time			80		ns	
SR	Slew Rate	Differential Output, $V_{\text{OUTDIFF}} = 4\text{V}_{\text{P-P}}$ +OUTA/+OUTB Rising (–OUTA/–OUTB Falling) +OUTA/+OUTB Falling (–OUTA/–OUTB Rising)		3300 1720 1580		$\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$	
GBW	Gain-Bandwidth Product	$R_I = 25\Omega$ , $R_F = 10\text{k}\Omega$ , $f_{\text{TEST}} = 100\text{MHz}$	●	9.5 8	10	GHz GHz	
$f_{-3\text{dB}}$	–3dB Frequency	$R_I = R_F = 150\Omega$ , $R_{\text{LOAD}} = 400\Omega$ , $C_F = 1.3\text{pF}$		1.4		GHz	
$f_{0.1\text{dB}}$	Frequency for 0.1dB Flatness	$R_I = R_F = 150\Omega$ , $R_{\text{LOAD}} = 400\Omega$ , $C_F = 1.3\text{pF}$		320		MHz	
FPBW	Full Power Bandwidth	$V_{\text{OUTDIFF}} = 2\text{V}_{\text{P-P}}$		550		MHz	
	Channel Separation (Note 12)	$f = 100\text{MHz}$		95		dB	
HD2 HD3	25MHz Distortion	Differential Input, $V_{\text{OUTDIFF}} = 2\text{V}_{\text{P-P}}$ , $R_I = R_F = 150\Omega$ , $R_{\text{LOAD}} = 400\Omega$ 2nd Harmonic 3rd Harmonic			–82 –106	$\text{dBc}$ $\text{dBc}$	
	100MHz Distortion	Differential Input, $V_{\text{OUTDIFF}} = 2\text{V}_{\text{P-P}}$ , $R_I = R_F = 150\Omega$ , $R_{\text{LOAD}} = 400\Omega$ 2nd Harmonic 3rd Harmonic			–85 –85	$\text{dBc}$ $\text{dBc}$	
HD2 HD3	25MHz Distortion	Single-Ended Input, $V_{\text{OUTDIFF}} = 2\text{V}_{\text{P-P}}$ , $R_I = R_F = 150\Omega$ , $R_{\text{LOAD}} = 400\Omega$ 2nd Harmonic 3rd Harmonic			–96 –105	$\text{dBc}$ $\text{dBc}$	
	100MHz Distortion	Single-Ended Input, $V_{\text{OUTDIFF}} = 2\text{V}_{\text{P-P}}$ , $R_I = R_F = 150\Omega$ , $R_{\text{LOAD}} = 400\Omega$ 2nd Harmonic 3rd Harmonic			–83 –85	$\text{dBc}$ $\text{dBc}$	

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V^+ = V^+A = V^+B = 5\text{V}$ ,  $V^- = 0\text{V}$ ,  $V_{\text{CM}} = V_{\text{ICM}} = V_{\text{OCMA}} = V_{\text{OCMB}} = 1.25\text{V}$ ,  $V_{\text{SHDNA}} = V_{\text{SHDNB}} = \text{open}$ .  $V_S$  is defined as  $(V^+ - V^-)$ .  $V_{\text{OUTCM}}$  is defined as  $(V_{+\text{OUT}} + V_{-\text{OUT}})/2$ .  $V_{\text{ICM}}$  is defined as  $(V_{+\text{IN}} + V_{-\text{IN}})/2$ .  $V_{\text{OUTDIFF}}$  is defined as  $(V_{+\text{OUT}} - V_{-\text{OUT}})$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IMD3	3rd Order IMD at 25MHz f1 = 24.9MHz, f2 = 25.1MHz	$V_{\text{OUTDIFF}} = 1V_{\text{P-P}}$ per Tone, $R_I = R_F = 150\Omega$ , $R_{\text{LOAD}} = 400\Omega$		-103		dBc
	3rd Order IMD at 100MHz f1 = 99.9MHz, f2 = 100.1MHz	$V_{\text{OUTDIFF}} = 1V_{\text{P-P}}$ per Tone, $R_I = R_F = 150\Omega$ , $R_{\text{LOAD}} = 400\Omega$		-87		dBc
	3rd Order IMD at 140MHz f1 = 139.9MHz, f2 = 140.1MHz	$V_{\text{OUTDIFF}} = 1V_{\text{P-P}}$ per Tone, $R_I = R_F = 150\Omega$ , $R_{\text{LOAD}} = 400\Omega$		-77		dBc
$t_S$	Settling Time	$V_{\text{OUTDIFF}} = 2V_{\text{P-P}}$ Step, $R_I = R_F = 150\Omega$ , $R_{\text{LOAD}} = 400\Omega$ 1% Settling		1.9		ns

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Input pins (+INA, -INA, +INB, -INB,  $V_{\text{OCMA}}$ ,  $V_{\text{OCMB}}$ ,  $\overline{\text{SHDNA}}$ ,  $\overline{\text{SHDNB}}$ ) are protected by steering diodes to either supply. If the inputs should exceed either supply voltage, the input current should be limited to less than 10mA. In addition, the inputs (+INA/-INA or +INB/-INB) are protected by a pair of back-to-back diodes. If the differential input voltage exceeds 1.4V, the input current should be limited to less than 10mA.

**Note 3:** A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

**Note 4:** The LTC6419I is guaranteed functional over the temperature range of  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC6419H is guaranteed functional over the temperature range of  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Note 5:** The LTC6419I is guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ . The LTC6419H is guaranteed to meet specified performance from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Note 6:** Input bias current is defined as the average of the input currents flowing into the inputs (-INA/+INA or -INB/+INB). Input offset current is defined as the difference between the input currents ( $I_{\text{OS}} = I_{\text{B}^+} - I_{\text{B}^-}$ ).

**Note 7:** Input common mode range is tested by testing at both  $V_{\text{ICM}} = 1.25\text{V}$  and at the Electrical Characteristics table limits to verify that the differential offset ( $V_{\text{OSDIFF}}$ ) and the common mode offset ( $V_{\text{OSCM}}$ ) have not deviated by more than  $\pm 1\text{mV}$  and  $\pm 2\text{mV}$  respectively from the  $V_{\text{ICM}} = 1.25\text{V}$  case.

The voltage range for the output common mode range is tested by applying a voltage on the  $V_{\text{OCM}}$  pin and testing at both  $V_{\text{OCM}} = 1.25\text{V}$  and at the Electrical Characteristics table limits to verify that the common mode offset ( $V_{\text{OSCM}}$ ) has not deviated by more than  $\pm 6\text{mV}$  from the  $V_{\text{OCM}} = 1.25\text{V}$  case.

**Note 8:** Input CMRR is defined as the ratio of the change in the input common mode voltage at the pins (+INA/-INA or +INB/-INB) to the change in differential input referred offset voltage. Output CMRR is defined as the ratio of the change in the voltage at the  $V_{\text{OCMA}}$  or  $V_{\text{OCMB}}$  pins to the change in differential input referred offset voltage. This specification is strongly dependent on feedback ratio matching between the two outputs and their respective inputs and it is difficult to measure actual amplifier performance (See Effects of Resistor Pair Mismatch in the Applications Information section of this data sheet). For a better indicator of actual amplifier performance independent of feedback component matching, refer to the PSRR specification.

**Note 9:** Differential power supply rejection (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred offset voltage. Common mode power supply rejection (PSRR<sub>CM</sub>) is defined as the ratio of the change in supply voltage to the change in the output common mode offset voltage.

**Note 10:** Supply voltage range is guaranteed by power supply rejection ratio test.

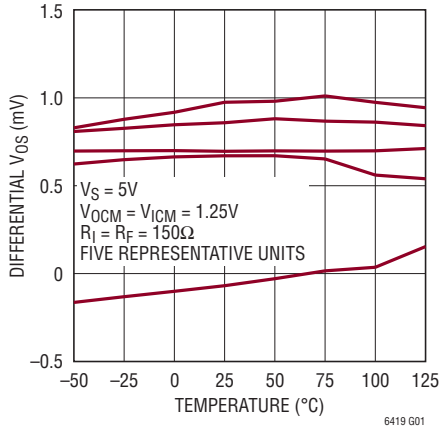
**Note 11:** Extended operation with the output shorted may cause the junction temperature to exceed the  $150^\circ\text{C}$  limit.

**Note 12:** Channel separation (the inverse of crosstalk) is measured by driving a signal into one input, while terminating the other input. Channel separation is the ratio of the resulting output signal at the driven channel to the channel that is not driven.

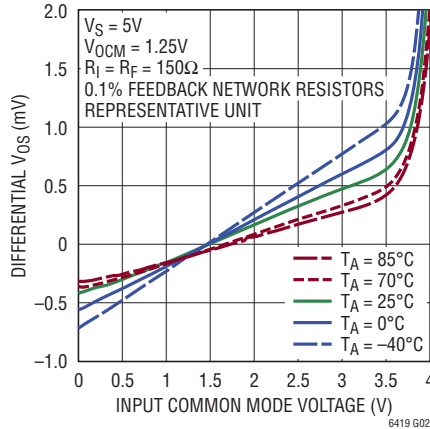
**Note 13:** The LTC6419 is capable of producing peak output currents in excess of 50mA. Current density limitations within the IC require the continuous RMS current supplied by the output (sourcing or sinking) over the operating lifetime of the part be limited to under 50mA (Absolute Maximum). Proper heat sinking may be required to keep the junction temperature below the absolute maximum rating.

# TYPICAL PERFORMANCE CHARACTERISTICS

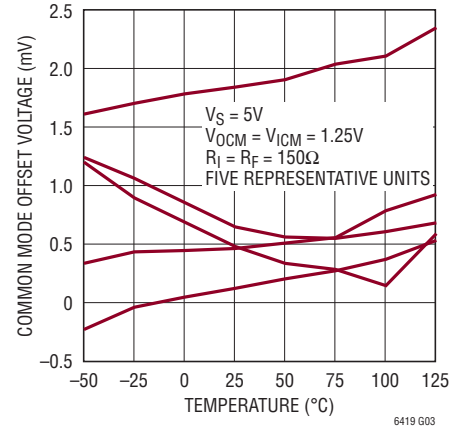
**Differential Input Offset Voltage vs Temperature**



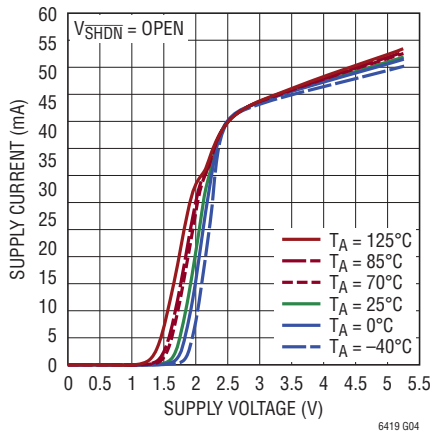
**Differential Input Offset Voltage vs Input Common Mode Voltage**



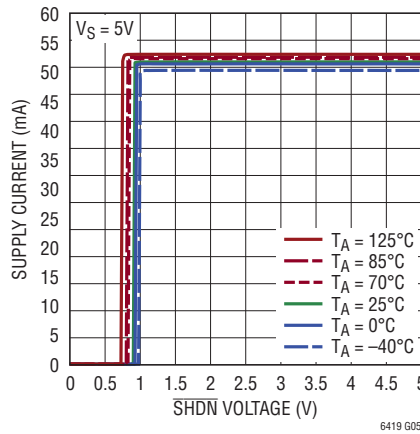
**Common Mode Offset Voltage vs Temperature**



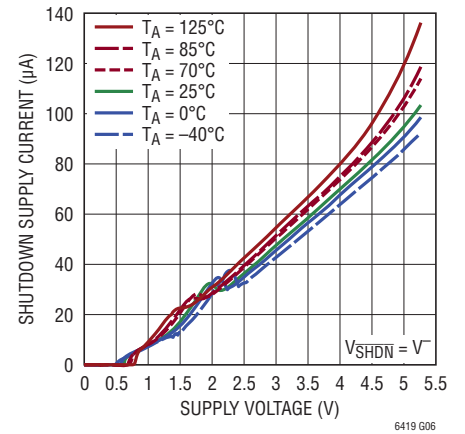
**Supply Current (per Amplifier) vs Supply Voltage**



**Supply Current (per Amplifier) vs SHDN Voltage**

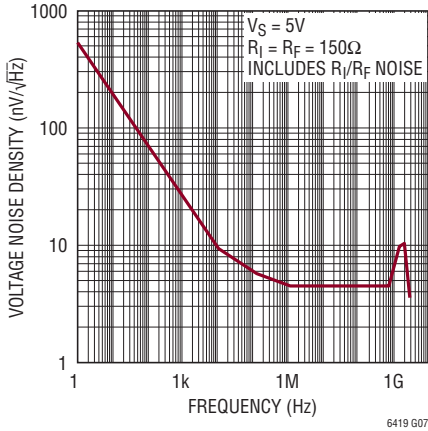


**Shutdown Supply Current (per Amplifier) vs Supply Voltage**

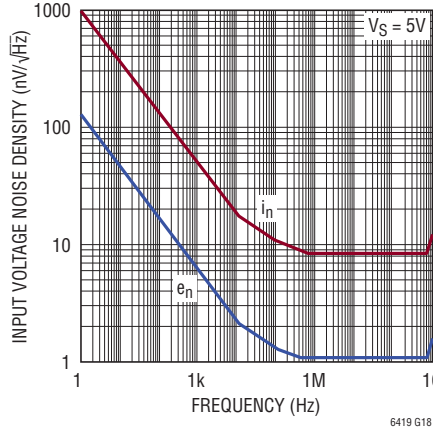


# TYPICAL PERFORMANCE CHARACTERISTICS

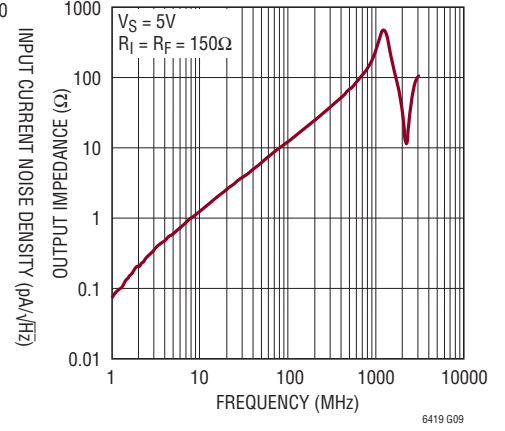
**Differential Output Voltage Noise vs Frequency**



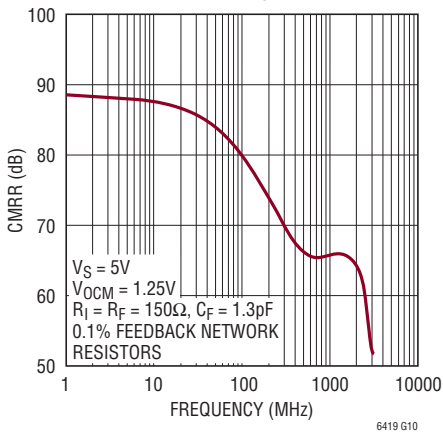
**Input Noise Density vs Frequency**



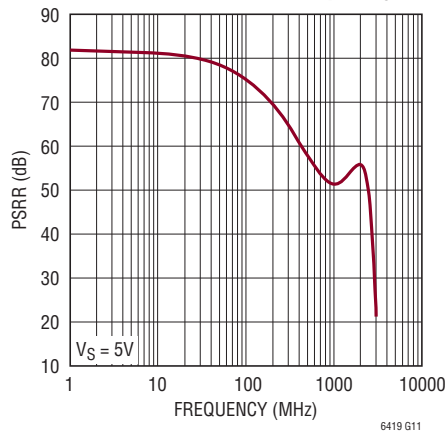
**Differential Output Impedance vs Frequency**



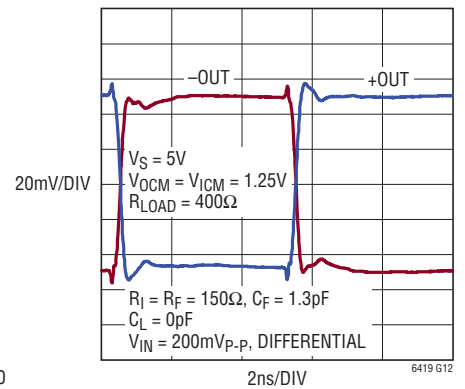
**CMRR vs Frequency**



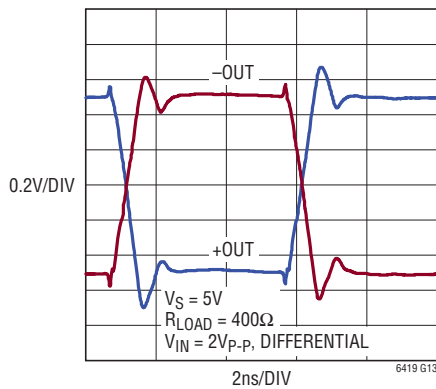
**Differential PSRR vs Frequency**



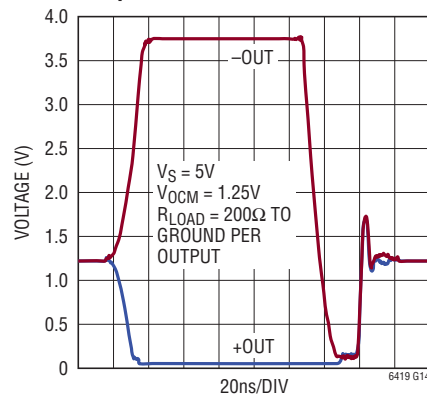
**Small Signal Step Response**



**Large Signal Step Response**

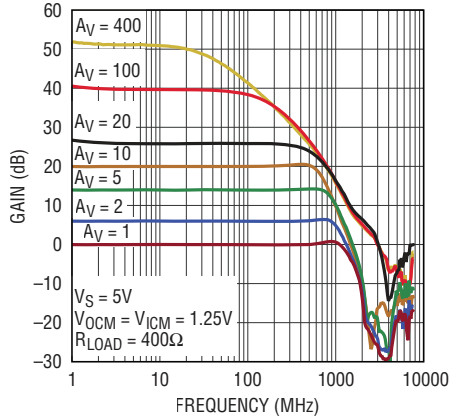


**Overdriven Output Transient Response**



## TYPICAL PERFORMANCE CHARACTERISTICS

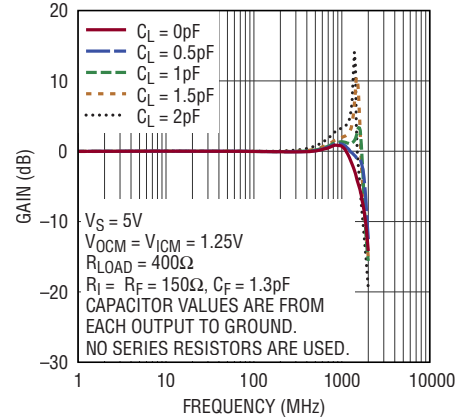
### Frequency Response vs Closed Loop Gain



$A_V$ (V/V)	$R_I$ ( $\Omega$ )	$R_F$ ( $\Omega$ )	$C_F$ (pF)
1	150	150	1.3
2	100	200	1
5	50	250	0.8
10	50	500	0.4
20	25	500	0.4
100	25	2.5k	0
400	25	10k	0

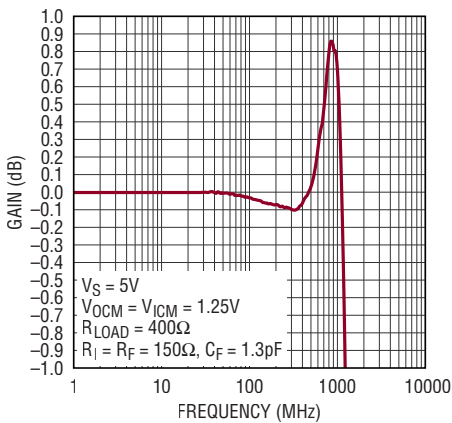
6419 G15

### Frequency Response vs Load Capacitance



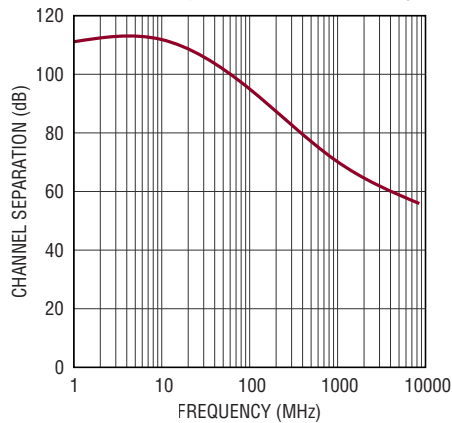
6419 G16

### Gain 0.1dB Flatness



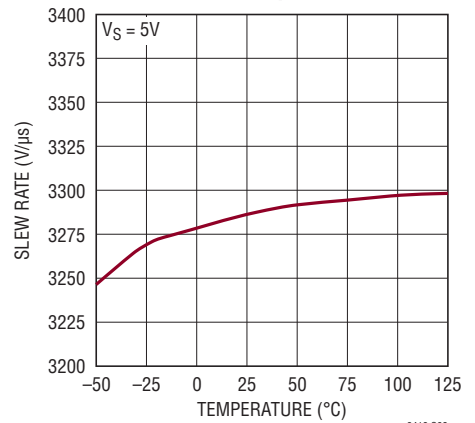
6419 G17

### Channel Separation vs Frequency



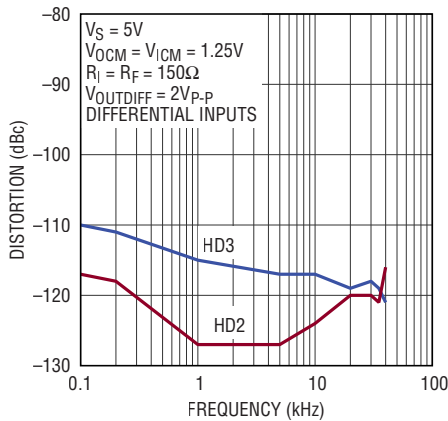
6419 G28

### Slew Rate vs Temperature



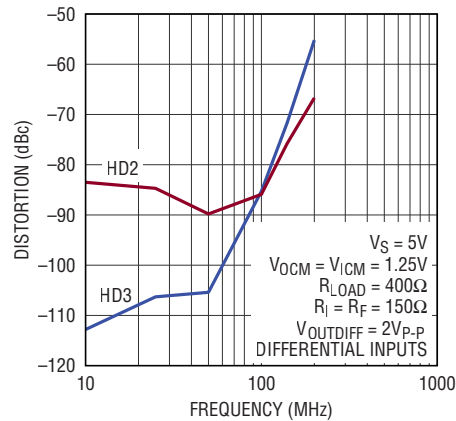
6419 G08

### Low-Frequency Harmonic Distortion



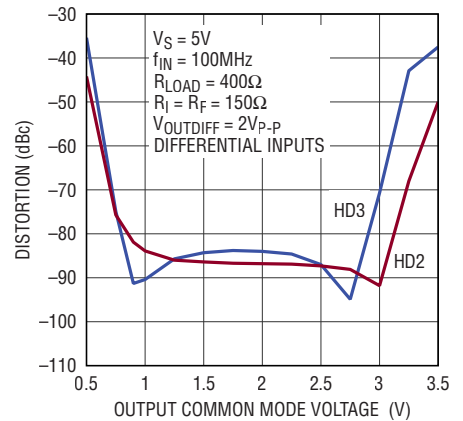
6419 G30

### Harmonic Distortion vs Frequency



6419 G19

### Harmonic Distortion vs Output Common Mode Voltage

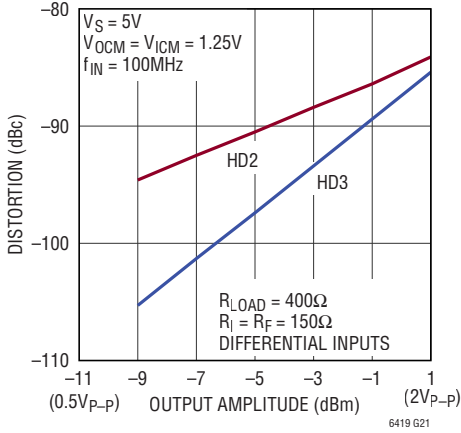


6419 G20

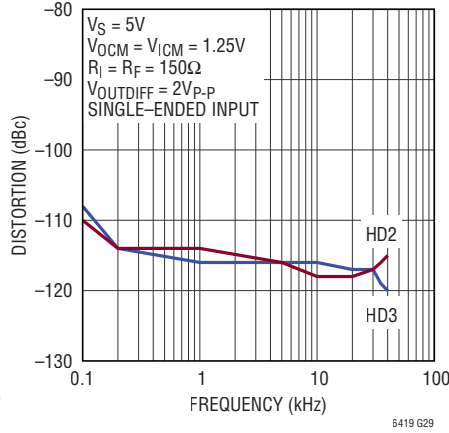


# TYPICAL PERFORMANCE CHARACTERISTICS

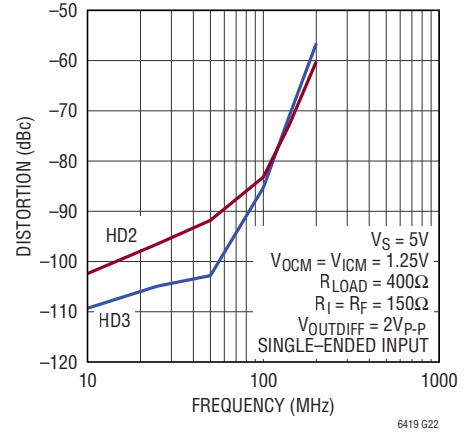
**Harmonic Distortion vs Output Amplitude**



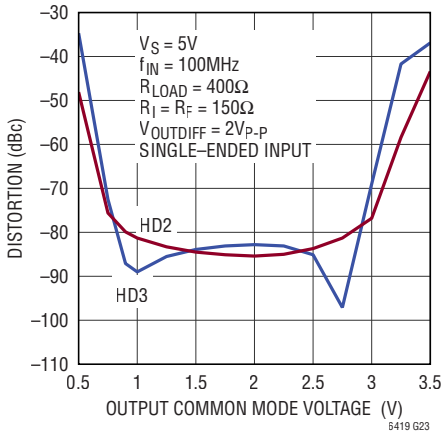
**Low-Frequency Harmonic Distortion**



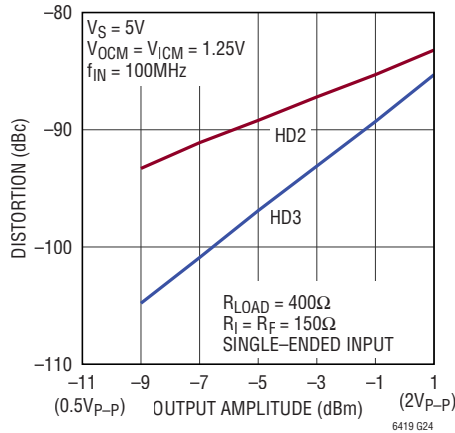
**Harmonic Distortion vs Frequency**



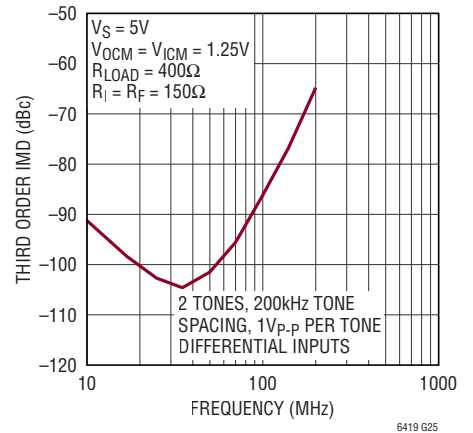
**Harmonic Distortion vs Output Common Mode Voltage**



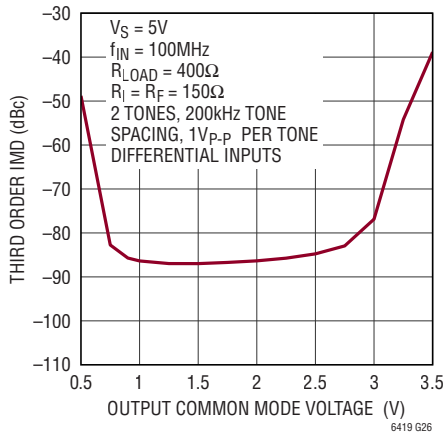
**Harmonic Distortion vs Output Amplitude**



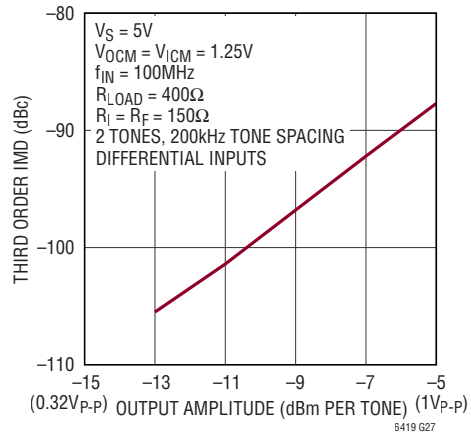
**Intermodulation Distortion vs Frequency**



**Intermodulation Distortion vs Output Common Mode Voltage**



**Intermodulation Distortion vs Output Amplitude**



## PIN FUNCTIONS

**-INA, +INA, -INB, +INB (Pins 1, 20, 6, 7):** Differential Input Pins of Channels A and B Respectively.

**+FBA, -FBA, +FBB, -FBB (Pins 2, 19, 5, 8):** Feedback Pins. These pins are located adjacent to the input pins on the package pinout, however they are internally connected to the output pins. They can be easily used for feedback components connections.

**SHDNA, SHDNB (Pins 3, 4):** When these pins are floating or directly tied to  $V^+$ , the respective amplifier is in the normal (active) operational mode. When these pins are connected to  $V^-$ , the respective amplifier is disabled and draws approximately  $100\mu\text{A}$  of supply current. Each amplifier has an independent SHDN pin.

**$V_{OCMA}$ ,  $V_{OCMB}$  (Pins 18, 9):** Output Common Mode Reference Voltage. The voltage on this pin sets the output

common mode voltage level for the respective amplifier. If left floating, an internal resistor divider develops a default voltage of 1.25V with a 5V supply.

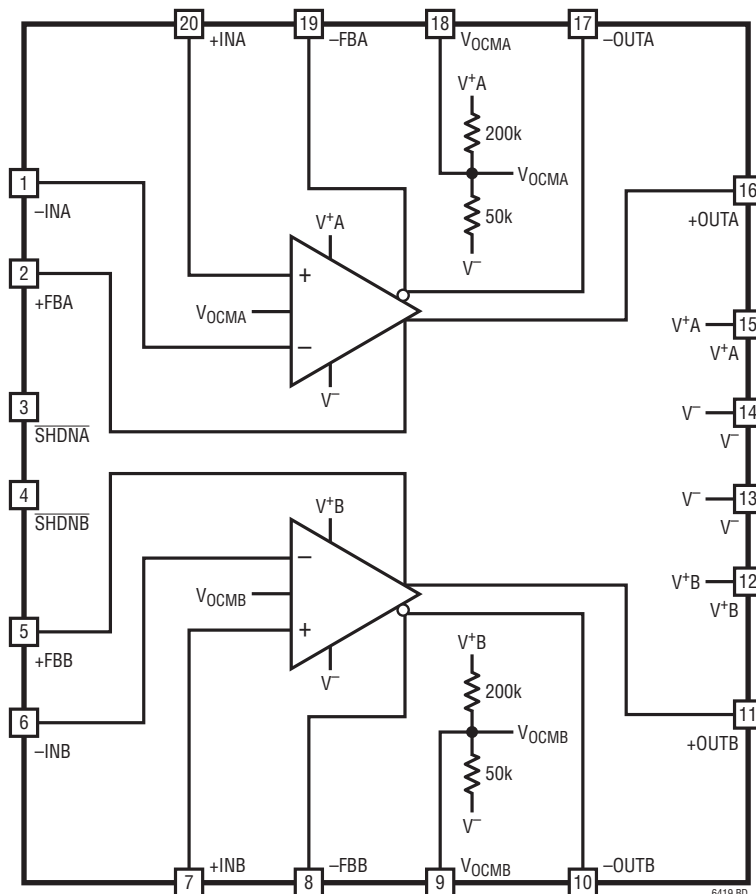
**+OUTA, -OUTA, +OUTB, -OUTB (Pins 16, 17, 11, 10):** Differential Output Pins of Channels A and B Respectively.

**$V^+A$ ,  $V^+B$  (Pins 15, 12):** Positive Power Supply Pins. Each amplifier has an independent  $V^+$  supply. However, since both amplifiers share a common substrate, they must share the same  $V^-$  supply.

**$V^-$  (Pins 13, 14, 21):** Negative Power Supply Pins. All pins, as well as the exposed pads, must be connected to same voltage.

**Exposed Pad (Pin 21):** Tie all four bottom pads to  $V^-$ . If split supplies are used, DO NOT tie the pads to ground.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### Functional Description

The LTC6419 is a small outline, wideband, high speed, low noise, and low distortion fully-differential dual amplifier with accurate output phase balancing. The amplifier is optimized to drive low voltage, single-supply, differential input analog-to-digital converters (ADCs). The LTC6419 input common mode range includes ground, which makes it ideal to DC-couple and convert ground-referenced, single-ended signals into differential signals that are referenced to the user-supplied output common mode voltage. This is ideal for driving these differential ADCs. The balanced differential nature of the amplifier also provides even-order harmonic distortion cancellation, and low susceptibility to common mode noise (like power supply noise). The LTC6419 can operate with a single-ended input and differential output, or with a differential input and differential output.

The outputs of the LTC6419 are capable of swinging from close-to-ground to 1V below  $V^+$ . They can source or sink up to approximately 70mA of current. Load capacitances should be decoupled with at least 10 $\Omega$  of series resistance from each output.

### Input Pin Protection

The LTC6419 input stage is protected against differential input voltages which exceed 1.4V by two pairs of series diodes connected back to back between +INA and -INA and between +INB and -INB. Moreover, the input pins, as well as  $V_{OCMA}$ ,  $V_{OCMB}$ ,  $\overline{SHDNA}$  and  $\overline{SHDNB}$  pins, have clamping diodes to either power supply. If these pins are driven to voltages which exceed either supply, the current should be limited to 10mA to prevent damage to the IC.

### SHDN Pins

The  $\overline{SHDNA}/\overline{SHDNB}$  pins are CMOS logic inputs with a 150k internal pull-up resistor. If the pin is driven low, the LTC6419 powers down. If the pin is left unconnected or driven high, the part is in normal active operation. Some care should be taken to control leakage currents at this pin to prevent inadvertently putting the LTC6419 into shutdown. The turn-on and turn-off time between the shutdown and active states is typically less than 200ns. Keep in mind that each channel of the amplifier has its own independent SHDN pin.

### General Amplifier Applications

In Figure 1, the gain to  $V_{OUTDIFF}$  from  $V_{INP}$  and  $V_{INM}$  is given by:

$$V_{OUTDIFF} = V_{+OUT} - V_{-OUT} \approx \frac{R_F}{R_I} \cdot (V_{INP} - V_{INM}) \quad (1)$$

Note from Equation (1), the differential output voltage ( $V_{+OUT} - V_{-OUT}$ ) is completely independent of input and output common mode voltages, or the voltage at the common mode pin. This makes the LTC6419 ideally suited for pre-amplification, level shifting and conversion of single-ended signals to differential output signals for driving differential input ADCs.

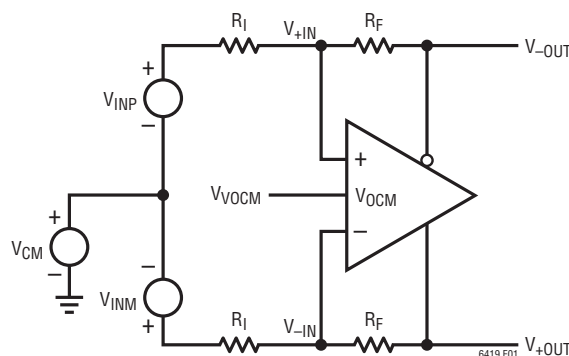


Figure 1. Circuit for Common Mode Range

### Output Common Mode and $V_{OCM}$ Pin

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = V_{OCM} = \frac{V_{+OUT} + V_{-OUT}}{2}$$

As the equation shows, the output common mode voltage is independent of the input common mode voltage, and is instead determined by the voltage on the  $V_{OCM}$  pin, by means of an internal common mode feedback loop.

If the  $V_{OCM}$  pin is left open, an internal resistor divider develops a default voltage of 1.25V with a 5V supply. The  $V_{OCM}$  pin can be overdriven to another voltage if desired. For example, when driving an ADC, if the ADC makes a reference available for setting the common mode voltage, it can be directly tied to the  $V_{OCM}$  pin, as long as the ADC is

## APPLICATIONS INFORMATION

capable of driving the 40k input resistance presented by the  $V_{OCM}$  pin. The Electrical Characteristics table specifies the valid range that can be applied to the  $V_{OCM}$  pin ( $V_{OUTCMR}$ ).

### Input Common Mode Voltage Range

The LTC6419's input common mode voltage ( $V_{ICM}$ ) is defined as the average of the two input pins,  $V_{+IN}$  and  $V_{-IN}$ . The valid range that can be used for  $V_{ICM}$  has been specified in the Electrical Characteristics table ( $V_{ICMR}$ ). However, due to external resistive divider action of the gain and feedback resistors, the effective range of signals that can be processed is even wider. The input common mode range at the op amp inputs depends on the circuit configuration (gain),  $V_{OCM}$  and  $V_{CM}$  (refer to Figure 1). For fully differential input applications, where  $V_{INP} = -V_{INM}$ , the common mode input is approximately:

$$V_{ICM} = \frac{V_{+IN} + V_{-IN}}{2} \approx V_{OCM} \cdot \frac{R_I}{R_I + R_F} + V_{CM} \cdot \frac{R_F}{R_I + R_F}$$

With single-ended inputs, there is an input signal component to the input common mode voltage. Applying only  $V_{INP}$  (setting  $V_{INM}$  to zero), the input common mode voltage is approximately:

$$V_{ICM} = \frac{V_{+IN} + V_{-IN}}{2} \approx V_{OCM} \cdot \frac{R_I}{R_I + R_F} + \quad (2)$$

$$V_{CM} \cdot \frac{R_F}{R_I + R_F} + \frac{V_{INP}}{2} \cdot \frac{R_F}{R_I + R_F}$$

This means that if, for example, the input signal ( $V_{INP}$ ) is a sine, an attenuated version of that sine signal also appears at the op amp inputs.

### Input Impedance and Loading Effects

The low frequency input impedance looking into the  $V_{INP}$  or  $V_{INM}$  input of Figure 1 depends on how the inputs are driven. For fully differential input sources ( $V_{INP} = -V_{INM}$ ), the input impedance seen at either input is simply:

$$R_{INP} = R_{INM} = R_I$$

For single-ended inputs, because of the signal imbalance at the input, the input impedance actually increases over the balanced differential case. The input impedance looking into either input is:

$$R_{INP} = R_{INM} = \frac{R_I}{1 - \frac{1}{2} \cdot \frac{R_F}{R_I + R_F}}$$

Input signal sources with non-zero output impedances can also cause feedback imbalance between the pair of feedback networks. For the best performance, it is recommended that the input source output impedance be compensated. If input impedance matching is required by the source, a termination resistor  $R_T$  should be chosen (see Figure 2) such that:

$$R_T = \frac{R_{INM} \cdot R_S}{R_{INM} - R_S}$$

According to Figure 2, the input impedance looking into the differential amp ( $R_{INM}$ ) reflects the single-ended source case, given above. Also,  $R_2$  is chosen as:

$$R_2 = R_T \parallel R_S = \frac{R_T \cdot R_S}{R_T + R_S}$$

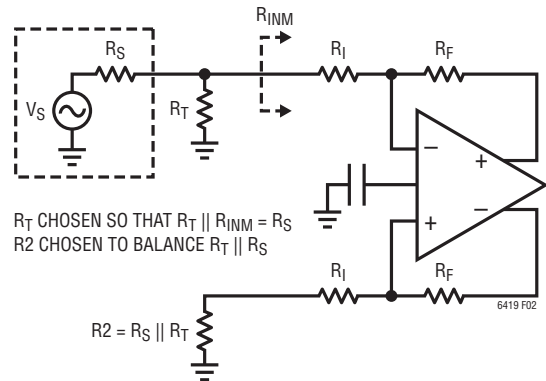


Figure 2. Optimal Compensation for Signal Source Impedance

### Effects of Resistor Pair Mismatch

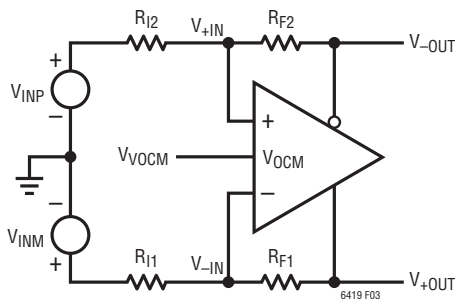
Figure 3 shows a circuit diagram which takes into consideration that real world resistors will not match perfectly.

## APPLICATIONS INFORMATION

Assuming infinite open loop gain, the differential output relationship is given by the equation:

$$V_{\text{OUTDIFF}} = V_{+\text{OUT}} - V_{-\text{OUT}} \approx V_{\text{INDIFF}} \cdot \frac{R_F}{R_I} + V_{\text{CM}} \cdot \frac{\Delta\beta}{\beta_{\text{AVG}}} - V_{\text{OCM}} \cdot \frac{\Delta\beta}{\beta_{\text{AVG}}}$$

where  $R_F$  is the average of  $R_{F1}$ , and  $R_{F2}$ , and  $R_I$  is the average of  $R_{I1}$ , and  $R_{I2}$ .



**Figure 3. Real-World Application with Feedback Resistor Pair Mismatch**

$\beta_{\text{AVG}}$  is defined as the average feedback factor from the outputs to their respective inputs:

$$\beta_{\text{AVG}} = \frac{1}{2} \cdot \left( \frac{R_{I1}}{R_{I1} + R_{F1}} + \frac{R_{I2}}{R_{I2} + R_{F2}} \right)$$

$\Delta\beta$  is defined as the difference in the feedback factors:

$$\Delta\beta = \frac{R_{I2}}{R_{I2} + R_{F2}} - \frac{R_{I1}}{R_{I1} + R_{F1}}$$

Here,  $V_{\text{CM}}$  and  $V_{\text{INDIFF}}$  are defined as the average and the difference of the two input voltages  $V_{\text{INP}}$  and  $V_{\text{INM}}$ , respectively:

$$V_{\text{CM}} = \frac{V_{\text{INP}} + V_{\text{INM}}}{2}$$

$$V_{\text{INDIFF}} = V_{\text{INP}} - V_{\text{INM}}$$

When the feedback ratios mismatch ( $\Delta\beta$ ), common mode to differential conversion occurs. Setting the differential input to zero ( $V_{\text{INDIFF}} = 0$ ), the degree of common mode to differential conversion is given by the equation:

$$V_{\text{OUTDIFF}} = V_{+\text{OUT}} - V_{-\text{OUT}} \approx (V_{\text{CM}} - V_{\text{OCM}}) \cdot \frac{\Delta\beta}{\beta_{\text{AVG}}} \quad (3)$$

In general, the degree of feedback pair mismatch is a source of common mode to differential conversion of both signals and noise. Using 0.1% resistors or better will mitigate most problems and will provide about 54dB worst case of common mode rejection. A low impedance ground plane should be used as a reference for both the input signal source and the  $V_{\text{OCM}}$  pin.

There may be concern on how feedback factor mismatch affects distortion. Feedback factor mismatch from using 1% resistors or better, has a negligible effect on distortion. However, in single supply level shifting applications where there is a voltage difference between the input common mode voltage and the output common mode voltage, resistor mismatch can make the apparent voltage offset of the amplifier appear worse than specified.

The apparent input referred offset induced by feedback factor mismatch is derived from Equation (3):

$$V_{\text{OSDIFF(APPARENT)}} \approx (V_{\text{CM}} - V_{\text{OCM}}) \cdot \Delta\beta$$

Using the LTC6419 in a single 5V supply application with 0.1% resistors, the input common mode grounded, and the  $V_{\text{OCM}}$  pin biased at 1.25V, the worst case mismatch can induce 1.25mV of apparent offset voltage.

### Noise and Noise Figure

The LTC6419's differential input referred voltage and current noise densities are  $1.1\text{nV}/\sqrt{\text{Hz}}$  and  $8.8\text{pA}/\sqrt{\text{Hz}}$ , respectively. In addition to the noise generated by the amplifier, the surrounding feedback resistors also contribute noise. A simplified noise model is shown in Figure 4. The output noise generated by both the amplifier and the feedback components is given by the equation:

$$e_{\text{no}} = \sqrt{\left[ e_{\text{ni}} \cdot \left( 1 + \frac{R_F}{R_I} \right) \right]^2 + 2 \cdot (i_{\text{n}} \cdot R_F)^2 + 2 \cdot \left( e_{\text{nRI}} \cdot \frac{R_F}{R_I} \right)^2 + 2 \cdot e_{\text{nRF}}^2}$$

APPLICATIONS INFORMATION

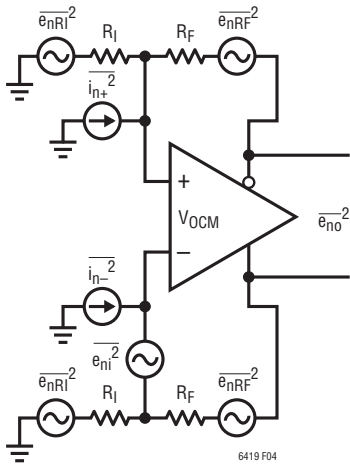


Figure 4. Simplified Noise Model

If the circuits surrounding the amplifier are well balanced, common mode noise ( $e_{nVOCM}$ ) of the amplifier does not appear in the differential output noise equation given above. A plot of this equation and a plot of the noise generated by the feedback components for the LTC6419 are shown in Figure 5.

The LTC6419’s input referred voltage noise contributes the equivalent noise of a 75Ω resistor. When the feedback network is comprised of resistors whose values are larger than this, the output noise is resistor noise and amplifier current noise dominant. For feedback networks consisting of resistors with values smaller than 75Ω, the output noise is voltage noise dominant (see Figure 5).

Lower resistor values always result in lower noise at the penalty of increased distortion due to increased loading

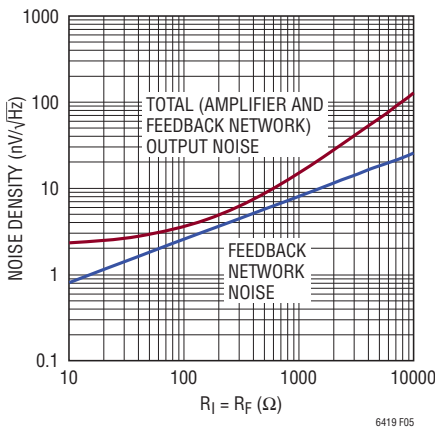


Figure 5. LTC6419 Output Noise vs Noise Contributed by Feedback Network Alone

by the feedback network on the output. Higher resistor values will result in higher output noise, but typically improved distortion due to less loading on the output. For this reason, when LTC6419 is configured in a differential gain of 1, using feedback resistors of at least 150Ω is recommended.

To calculate noise figure (NF), a source resistance and the noise it generates should also come into consideration. Figure 6 shows a noise model for the amplifier which includes the source resistance ( $R_S$ ). To generalize the calculation, a termination resistor ( $R_T$ ) is included and its noise contribution is taken into account.

Now, the total output noise power (excluding the noise contribution of  $R_S$ ) is calculated as:

$$e_{no}^2 = \left[ e_{ni} \cdot \left( 1 + \frac{R_F}{R_I + \left( \frac{R_T || R_S}{2} \right)} \right) \right]^2 + 2 \cdot (i_n \cdot R_F)^2 + 2 \cdot \left( e_{nRI} \cdot \frac{R_F}{R_I + \left( \frac{R_T || R_S}{2} \right)} \right)^2 + 2 \cdot e_{nRF}^2 + \left[ e_{nRT} \cdot \frac{R_F}{R_I} \cdot \left( \frac{2R_I || R_S}{R_T + (2R_I || R_S)} \right) \right]^2$$

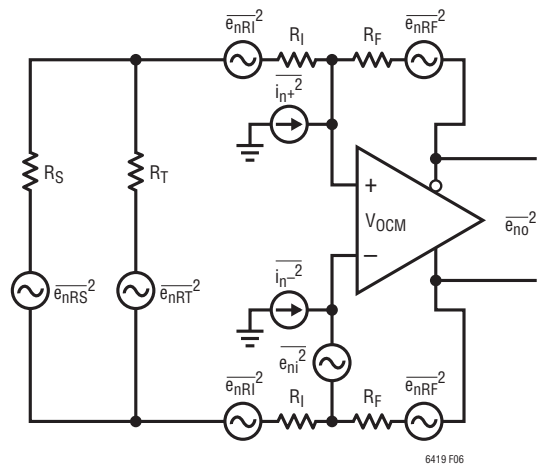


Figure 6. A More General Noise Model Including Source and Termination Resistors

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Meanwhile, the output noise power due to noise of  $R_S$  is given by:

$$e_{no^2 (RS)} = \left[ e_{nRS} \cdot \frac{R_F}{R_I} \cdot \left( \frac{2R_I || R_T}{R_S + (2R_I || R_T)} \right) \right]^2$$

Finally, noise figure can be obtained as:

$$NF = 10 \log \left( 1 + \frac{e_{no^2}}{e_{no^2 (RS)}} \right)$$

Figure 7 specifies the measured total output noise ( $e_{no}$ ), excluding the noise contribution of source resistance, and noise figure (NF) of LTC6419 configured at closed loop gains ( $A_V = R_F/R_I$ ) of 1V/V, 2V/V and 5V/V. The circuits in the left column use termination resistors and transformers to match to the 50Ω source resistance, while the circuits in the right column do not have such matching. For simplicity, DC-blocking and bypass capacitors have not been shown in the circuits, as they do not affect the noise results.

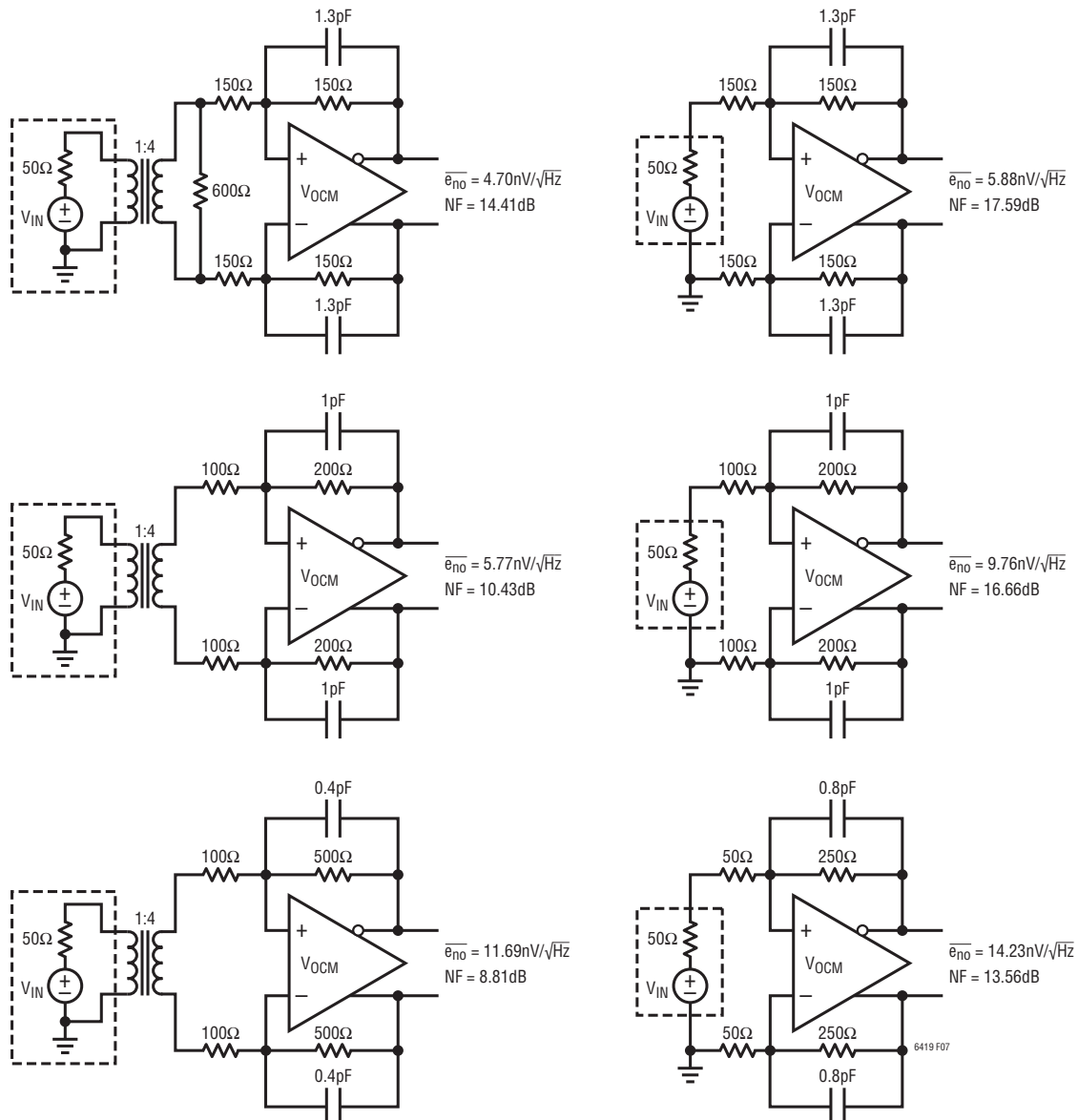


Figure 7. LTC6419 Measured Output Noise and Noise Figure at Different Closed Loop Gains with and without Source Impedance Matching

6419fa

## APPLICATIONS INFORMATION

### GBW vs $f_{-3dB}$

Gain-bandwidth product (GBW) and  $-3dB$  frequency ( $f_{-3dB}$ ) have been both specified in the Electrical Characteristics table as two different metrics for the speed of the LTC6419. GBW is obtained by measuring the gain of the amplifier at a specific frequency ( $f_{TEST}$ ) and calculate  $gain \cdot f_{TEST}$ . To measure gain, the feedback factor (i.e.  $\beta = R_I / (R_I + R_F)$ ) is chosen sufficiently small so that the feedback loop does not limit the available gain of the LTC6419 at  $f_{TEST}$ , ensuring that the measured gain is the open loop gain of the amplifier. As long as this condition is met, GBW is a parameter that depends only on the internal design and compensation of the amplifier and is a suitable metric to specify the inherent speed capability of the amplifier.

$f_{-3dB}$ , on the other hand, is a parameter of more practical interest in different applications and is by definition the frequency at which the gain is 3dB lower than its low frequency value. The value of  $f_{-3dB}$  depends on the speed of the amplifier as well as the feedback factor. Since the LTC6419 is designed to be stable in a differential signal gain of 1 (where  $R_I = R_F$  or  $\beta = 1/2$ ), the maximum  $f_{-3dB}$  is obtained and measured in this gain setting, as reported in the Electrical Characteristics table.

In most amplifiers, the open loop gain response exhibits a conventional single-pole roll-off for most of the frequencies before crossover frequency and the GBW and  $f_{-3dB}$  numbers are close to each other. However, the LTC6419 is intentionally compensated in such a way that its GBW is significantly larger than its  $f_{-3dB}$ . This means that at lower frequencies (where the input signal frequencies typically lie, e.g. 100MHz) the amplifier's gain and thus the feedback loop gain is larger. This has the important advantage of further linearizing the amplifier and improving distortion at those frequencies.

Looking at the Frequency Response vs Closed Loop Gain graph in the Typical Performance Characteristics section of this data sheet, one sees that for a closed loop gain ( $A_V$ ) of 1 (where  $R_I = R_F = 150\Omega$ ),  $f_{-3dB}$  is about 1.4GHz. However, for  $A_V = 400$  (where  $R_I = 25\Omega$  and  $R_F = 10k\Omega$ ), the gain at 100MHz is close to 40dB = 100V/V, implying a GBW value of 10GHz.

### Feedback Capacitors

When the LTC6419 is configured in low differential gains, it is often advantageous to utilize a feedback capacitor ( $C_F$ ) in parallel with each feedback resistor ( $R_F$ ). The use of  $C_F$  implements a pole-zero pair (in which the zero frequency is usually smaller than the pole frequency) and adds positive phase to the feedback loop gain around the amplifier. Therefore, if properly chosen, the addition of  $C_F$  boosts the phase margin and improves the stability response of the feedback loop. For example, with  $R_I = R_F = 150\Omega$ , it is recommended for most general applications to use  $C_F = 1.3pF$  across each  $R_F$ . This value has been selected to maximize  $f_{-3dB}$  for the LTC6419 while keeping the peaking of the closed loop gain versus frequency response under a reasonable level ( $<1dB$ ). It also results in the highest frequency for 0.1dB gain flatness ( $f_{0.1dB}$ ).

However, other values of  $C_F$  can also be utilized and tailored to other specific applications. In general, a larger value for  $C_F$  reduces the peaking (overshoot) of the amplifier in both frequency and time domains, but also decreases the closed loop bandwidth ( $f_{-3dB}$ ). For example, while for a closed loop gain ( $A_V$ ) of 5,  $C_F = 0.8pF$  results in maximum  $f_{-3dB}$  (as previously shown in the Frequency Response vs Closed Loop Gain graph of this data sheet), if  $C_F = 1.2pF$  is used, the amplifier exhibits no overshoot in the time domain which is desirable in certain applications. Both the circuits discussed in this section have been shown in the Typical Applications section of this data sheet.

### Board Layout and Bypass Capacitors

For single supply applications, it is recommended that high quality 0.1 $\mu F$ ||1000pF ceramic bypass capacitors be placed directly between each  $V^+$  pin and its closest  $V^-$  pin with short connections. The  $V^-$  pins (including the Exposed Pads) should be tied directly to a low impedance ground plane with minimal routing.

For dual (split) power supplies, it is recommended that additional high quality 0.1 $\mu F$ ||1000pF ceramic capacitors be used to bypass  $V^+$  pins to ground and  $V^-$  pins to ground, again with minimal routing.

For driving heavy differential loads ( $<200\Omega$ ), additional bypass capacitance may be needed for optimal perfor-



## APPLICATIONS INFORMATION

mance. Keep in mind that small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self-resonant frequency than do leaded capacitors, and perform best in high speed applications.

To prevent degradation in stability response, it is highly recommended that any stray capacitance at the input pins, +INA/–INA and +INB/–INB, be kept to an absolute minimum by keeping printed circuit connections as short as possible. This becomes especially true when the feedback resistor network uses resistor values greater than  $500\Omega$  in circuits with  $R_I = R_F$ .

At the output, always keep in mind the differential nature of the LTC6419, because it is critical that the load impedances seen by both outputs of each channel (stray or intended), be as balanced and symmetric as possible. This will help preserve the balanced operation of the LTC6419 that minimizes the generation of even-order harmonics and maximizes the rejection of common mode signals and noise.

The  $V_{OCMA}$  and  $V_{OCMB}$  pins should be bypassed to the ground plane with a high quality ceramic capacitor of at least  $0.01\mu\text{F}$ . This will prevent common mode signals and noise on these pins from being inadvertently converted to differential signals and noise by impedance mismatches both externally and internally to the IC.

### Driving ADCs

The LTC6419's ground-referenced input, differential output and adjustable output common mode voltage make it ideal for interfacing to differential input ADCs. These ADCs are typically supplied from a single-supply

voltage and have an optimal common mode input range near mid-supply. The LTC6419 interfaces to these ADCs by providing single-ended to differential conversion and common mode level shifting.

The sampling process of ADCs creates a transient that is caused by the switching in of the ADC sampling capacitor. This momentarily shorts the output of the amplifier as charge is transferred between amplifier and sampling capacitor. The amplifier must recover and settle from this load transient before the acquisition period has ended, for a valid representation of the input signal. The LTC6419 will settle quickly from these periodic load impulses. The RC network between the outputs of the driver and the inputs of the ADC decouples the sampling transient of the ADC (see Figure 8). The capacitance serves to provide the bulk of the charge during the sampling process, while the two resistors at the outputs of the LTC6419 are used to dampen and attenuate any charge injected by the ADC. The RC filter gives the additional benefit of band limiting broadband output noise. Generally, longer time constants improve SNR at the expense of settling time. The resistors in the decoupling network should be at least  $10\Omega$ . These resistors also serve to decouple the LTC6419 outputs from load capacitance. Too large of a resistor will leave insufficient settling time. Too small of a resistor will not properly dampen the load transient of the sampling process, prolonging the time required for settling. In 16-bit applications, this will typically require a minimum of eleven RC time constants. For lowest distortion, choose capacitors with low dielectric absorption (such as a COG multilayer ceramic capacitor).

APPLICATIONS INFORMATION

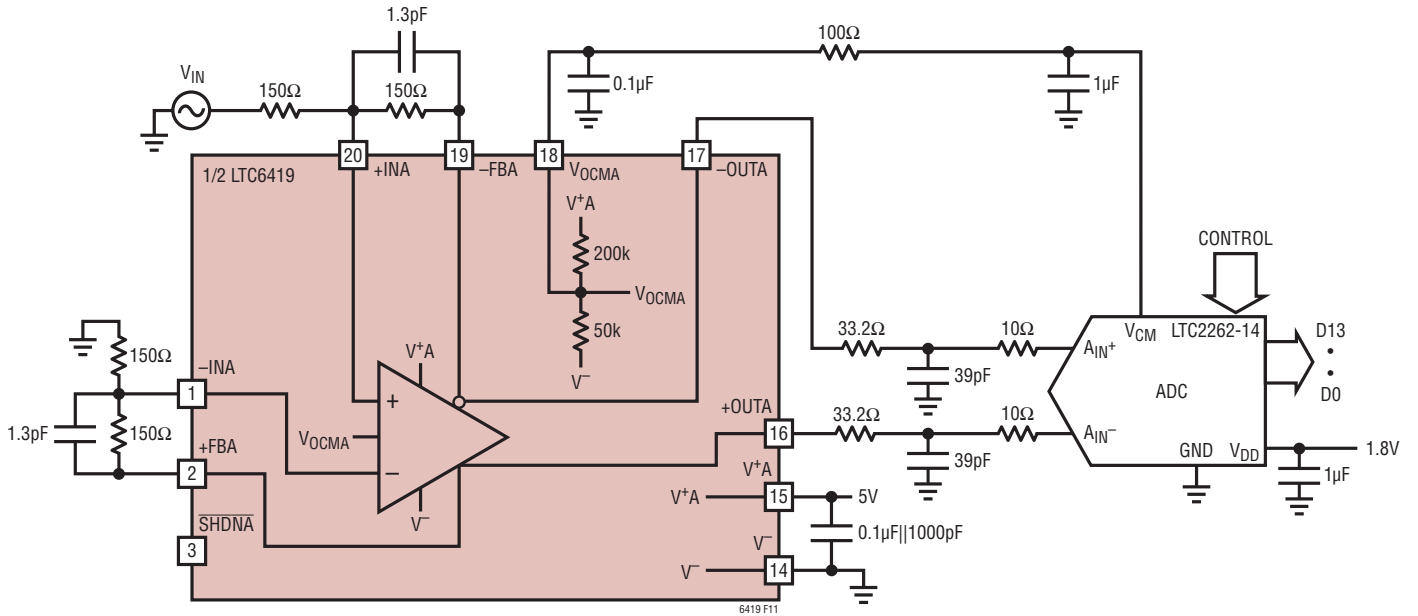
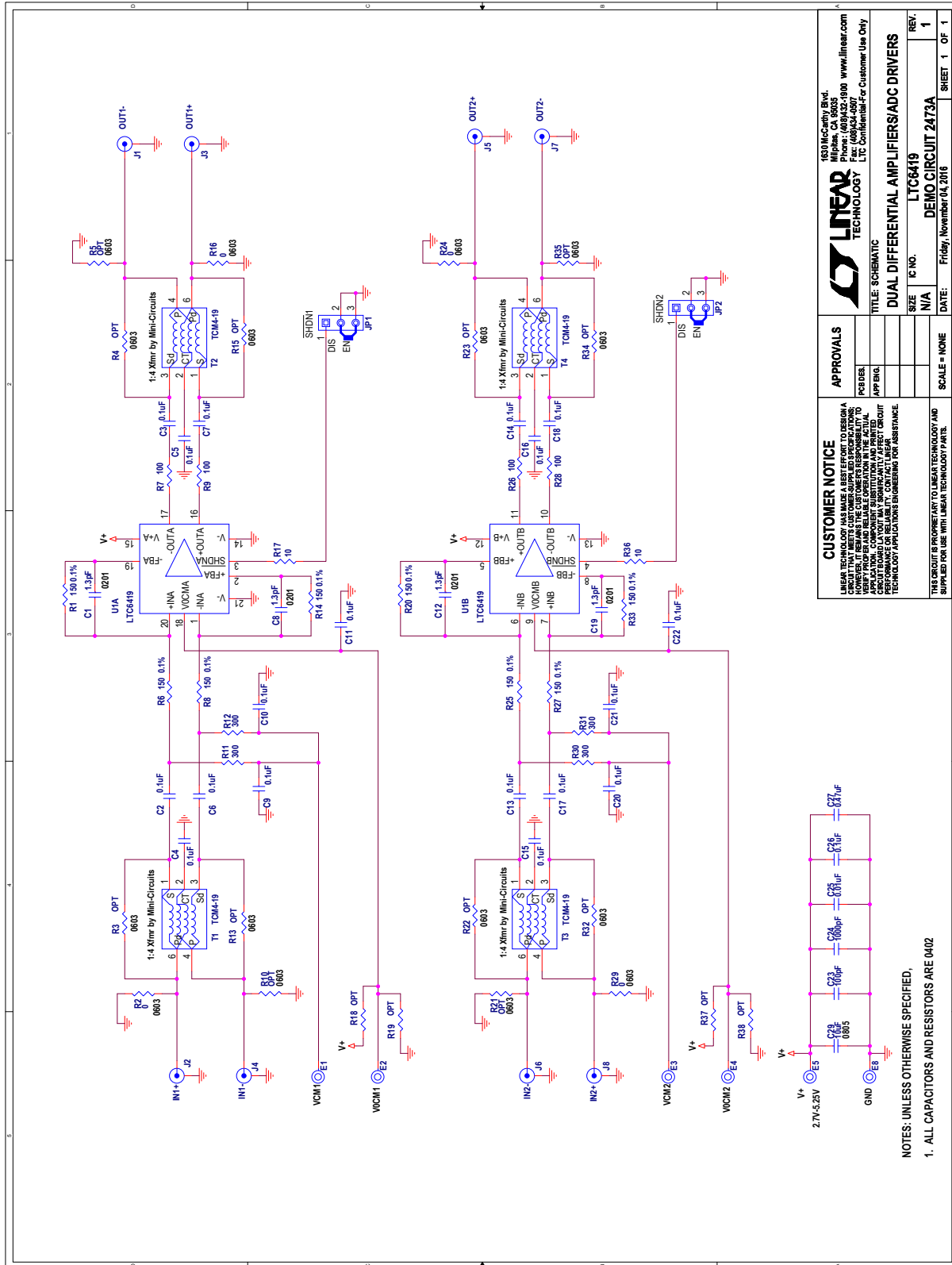


Figure 8. Driving an ADC

# APPLICATIONS INFORMATION



<p><b>CUSTOMER NOTICE</b></p> <p>LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A BOARD LAYOUT THAT DOES NOT SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE. HOWEVER, IT REMAINS THE CUSTOMER'S RESPONSIBILITY TO VERIFY THAT THE BOARD LAYOUT DOES NOT SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE. COMPONENT SUBSTITUTION AND BOARD LAYOUT CHANGES MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE. LINEAR TECHNOLOGY ENGINEERING FOR ASSISTANCE.</p>	<p><b>APPROVALS</b></p> <p>PCB DES: _____</p> <p>APP ENG: _____</p>	<p>1570 MacArthur Blvd Folsom, CA 95633 Phone: (494)32-6900 www.linear.com Fax: (494)32-4507 E-Mail: ltc@linear.com</p>
	<p><b>TITLE: SCHEMATIC</b></p> <p>SIZE: C NO. _____</p> <p>SCALE: NONE</p>	<p><b>LINEAR TECHNOLOGY</b></p> <p><b>DUAL DIFFERENTIAL AMPLIFIERS/ADC DRIVERS</b></p> <p>REV: 1</p>

NOTES: UNLESS OTHERWISE SPECIFIED,  
1. ALL CAPACITORS AND RESISTORS ARE 0402

Figure 9. LTC6419 Demo Board Schematic

APPLICATIONS INFORMATION

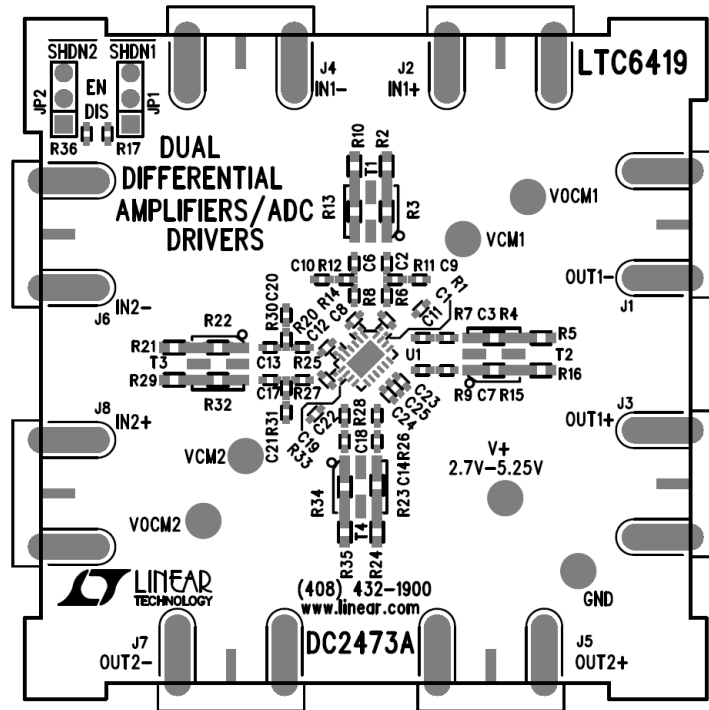
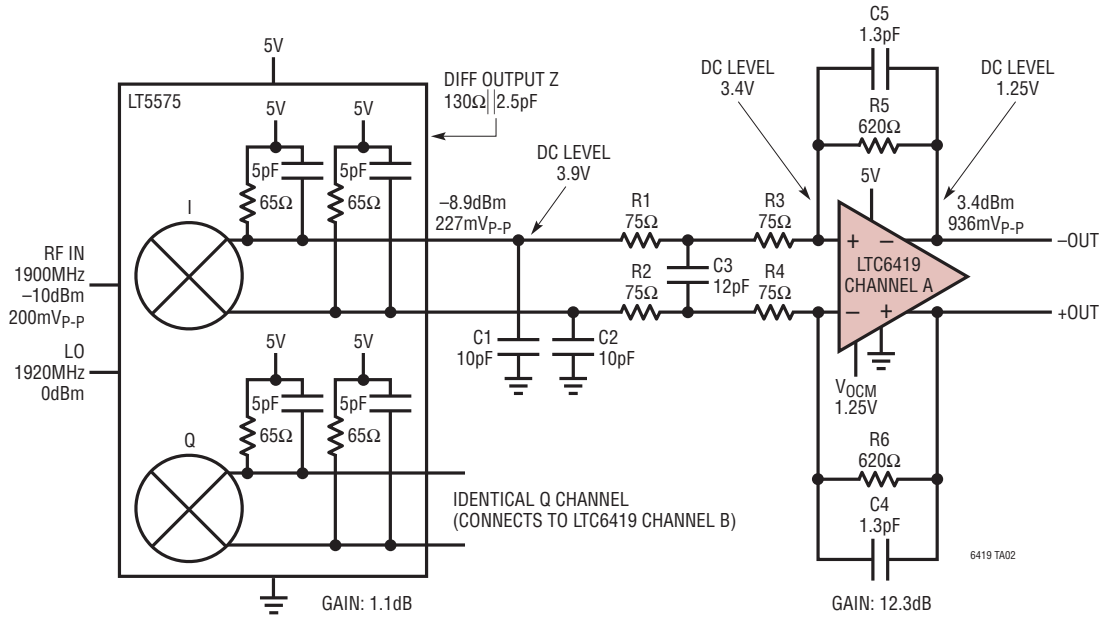


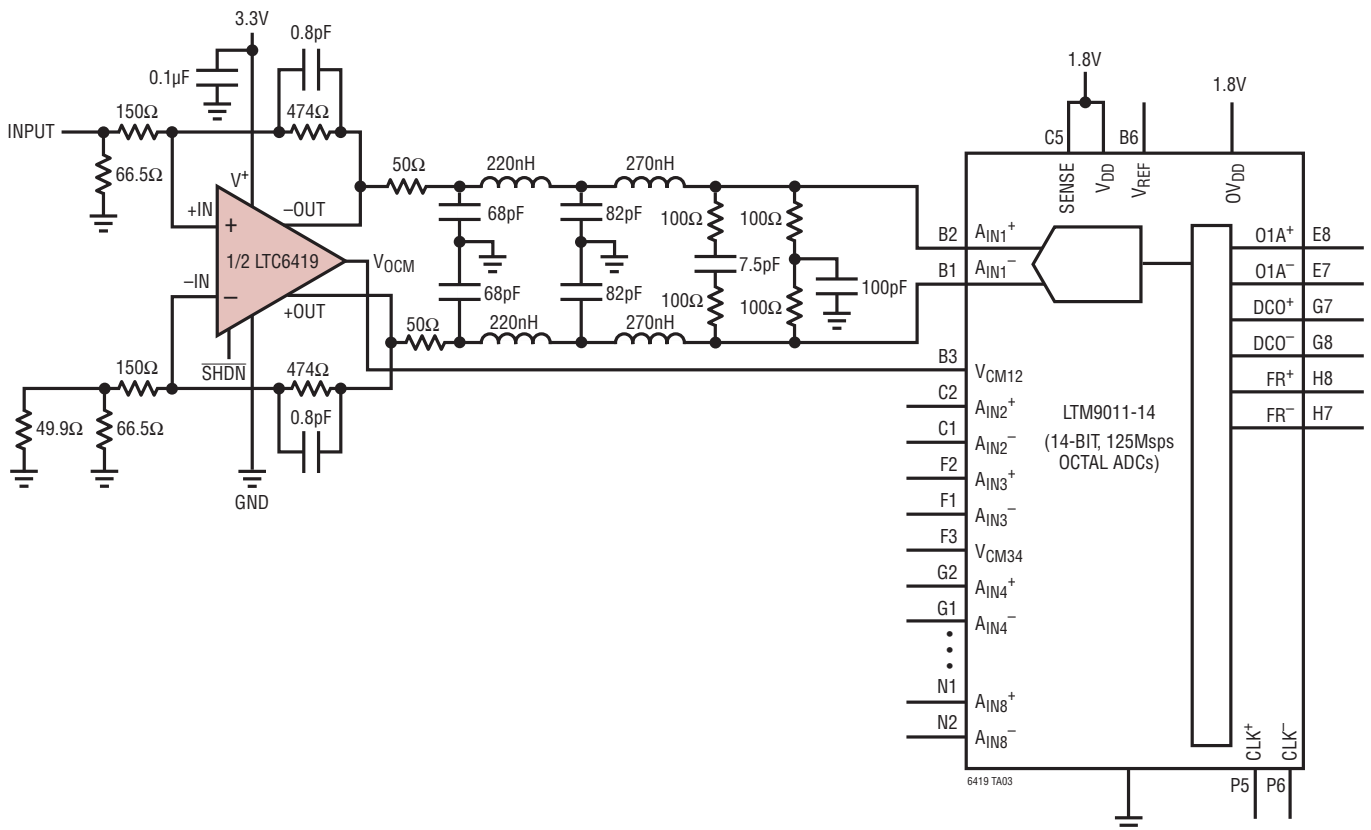
Figure 10. LTC6419 Demo Board Layout

TYPICAL APPLICATIONS

I/Q Demodulator Post-Amplifier with DC-Coupling and Level Shifting



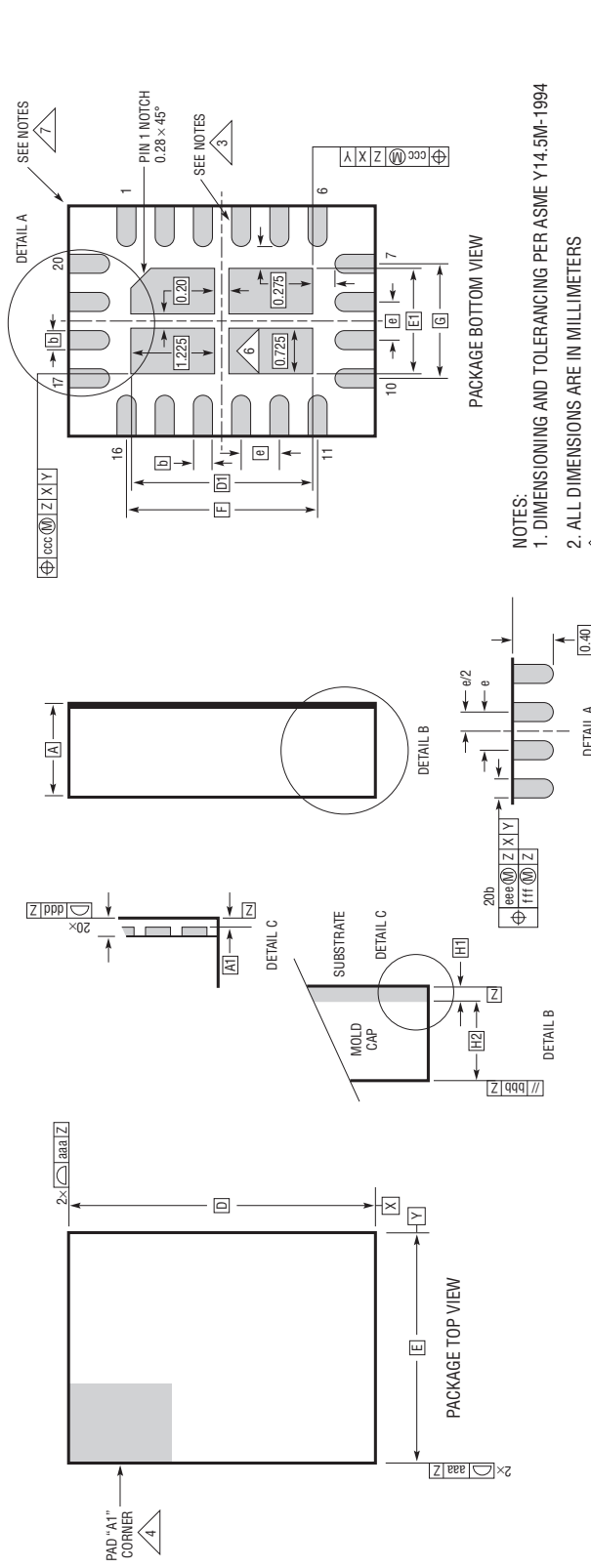
Single-Ended to Differential Conversion Using LTC6419 and 50MHz Lowpass Filter (Only One Channel Shown)



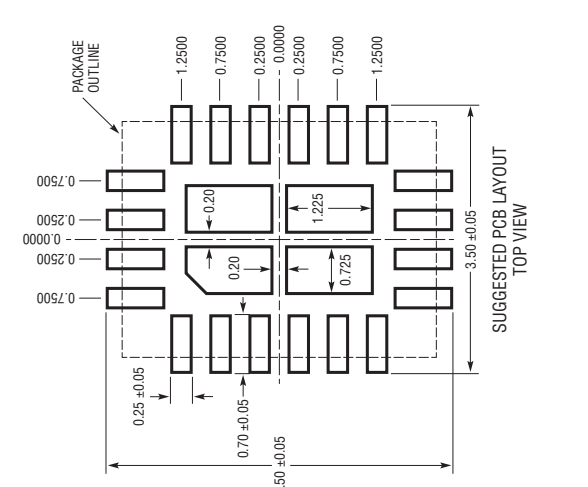
# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC6419#packaging> for the most recent package drawings.

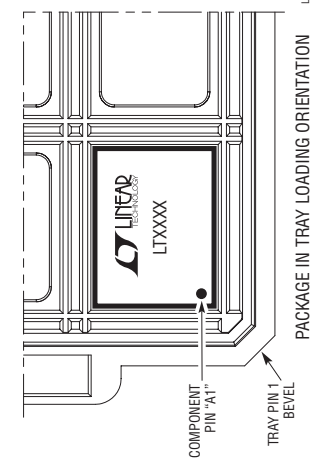
## LQFN Package 20-Lead (4mm × 3mm × 0.75mm) (Reference LTC DWG # 05-08-1519 Rev C)



SYMBOL	DIMENSIONS			NOTES
	MIN	NOM	MAX	
A	0.61	0.75	0.84	
A1	0.02	0.03	0.04	
b	0.22	0.25	0.28	
D		4.00		
E		3.00		
e		0.50		
F		2.50		
G		1.50		
D1		2.65		
E1		1.65		
H1	0.16	0.20	0.24	
H2	0.45	0.55	0.60	
aaa		0.10	0.10	
bbb		0.10	0.10	
ccc		0.10	0.10	
ddd		0.10	0.10	
eee		0.15	0.15	
fff			0.08	
TOTAL NUMBER OF LOFN PADS: 20				



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  3. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
  4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
  5. PRIMARY DATUM -Z- IS SEATING PLANE
  6. THE EXPOSED HEAT FEATURE IS SEGMENTED AND ARRANGED IN A MATRIX FORMAT. IT MAY HAVE OPTIONAL CORNER RADI ON EACH SEGMENT
  7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY



LOFN 20/027 REV C

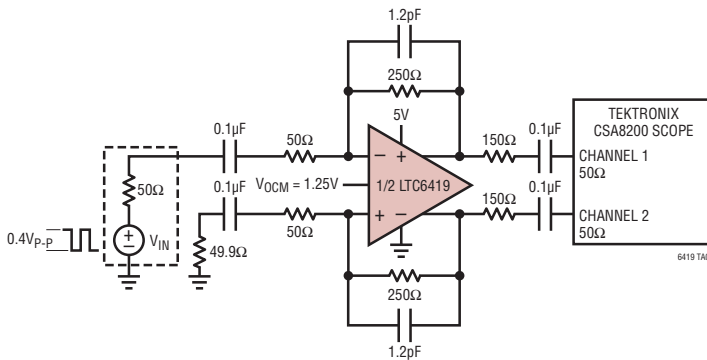
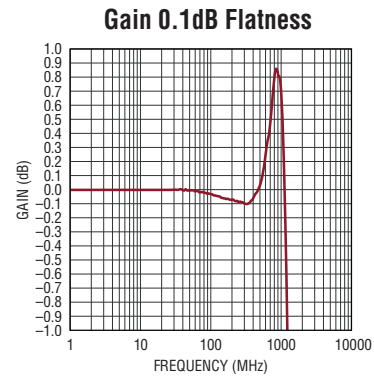
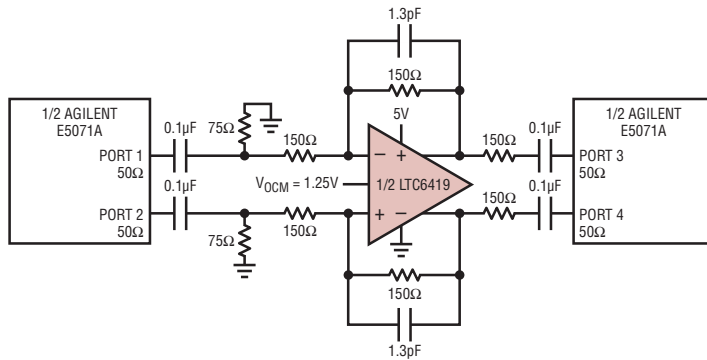
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**REVISION HISTORY**

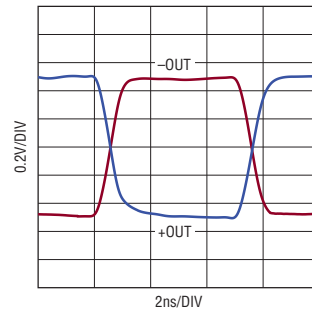
REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/17	LQFN designation	All

## TYPICAL APPLICATIONS

### LTC6419 Externally Compensated for Maximum Gain Flatness and for No-Overshoot Time-Domain Response



### No-Overshoot Step Response



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTC6409</a>	10GHz GBW, 1.1nV/√Hz Differential Amplifier/ADC Driver	88dB SFDR at 100MHz, I <sub>S</sub> = 52mA, 5V Supply, AC- or DC-Coupled Inputs
<a href="#">LTC6400-8/LTC6400-14/LTC6400-20/LTC6400-26</a>	1.8GHz Low Noise, Low Distortion, Differential ADC Drivers	-71dBc IM3 at 240MHz 1V <sub>p-p</sub> per Tone, I <sub>S</sub> = 90mA, A <sub>V</sub> = 8dB/14dB/20dB/26dB
<a href="#">LTC6401-8/LTC6401-14/LTC6401-20/LTC6401-26</a>	1.3GHz Low Noise, Low Distortion, Differential ADC Drivers	-74dBc IM3 at 140MHz 1V <sub>p-p</sub> per Tone, I <sub>S</sub> = 50mA, A <sub>V</sub> = 8dB/14dB/20dB/26dB
<a href="#">LTC6420-20</a>	Dual 1.8GHz Low Noise, Low Distortion, Differential ADC Drivers	Dual Version of the LTC6400-20, A <sub>V</sub> = 20dB
<a href="#">LTC6421-20</a>	Dual 1.3GHz Low Noise, Low Distortion, Differential ADC Drivers	Dual Version of the LTC6401-20, A <sub>V</sub> = 20dB
<a href="#">LTC6406/LTC6405</a>	3GHz/2.7GHz Low Noise, Rail-to-Rail Input Differential Amplifier/Driver	-70dBc/-65dBc Distortion at 50MHz, I <sub>S</sub> = 18mA, 1.6nV/√Hz Noise, 3V/5V Supply
<a href="#">LTC6430-15/LTC6430-20</a>	15dB/20dB Gain Block IF Amplifier—Differential	OIP3 = 50dBm at 240MHz, 20MHz to 1700MHz Bandwidth, 3.3dB/2.6dB NF
<a href="#">LTC6417</a>	1.6GHz Low Noise High Linearity Differential Buffer/ADC Driver	OIP3 = 41dBm at 300MHz; Can Drive 50Ω Differential Output
<a href="#">LTC6416</a>	2GHz Low Noise, Differential 16-Bit ADC Buffer	-72.5dBc IM3 at 300MHz 1V <sub>p-p</sub> per Tone, 150mW on 3.6V Supply
<a href="#">LTC2209</a>	16-Bit, 160Msps ADC	100dB SFDR, V <sub>DD</sub> = 3.3V, V <sub>CM</sub> = 1.25V
<a href="#">LTC2262-14</a>	14-Bit, 150Msps Ultralow Power 1.8V ADC	88dB SFDR, 149mW, V <sub>DD</sub> = 1.8V, V <sub>CM</sub> = 0.9V
<a href="#">LTC2268-14/LTC2175-14/LTM9011-14</a>	Dual/Quad/Octal 14-Bit, 125Msps Ultralow Power 1.8V ADCs	88dB SFDR, 140mW per Channel, V <sub>DD</sub> = 1.8V, V <sub>CM</sub> = 0.9V



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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
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- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
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- Защиту от снятия компонента с производства.
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