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1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

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About Cypress

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MB9B360L Series

32-Bit Arm® Cortex®-M4F FM4 Microcontroller

Devices in the MB9B360L Series are highly integrated 32-bit microcontrollers with high performance and competitive cost.

This series is based on the Arm® Cortex®-M4F Processor with on-chip Flash memory and SRAM. The series has peripheral functions such as Motor Control Timers, ADCs and Communication Interfaces (USB, UART, CSIO, I^2C, LIN). The products that are described in this datasheet are placed into TYPE2-M4 product categories in the "FM4 Family Peripheral Manual Main Part (002-04856)".

Features

32-bit Arm® Cortex®-M4F Core

- Processor version: r0p1
- Up to 160 MHz Frequency Operation
- FPU built-in
- Support DSP instruction
- Memory Protection Unit (MPU): improves the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-Chip Memories

[Flash Memory]

These series are based on two independent on-chip Flash memories.

- MainFlash memory
  - Up to 512 Kbytes
  - Built-in Flash Accelerator System with 16 Kbytes trace buffer memory
  - The read access to Flash memory can be achieved without wait-cycle up to operation frequency of 72 MHz. Even at the operation frequency more than 72 MHz, an equivalent access to Flash memory can be obtained by Flash Accelerator System.
  - Security function for code protection
- WorkFlash memory
  - 32 Kbytes
  - Read cycle:
    - 6wait-cycle: the operation frequency more than 120 MHz, and up to 160 MHz
    - 4wait-cycle: the operation frequency more than 72 MHz, and up to 120 MHz
    - 2wait-cycle: the operation frequency more than 40 MHz, and up to 72 MHz
    - 0wait-cycle: the operation frequency up to 40 MHz
  - Security function is shared with code protection

[SRAM]

This is composed of three independent SRAMs (SRAM0, SRAM1, and SRAM2). SRAM0 is connected to I-code bus and D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to System bus of Cortex-M4F core.

- SRAM0: Up to 32 Kbytes
- SRAM1: Up to 16 Kbytes
- SRAM2: Up to 16 Kbytes

USB Interface

USB interface is composed of Device and Host.

- USB device
  - USB2.0 Full-Speed supported
  - Max 6 Endpoint supported
    - Endpoint 0 is control transfer
    - Endpoint 1, 2 can be selected Bulk-transfer, Interrupt-transfer or Isochronous-transfer
    - Endpoint 3 to 5 can select Bulk-transfer or Interrupt-transfer
    - Endpoint 1 to 5 comprise Double Buffer
  - The size of each endpoint is according to the follows.
    - Endpoint 0, 2 to 5: 64 bytes
    - Endpoint 1: 256 bytes
- USB host
  - USB2.0 Full/Low-speed supported
  - Bulk-transfer, interrupt-transfer and Isochronous-transfer support
  - USB Device connected/dis-connected automatically detect
  - IN/OUT token handshake packet automatically
  - Max 256-byte packet-length supported
  - Wake-up function supported

Multi-Function Serial Interface (Max 6 Channels)

- 64 bytes with FIFO (the FIFO step numbers are variable depending on the settings of the communication mode or bit length.)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch.6 only)
  - Supports high-speed SPI (ch.0 and ch.6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/Slave mode supported
  - LIN break field generation (can change to 13 to 16-bit length)
  - LIN break delimiter generation (can change to 1 to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- I^2C
  - Standard mode (Max 100 kbps) / Fast-mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3=ch.A and ch.4=ch.B) supported

DMA Controller (8 Channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller) (128 Channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor which has already been constructed on the memory, can access directly the memory /peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation and the chain activation functions.

A/D Converter (Max 15 Channels) [12-bit A/D Converter]

- Successive Approximation type
- Built-in 2 units
- Conversion time: 0.5 µs @ 5 V
- Priority conversion available (priority at 2levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16steps, for Priority conversion: 4steps)

DA Converter (Max 2 Channels)

- R-2R type
- 12-bit resolution

Base Timer (Max 8 Channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 48 high-speed general-purpose I/O ports @ 64 pin Package
- Some pin is 5 V tolerant I/O.
  See 4. Pin Description and 5. I/O Circuit Type for the corresponding pins.

Multi-Function Timer (Max 2 Units)

The Multi-function timer is composed of the following blocks.

Minimum resolution: 6.25 ns

- 16-bit free-run timer × 3 ch./unit
- Input capture × 4 ch./unit
- Output compare × 6 ch./unit
- A/D activation compare × 6 ch./unit
- Waveform generator × 3 ch./unit
- 16-bit PPG timer × 3 ch./unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Real-Time Clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC) (1 Channel)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN, and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from the low-power consumption mode. It is possible to select the main clock, sub clock, built-in high-speed CR clock or built-in low-speed CR clock as the clock source.

Interval timer: up to 64 s (Max) @ Sub Clock: 32.768 kHz

External Interrupt Controller Unit

- External interrupt input pin: Max 16 pins
- Include one non-maskable interrupt (NMI)

Watchdog Timer (2 Channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a "Hardware" watchdog and a "Software" watchdog.

"Hardware" watchdog timer is clocked by low-speed internal CR oscillator. Therefore, "Hardware" watchdog is active in any power saving mode except STOP.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

Clock and Reset

[Clocks]

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- High-speed internal CR Clock: 4 MHz
- Low-speed internal CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low voltage detector reset
- Clock supervisor reset

Clock Super Visor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-Power Consumption Mode

Six low-power consumption modes are supported.

- SLEEP
- TIMER
- RTC
- STOP
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32 kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

Debug

- Serial Wire JTAG Debug Port (SWJ-DP)

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

Three Power Supplies (when 64 pin Package)

Two Power Supplies (when 48 pin Package)

- Wide range voltage:
  VCC = 2.7 V to 5.5 V
- Power supply for USB I/O:
  USBVCC = 3.0 V to 3.6 V (when USB is used)
  = 2.7 V to 5.5 V (when GPIO is used)
- Power supply for VBAT (only 64 pin Package):
  VBAT = 2.7 V to 5.5 V

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1. Product Lineup

Memory Size

Product Name		MB9BF364K/L	MB9BF365K/L	MB9BF366K/L
MainFlash memory		256 Kbytes	384 Kbytes	512 Kbytes
WorkFlash memory		32 Kbytes	32 Kbytes	32 Kbytes
On-chip SRAM		32 Kbytes	48 Kbytes	64 Kbytes
	SRAM0	16 Kbytes	24 Kbytes	32 Kbytes
	SRAM1	8 Kbytes	12 Kbytes	16 Kbytes
	SRAM1	8 Kbytes	12 Kbytes	16 Kbytes

Function

Product Name			MB9BF364K MB9BF365K MB9BF366K	MB9BF364L MB9BF365L MB9BF366L
Pin count			48	64
CPU			Cortex-M4F, MPU, NVIC 128ch.	
	Freq.		160 MHz	
Power supply voltage range			2.7 V to 5.5 V	
USB2.0 (Device/Host)			1ch.	
DMAC			8ch.	
DSTC			128ch.	
Multi-function Serial Interface (UART/CSIO/LIN/I^{2}C)			6ch. (Max) (In ch.1, only I^{2}C is available.)	6ch. (Max)
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)	
MF Timer	A/D activation compare	6ch.	1 unit	2 units (Max)
	Input capture	4ch.		
	Free-run timer	3ch.		
	Output compare	6ch.		
	Waveform generator	3ch.		
	PPG	3ch.		
QPRC			1ch.	
Dual Timer			1 unit	
Real-Time Clock			1 unit	
Watch Counter			1 unit	
CRC Accelerator			Yes	
Watchdog Timer			1ch. (SW) + 1ch. (HW)	
External Interrupts			15 pins (Max) + NMI × 1	16 pins (Max) + NMI × 1
I/O Ports			33 pins (Max)	48 pins (Max)
12-bit A/D Converter			8ch. (2 units)	15ch. (2 units)
12-bit D/A Converter			2 units (Max)	
CSV (Clock Super Visor)			Yes	
LVD (Low-Voltage Detector)			2ch.	
Built-in CR	High-speed		4 MHz	
	Low-speed		100 kHz	
Debug Function			SWJ-DP	
Unique ID			Yes	

Note:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See "12. Electrical Characteristics 12.4. AC Characteristics 12.4.3. Internal CR Oscillation Characteristics" for accuracy of built-in CR.*

2. Packages

Package \ Product Name	MB9BF364K MB9BF365K MB9BF366K	MB9BF364L MB9BF365L MB9BF366L
LQFP: LQG064 (0.65mm pitch)	-	❍
LQFP: LQD064 (0.5mm pitch)	-	❍
LQFP: LQA048 (0.5mm pitch)	❍	-
QFN: VNC064 (0.5mm pitch)	-	❍
QFN: VNA048 (0.5mm pitch)	❍	-

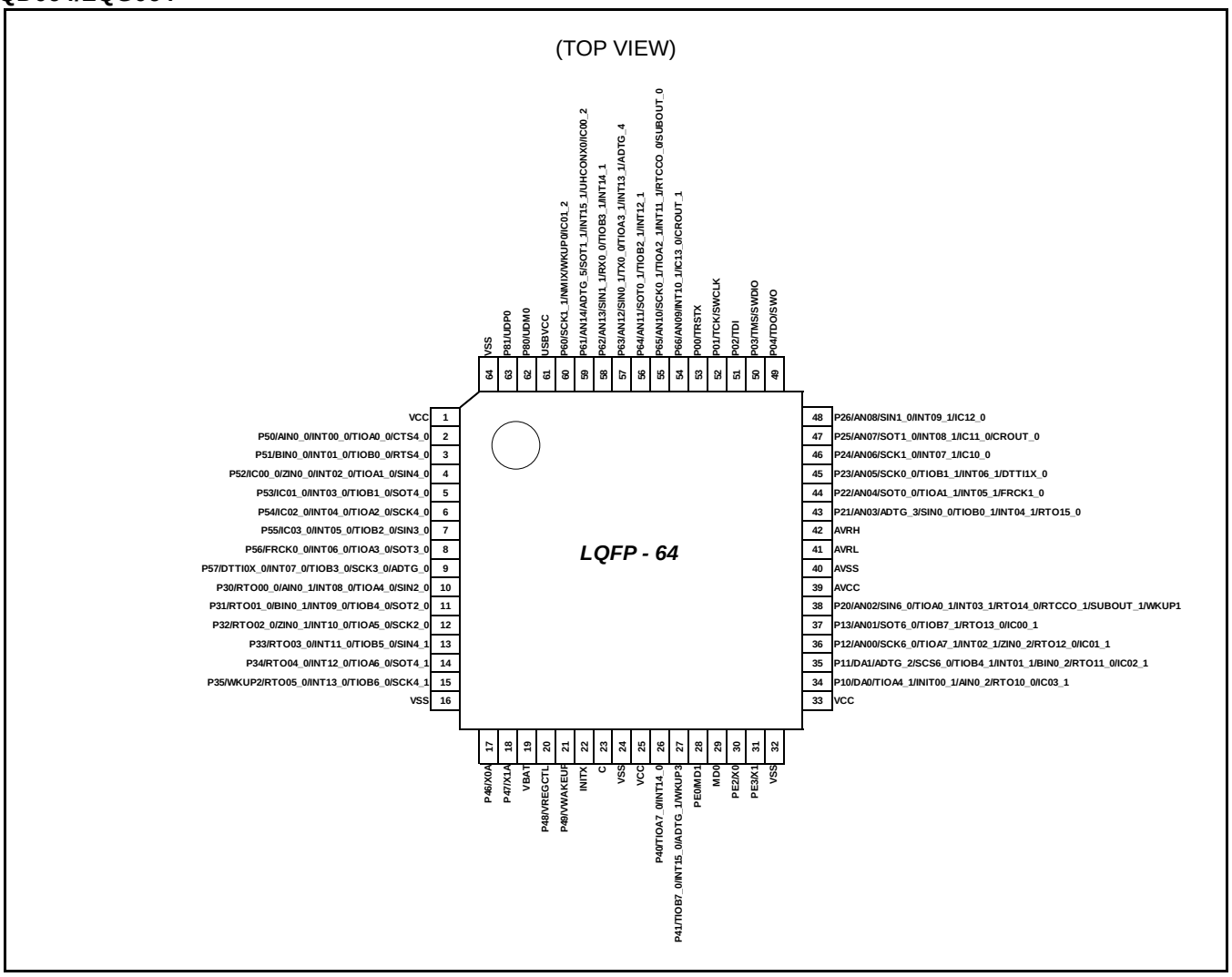
❍: Supported

Note:

- *See 14. Package Dimensions for detailed information on each package.*

3. Pin Assignment

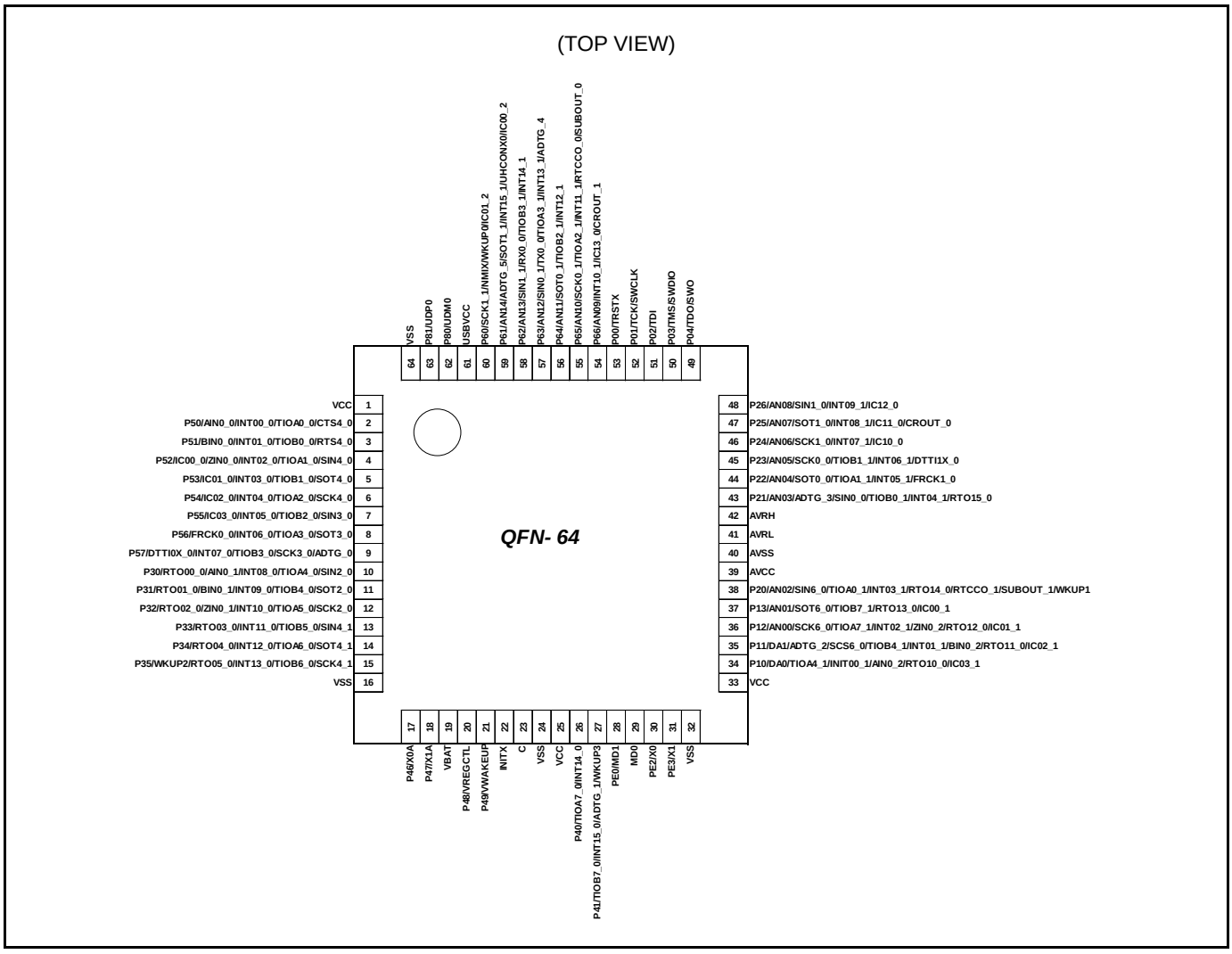
LQD064/LQG064



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

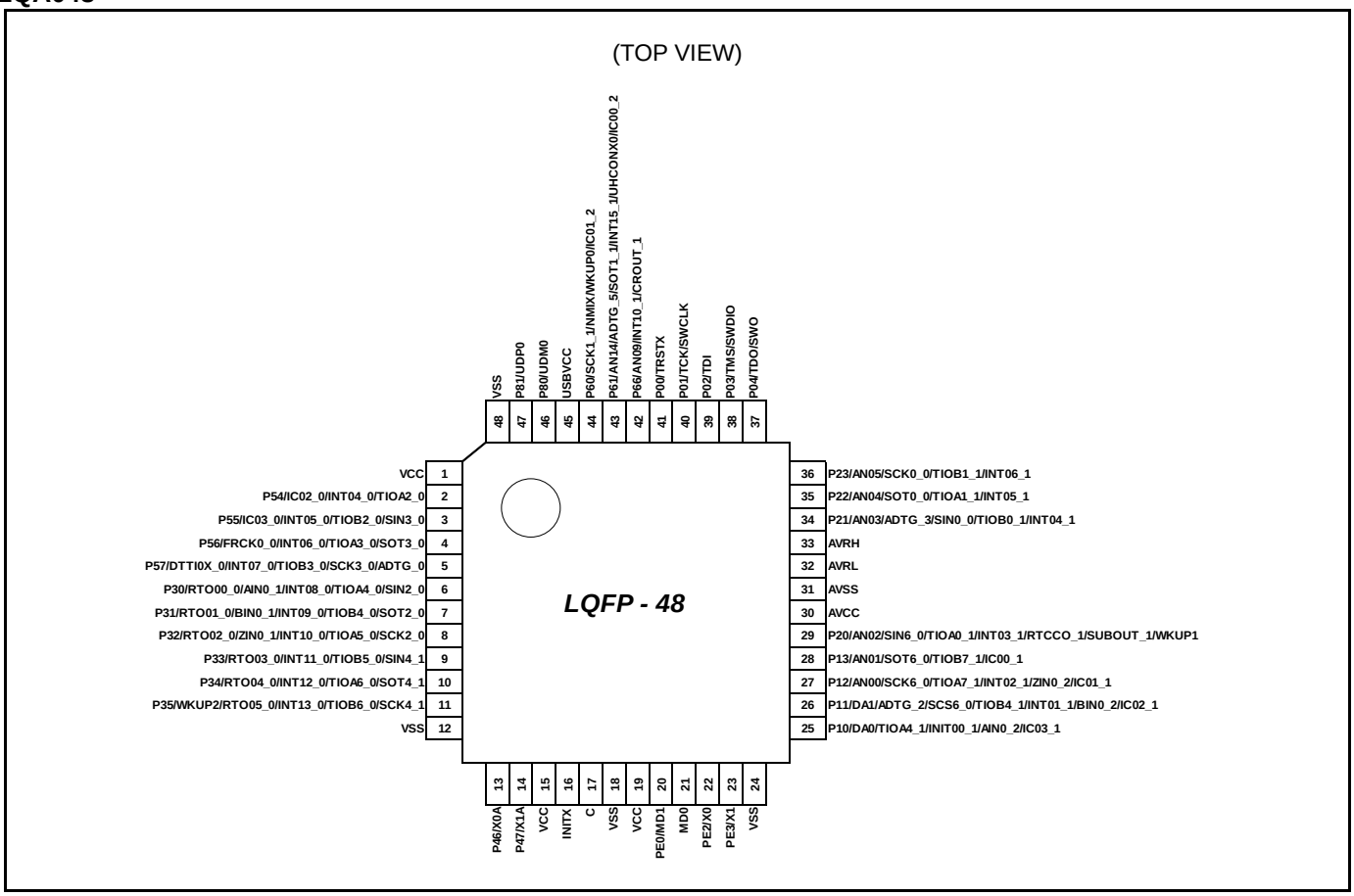
VNC064



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

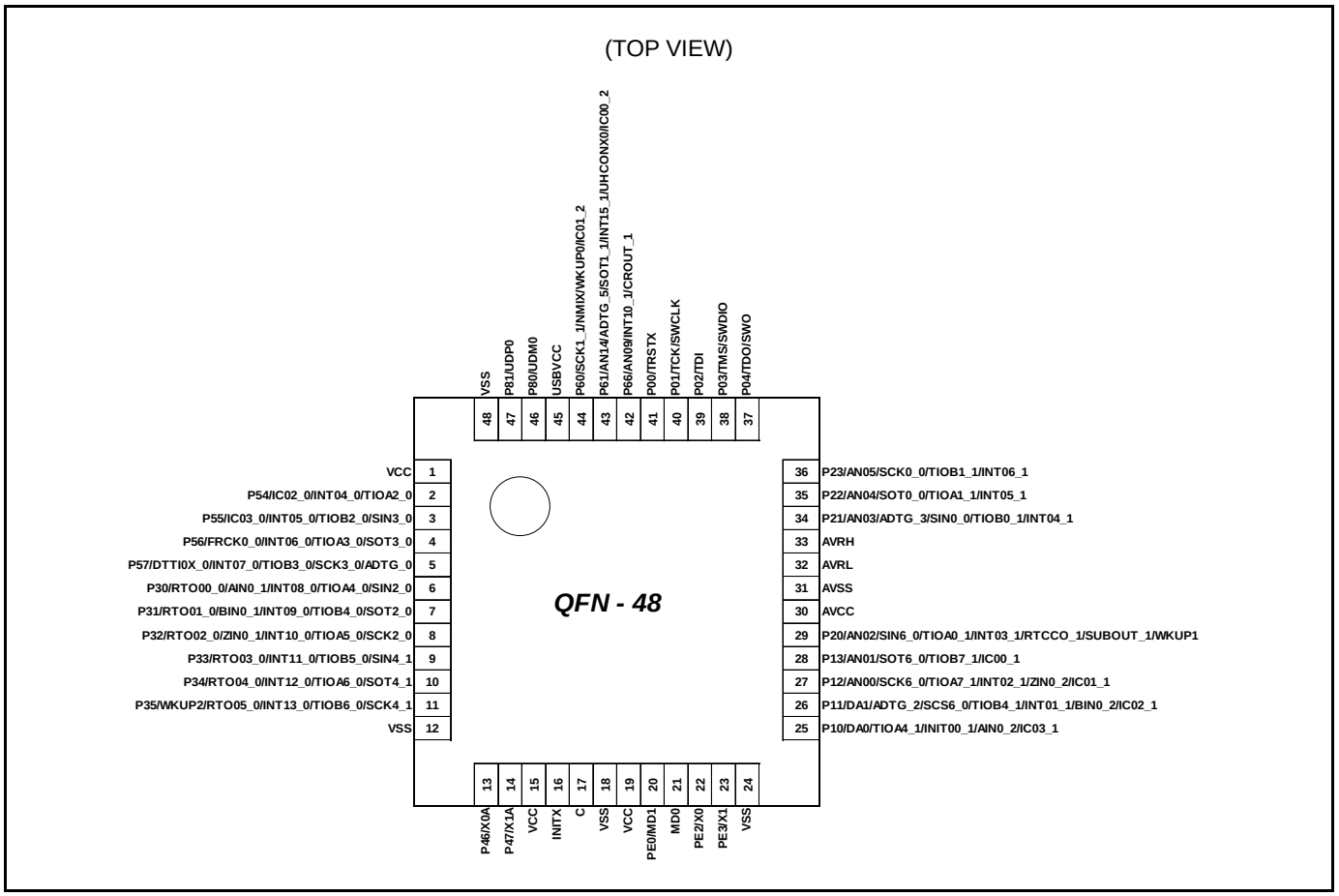
LQA048



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

VNA048



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

4. Pin Description

4.1 List of Pin Numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin No		Pin Name	I/O Circuit Type	Pin State Type
LQFP64 QFN64	LQFP48 QFN48			
1	1	VCC	-	-
2	-	P50 AIN0_0 INT00_0 TIOA0_0 CTS4_0	E	K
3	-	P51 BIN0_0 INT01_0 TIOB0_0 RTS4_0	E	K
4	-	P52 IC00_0 ZIN0_0 INT02_0 TIOA1_0 SIN4_0	I	K
5	-	P53 IC01_0 INT03_0 TIOB1_0 SOT4_0 (SDA4_0)	N	K
6	2	P54 IC02_0 INT04_0 TIOA2_0	N	K
	-	SCK4_0 (SCL4_0)		
7	3	P55 IC03_0 INT05_0 TIOB2_0 SIN3_0	I	K
8	4	P56 FRCK0_0 INT06_0 TIOA3_0 SOT3_0 (SDA3_0)	N	K

Pin No		Pin Name	I/O Circuit Type	Pin State Type
LQFP64 QFN64	LQFP48 QFN48			
9	5	P57	N	K
		DTTI0X_0		
		INT07_0		
		TIOB3_0		
		SCK3_0 (SCL3_0)		
		ADTG_0		
10	6	P30	G	K
		RTO00_0		
		AIN0_1		
		INT08_0		
		TIOA4_0		
		SIN2_0		
11	7	P31	G	K
		RTO01_0		
		BIN0_1		
		INT09_0		
		TIOB4_0		
		SOT2_0 (SDA2_0)		
12	8	P32	G	K
		RTO02_0		
		ZIN0_1		
		INT10_0		
		TIOA5_0		
		SCK2_0 (SCL2_0)		
13	9	P33	G	K
		RTO03_0		
		INT11_0		
		TIOB5_0		
		SIN4_1		
14	10	P34	G	K
		RTO04_0		
		INT12_0		
		TIOA6_0		
		SOT4_1 (SDA4_1)		
15	11	P35	G	Q
		WKUP2		
		RTO05_0		
		INT13_0		
		TIOB6_0		
		SCK4_1 (SCL4_1)		

Pin No		Pin Name	I/O Circuit Type	Pin State Type
LQFP64 QFN64	LQFP48 QFN48			
16	12	VSS	-	-
17	13	P46	P	S
		X0A		
18	14	P47	Q	T
		X1A		
19	-	VBAT	-	-
-	15	VCC	-	-
20	-	P48	O	U
		VREGCTL		
21	-	P49	O	U
		VWAKEUP		
22	16	INITX	B	C
23	17	C	-	-
24	18	VSS	-	-
25	19	VCC	-	-
26	-	P40	E	K
		TIOA7_0		
		INT14_0		
27	-	P41	E	Q
		TIOB7_0		
		INT15_0		
		ADTG_1		
		WKUP3		
28	20	PE0	C	E
		MD1		
29	21	MD0	J	D
30	22	PE2	A	A
		X0		
31	23	PE3	A	B
		X1		
32	24	VSS	-	-
33	-	VCC	-	-
34	25	P10	R	J
		DA0		
		TIOA4_1		
		INT00_1		
		AIN0_2		
		IC03_1		
	-	RTO10_0		
35	26	P11	R	J
		DA1		
		ADTG_2		
		SCS6_0		
		TIOB4_1		
		INT01_1		
		BIN0_2		
		IC02_1		
	-	RTO11_0		

Pin No		Pin Name	I/O Circuit Type	Pin State Type
LQFP64 QFN64	LQFP48 QFN48			
36	27	P12	M	M
		AN00		
		SCK6_0		
		TIOA7_1		
		INT02_1		
		ZIN0_2		
		IC01_1		
	-	RTO12_0		
37	28	P13	M	L
		AN01		
		SOT6_0 (SDA6_0)		
		TIOB7_1		
		IC00_1		
	-	RTO13_0		
38	29	P20	F	O
		AN02		
		SIN6_0		
		TIOA0_1		
		INT03_1		
		RTCCO_1		
		SUBOUT_1		
		WKUP1		
	-	RTO14_0		
39	30	AVCC	-	-
40	31	AVSS	-	-
41	32	AVRL	-	-
42	33	AVRH	-	-
43	34	P21	F	M
		AN03		
		ADTG_3		
		SIN0_0		
		TIOB0_1		
		INT04_1		
	-	RTO15_0		
44	35	P22	F	M
		AN04		
		SOT0_0 (SDA0_0)		
		TIOA1_1		
		INT05_1		
	-	FRCK1_0		
45	36	P23	F	M
		AN05		
		SCK0_0 (SCL0_0)		
		TIOB1_1		
		INT06_1		
	-	DTTI1X_0		

Pin No		Pin Name	I/O Circuit Type	Pin State Type
LQFP64 QFN64	LQFP48 QFN48			
46	-	P24	F	M
		AN06		
		SCK1_0 (SCL1_0)		
		INT07_1		
		IC10_0		
47	-	P25	F	M
		AN07		
		SOT1_0 (SDA1_0)		
		INT08_1		
		IC11_0		
		CROUT_0		
48	-	P26	F	M
		AN08		
		SIN1_0		
		INT09_1		
		IC12_0		
49	37	P04	E	G
		TDO		
		SWO		
50	38	P03	E	G
		TMS		
		SWDIO		
51	39	P02	E	G
		TDI		
52	40	P01	E	G
		TCK		
		SWCLK		
53	41	P00	E	G
		TRSTX		
54	42	P66	F	M
		AN09		
		INT10_1		
		CROUT_1		
	-	IC13_0		
55	-	P65	L	M
		AN10		
		SCK0_1 (SCL0_1)		
		TIOA2_1		
		INT11_1		
		RTCCO_0		
		SUBOUT_0		
56	-	P64	L	M
		AN11		
		SOT0_1 (SDA0_1)		
		TIOB2_1		
		INT12_1		

Pin No		Pin Name	I/O Circuit Type	Pin State Type
LQFP64 QFN64	LQFP48 QFN48			
57	-	P63	F	M
		AN12		
		SIN0_1		
		TIOA3_1		
		INT13_1		
		ADTG_4		
58	-	P62	F	M
		AN13		
		SIN1_1		
		TIOB3_1		
		INT14_1		
59	43	P61	F	M
		AN14		
		ADTG_5		
		SOT1_1 (SDA1_1)		
		INT15_1		
		UHCONX0		
		IC00_2		
60	44	P60	I	F
		SCK1_1 (SCK1_1)		
		NMIX		
		WKUP0		
		IC01_2		
61	45	USBVCC	-	-
62	46	P80	H	R
		UDM0		
63	47	P81	H	R
		UDP0		
64	48	VSS	-	-

4.2 List of Pin Functions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Function	Pin Name	Function Description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
ADC	ADTG_0	A/D converter external trigger input pin	9	5
	ADTG_1		27	-
	ADTG_2		35	26
	ADTG_3		43	34
	ADTG_4		57	-
	ADTG_5		59	43
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	36	27
	AN01		37	28
	AN02		38	29
	AN03		43	34
	AN04		44	35
	AN05		45	36
	AN06		46	-
	AN07		47	-
	AN08		48	-
	AN09		54	42
	AN10		55	-
	AN11		56	-
	AN12		57	-
	AN13		58	-
	AN14		59	43
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	2	-
	TIOA0_1		38	29
	TIOB0_0	Base timer ch.0 TIOB pin	3	-
	TIOB0_1		43	34
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	4	-
	TIOA1_1		44	35
	TIOB1_0	Base timer ch.1 TIOB pin	5	-
	TIOB1_1		45	36
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	6	2
	TIOA2_1		55	-
	TIOB2_0	Base timer ch.2 TIOB pin	7	3
	TIOB2_1		56	-
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	8	4
	TIOA3_1		57	-
	TIOB3_0	Base timer ch.3 TIOB pin	9	5
	TIOB3_1		58	-
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	10	6
	TIOA4_1		34	25
	TIOB4_0	Base timer ch.4 TIOB pin	11	7
	TIOB4_1		35	26
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	12	8
	TIOB5_0	Base timer ch.5 TIOB pin	13	9

Pin Function	Pin Name	Function Description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	14	10
	TIOB6_0	Base timer ch.6 TIOB pin	15	11
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	26	-
	TIOA7_1		36	27
	TIOB7_0	Base timer ch.7 TIOB pin	27	-
	TIOB7_1		37	28
Debugger	SWCLK	Serial wire debug interface clock input pin	52	40
	SWDIO	Serial wire debug interface data input / output pin	50	38
	SWO	Serial wire viewer output pin	49	37
	TCK	JTAG test clock input pin	52	40
	TDI	JTAG test data input pin	51	39
	TDO	JTAG debug data output pin	49	37
	TMS	JTAG test mode state input/output pin	50	38
	TRSTX	JTAG test reset Input pin	53	41
External Interrupt	INT00_0	External interrupt request 00 input pin	2	-
	INT00_1		34	25
	INT01_0	External interrupt request 01 input pin	3	-
	INT01_1		35	26
	INT02_0	External interrupt request 02 input pin	4	-
	INT02_1		36	27
	INT03_0	External interrupt request 03 input pin	5	-
	INT03_1		38	29
	INT04_0	External interrupt request 04 input pin	6	2
	INT04_1		43	34
	INT05_0	External interrupt request 05 input pin	7	3
	INT05_1		44	35

Pin Function	Pin Name	Function Description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
External Interrupt	INT06_0	External interrupt request 06 input pin	8	4
	INT06_1		45	36
	INT07_0	External interrupt request 07 input pin	9	5
	INT07_1		46	-
	INT08_0	External interrupt request 08 input pin	10	6
	INT08_1		47	-
	INT09_0	External interrupt request 09 input pin	11	7
	INT09_1		48	-
	INT10_0	External interrupt request 10 input pin	12	8
	INT10_1		54	42
	INT11_0	External interrupt request 11 input pin	13	9
	INT11_1		55	-
	INT12_0	External interrupt request 12 input pin	14	10
	INT12_1		56	-
	INT13_0	External interrupt request 13 input pin	15	11
	INT13_1		57	-
	INT14_0	External interrupt request 14 input pin	26	-
	INT14_1		58	-
	INT15_0	External interrupt request 15 input pin	27	-
	INT15_1		59	43
	NMIX	Non-Maskable Interrupt input pin	60	44
GPIO	P00	General-purpose I/O port 0	53	41
	P01		52	40
	P02		51	39
	P03		50	38
	P04		49	37
	P10	General-purpose I/O port 1	34	25
	P11		35	26
	P12		36	27
	P13		37	28
	P20	General-purpose I/O port 2	38	29
	P21		43	34
	P22		44	35
	P23		45	36
	P24		46	-
	P25		47	-
	P26		48	-
	P30	General-purpose I/O port 3	10	6
	P31		11	7
	P32		12	8
	P33		13	9
	P34		14	10
	P35		15	11

Pin Function	Pin Name	Function Description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
GPIO	P40	General-purpose I/O port 4	26	-
	P41		27	-
	P46		17	13
	P47		18	14
	P48		20	-
	P49		21	-
	P50	General-purpose I/O port 5	2	-
	P51		3	-
	P52		4	-
	P53		5	-
	P54		6	2
	P55		7	3
	P56		8	4
	P57		9	5
	P60	General-purpose I/O port 6	60	44
	P61		59	43
	P62		58	-
	P63		57	-
	P64		56	-
	P65		55	-
	P66		54	42
	P80	General-purpose I/O port 8	62	46
	P81		63	47
	PE0	General-purpose I/O port E	28	20
	PE2		30	22
	PE3		31	23

Pin Function	Pin Name	Function Description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	43	34
	SIN0_1		57	-
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	44	35
	SOT0_1 (SDA0_1)		56	-
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation modes 2) and as SCL0 when it is used in an I^2C (operation mode 4).	45	36
	SCK0_1 (SCL0_1)		55	-
Multi-function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	48	-
	SIN1_1		58	-
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	47	-
	SOT1_1 (SDA1_1)		59	43
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 2) and as SCL1 when it is used in an I^2C (operation mode 4).	46	-
	SCK1_1 (SCL1_1)		60	44
Multi-function Serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	10	6
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	11	7
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an I^2C (operation mode 4).	12	8

Pin Function	Pin Name	Function Description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	7	3
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I^2C (operation mode 4).	8	4
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I^2C (operation mode 4).	9	5
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	4	-
	SIN4_1		13	9
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I^2C (operation mode 4).	5	-
	SOT4_1 (SDA4_1)		14	10
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation modes 2) and as SCL4 when it is used in an I^2C (operation mode 4).	6	-
	SCK4_1 (SCL4_1)		15	11
	CTS4_0	Multi-function serial interface ch.4 CTS input pin	2	-
	RTS4_0	Multi-function serial interface ch.4 RTS output pin	3	-
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin	38	29
	SOT6_0 (SDA6_0)	This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I^2C (operation mode 4).	37	28
	SCK6_0 (SCL6_0)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation modes 2) and as SCL6 when it is used in an I^2C (operation mode 4).	36	27
	SCS6_0	Multi-function serial interface ch.6 serial chip select pin	35	26

Pin Function	Pin Name	Function Description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
Multi-function Timer 0	DTTI0X_0	Input signal controlling wave form generator outputs RTO00 to RTO05 of Multi-function timer 0.	9	5
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin	8	4
	IC00_0	16-bit input capture ch.0 input pin of Multi-function timer 0. ICxx describes channel number.	4	-
	IC00_1		37	28
	IC00_2		59	43
	IC01_0		5	-
	IC01_1		36	27
	IC01_2		60	44
	IC02_0		6	2
	IC02_1		35	26
	IC03_0		7	3
	IC03_1		34	25
	RTO00_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	10	6
	RTO01_0 (PPG00_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	11	7
	RTO02_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	12	8
	RTO03_0 (PPG02_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	13	9
	RTO04_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	14	10
	RTO05_0 (PPG04_0)	Wave form generator output pin of Multi-function timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	15	11

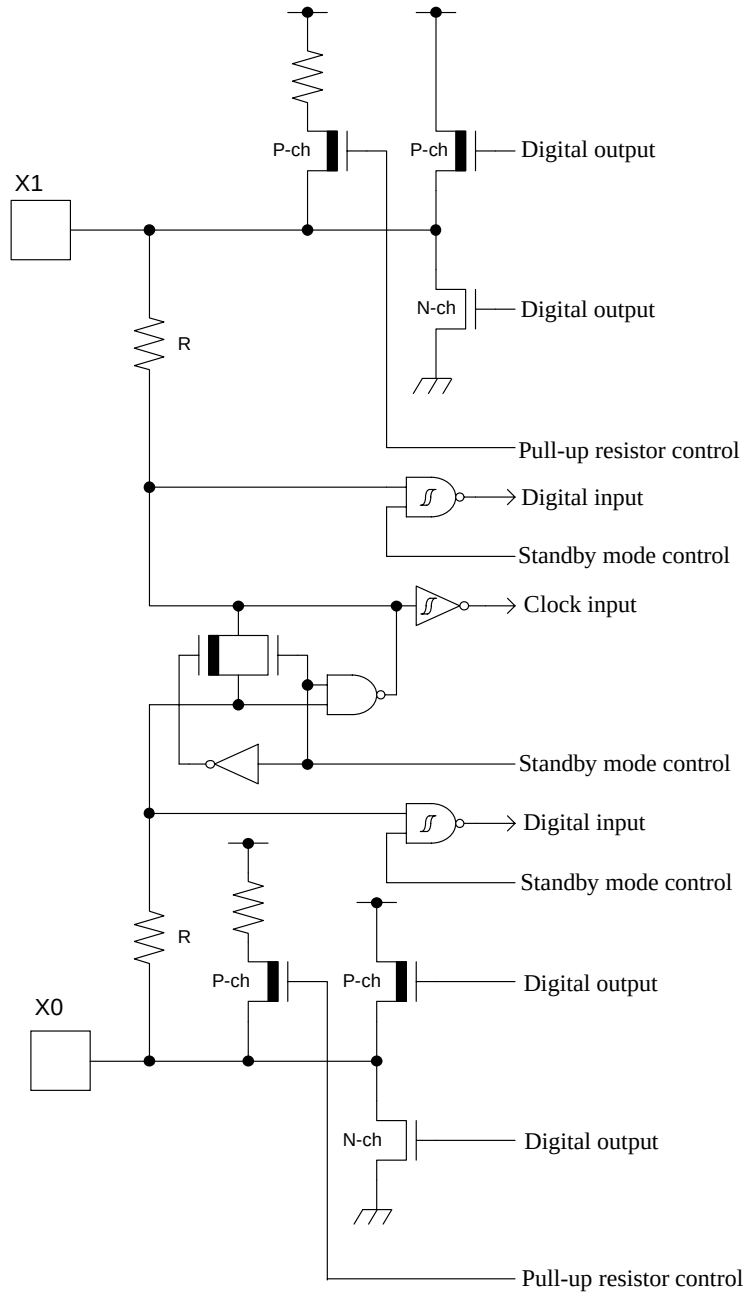
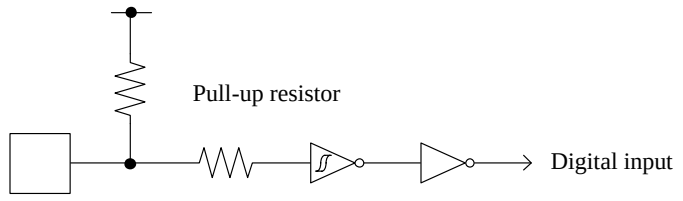
Pin Function	Pin Name	Function Description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
Multi-function Timer 1	DTTI1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of Multi-function timer 1.	45	-
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	44	-
	IC10_0	16-bit input capture ch.1 input pin of Multi-function timer 1. ICxx describes channel number.	46	-
	IC11_0		47	-
	IC12_0		48	-
	IC13_0		54	-
	RTO10_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	34	-
	RTO11_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	35	-
	RTO12_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	36	-
	RTO13_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	37	-
	RTO14_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	38	-
	RTO15_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	43	-
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	2	-
	AIN0_1		10	6
	AIN0_2		34	25
	BIN0_0	QPRC ch.0 BIN input pin	3	-
	BIN0_1		11	7
	BIN0_2		35	26
	ZIN0_0	QPRC ch.0 ZIN input pin	4	-
	ZIN0_1		12	8
	ZIN0_2		36	36

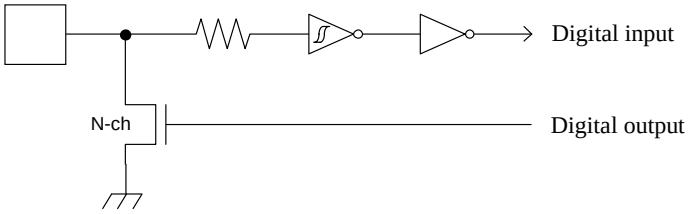
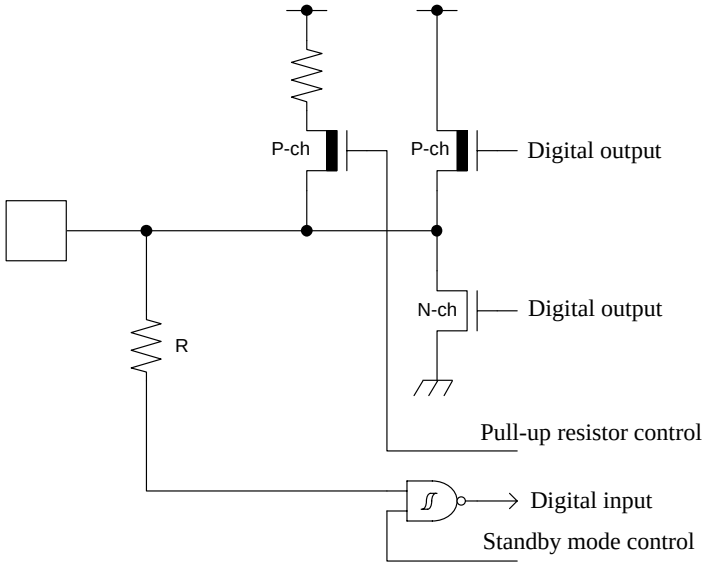
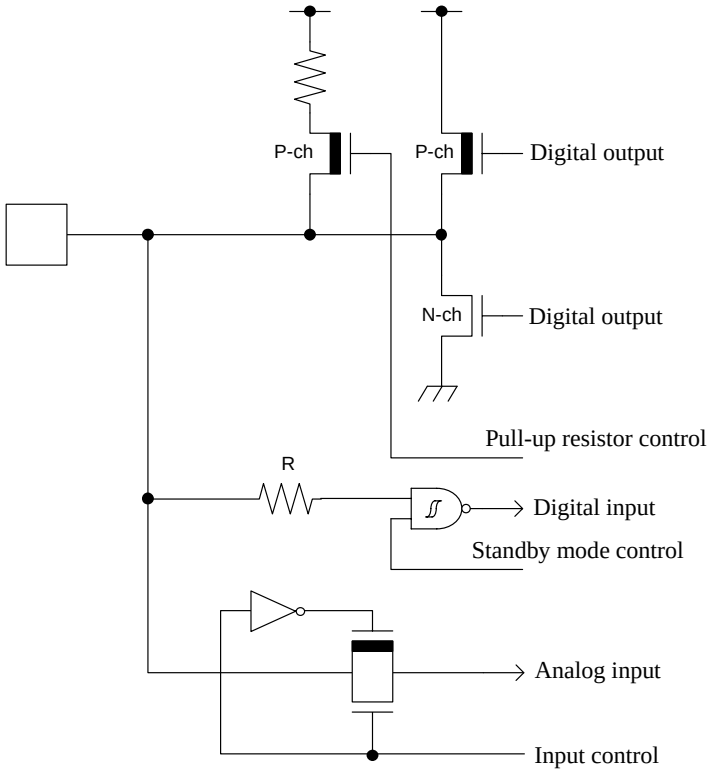
Pin Function	Pin Name	Function Description	Pin No	
			LQFP64 QFN64	LQFP48 QFN48
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	55	-
	RTCCO_1	Sub clock output pin	38	29
	SUBOUT_0	Sub clock output pin	55	-
	SUBOUT_1		38	29
USB	UDM0	USB device/host D – pin	62	46
	UDP0	USB device/host D + pin	63	47
	UHCONX0	USB external pull-up control pin	59	43
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	60	44
	WKUP1	Deep standby mode return signal input pin 1	38	29
	WKUP2	Deep standby mode return signal input pin 2	15	11
	WKUP3	Deep standby mode return signal input pin 3	27	-
DAC	DA0	D/A converter ch.0 analog output pin	34	25
	DA1	D/A converter ch.1 analog output pin	35	26
VBAT	VREGCTL	On-board regulator control pin	20	-
	VWAKEUP	The return signal input pin from a hibernation state	21	-
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	22	16
Mode	MD1	Mode 1 pin. During serial programming to Flash memory, MD1="L" must be input.	28	20
	MD0	Mode 0 pin. During normal operation, MD0="L" must be input. During serial programming to Flash memory, MD0="H" must be input.	29	21
Power	VCC	Power supply Pin	1	1
			-	15
			25	19
			33	-
	USBVCC	3.3V Power supply port for USB I/O	61	45
GND	VSS	GND Pin	16	12
			24	18
			32	24
			64	48
Clock	X0	Main clock (oscillation) input pin	30	22
	X1	Main clock (oscillation) I/O pin	31	23
	X0A	Sub clock (oscillation) input pin	17	13
	X1A	Sub clock (oscillation) I/O pin	18	14
	CROUT_0	Built-in high-speed CR-osc clock output port	47	-
	CROUT_1		54	42
Analog Power	AVCC	A/D converter and D/A converter analog power supply pin	39	30
	AVRH	A/D converter analog reference voltage input pin	42	33
VBAT Power	VBAT	VBAT power supply pin. Backup power supply (battery etc.) and system power supply.	19	-
Analog GND	AVSS	A/D converter and D/A converter GND pin	40	31
	AVRL	A/D converter analog reference voltage input pin	41	32
C pin	C	Power supply stabilization capacity pin	23	17

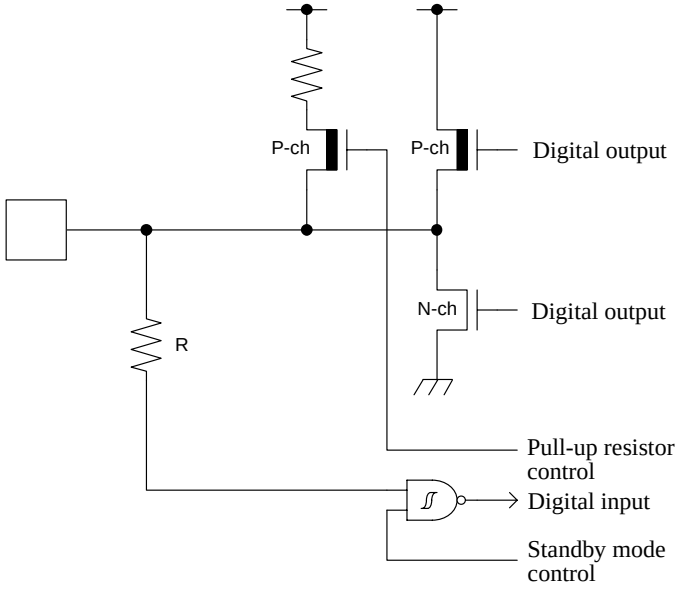
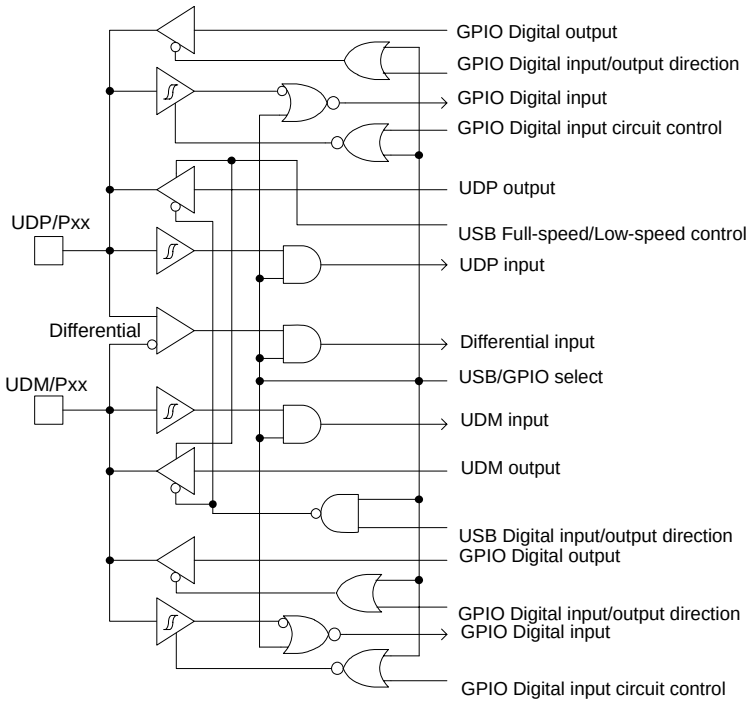
Note:

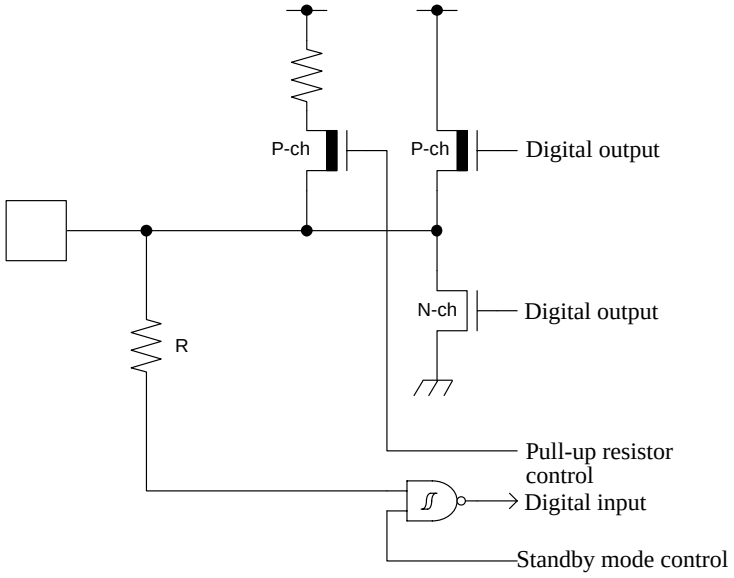
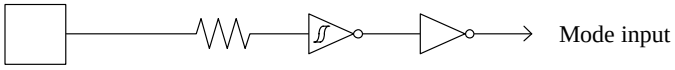
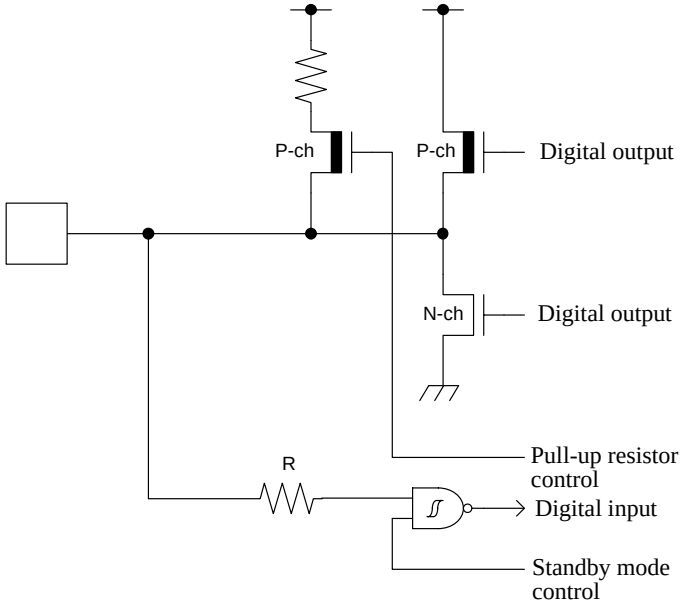
- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

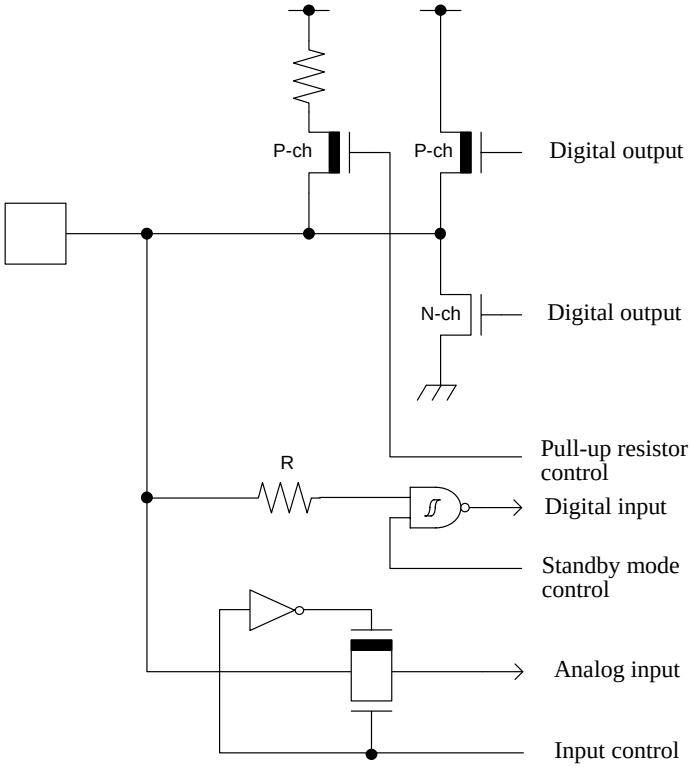
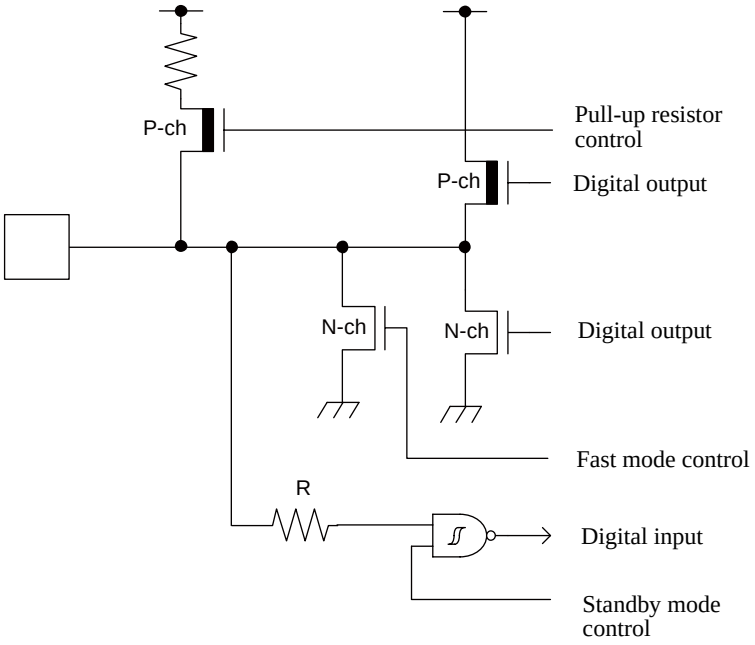
5. I/O Circuit Type

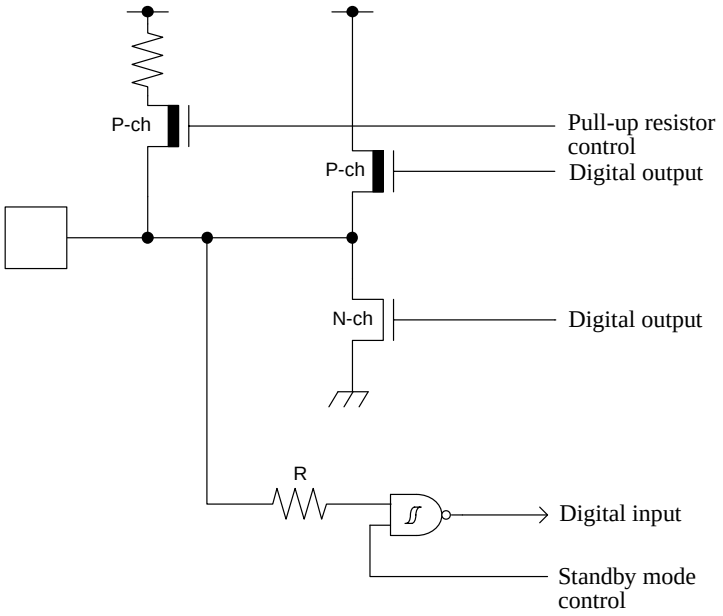
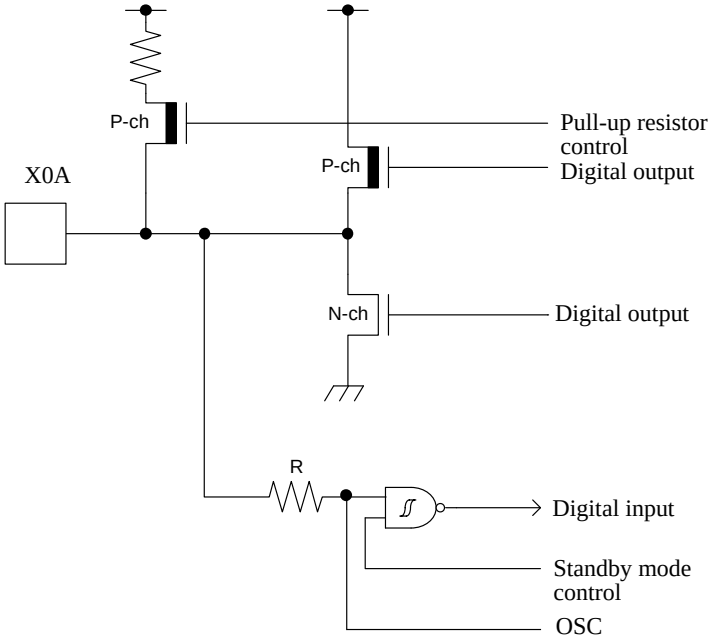
Type	Circuit	Remarks
A		It is possible to select the main oscillation / GPIO function When the main oscillation is selected. • Oscillation feedback resistor : Approximately 1 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA
B		• CMOS level hysteresis input • Pull-up resistor : Approximately 50 kΩ

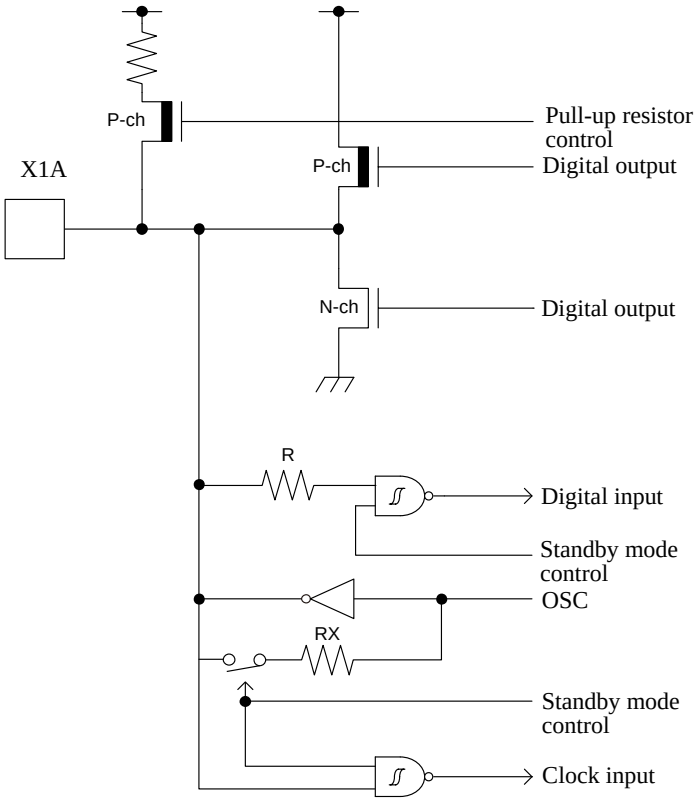
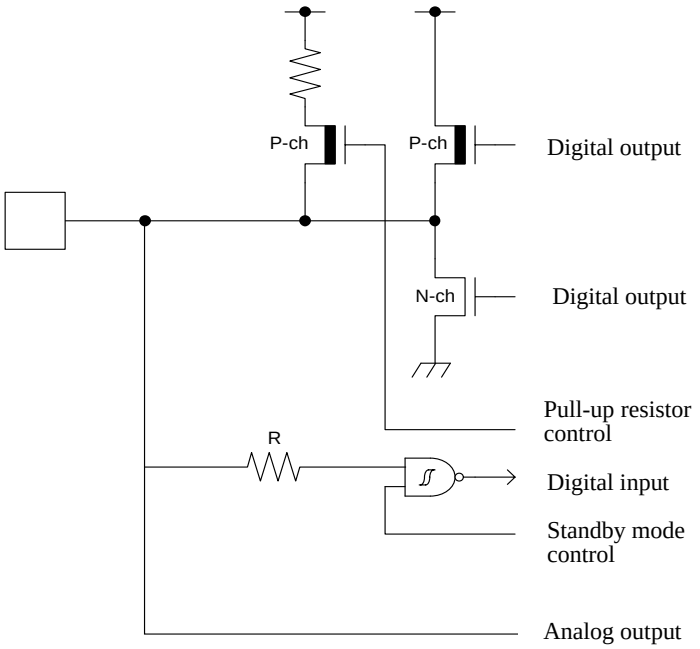
Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
E		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA
F		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
G		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -12 mA, I_{OL} = 12 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
H		It is possible to select the USB I/O / GPIO function. When the USB I/O is selected. • Full-speed, Low-speed control When the GPIO is selected. • CMOS level output • CMOS level hysteresis input • With standby mode control • I_{OH} = -20.5 mA, I_{OL} = 18.5 mA

Type	Circuit	Remarks
I		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • 5 V tolerant • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • Available to control of PZR registers. • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
J		CMOS level hysteresis input
L		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -8 mA, I_{OL} = 8 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
M		• CMOS level output • CMOS level hysteresis input • With input control • Analog input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -8 mA, I_{OL} = 8 mA • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off
N		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA (GPIO) • I_{OL} = 20 mA (Fast Mode Plus) • When this pin is used as an I^2C pin, the digital output P-ch transistor is always off

Type	Circuit	Remarks
O		• CMOS level output • CMOS level hysteresis input • 5 V tolerant • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • For I/O setting, refer to VBAT Domain in the Peripheral Manual
P		• CMOS level output • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • For I/O setting, refer to VBAT Domain in the Peripheral Manual

Type	Circuit	Remarks
Q		It is possible to select the sub oscillation / GPIO function When the sub oscillation is selected. • Oscillation feedback resistor : Approximately 10 MΩ • With Standby mode control When the GPIO is selected. • CMOS level output. • CMOS level hysteresis input • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -4 mA, I_{OL} = 4 mA • For I/O setting, refer to VBAT Domain in the Peripheral Manual
R		• CMOS level output • CMOS level hysteresis input • With input control • Analog output • With pull-up resistor control • With standby mode control • Pull-up resistor : Approximately 50 kΩ • I_{OH} = -12 mA, I_{OL} = 12 mA (4.5 V to 5.5 V) • I_{OH} = -8 mA, I_{OL} = 8 mA (2.7 V to 4.5 V)

6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and have established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

   CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

7. Handling Devices

Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each POWER pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 µF be connected as a bypass capacitor between VCC and VSS near this device.

Power Supply Pins

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1 V/µs at a momentary fluctuation such as switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

Sub Crystal Oscillator

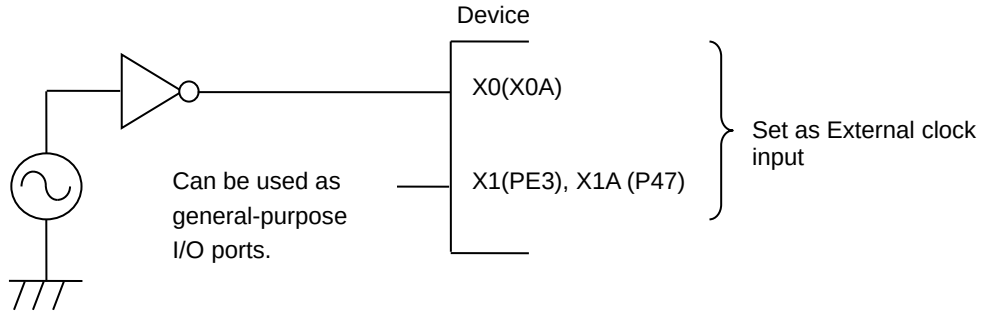
This series sub oscillator circuit is low gain to keep the low current consumption.
The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

- Surface mount type
  - Size : More than 3.2 mm × 1.5 mm
  - Load capacitance : Approximately 6 pF to 7 pF
- Lead type
  - Load capacitance : Approximately 6 pF to 7 pF

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1 (PE3) can be used as a general-purpose I/O port.
Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

Example of Using an External Clock

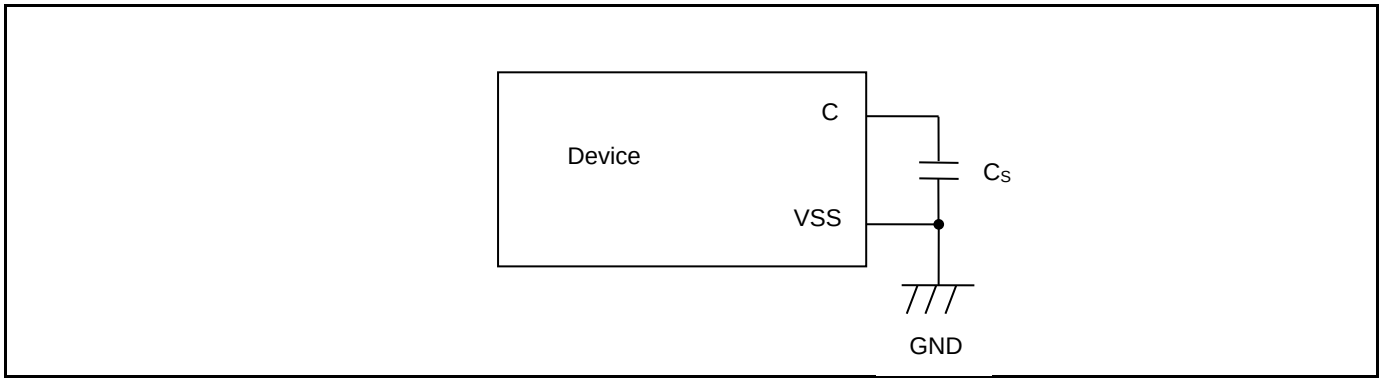


Handling when Using Multi-Function Serial Pin as I²C Pin

If it is using the multi-function serial pin as I²C pins, P-ch transistor of digital output is always disabled.
However, I²C pins need to keep the electrical characteristic like other pins and not to connect to the external I²C bus system with power OFF.

C Pin

This series contains the regulator. Be sure to connect a smoothing capacitor (C_S) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor.
However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor.
A smoothing capacitor of about 4.7 µF would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

Notes on Power-on

Turn power on/off in the following order or at the same time. The device operates normally after all power on.

In the case of 64pin package, VBAT only Power-on is possible when turns all power on and Hibernation control is setting and then except for VBAT turns power off. About Hibernation control, see Chapter 7-2: VBAT Domain (A) in FM4 Family Peripheral Manual (002-04856).
If not using the A/D converter and D/A converter, connect AVCC = VCC and AVSS = VSS.

Turning on:	VBAT → VCC → USBVCC
	VCC → AVCC → AVRH
Turning off:	AVRH → AVCC → VCC
	USBVCC → VCC → VBAT

Serial Communication

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.
Therefore, design a printed circuit board so as to avoid noise.
Consider the case of receiving wrong data due to noise, perform error detection such as by applying a checksum of data at the end.
If an error is detected, retransmit the data.

Differences in Features among the Products with Different Memory Sizes and between Flash Products and MASK Products

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash products and MASK products are different because chip layout and memory structures are different.
If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

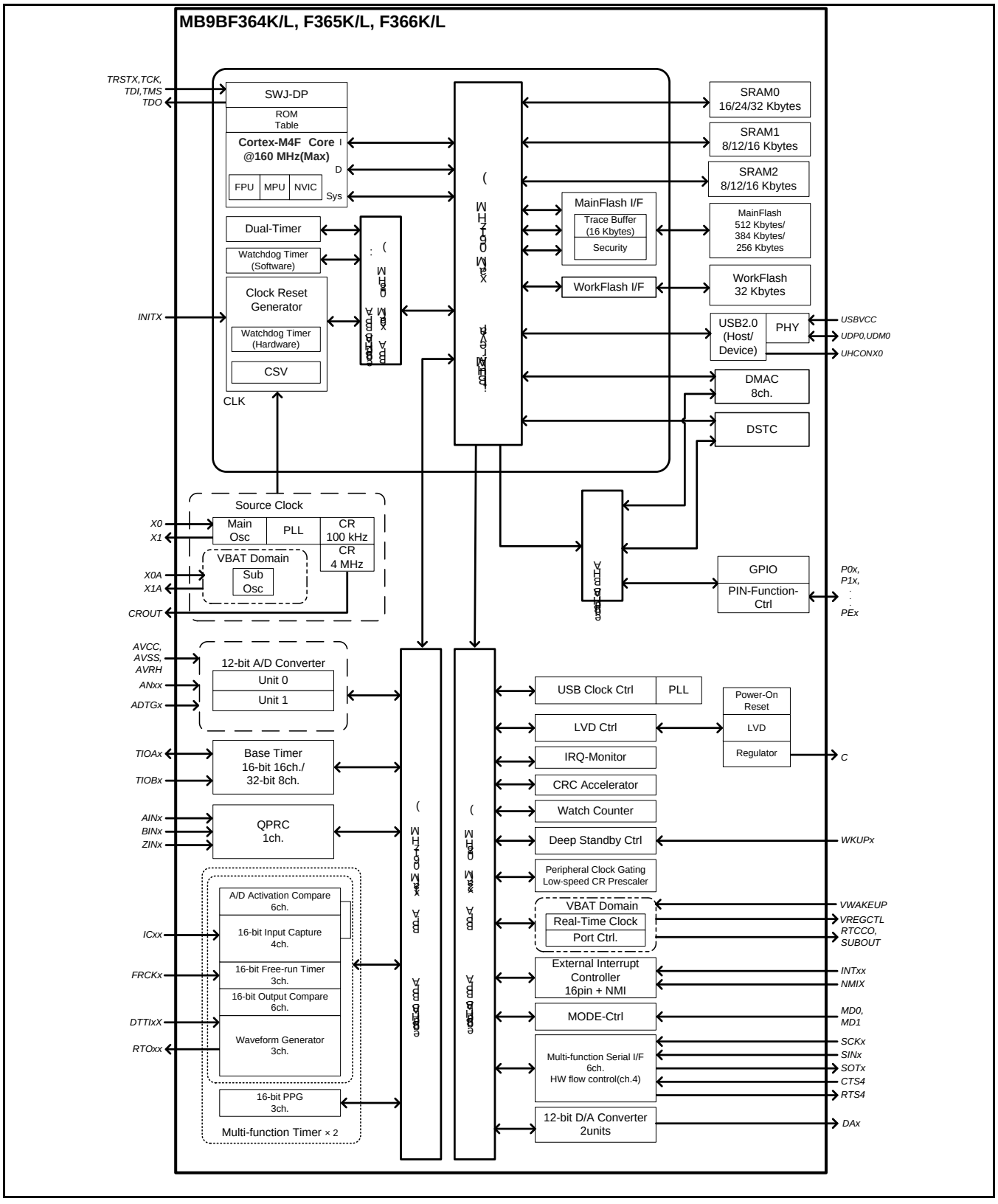
Pull-Up Function of 5 V Tolerant I/O

Please do not input the signal more than VCC voltage at the time of pull-up function use of 5V tolerant I/O.

Handling when Using Debug Pins

When debug pins (TDO/TMS/TDI/TCK/TRSTX or SWO/SWDIO/SWCLK) are set to GPIO or other peripheral functions, only set them as output, do not set them as input.

8. Block Diagram

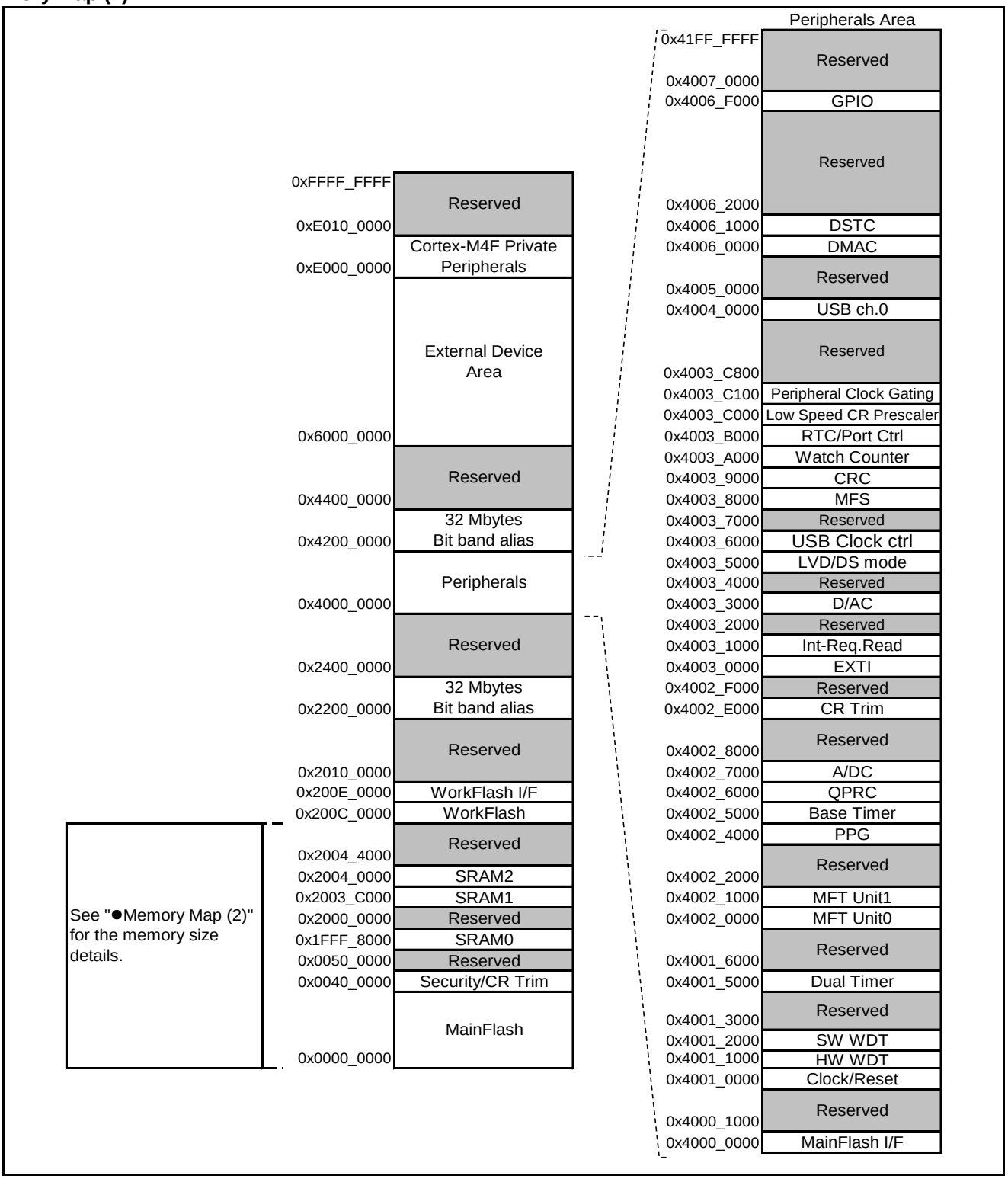


9. Memory Size

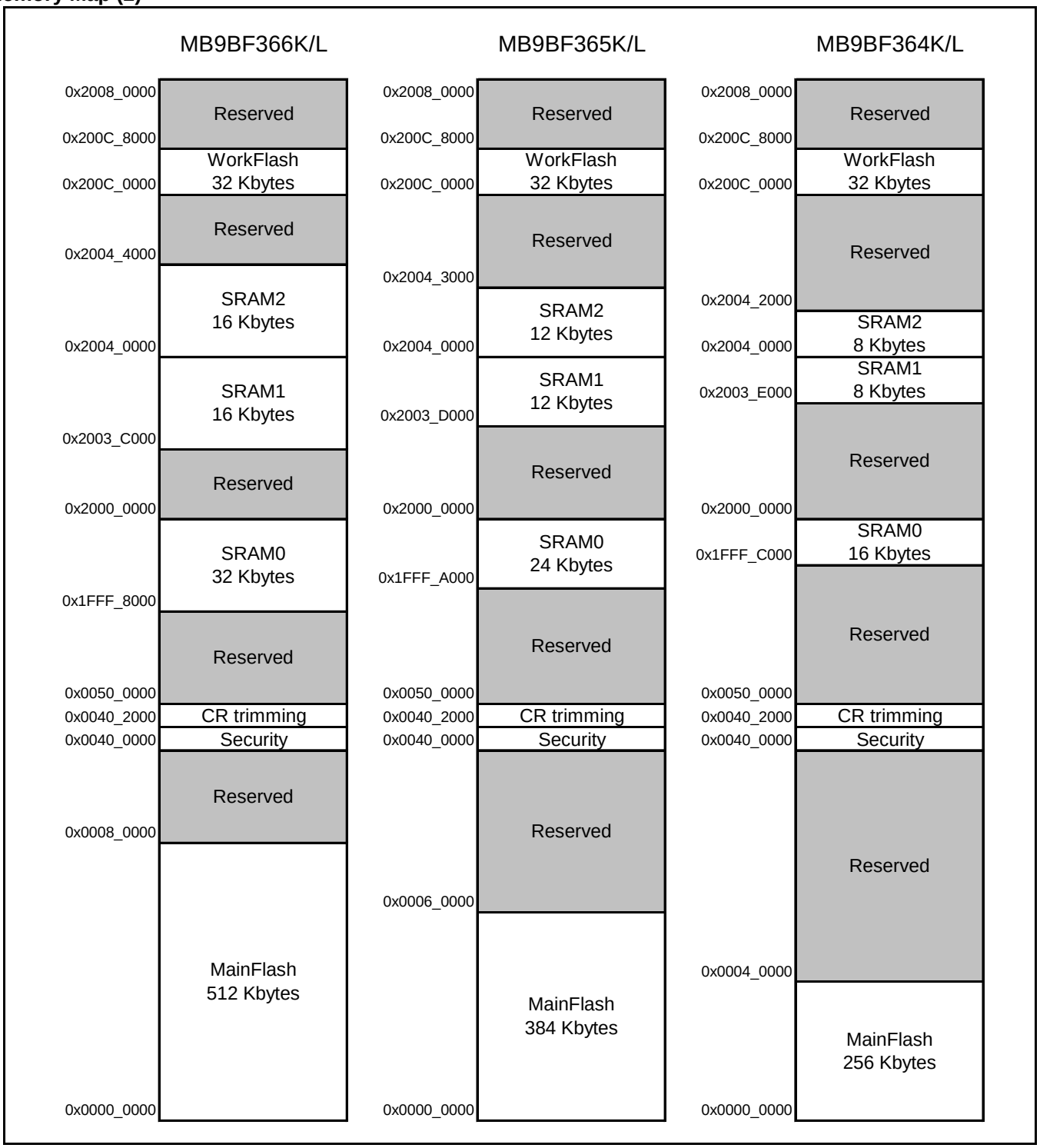
See Memory size in 1. Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)



Memory Map (2)


MB9BF366K/L
0x2008_0000
Reserved
0x200C_8000
WorkFlash
32 Kbytes
0x200C_0000
Reserved
0x2004_4000
SRAM2
16 Kbytes
0x2004_0000
SRAM1
16 Kbytes
0x2003_C000
Reserved
0x2000_0000
SRAM0
32 Kbytes
0x1FFF_8000
Reserved
0x0050_0000
0x0040_2000
CR trimming
0x0040_0000
Security
Reserved
0x0008_0000
MainFlash
512 Kbytes
0x0000_0000
MB9BF365K/L
0x2008_0000
Reserved
0x200C_8000
WorkFlash
32 Kbytes
0x200C_0000
Reserved
0x2004_3000
SRAM2
12 Kbytes
0x2004_0000
SRAM1
12 Kbytes
0x2003_D000
Reserved
0x2000_0000
SRAM0
24 Kbytes
0x1FFF_A000
Reserved
0x0050_0000
0x0040_2000
CR trimming
0x0040_0000
Security
Reserved
0x0006_0000
MainFlash
384 Kbytes
0x0000_0000
MB9BF364K/L
0x2008_0000
Reserved
0x200C_8000
WorkFlash
32 Kbytes
0x200C_0000
Reserved
0x2004_2000
SRAM2
8 Kbytes
0x2004_0000
SRAM1
8 Kbytes
0x2003_E000
Reserved
0x2000_0000
SRAM0
16 Kbytes
0x1FFF_C000
Reserved
0x0050_0000
0x0040_2000
CR trimming
0x0040_0000
Security
Reserved
0x0004_0000
MainFlash
256 Kbytes
0x0000_0000

Peripheral Address Map

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control
0x4001_1000	0x4001_1FFF		Hardware Watchdog timer
0x4001_2000	0x4001_2FFF		Software Watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-Timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-function timer unit0
0x4002_1000	0x4002_1FFF		Multi-function timer unit1
0x4002_2000	0x4003_FFFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base Timer
0x4002_6000	0x4002_6FFF		Quadrature Position/Revolution Counter
0x4002_7000	0x4002_7FFF		A/D Converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External Interrupt Controller
0x4003_1000	0x4003_1FFF		Interrupt Request Batch-Read Function
0x4003_2000	0x4003_4FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A Converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low Voltage Detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		Reserved
0x4003_8000	0x4003_8FFF		Multi-function serial Interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch Counter
0x4003_B000	0x4003_BFFF		RTC/Port Ctrl
0x4003_C000	0x4003_C0FF		Low-speed CR Prescaler
0x4003_C100	0x4003_C7FF		Peripheral Clock Gating
0x4003_C800	0x4003_FFFF		Reserved
0x4004_0000	0x4004_FFFF	AHB	USB ch.0
0x4005_0000	0x4005_FFFF		Reserved
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_EFFF		Reserved
0x4006_F000	0x4006_FFFF		GPIO
0x4006_7000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		WorkFlash I/F register

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

■INITX=0
This is the period when the INITX pin is the L level.

■INITX=1
This is the period when the INITX pin is the H level.

■SPL=0
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

■SPL=1
This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

■Input enabled
Indicates that the input function can be used.

■Internal input fixed at 0
This is the status that the input function cannot be used. Internal input is fixed at L.

■Hi-Z
Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

■Setting disabled
Indicates that the setting is disabled.

■Maintain previous state
Maintains the state that was immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

■Analog input is enabled
Indicates that the analog input is enabled.

■Trace output
Indicates that the trace function can be used.

■GPIO selected
In Deep standby mode, pins switch to the general-purpose I/O port.

■Setting prohibition
Prohibition of a setting by specification limitation.

List of Pin Status

Pin Status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at "0"/ or Input enable	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0					
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin Status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or SLEEP Mode State	TIMER Mode, RTC Mode, or STOP Mode State		Deep Standby RTC Mode or Deep Standby STOP Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
F	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									Maintain previous state
G	JTAG selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
J	Analog output selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	*2	*3	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled		Maintain previous state	Hi-Z / Internal input fixed at 0			
	GPIO selected									
K	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than above selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
M	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
O	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z Input enabled	Hi-Z Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
P	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	GPIO selected									

Pin Status Type	Function Group	Power-on Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	External interrupt enabled selected							GPIO selected Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected Internal input fixed at "0" Hi-Z / Input enabled	Hi-Z / Internal input fixed at "0" Hi-Z / Input enabled	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled		Hi-Z at trans-mission/ Input enabled/ Internal input fixed at 0 at reception	Hi-Z at trans-mission/ Input enabled/ Internal input fixed at 0 at reception	Hi-Z / Input enabled	Hi-Z / Input enabled	Hi-Z / Input enabled

*1: Oscillation is stopped at Sub timer mode, sub CR timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

*2: Maintain previous state at timer mode. GPIO selected Internal input fixed at 0 at RTC mode, Stop mode.

*3: Maintain previous state at timer mode. Hi-Z/Internal input fixed at 0 at RTC mode, Stop mode.

List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	Power-on Reset *1	INITX Input State	Device Internal Reset State	Run Mode or Sleep Mode State	Timer Mode, RTC Mode, or Stop Mode State		Deep Standby RTC Mode or Deep Standby Stop Mode State		Return from Deep Standby Mode State	VBAT RTC Mode State	Return from VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ or Input enable	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state/When oscillation stops, Hi-Z *2	Maintain previous state/When oscillation stops, Hi-Z *2	Maintain previous state/When oscillation stops, Hi-Z *2	Maintain previous state/When oscillation stops, Hi-Z *2	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected / GPIO selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state

*1: When VBAT and VCC power on.

*2: When The SOSCNTL bit in the WTOSCCNT Register is “0”, Sub crystal oscillator output pin is maintain previous state.
When The SOSCNTL bit in the WTOSCCNT Register is “1”, Oscillation is stopped at STOP mode and Deep standby STOP mode.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage *1, *2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (for USB) *1, *3	$USBV_{CC}$	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (VBAT) *1, *4	V_{BAT}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1, *5	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1, *5	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	Except for USB pin
		V_{SS} - 0.5	$USBV_{CC}$ + 0.5 (≤ 6.5V)	V	USB pin
		V_{SS} - 0.5	V_{SS} + 6.5	V	5 V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5V)	V	
"L" level maximum output current *6	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	12 mA type
			22.4	mA	I^2C Fm+
"L" level average output current *7	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			12	mA	12 mA type
			20	mA	I^2C Fm+
"L" level total maximum output current	$\sum I_{OL}$	-	100	mA	
"L" level total average output current *8	$\sum I_{OLAV}$	-	50	mA	
"H" level maximum output current *6	I_{OH}	-	- 10	mA	4 mA type
			- 20	mA	8 mA type
			- 20	mA	12 mA type
"H" level average output current *7	I_{OHAV}	-	- 4	mA	4 mA type
			- 8	mA	8 mA type
			- 12	mA	12 mA type
"H" level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
"H" level total average output current *8	$\sum I_{OHAV}$	-	- 50	mA	
Storage temperature	T_{STG}	- 55	+ 150	°C	

*1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

*2: V_{CC} must not drop below V_{SS} - 0.5 V.

*3: $USBV_{CC}$ must not drop below V_{SS} - 0.5 V.

*4: V_{BAT} must not drop below V_{SS} - 0.5 V.

*5: Ensure that the voltage does not exceed V_{CC} + 0.5 V, for example, when the power is turned on.

*6: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

*7: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100ms period.

*8: The total average output current is defined as the average current value flowing through all of corresponding pins for a period of 100 ms.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.*
  Do not exceed any of these ratings.

12.2 Recommended Operating Conditions

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V_{CC}	-	2.7 *5	5.5	V	
Power supply voltage (for USB)		$USBV_{CC}$	-	3.0	3.6 (≤ V_{CC})	V	*1
				2.7	5.5 (≤ V_{CC})		*2
Power supply voltage (VBAT)		V_{BAT}	-	2.7	5.5	V	
Analog power supply voltage		AV_{CC}	-	2.7	5.5	V	AV_{CC}=V_{CC}
Analog reference voltage		AVRH	-	*3	AV_{CC}	V	
Smoothing capacitor		C_S	-	1	10	µF	for built-in regulator *6
Operating temperature	Junction temperature	Tj	-	- 40	+ 125	°C	
	Ambient temperature	T_A	-	- 40	*4	°C	

*1: When P81/UDP0 and P80/UDM0 pins are used as USB (UDP0, UDM0).

*2: When P81/UDP0 and P80/UDM0 pins are used as GPIO (P81, P80).

*3: The minimum value of Analog reference voltage depends on the value of compare clock cycle (Tcck).
See "5. 12-bit A/D Converter" for the details.

*4: The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (Tj).
The calculation formula of the ambient temperature (T_A) is shown below.

$T_A(Max) = Tj(Max) - Pd(Max) \times \theta ja$

Pd: Power dissipation (W)
θja: Package thermal resistance (°C/W)

$Pd\ (Max) = V_{CC} \times I_{CC}\ (Max) + \Sigma\ (I_{OL} \times V_{OL}) + \Sigma\ ((V_{CC} - V_{OH}) \times (-I_{OH}))$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

*5: In between less than the minimum power supply voltage and low voltage reset/interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

*6: See "C pin" in "Handling Devices" for the connection of the smoothing capacitor.

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal resistance θja (°C/W)	Maximum permissible Power (mW)	
			T_A=+85°C	T_A=+105°C
LQA048 (0.5mm pitch)	Single-layered both sides	87	460	230
	4 layers	53	755	377
VNA048 (0.5mm pitch)	Single-layered both sides	30	1333	667
	4 layers	24	1667	833
LQD064 (0.5mm pitch)	Single-layered both sides	70	571	286
	4 layers	45	889	444
LQG064 (0.65mm pitch)	Single-layered both sides	61	656	328
	4 layers	40	1000	500
VNC064 (0.5mm pitch)	Single-layered both sides	24	1667	833
	4 layers	21	1905	952

WARNING:

- *The recommended operating conditions are required to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.*
  Any use of semiconductor devices will be under their recommended operating condition.

Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.
No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$

I_{OL}: "L" level output current

I_{OH}: "H" level output current

V_{OL}: "L" level output voltage

V_{OH}: "H" level output voltage

I_{CC} is a current consumed in device.
It can be analyzed as follows.

$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$

$I_{CC}(INT)$: Current consumed in internal logic and memory, etc. through regulator

$\Sigma I_{CC}(IO)$: Sum of current (I/O switching current) consumed in output pin

For I_{CC} (INT), it can be anticipated by "12.3.1 Current Rating" in "12.3 DC Characteristics" (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For Icc (IO), it depends on system used by customers.
The calculation formula is shown below.

$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times fsw$

C_{INT}: Pin internal load capacitance

C_{EXT}: External load capacitance of output pin

f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

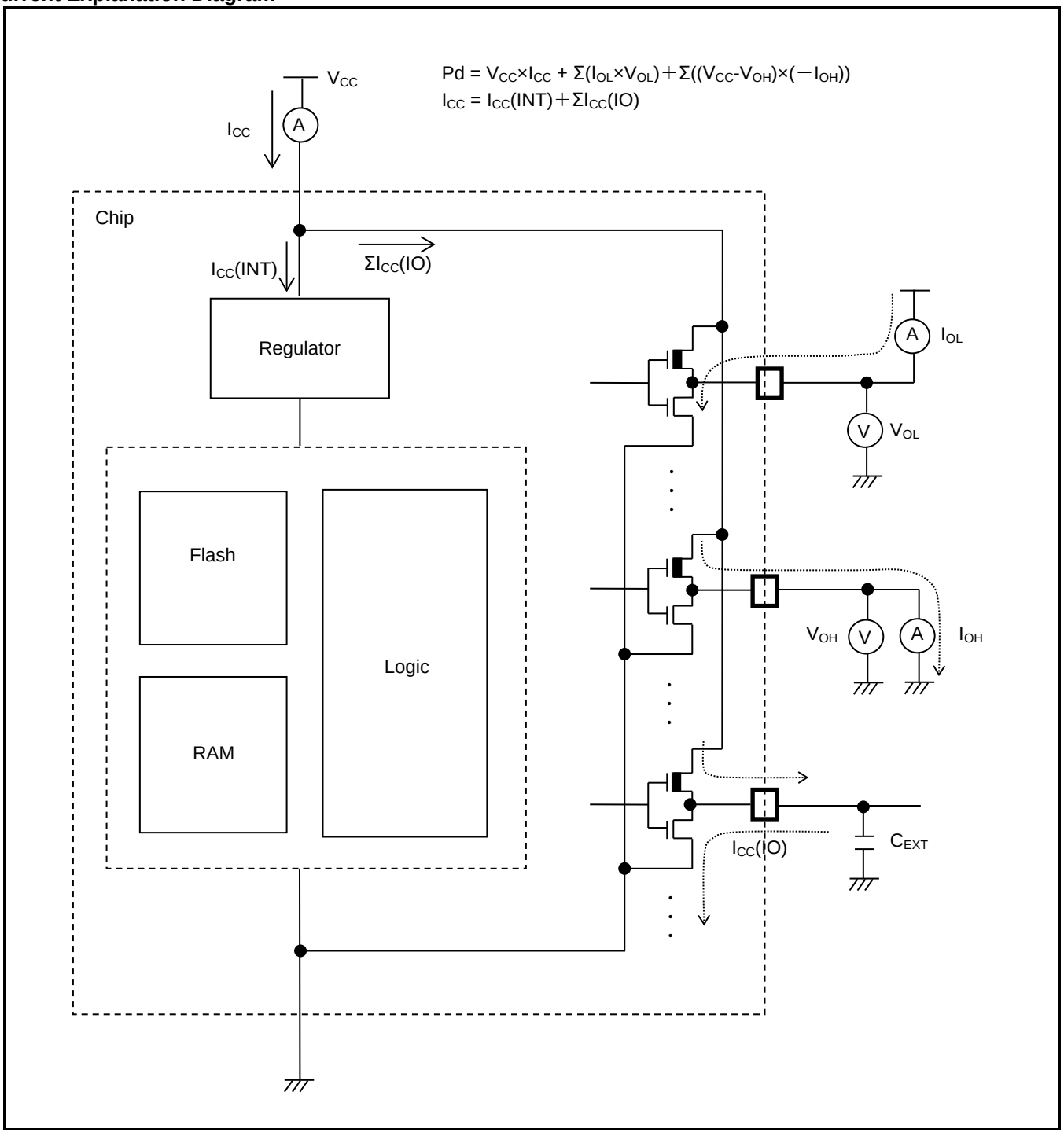
Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated.

1. Measure current value I_{CC} (Typ) at normal temperature (+25°C).
2. Add maximum leak current value I_{CC} (leak_max) at operating on a value in (1).

$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak_max)$

Parameter	Symbol	Conditions	Current Value
Maximum leak current at operating	I_{CC}(leak_max)	Tj = +125 °C	28 mA
		Tj = +105 °C	17 mA
		Tj = +85 °C	13 mA

Current Explanation Diagram



12.3 DC Characteristics

12.3.1 Current Rating

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (PLL)	*5, *6	160 MHz	44	72	mA	*3 When all peripheral clocks are ON
					144 MHz	40	67		
					120 MHz	34	60		
					100 MHz	29	55		
					80 MHz	23	48		
					60 MHz	18	42		
					40 MHz	13	37		
					20 MHz	7.7	31		
					8 MHz	4.6	27		
					4 MHz	3.6	26		
					160 MHz	30	58	mA	*3 When all peripheral clocks are OFF
					144 MHz	27	54		
					120 MHz	23	49		
					100 MHz	20	46		
					80 MHz	16	41		
					60 MHz	13	38		
					40 MHz	9	33		
					20 MHz	5.7	30		
					8 MHz	3.7	27		
					4 MHz	3	26		

Parameter	Symbol	Pin Name	Conditions		Frequency*7	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (PLL)	*8	160 MHz	64	101	mA	*3 When all peripheral clocks are ON
					144 MHz	60	96		
					120 MHz	52	88		
					100 MHz	46	81		
					80 MHz	39	73		
					60 MHz	32	65		
					40 MHz	25	58		
					20 MHz	15	47		
					8 MHz	7.8	39		
					4 MHz	5.2	36		
					160 MHz	47	80	mA	*3 When all peripheral clocks are OFF
					144 MHz	43	75		
					120 MHz	39	71		
					100 MHz	35	66		
					80 MHz	30	61		
					60 MHz	25	55		
					40 MHz	20	50		
					20 MHz	13	42		
					8 MHz	6.7	36		
					4MHz	4.6	34		

*1: T_A=+25 °C, V_{CC}=3.3 V

*2: Tj=+125 °C, V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0".

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When operating flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

*6: Data access is nothing to MainFlash memory

*7: Frequency is a value of HCLK. PCLK0=PCLK2=HCLK/2, PCLK1=HCLK

*8: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 0)

Parameter	Symbol	Pin Name	Conditions		Frequency*4 (MHz)	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (PLL)	*5	72 MHz	41	75	mA	*3 When all peripheral clocks are ON
					60 MHz	36	69		
					48 MHz	31	64		
					36 MHz	25	57		
					24 MHz	18	50		
					12 MHz	11	42		
					8 MHz	8.1	39		
					4 MHz	5.4	37		
					72 MHz	32	63	mA	*3 When all peripheral clocks are OFF
					60 MHz	28	58		
					48 MHz	24	54		
					36 MHz	20	50		
					24 MHz	15	45		
					12 MHz	9.1	38		
					8 MHz	6.9	36		
					4 MHz	4.6	34		

*1: T_A=+25 °C, V_{CC}=3.3 V

*2: Tj=+125 °C, V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0".

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 00)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation (built-in high-speed CR)	*5	4 MHz	3.3	29	mA	*3 When all peripheral clocks are ON
						2.8	29	mA	*3 When all peripheral clocks are OFF
			Normal operation (sub oscillation)	*5	32 kHz	0.51	27	mA	*3 When all peripheral clocks are ON
						0.50	27	mA	*3 When all peripheral clocks are OFF
			Normal operation (built-in low-speed CR)	*5	100 kHz	0.54	27	mA	*3 When all peripheral clocks are ON
						0.52	27	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25 °C, V_{CC}=3.3 V

*2: Tj=+125 °C, V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0".

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: When 0 wait-cycle mode (FRWTR.RWT = 00, FSYNDN.SD = 000)

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation (PLL)	160 MHz	28	58	mA	*3 When all peripheral clocks are ON
				144 MHz	25	55		
				120 MHz	21	50		
				100 MHz	18	46		
				80 MHz	15	43		
				60 MHz	12	39		
				40 MHz	8.8	36		
				20 MHz	5.6	32		
				8 MHz	3.8	30		
				4 MHz	3.2	29		
				160 MHz	14	44	mA	*3 When all peripheral clocks are OFF
				144 MHz	13	43		
				120 MHz	11	40		
				100 MHz	9.7	38		
				80 MHz	8.1	36		
				60 MHz	6.7	34		
				40 MHz	5.2	32		
				20 MHz	3.7	30		
				8 MHz	2.9	29		
				4 MHz	2.6	29		

Parameter	Symbol	Pin Name	Conditions	Frequency*5	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation (PLL)	72 MHz	19	47	mA	*3 When all peripheral clocks are ON
				60 MHz	16	43		
				48 MHz	13	40		
				36 MHz	10	37		
				24 MHz	7.8	34		
				12 MHz	5.2	31		
				8 MHz	4.3	30		
				4 MHz	3.5	29		
				72 MHz	8.8	36	mA	*3 When all peripheral clocks are OFF
				60 MHz	7.7	35		
				48 MHz	6.6	34		
				36 MHz	5.5	32		
				24 MHz	4.4	31		
				12 MHz	3.4	30		
				8 MHz	3	29		
				4 MHz	2.7	29		

*1: T_A=+25 °C, V_{CC}=3.3 V

*2: Tj=+125 °C, V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0".

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

*5: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation (built-in high-speed CR)	4 MHz	1.3	27	mA	*3 When all peripheral clocks are ON
					0.91	27	mA	*3 When all peripheral clocks are OFF
			Sleep operation (sub oscillation)	32 kHz	0.49	27	mA	*3 When all peripheral clocks are ON
					0.48	27	mA	*3 When all peripheral clocks are OFF
			Sleep operation (built-in low-speed CR)	100 kHz	0.51	27	mA	*3 When all peripheral clocks are ON
					0.49	27	mA	*3 When all peripheral clocks are OFF

*1: T_A=+25 °C, V_{CC}=3.3 V

*2: Tj=+125 °C, V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0".

*4: Frequency is a value of HCLK. PCLK0=PCLK1=PCLK2=HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	STOP mode	-	0.25	1.0	mA	*3, *4 T_A=+25°C
					-	11	mA	*3, *4 T_A =+85°C
					-	14	mA	*3, *4 T_A =+105°C
	I_{CCT}		TIMER mode (built-in high-speed CR)	4 MHz	0.54	1.54	mA	*3, *4 T_A =+25°C
					-	12	mA	*3, *4 T_A =+85°C
					-	15	mA	*3, *4 T_A =+105°C
			TIMER mode (sub oscillation)	32 kHz	0.25	1.0	mA	*3, *4 T_A =+25°C
					-	11	mA	*3, *4 T_A =+85°C
					-	14	mA	*3, *4 T_A =+105°C
			TIMER mode (built-in low-speed CR)	100 kHz	0.26	1.0	mA	*3, *4 T_A =+25°C
					-	11	mA	*3, *4 T_A =+85°C
					-	14	mA	*3, *4 T_A =+105°C
	I_{CCR}		RTC mode (sub oscillation)	32 kHz	0.25	1.0	mA	*3, *4 T_A =+25°C
					-	11	mA	*3, *4 T_A =+85°C
					-	14	mA	*3, *4 T_A =+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0".

*4: When LVD is OFF

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCHD}	VCC	Deep standby STOP mode (When RAM is OFF)*6	-	27	140	µA	*3, *4 T_A=+25°C
					-	590	µA	*3, *4 T_A =+85°C
					-	770	µA	*3, *4 T_A =+105°C
			Deep standby STOP mode (When RAM is ON)*6		32	180	µA	*3, *4 T_A =+25°C
					-	870	µA	*3, *4 T_A =+85°C
					-	1200	µA	*3, *4 T_A =+105°C
	I_{CCRD}		Deep standby RTC mode (When RAM is OFF)*7	32 kHz	27	140	µA	*3, *4 T_A =+25°C
					-	590	µA	*3, *4 T_A =+85°C
					-	770	µA	*3, *4 T_A =+105°C
			Deep standby RTC mode (When RAM is ON)*7		32	180	µA	*3, *4 T_A =+25°C
					-	870	µA	*3, *4 T_A =+85°C
					-	1200	µA	*3, *4 T_A =+105°C
	I_{CCVBAT}	VBAT	RTC stop*9	-	0.015	0.14	µA	*3, *4, *5 T_A =+25°C
					-	4.0	µA	*3, *4, *5 T_A =+85°C
					-	9.4	µA	*3, *4, *5 T_A =+105°C
			RTC operation*8, *9	32 kHz	1.3	2.4	µA	*3, *4 T_A =+25°C
					-	6.2	µA	*3, *4 T_A =+85°C
					-	12	µA	*3, *4 T_A =+105°C

*1: V_{CC}=3.3 V

*2: V_{CC}=5.5 V

*3: When all ports are input and are fixed at "0".

*4: When LVD is OFF

*5: When sub oscillation is OFF

*6: When 48 pin Package, add supply current of RTC stop.

*7: When 48 pin Package, add supply current of RTC operation.

*8: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit).

*9: In the case of setting RTC after VCC power on.

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	-	4	7	µA	For occurrence of interrupt
Main flash memory write/erase current	$I_{CCFLASH}$		At Write/Erase	-	13.4	15.9	mA	
Work flash memory write/erase current	$I_{CCWFLASH}$		At Write/Erase	-	11.5	13.6	mA	

Peripheral Current Dissipation

Clock System	Peripheral	Unit	Frequency (MHz)			Unit	Remarks
			40	80	160		
HCLK	GPIO	All ports	0.21	0.43	0.92	mA	
	DMAC	-	0.71	1.43	2.74		
	DSTC	-	0.36	0.72	1.46		
	USB	1ch.	0.42	0.80	1.60		
PCLK1	Base timer	4ch.	0.18	0.36	0.70	mA	
	Multi-functional timer/PPG	1 unit/4ch.	0.57	1.13	2.24		
	Quadrature position/Revolution counter	1 unit	0.04	0.08	0.16		
	A/DC	1 unit	0.21	0.40	0.79		
PCLK2	Multi-function serial	1ch.	0.33	0.67	-	mA	

12.3.2 Pin Characteristics

(V_{CC} = $USBV_{CC}$ = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
		5V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
"L" level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
"H" level output voltage	V_{OH}	4mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 2 mA					
		8mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 4 mA					
		12mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8 mA					
		The pin doubled as USB I/O	$USBV_{CC}$ ≥ 4.5 V, I_{OH} = - 20.5 mA	$USBV_{CC}$ - 0.4	-	$USBV_{CC}$	V	
			$USBV_{CC}$ < 4.5 V, I_{OH} = - 13.0 mA					
		The pin doubled as I^2C Fm+	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO
			V_{CC} < 4.5 V, I_{OH} = - 3 mA					

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5$ V, $I_{OL} = 4$ mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, $I_{OL} = 2$ mA					
		8 mA type	$V_{CC} \geq 4.5$ V, $I_{OH} = 8$ mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, $I_{OH} = 4$ mA					
		12 mA type	$V_{CC} \geq 4.5$ V, $I_{OL} = 12$ mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, $I_{OL} = 8$ mA					
		The pin doubled as USB I/O	$USBV_{CC} \geq 4.5$ V, $I_{OL} = 18.5$ mA	V_{SS}	-	0.4	V	
			$USBV_{CC} < 4.5$ V, $I_{OL} = 10.5$ mA					
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5$ V, $I_{OH} = 4$ mA	V_{SS}	-	0.4	V	At GPIO
			$V_{CC} < 4.5$ V, $I_{OH} = 3$ mA					
			$V_{CC} \leq 5.5$ V, $I_{OH} = 20$ mA					At I^2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	25	50	100	kΩ	
			$V_{CC} < 4.5$ V	30	80	200		
Input capacitance	C_{IN}	Other than VCC, USBVCC, VBAT, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

12.4 AC Characteristics

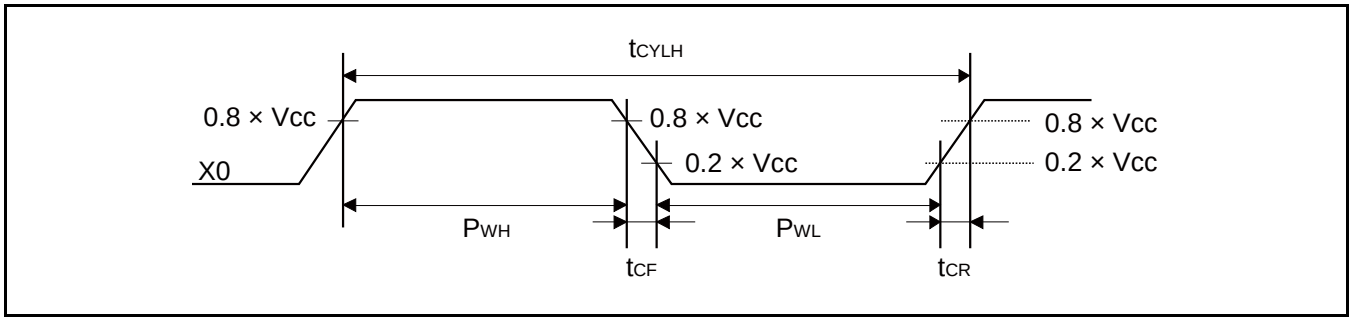
12.4.1 Main Clock Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CH}	X0, X1	$V_{CC} \geq 4.5$ V	4	48	MHz	When crystal oscillator is connected
			$V_{CC} < 4.5$ V	4	20		
			$V_{CC} \geq 4.5$ V	4	48	MHz	When using external clock
			$V_{CC} < 4.5$ V	4	20		
Input clock cycle	t_{CYLH}		$V_{CC} \geq 4.5$ V	20.83	250	ns	When using external clock
			$V_{CC} < 4.5$ V	50	250		
Input clock pulse width	-		P_{WH}/t_{CYLH}, P_{WL}/t_{CYLH}	45	55	%	When using external clock
Input clock rising time and falling time	t_{CF}, t_{CR}		-	-	5	ns	When using external clock
Internal operating clock*1 frequency	f_{CC}	-	-	-	160	MHz	Base clock (HCLK/FCLK)
	f_{CP0}	-	-	-	80	MHz	APB0 bus clock*2
	f_{CP1}	-	-	-	160	MHz	APB1 bus clock*2
	f_{CP2}	-	-	-	80	MHz	APB2 bus clock*2
Internal operating clock*1 cycle time	t_{CYCC}	-	-	6.25	-	ns	Base clock (HCLK/FCLK)
	t_{CYCP0}	-	-	12.5	-	ns	APB0 bus clock*2
	t_{CYCP1}	-	-	6.25	-	ns	APB1 bus clock*2
	t_{CYCP2}	-	-	12.5	-	ns	APB2 bus clock*2

*1: For more information about each internal operating clock, see CHAPTER 2-1: Clock in FM4 Family Peripheral Manual Main part (002-04856).

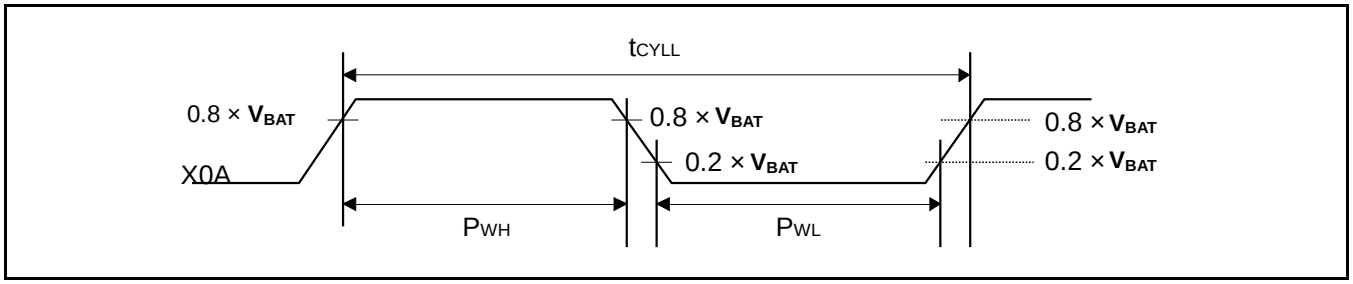
*2: For about each APB bus which each peripheral is connected to, see 8. Block Diagram in this data sheet.



12.4.2 Sub Clock Input Characteristics

(V_{BAT} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	1/ t_{CYLL}	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock



In the case of 48 pin Package, V_{BAT} is V_{CC}.

12.4.3 Built-in CR Oscillation Characteristics

Built-in High-Speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_J = -20°C to +105°C	3.92	4	4.08	MHz	When trimming *
		T_J = - 40°C to +125°C	3.88	4	4.12		
		T_J = - 40°C to +125°C	3	4	5		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µS	*2

*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency/temperature trimming.

*2: This is the time to stabilize the frequency of high-speed CR clock after setting trimming value.
This period is able to use high-speed CR clock as source clock.

Built-in Low-Speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.4 Operating Conditions of Main PLL (In the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	80	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	320	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	160	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see CHPATER 2-1: Clock in FM4 Family Peripheral Manual Main part (002-04856).

12.4.5 Operating Conditions of USB PLL (In the Case of Using Main Clock for Input Clock of PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	100	-	-	µs	
PLL input clock frequency	f_{PLLI}	4	-	16	MHz	
PLL multiplication rate	-	13	-	80	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	200	-	320	MHz	
USB clock frequency*2	$f_{CLKSPLL}$	-	-	48	MHz	After the M frequency division

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about USB clock, see CHAPTER 2-2: USB Clock Generation in FM4 Family Peripheral Manual Communication Macro part (002-04862).

12.4.6 Operating Conditions of Main PLL (In the Case of Using Built-in High-Speed CR Clock for Input Clock of Main PLL)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time*1 (LOCK UP time)	t_{LOCK}	200	-	-	µs	
PLL input clock frequency	f_{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	50	-	75	multiplier	
PLL macro oscillation clock frequency	f_{PLLO}	190	-	320	MHz	
Main PLL clock frequency*2	f_{CLKPLL}	-	-	160	MHz	

*1: Time from when the PLL starts operating until the oscillation stabilizes.

*2: For more information about Main PLL clock (CLKPLL), see CHAPTER 2-1: Clock in FM4 Family Peripheral Manual Main part (002-04856).

Note:

- *Make sure to input to the main PLL source clock, the high-speed CR clock (CLKHC) that the frequency and temperature has been trimmed.*

12.4.7 Reset Input Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{INITX}	INITX	-	500	-	ns	

12.4.8 Power-on Reset Timing

(V_{SS} = 0V, T_A = - 40°C to + 85°C)

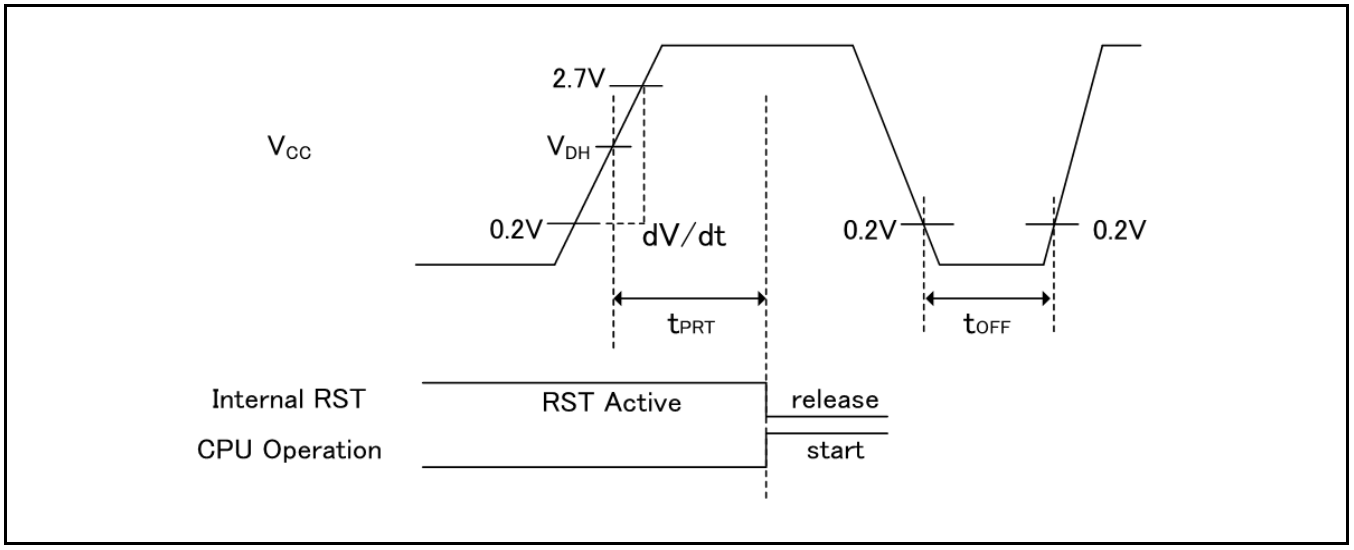
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	50	-	-	ms	*1
Power ramp rate	dV/dt		V_{CC}: 0.2V to 2.70V	1.3	-	1000	mV/µs	*2
Time until releasing Power-on reset	t_{PRT}		-	0.33	-	0.60	ms	

*1: V_{CC} must be held below 0.2V for a minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>50ms).

Note:

- *t_{OFF} must be satisfied. When t_{OFF} cannot be satisfied, assert external reset (INITX) at power-up and at any brownout event.*



Glossary

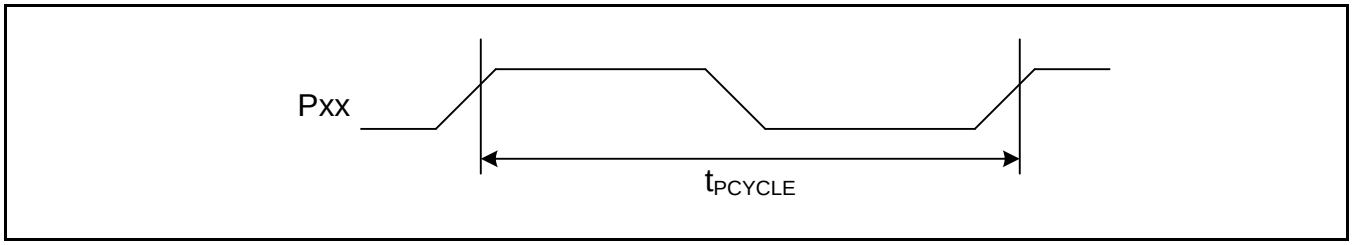
□ VDH: detection voltage of Low-Voltage detection reset. See 12.8 Low-Voltage Detection Characteristics.

12.4.9 GPIO Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Output frequency	t_{PCYCLE}	Pxx*	$V_{CC} \geq 4.5$ V	-	50	MHz
			$V_{CC} < 4.5$ V	-	32	MHz

*: GPIO is a target.

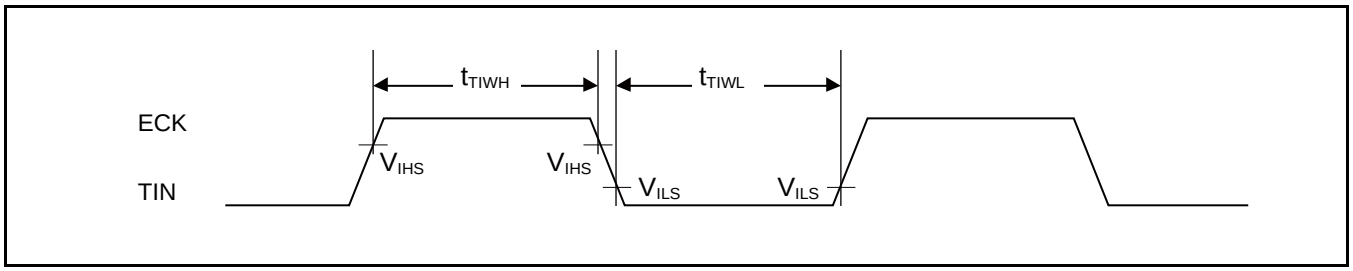


12.4.10 Base Timer Input Timing

Timer Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

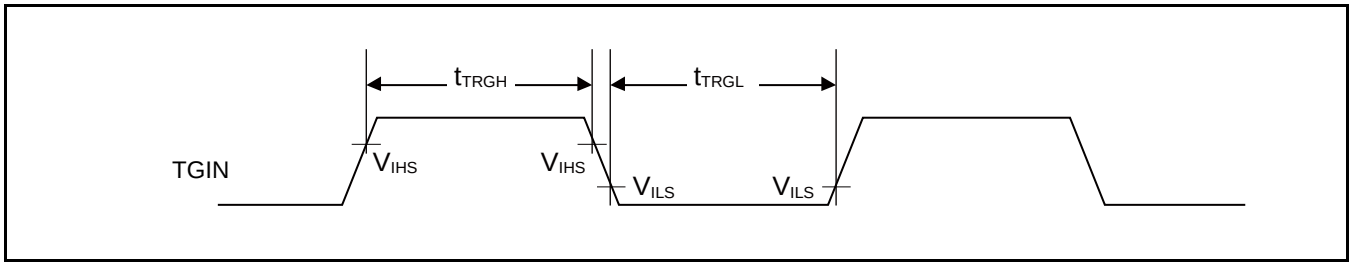
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which the Base Timer is connected to, see 8. Block Diagram in this data sheet.

12.4.11 CSIO/UART Timing

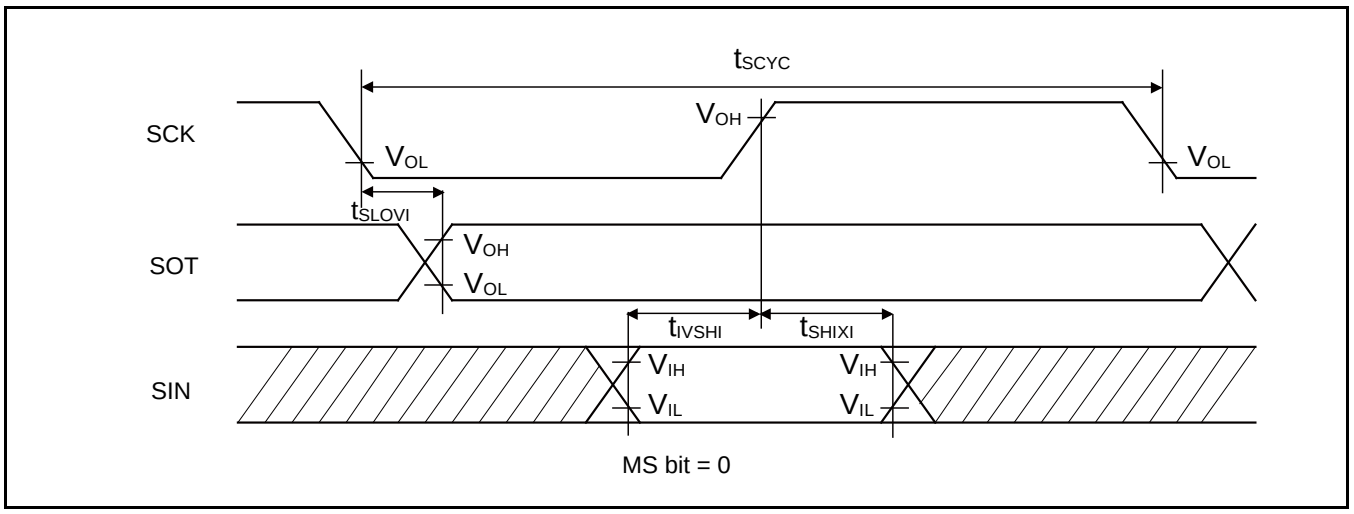
Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

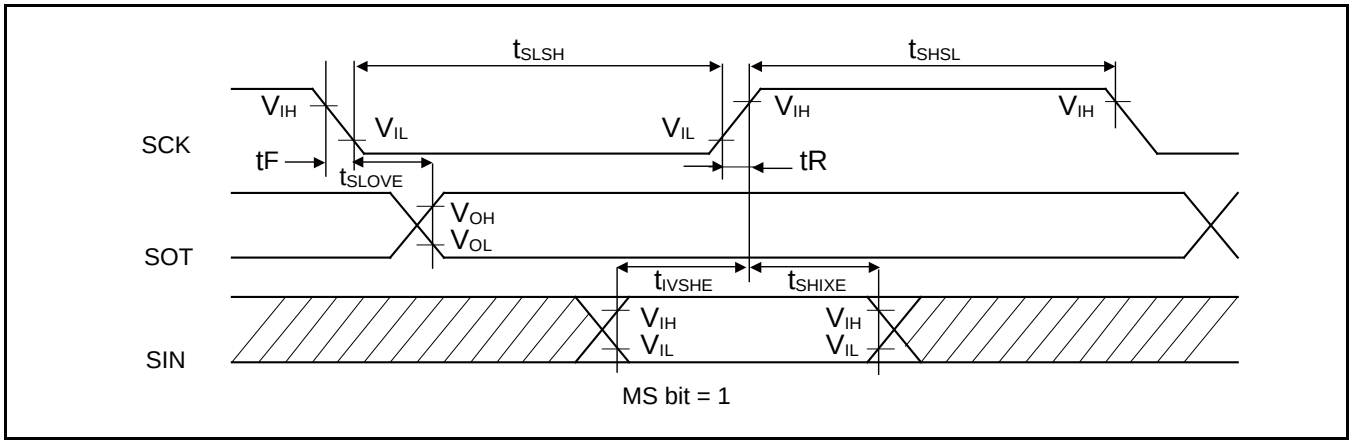
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

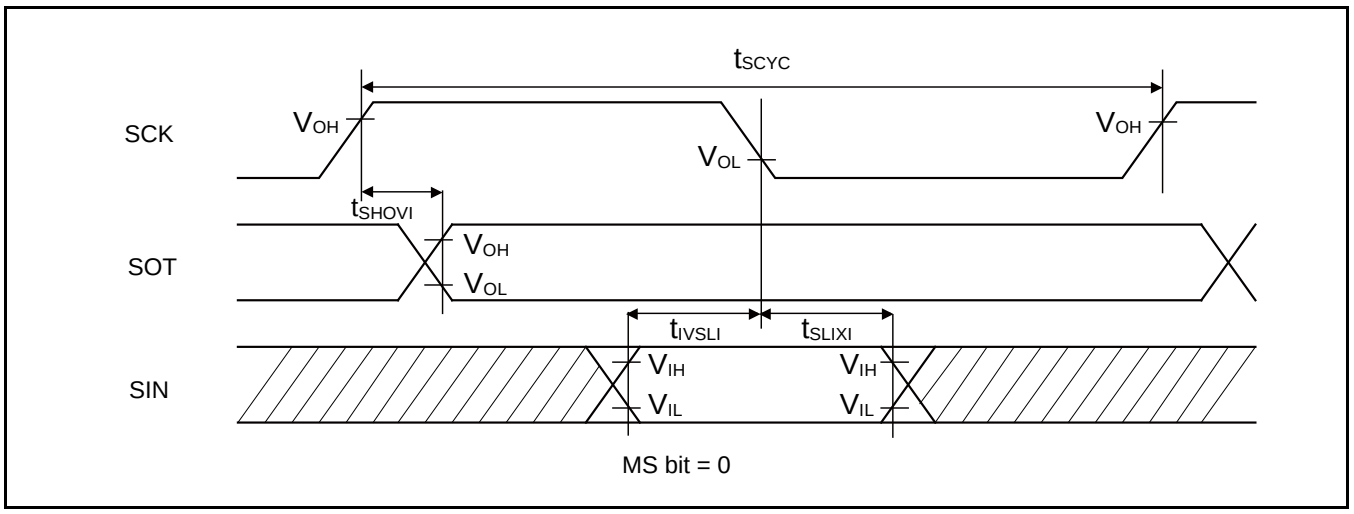
Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

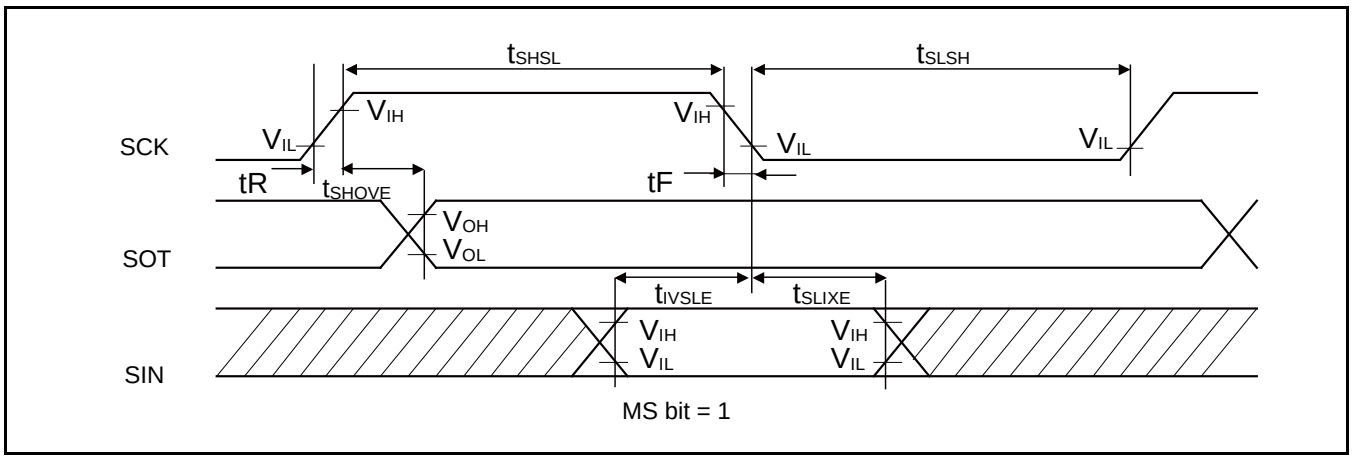
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

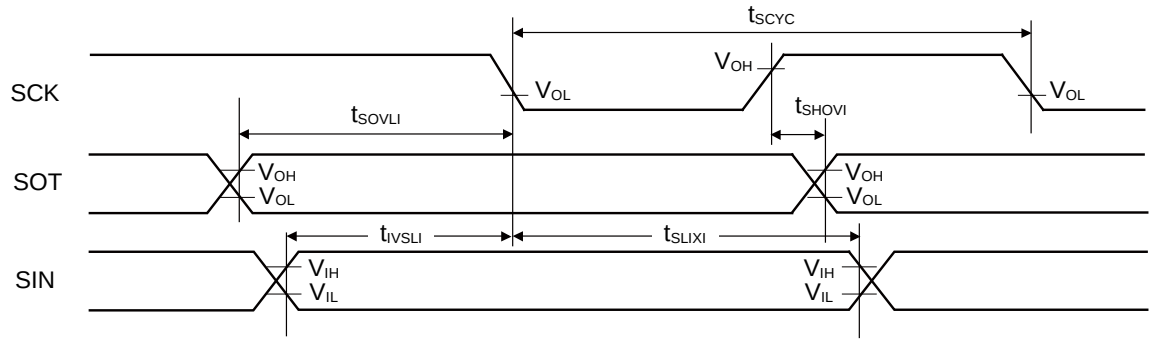
Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

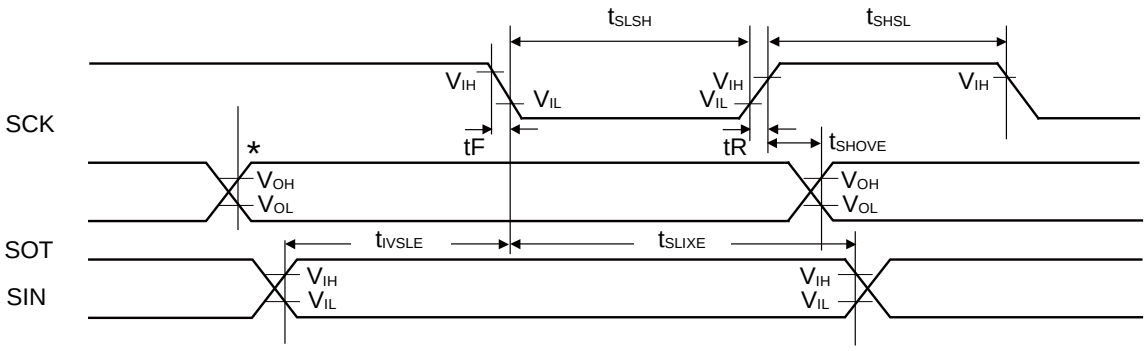
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

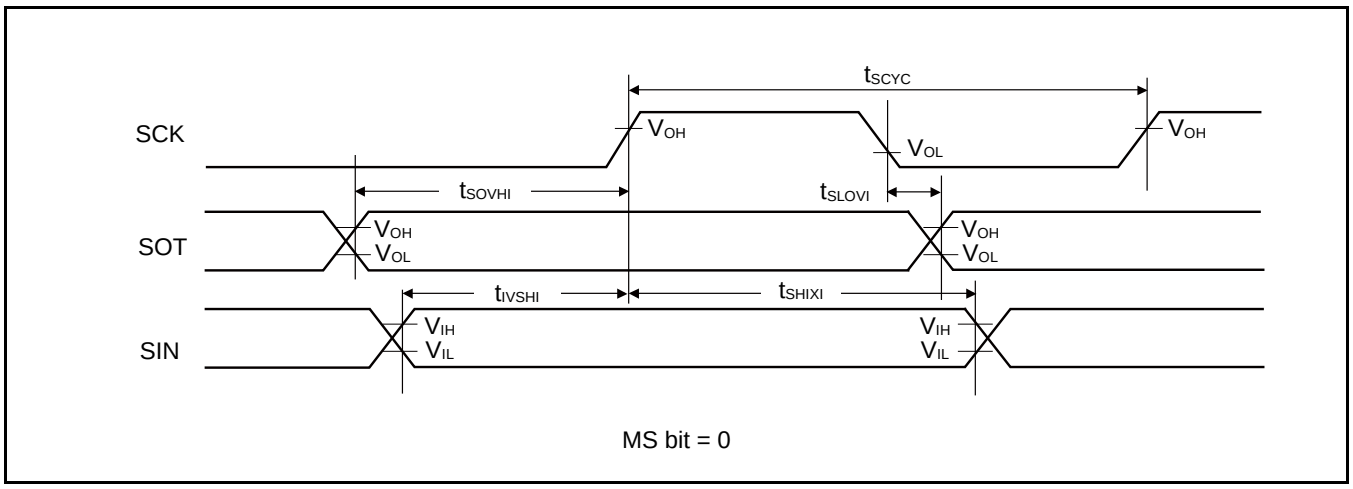
Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

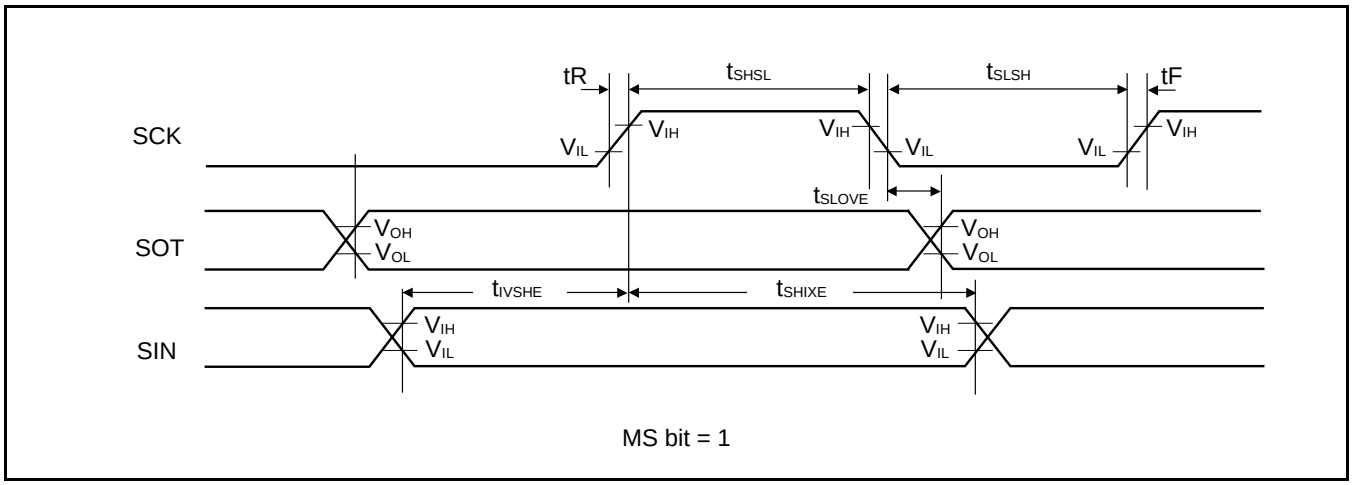
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2tC_{YCP}$ - 30	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the same relocate port number.*
  For example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

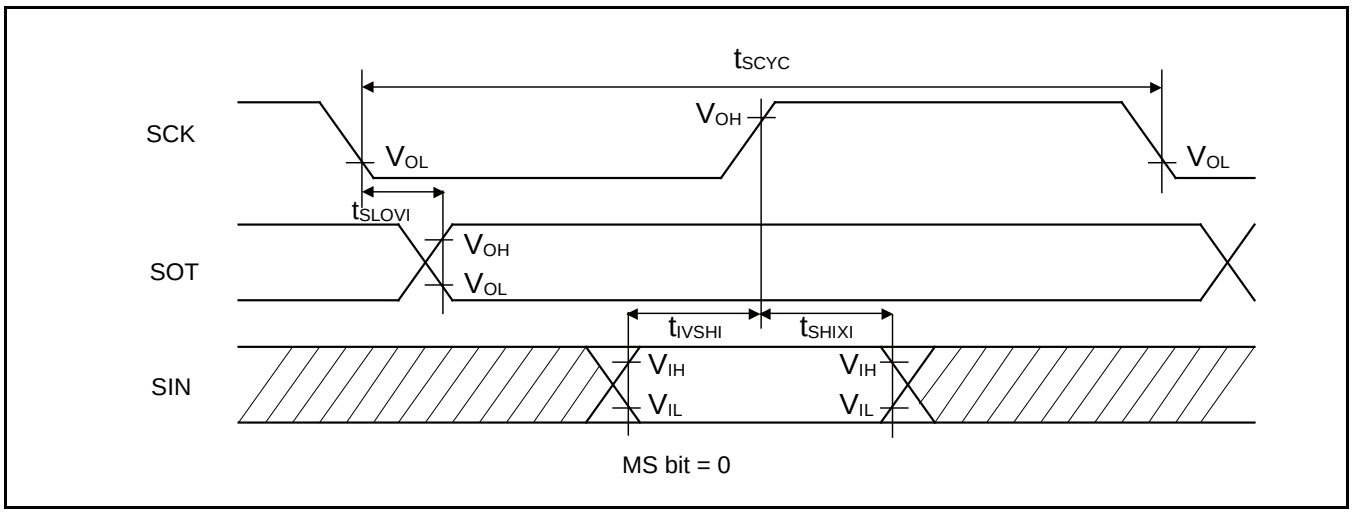
High-Speed Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

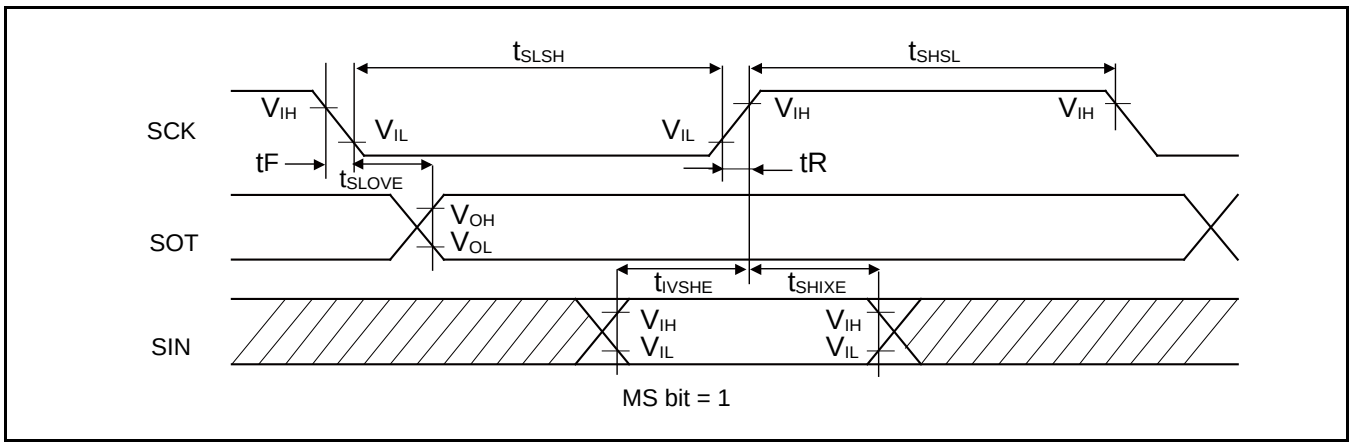
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5V		V_{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN0_1, SOT0_1, SCK0_1*
  - *Chip select: SIN6_0, SOT6_0, SCK6_0, SCS6_0*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

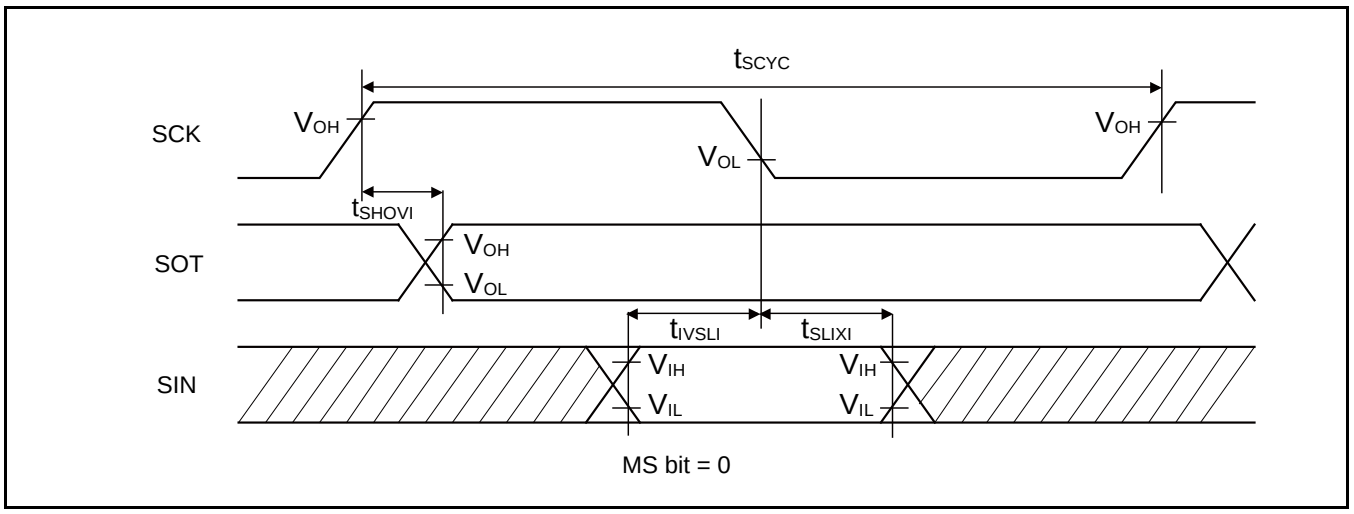
High-Speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

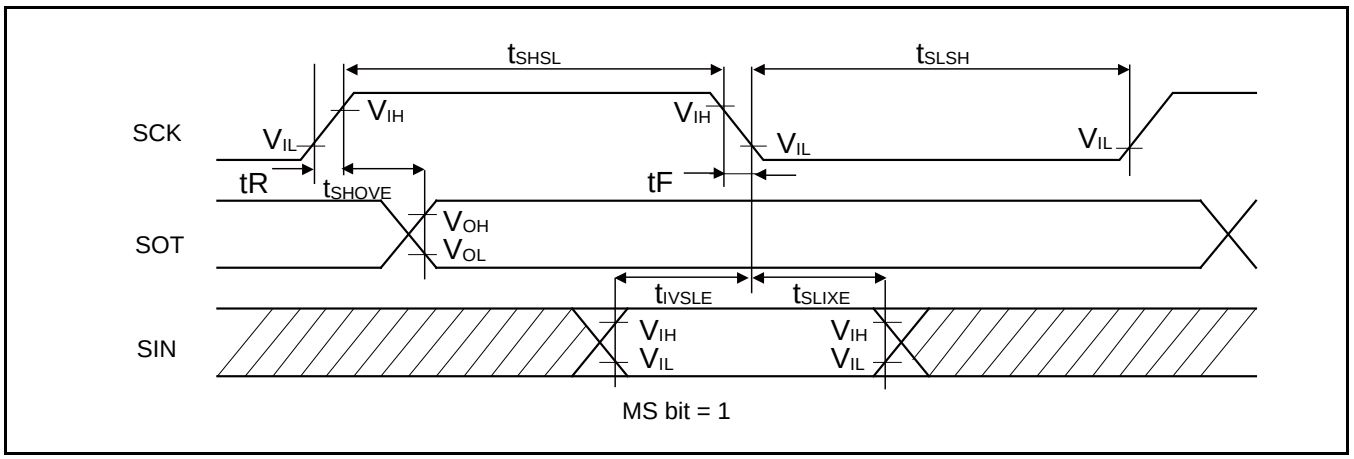
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↑ →SOT delay time	t_{SHOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK ↓ →SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↑ →SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK ↓ →SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN0_1, SOT0_1, SCK0_1*
  - *Chip select: SIN6_0, SOT6_0, SCK6_0, SCS6_0*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

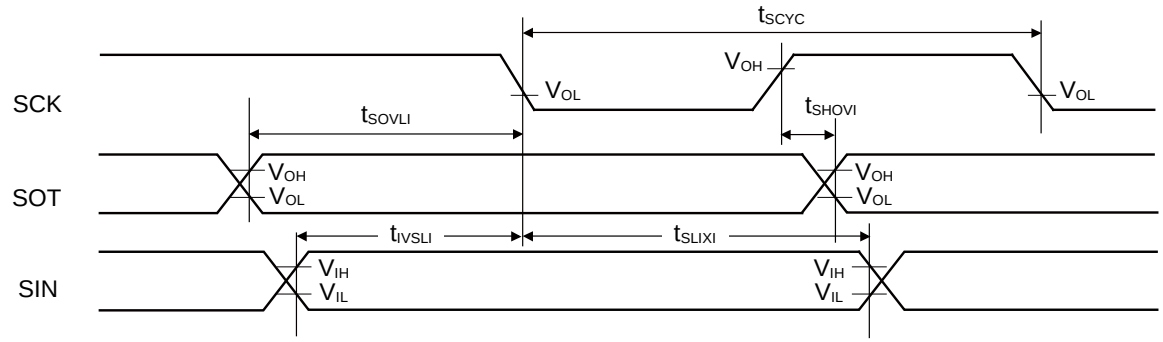
High-Speed Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

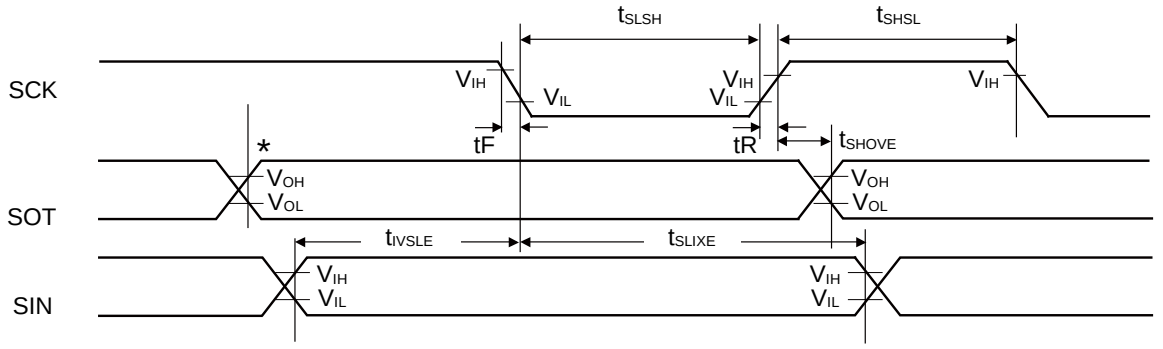
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ – 10	-	$2t_{CYCP}$ – 10	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN0_1, SOT0_1, SCK0_1*
  - *Chip select: SIN6_0, SOT6_0, SCK6_0, SCS6_0*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

*: Changes when writing to TDR register

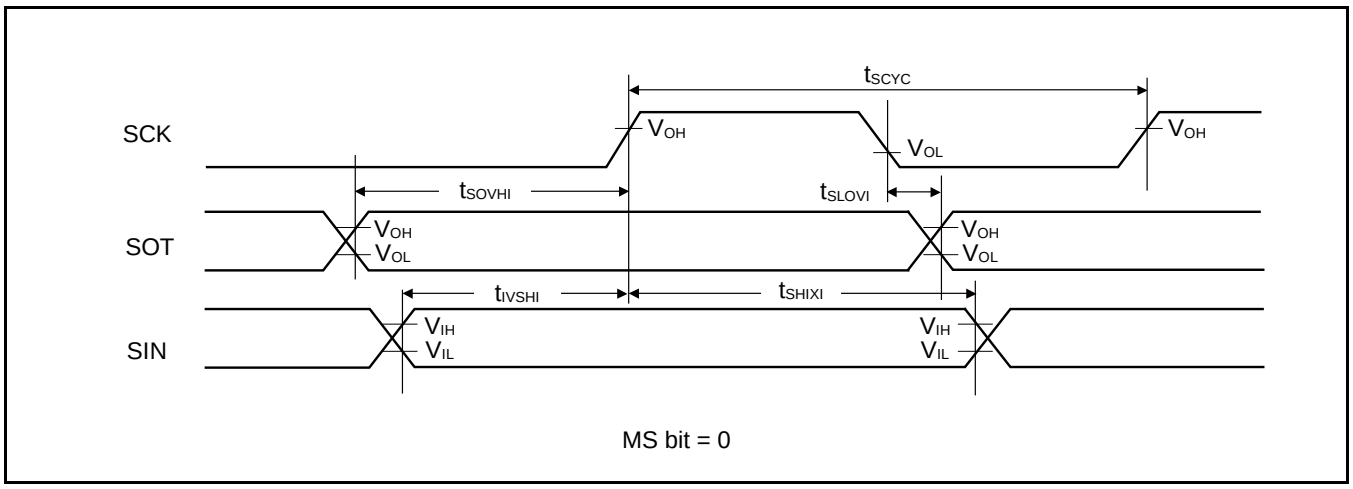
High-Speed Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

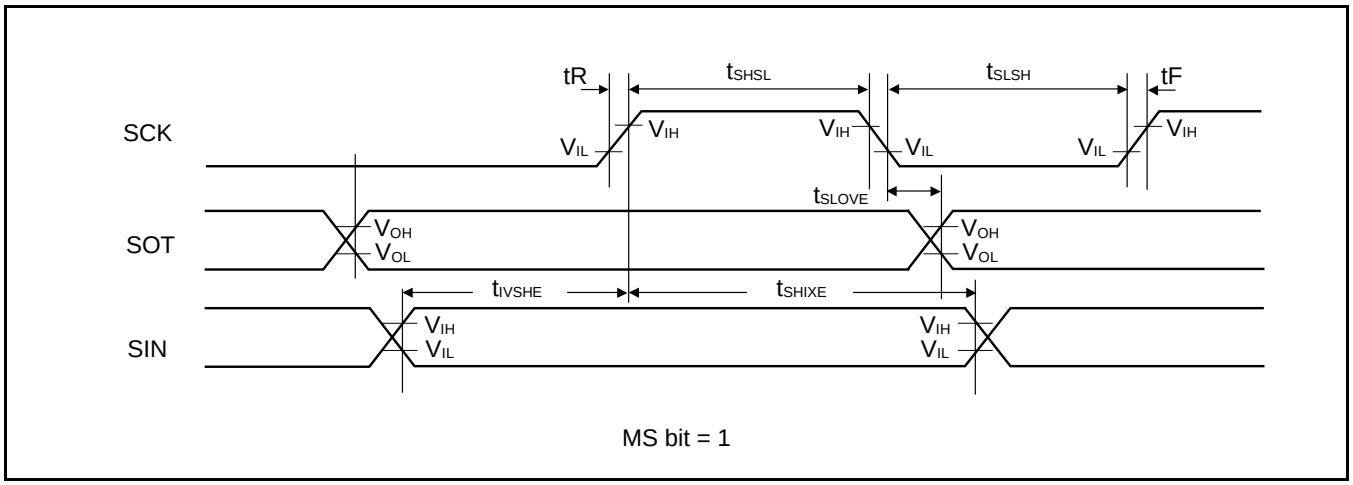
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Internal shift clock operation	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK ↓ →SOT delay time	t_{SLOVI}	SCKx, SOTx		-10	+10	-10	+10	ns
SIN→SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK ↑ →SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ – 10	-	$2t_{CYCP}$ – 10	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ – 5	-	$2t_{CYCP}$ – 5	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK ↓ →SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK ↑ →SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK falling time	tF	SCKx		-	5	-	5	ns
SCK rising time	tR	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *These characteristics only guarantee the following pins.*
  - *No chip select: SIN0_1, SOT0_1, SCK0_1*
  - *Chip select: SIN6_0, SOT6_0, SCK6_0, SCS6_0*
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL=1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	ns
SCS↓→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

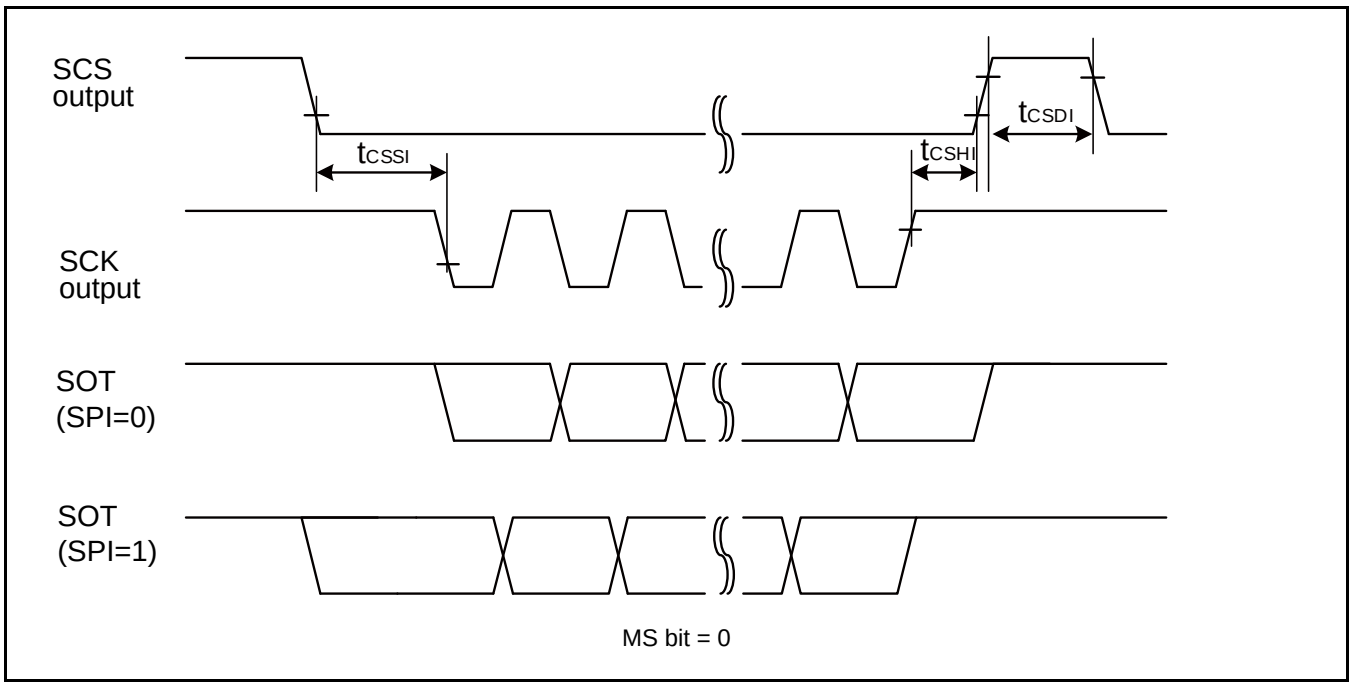
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

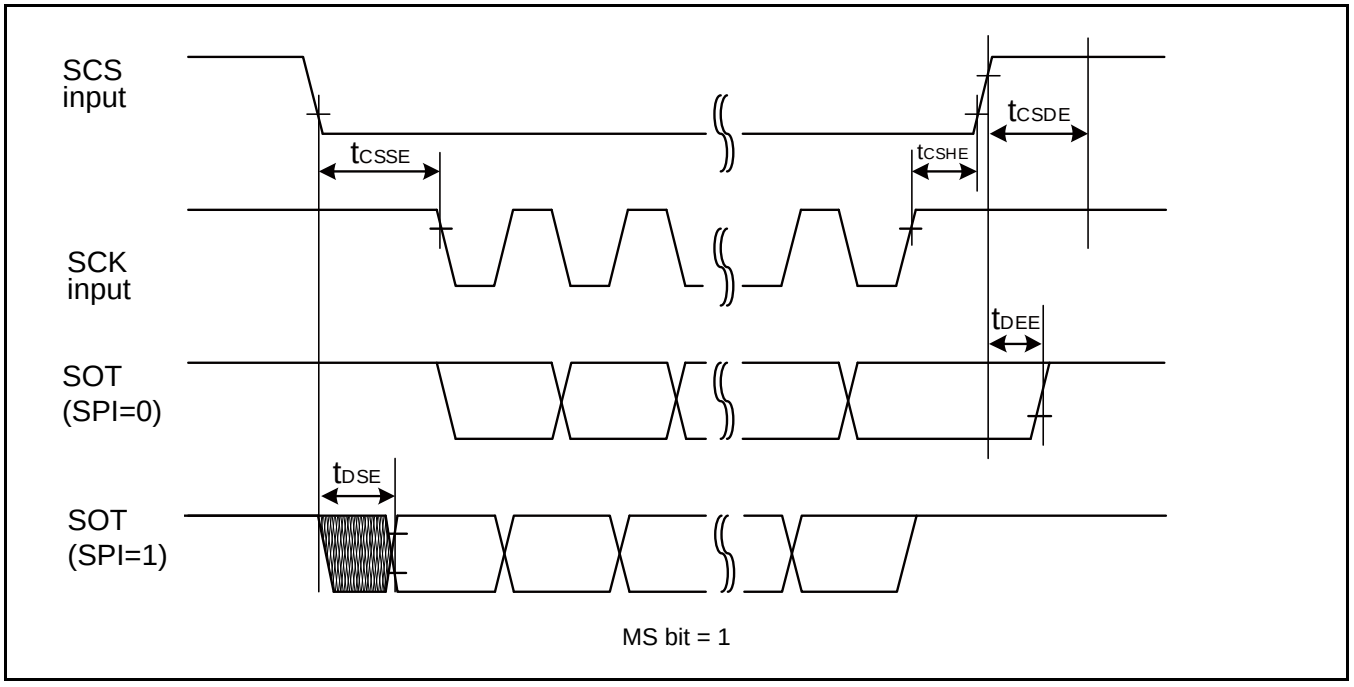
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual.*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL=1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↓→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	ns
SCS↓→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↓→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

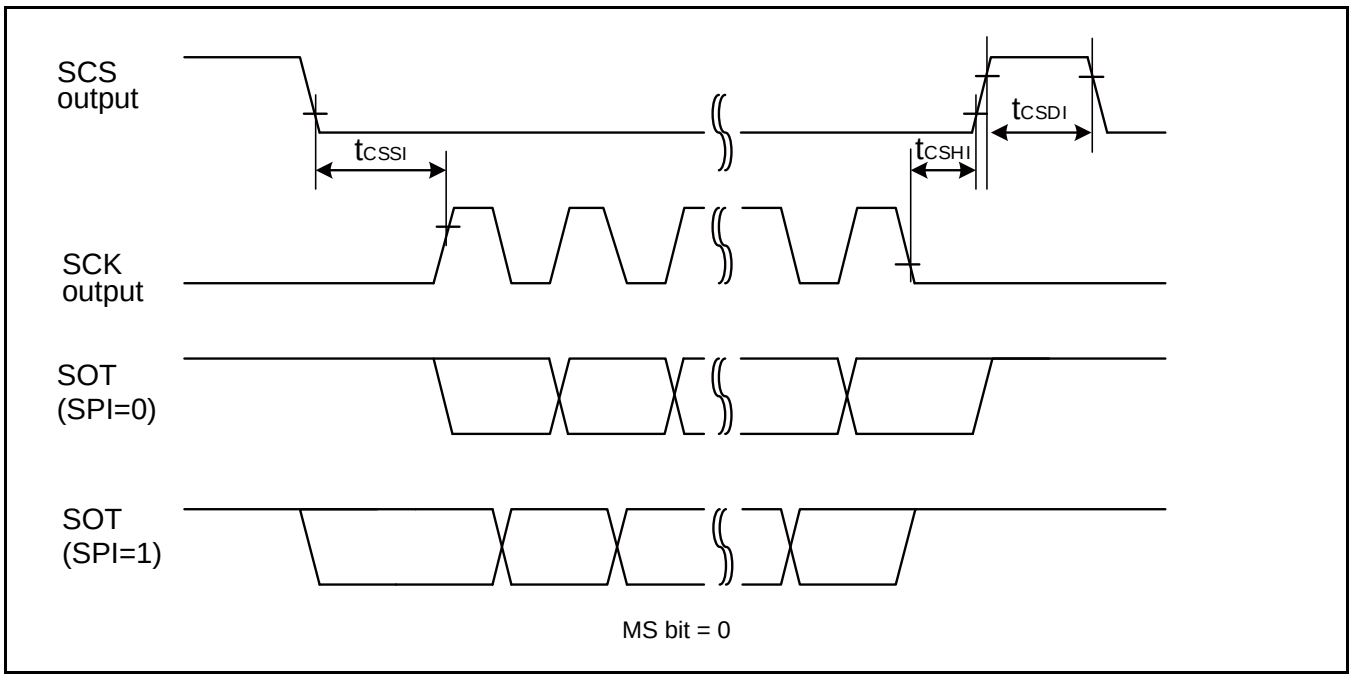
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

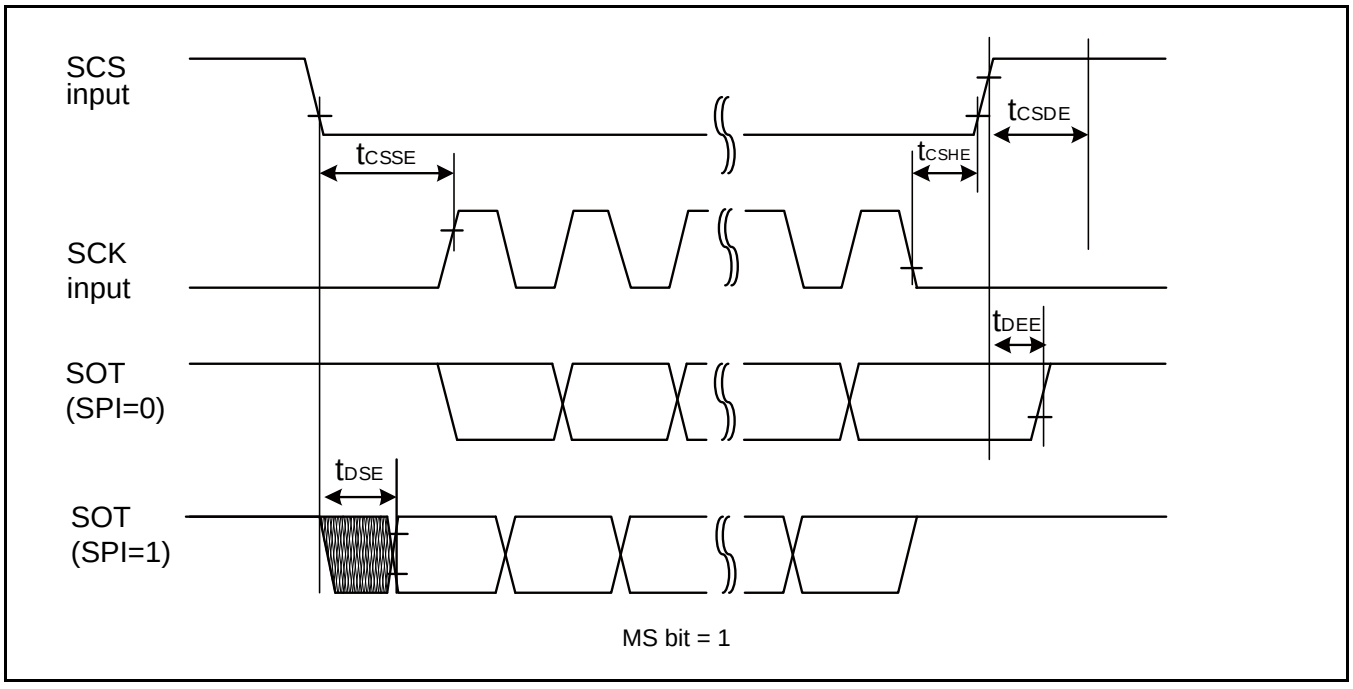
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	ns
SCS↑→SCK↓setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

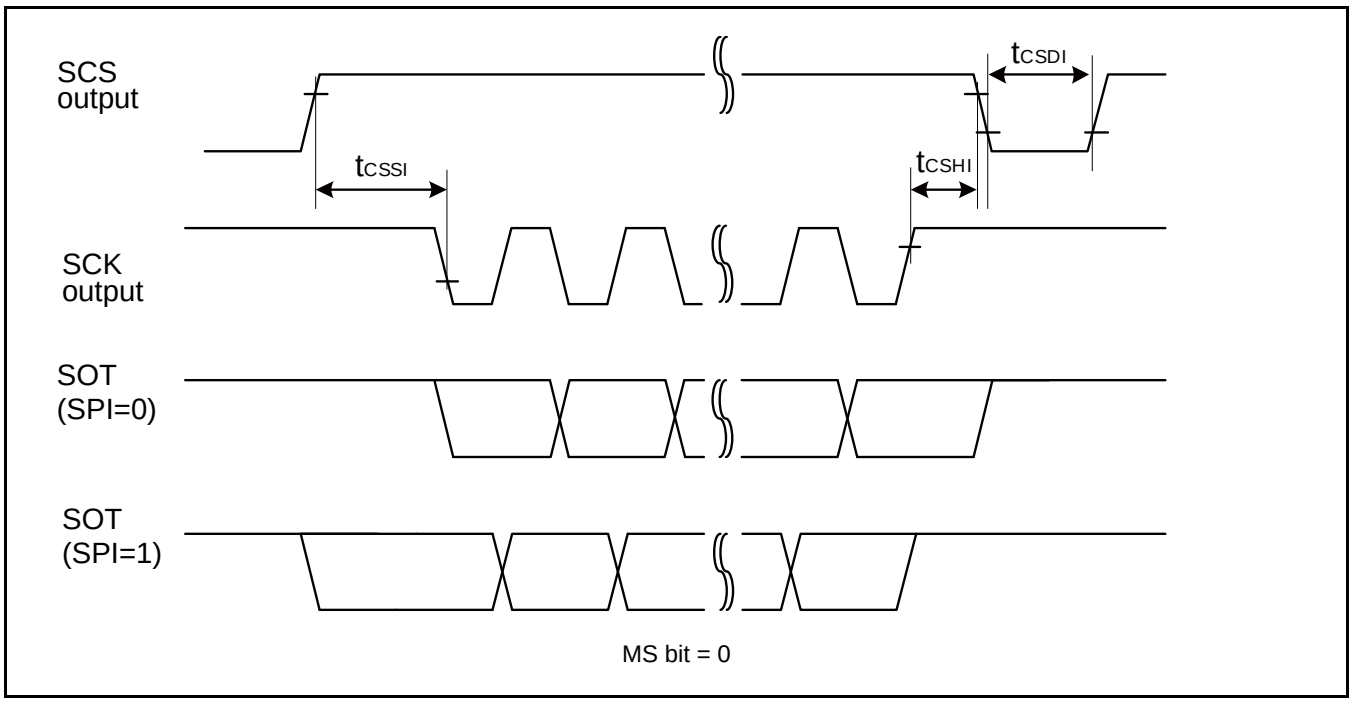
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

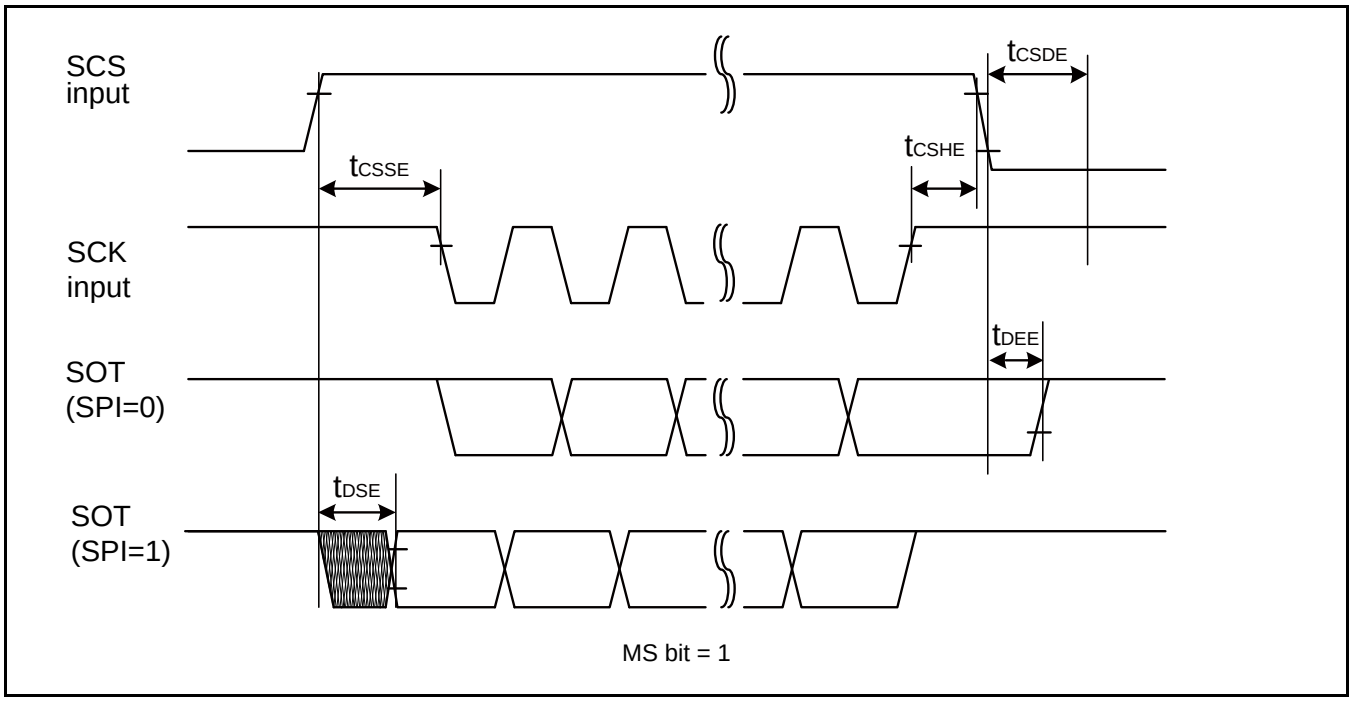
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL=0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↑setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↓→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	(*3)-20+5t_{CYCP}	(*3)+20+5t_{CYCP}	ns
SCS↑→SCK↑setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↓→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

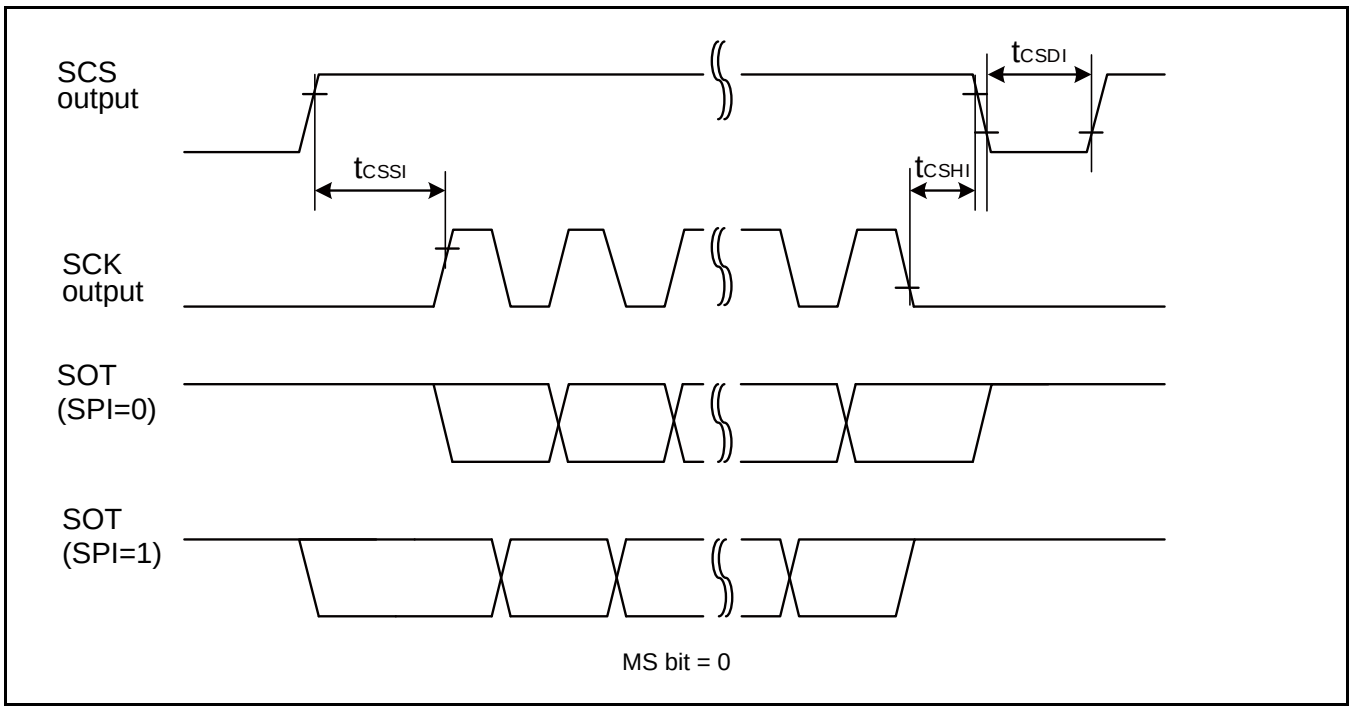
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

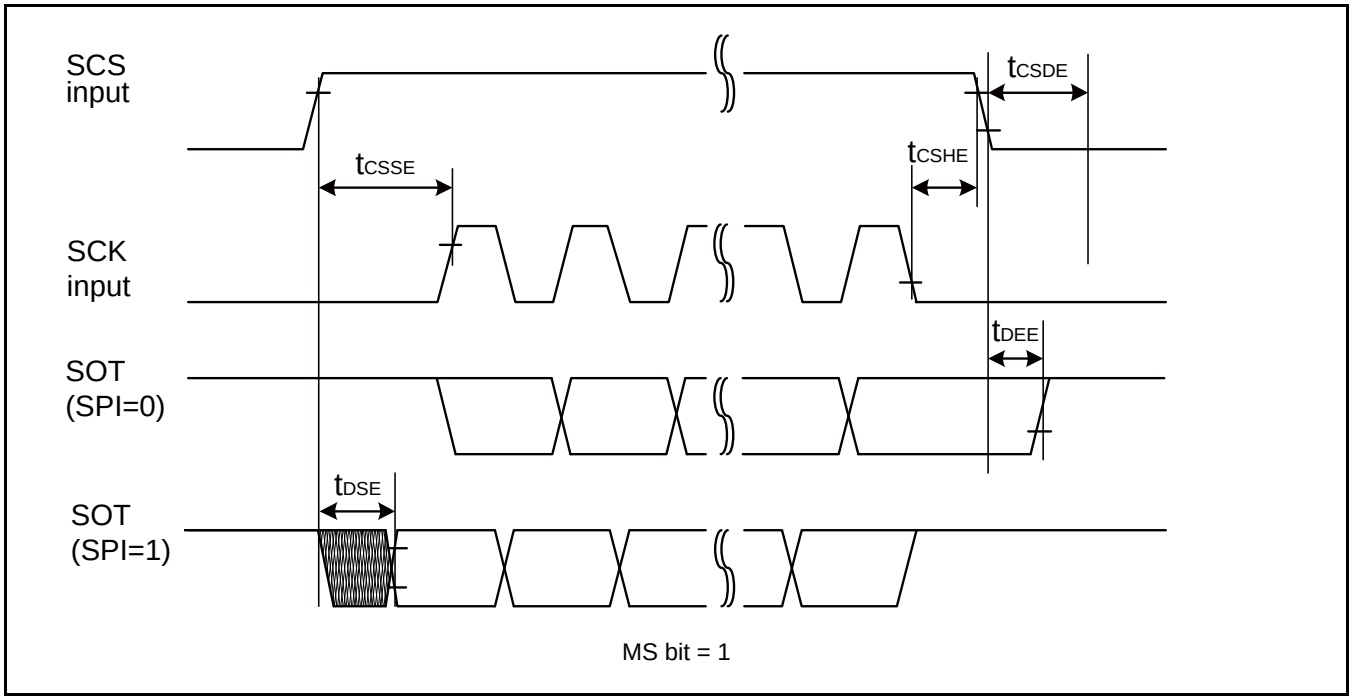
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time.*
  About the APB bus number which UART is connected to, see 8. Block Diagram in this data sheet.
- *About CSSU, CSHD, CSDS, serial chip select timing operating clock, see FM4 Family Peripheral Manual Main part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*



MS bit = 0

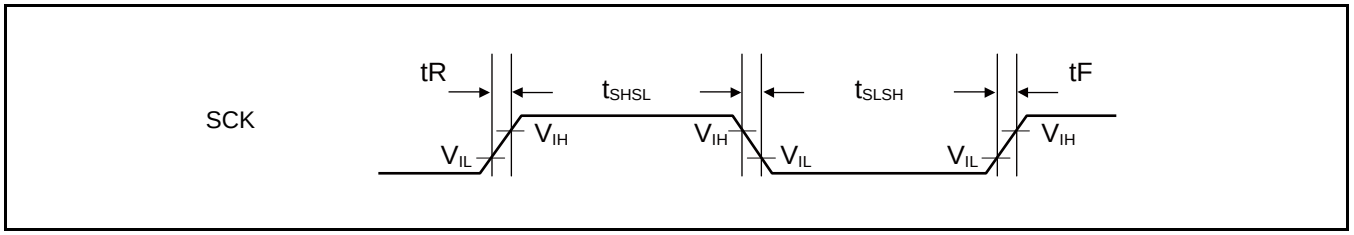


MS bit = 1

External Clock (EXT = 1): when in Asynchronous Mode Only

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min	Max		
Serial clock "L" pulse width	t_{SLSH}	C_L = 30 pF	t_{CYCP} + 10	-	ns	
Serial clock "H" pulse width	t_{SHSL}		t_{CYCP} + 10	-	ns	
SCK falling time	tF		-	5	ns	
SCK rising time	tR		-	5	ns	



12.4.12 External Input Timing

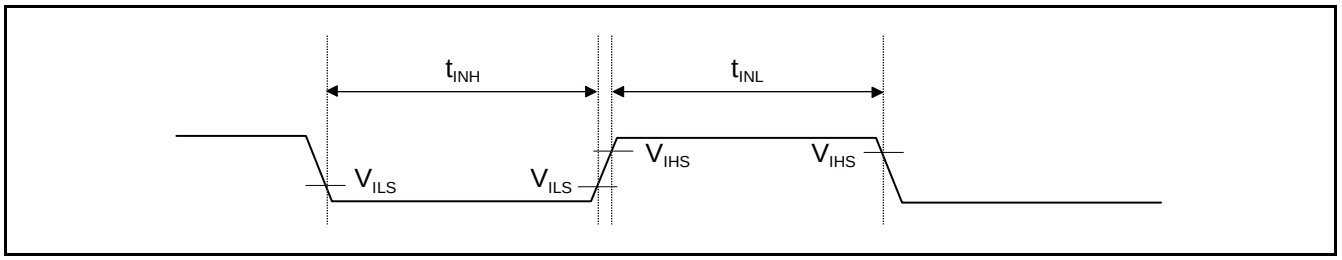
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTG	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INT00 to INT31, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	
		WKUPx	-	500*3	-	ns	Deep standby wake up

*1: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode.
About the APB bus number which the A/D converter, multi-function timer, external interrupt are connected to, see 8. Block Diagram in this data sheet.

*2: When in Stop mode, in timer mode.

*3: When in deep standby RTC mode, in Deep Standby Stop mode.

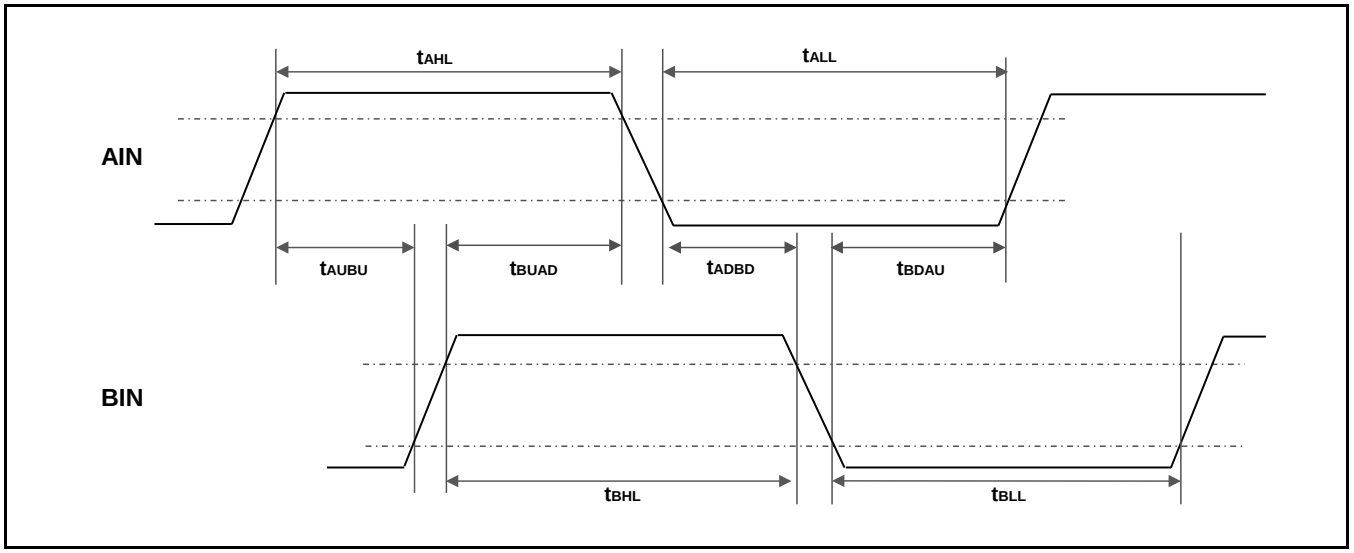


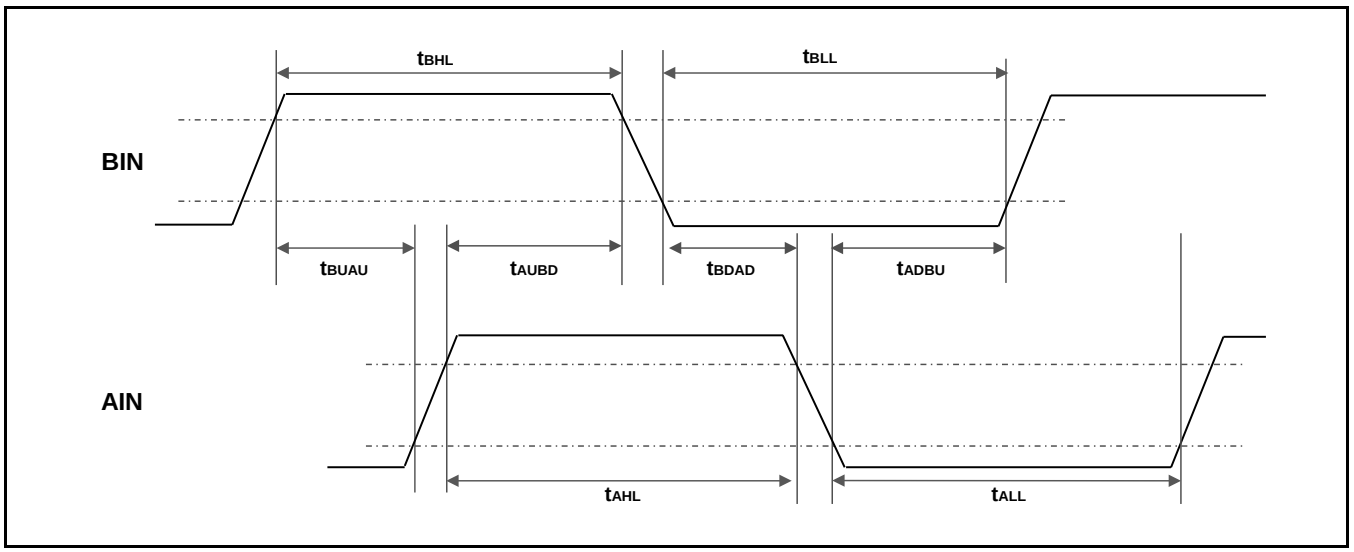
12.4.13 Quadrature Position/Revolution Counter Timing

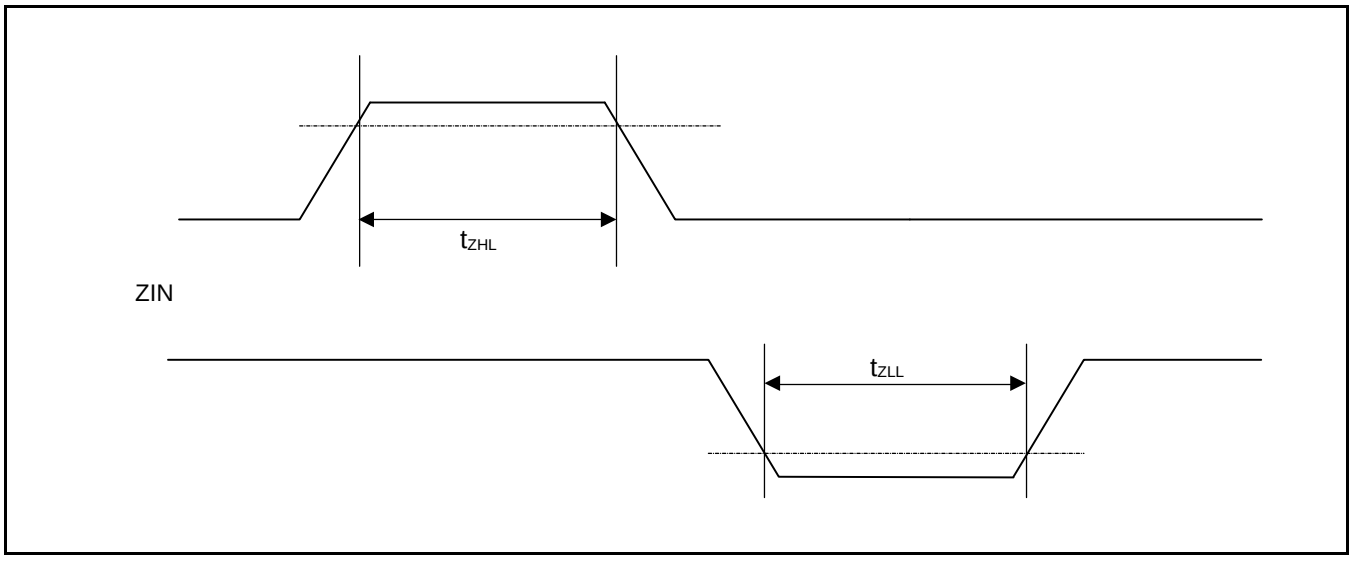
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

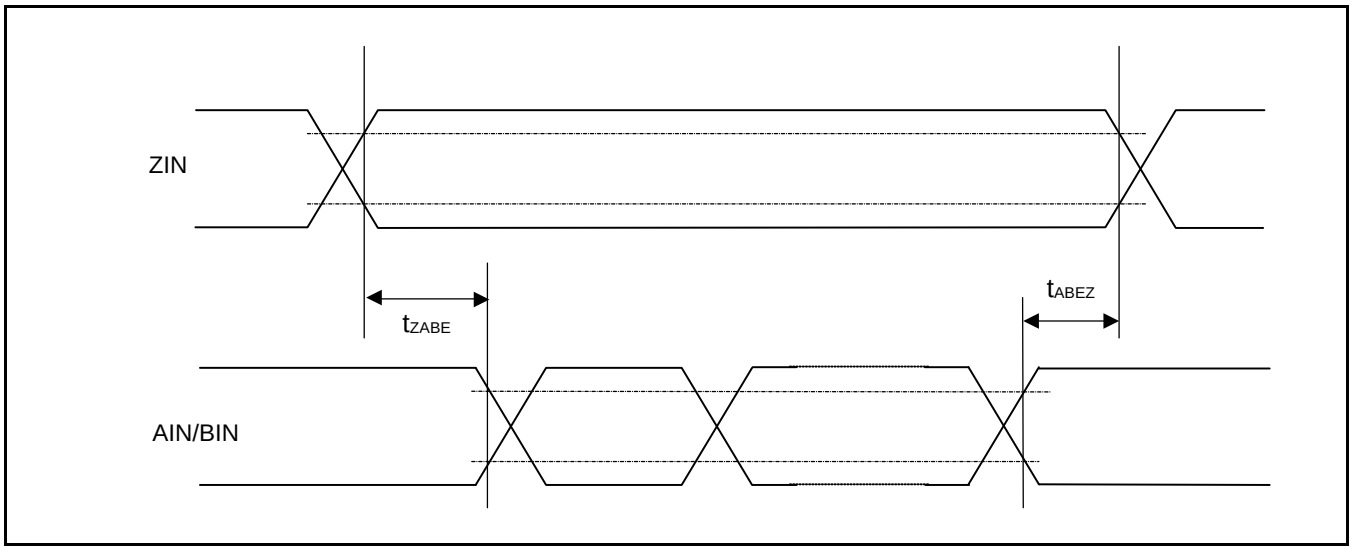
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}$*	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rising time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rising time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN falling time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN falling time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rising time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR:CGSC = 0			
ZIN pin L width	t_{ZLL}	QCR:CGSC = 0			
AIN/BIN rising and falling time from determined ZIN level	t_{ZABE}	QCR:CGSC = 1			
Determined ZIN level from AIN/BIN rising and falling time	t_{ABEZ}	QCR:CGSC = 1			

*: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in timer mode.
About the APB bus number which Quadrature Position/Revolution Counter is connected to, see 8. Block Diagram in this data sheet.




tBHL
tBLL
BIN
tBUAU
tAUBD
tBDAD
tADBU
AIN
tAHL
tALL


tZHL
ZIN
tZLL


ZIN
tZABE
tABEZ
AIN/BIN

12.4.14 I^2C Timing

Standard-Mode, Fast-Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Standard-Mode		Fast-Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30 pF, R = (V_p/I_{OL})*1	0	100	0	400	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs	
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs	
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs	
(Repeated) START condition setup time SCL ↑ → SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		4.7	-	1.3	-	µs	
Noise filter	t_{SP}	2 MHz ≤ t_{CYCP}<40 MHz	$2t_{CYCP}$*4	-	$2t_{CYCP}$*4	-	ns	*5
		40 MHz ≤ t_{CYCP}<60 MHz	$4t_{CYCP}$*4	-	$4t_{CYCP}$*4	-	ns	
		60 MHz ≤ t_{CYCP}<80 MHz	$6t_{CYCP}$*4	-	$6t_{CYCP}$*4	-	ns	
		80 MHz ≤ t_{CYCP}<100 MHz	$8t_{CYCP}$*4	-	$8t_{CYCP}$*4	-	ns	
		100 MHz ≤ t_{CYCP}<120 MHz	$10t_{CYCP}$*4	-	$10t_{CYCP}$*4	-	ns	
		120 MHz ≤ t_{CYCP}<140 MHz	$12t_{CYCP}$*4	-	$12t_{CYCP}$*4	-	ns	
		140 MHz ≤ t_{CYCP}<160 MHz	$14t_{CYCP}$*4	-	$14t_{CYCP}$*4	-	ns	
		160 MHz ≤ t_{CYCP}<180 MHz	$16t_{CYCP}$*4	-	$16t_{CYCP}$*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum $t_{HDDA}T$ must satisfy that it does not extend at least "L" period (t_{LOW}) of device's SCL signal.

*3: A Fast-mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of t_{SUDAT} ≥ 250 ns.

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see "8. Block Diagram" in this data sheet.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

Fast Mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast Mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	F_{SCL}	C_L = 30 pF, R = (Vp/I_{OL})*1	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock "L" width	t_{LOW}		0.5	-	µs	
SCL clock "H" width	t_{HIGH}		0.26	-	µs	
SCL clock frequency	t_{SUSTA}		0.26	-	µs	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between "STOP condition" and "START condition"	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60 MHz ≤ t_{CYCP}<80 MHz	6 t_{CYCP}*4	-	ns	*5
		80 MHz ≤ t_{CYCP}<100 MHz	8 t_{CYCP}*4	-	ns	
		100 MHz ≤ t_{CYCP}<120 MHz	10 t_{CYCP}*4	-	ns	
		120 MHz ≤ t_{CYCP}<140 MHz	12 t_{CYCP}*4	-	ns	
		140 MHz ≤ t_{CYCP}<160 MHz	14 t_{CYCP}*4	-	ns	
		160 MHz ≤ t_{CYCP}<180 MHz	16 t_{CYCP}*4	-	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

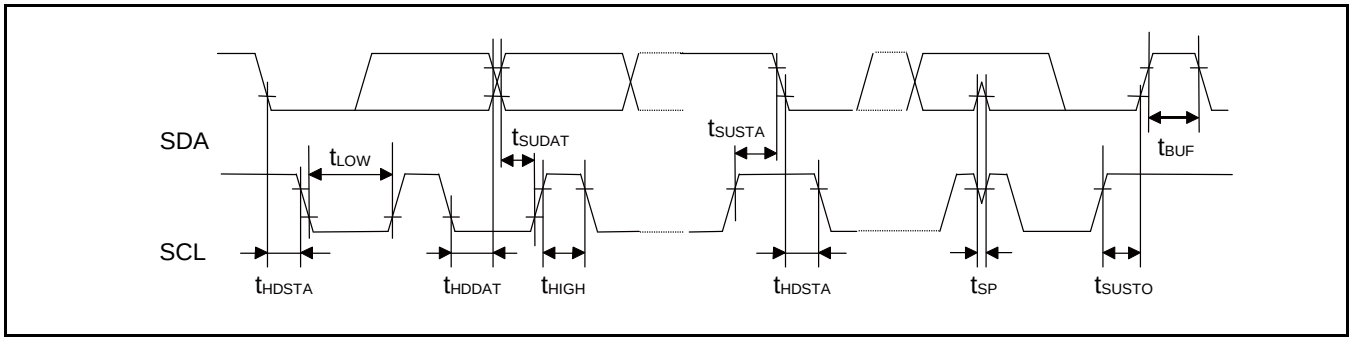
*2: The maximum t_{HDDAT} must satisfy that it does not extend at least L period (t_{LOW}) of device's SCL signal.

*3: A Fast-mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CYCP} is the APB bus clock cycle time.
About the APB bus number that I^2C is connected to, see 8. Block Diagram in this data sheet.
To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.

*5: The noise filter time can be changed by register settings.
Change the number of the noise filter steps according to APB bus clock frequency.

*6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register. See CHAPTER 12: I/O Port in FM4 Family Peripheral Manual Main part (002-04856) for the details.



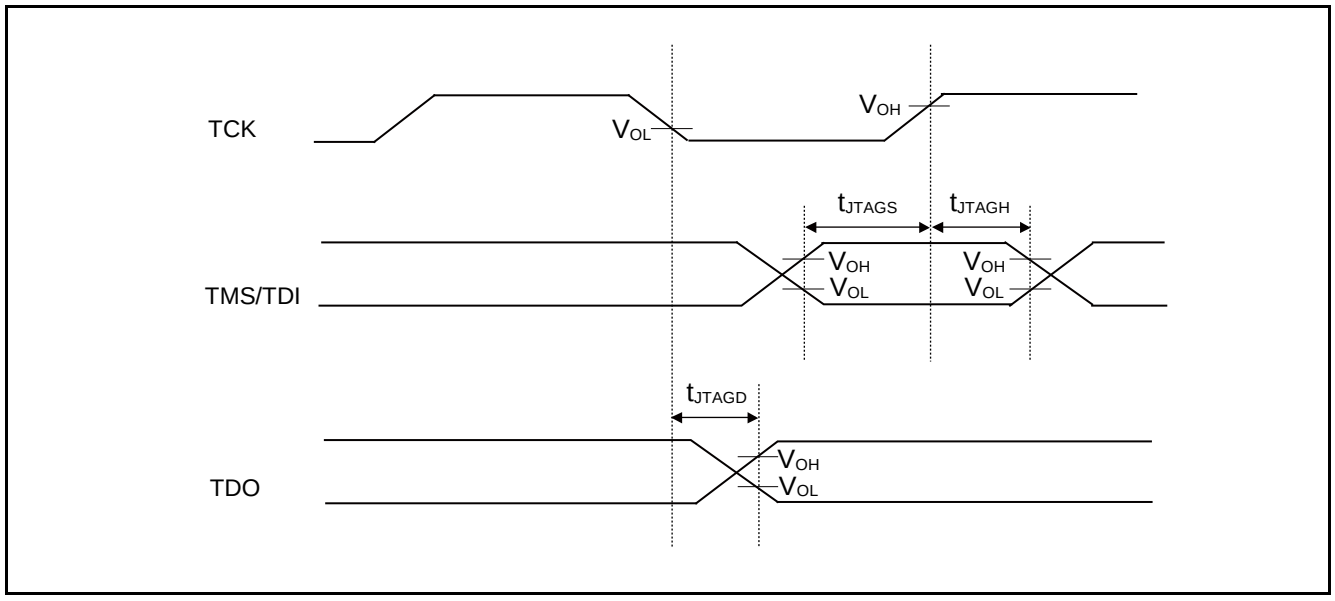
12.4.15 JTAG Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAGS}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TMS, TDI hold time	t_{JTAGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5$ V	15	-	ns	
			$V_{CC} < 4.5$ V				
TDO delay time	t_{JTAGD}	TCK, TDO	$V_{CC} \geq 4.5$ V	-	25	ns	
			$V_{CC} < 4.5$ V	-	45		

Note:

- *When the external load capacitance C_L= 30 pF.*



12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

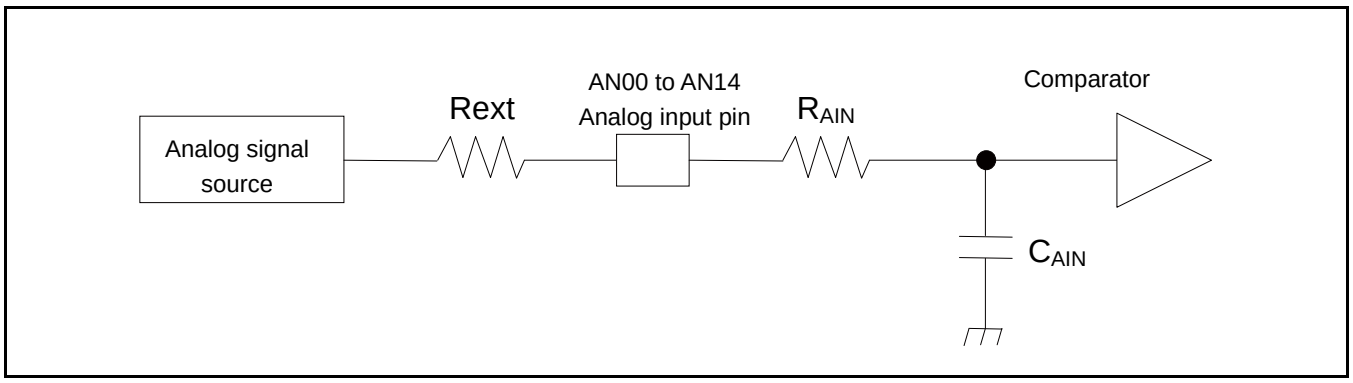
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	-4.5	-	+4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential Nonlinearity	-	-	-2.5	-	+2.5	LSB	
Zero transition voltage	V_{ZT}	AN00 to AN14	-15	-	+15	mV	
Full-scale transition voltage	V_{FST}	AN00 to AN14	AVRH - 15	-	AVRH + 15	mV	
Conversion time	-	-	0.5*1	-	-	µs	AV_{CC} ≥ 4.5V
Sampling time	Ts	-	*2	-	10	µs	AV_{CC} ≥ 4.5V
			*2	-			AV_{CC} < 4.5V
Compare clock cycle*3	Tcck	-	25	-	1000	ns	AV_{CC} ≥ 4.5V
			50	-	1000		AV_{CC} < 4.5V
State transition time to operation permission	Tstt	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	0.3	12	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1unit operation AVRH=5.5 V
				0.2	4.2	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	10	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	AN00 to AN14	-	-	5	µA	
Analog input voltage	-	AN00 to AN14	AV_{SS}	-	AVRH	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck < 50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns

*1: The conversion time is the value of sampling time (Ts) + compare time (Tc).
The condition of the minimum conversion time is when the value of sampling time: 150 ns, the value of compare time: 350 ns (AV_{CC} ≥ 4.5 V). Ensure that it satisfies the value of sampling time (Ts) and compare clock cycle (Tcck). For setting*4 of sampling time and compare clock cycle, see CHAPTER 1-1: A/D Converter in FM4 Family Peripheral Manual Analog macro part (002-04860). The register setting of the A/D Converter is reflected by the peripheral clock timing. The sampling and compare clock are set at Base clock (HCLK).

*2: A necessary sampling time changes by external impedance. Ensure that it set the sampling time to satisfy (Equation 1).

*3: The compare time (Tc) is the value of (Equation 2).

*4: The register setting of the A/D Converter is reflected by the timing of the APB bus clock. The sampling clock and compare clock are set in base clock (HCLK). About the APB bus number which the A/D Converter is connected to, see 8. Block Diagram in this data sheet.



(Equation 1) $Ts \geq (R_{AIN} + Rext) \times C_{AIN} \times 9$

Ts: Sampling time

R_{AIN}: Input resistance of A/D = 1.2 kΩ at 4.5 V < AV_{CC} < 5.5 V
Input resistance of A/D = 1.8 kΩ at 2.7 V < AV_{CC} < 4.5 V

C_{AIN}: Input capacity of A/D = 10 pF at 2.7 V < AV_{CC} < 5.5 V

Rext: Output impedance of external circuit

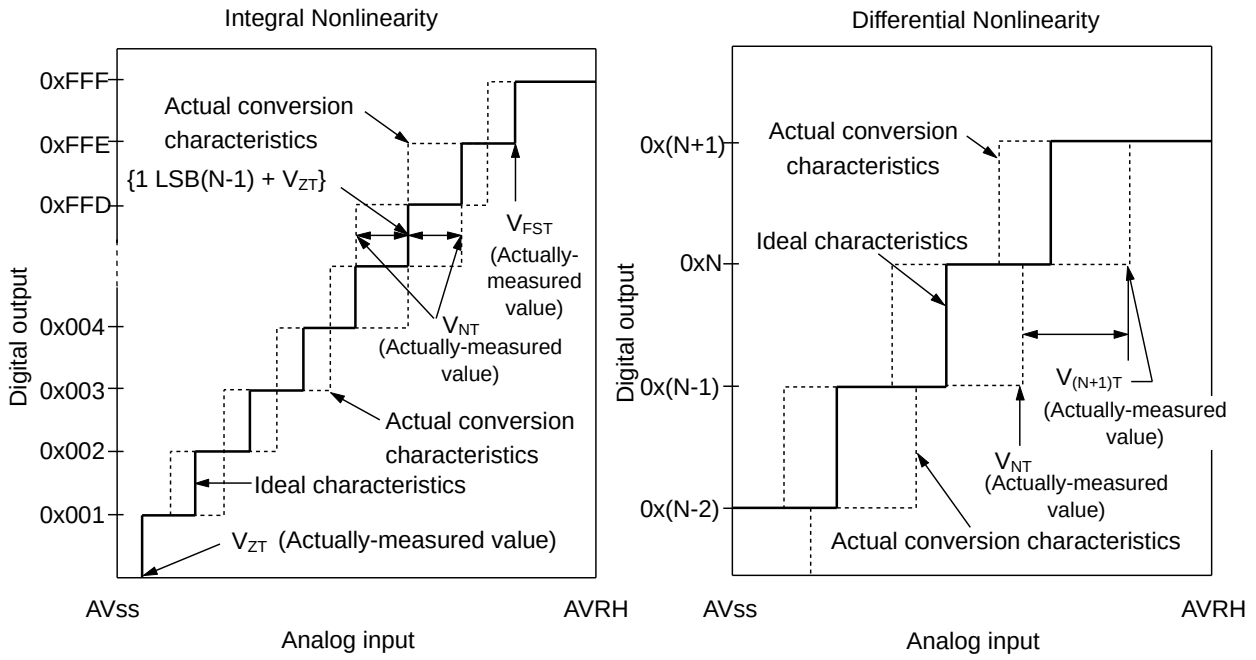
(Equation 2) $Tc = Tcck \times 14$

Tc: Compare time

Tcck: Compare clock cycle

Definition of 12-bit A/D Converter Terms

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)}T - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.

V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.

V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.

V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

12.6 12-bit D/A Converter

Electrical Characteristics for the D/A Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	12	bit	
Conversion time	tc20		0.56	0.69	0.81	µs	Load 20pF
	tc100		2.79	3.42	4.06	µs	Load 100pF
Integral Nonlinearity*	INL		-16	-	+16	LSB	
Differential Nonlinearity*	DNL		-0.98	-	+1.5	LSB	
Output voltage offset	V_{OFF}		-	-	10.0	mV	When setting 0x000
			-20.0	-	+1.4	mV	When setting 0xFFF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	When D/A stop
Power supply current*	IDDA	AVCC	260	330	410	µA	D/A 1unit operation AV_{CC}=3.3 V
			400	519	620	µA	D/A 1unit operation AV_{CC}=5.0 V
	IDSA		-	-	14	µA	When D/A stop

*: During no load

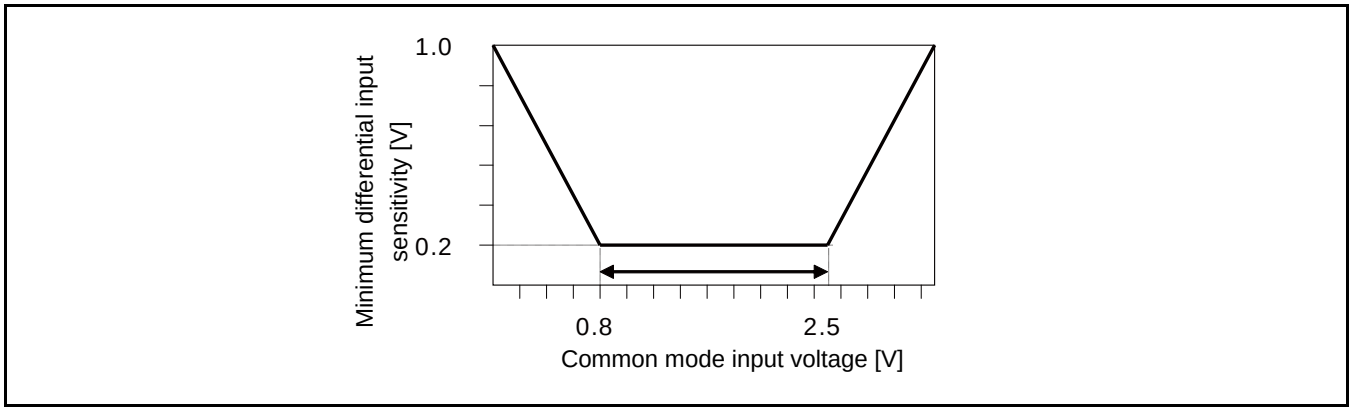
12.7 USB Characteristics

(V_{CC} = 2.7V to 5.5V, $USBV_{CC}$ = 3.0V to 3.6V, V_{SS} = 0V)

Parameter		Symbol	Pin Name	Conditions	Value		Unit	Remarks
					Min	Max		
Input character -istics	Input H level voltage	V_{IH}	UDP0,UDM0	-	2.0	$USBV_{CC}$ + 0.3	V	*1
	Input L level voltage	V_{IL}		-	V_{SS} - 0.3	0.8	V	*1
	Differential input sensitivity	V_{DI}		-	0.2	-	V	*2
	Different common mode range	V_{CM}		-	0.8	2.5	V	*2
Output character -istics	Output "H" level voltage	V_{OH}		External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output "L" level voltage	V_{OL}		External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V_{CRS}		-	1.3	2.0	V	*4
	Rising time	t_{FR}		Full-Speed	4	20	ns	*5
	Falling time	t_{FF}		Full-Speed	4	20	ns	*5
	Rising/falling time matching	t_{FRFM}		Full-Speed	90	111.11	%	*5
	Output impedance	Z_{DRV}		Full-Speed	28	44	Ω	*6
	Rising time	t_{LR}		Low-Speed	75	300	ns	*7
	Falling time	t_{LF}		Low-Speed	75	300	ns	*7
	Rising/falling time matching	t_{LRFM}		Low-Speed	80	125	%	*7

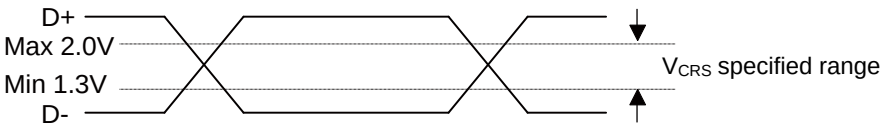
*1: The switching threshold voltage of Single-End-Receiver of USB I/O buffer is set as within V_{IL} (Max) = 0.8 V, V_{IH} (Min) = 2.0 V (TTL input standard).
There are some hysteresises to lower noise sensitivity.

*2: Use differential-Receiver to receive USB differential data signal.
Differential-Receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.
Above voltage range is the common mode input voltage range.

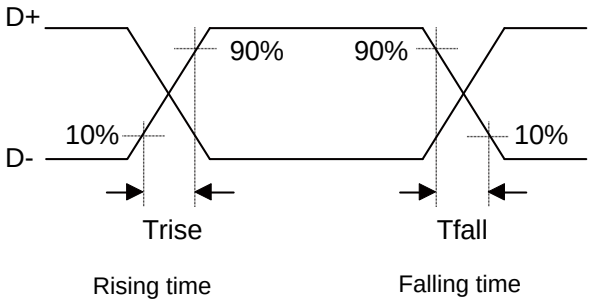


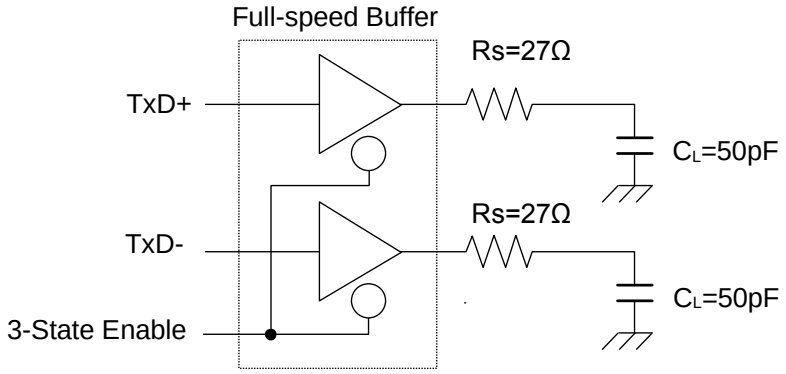
*3: The output drive capability of the driver is below 0.3 V at Low-State (V_{OL}) (to 3.6 V and 1.5 kΩ load), and 2.8 V or above (to the V_{SS} and 1.5 kΩ load) at High-State (V_{OH}).

*4: The cross voltage of the external differential output signal (D + /D −) of USB I/O buffer is within 1.3 V to 2.0 V.

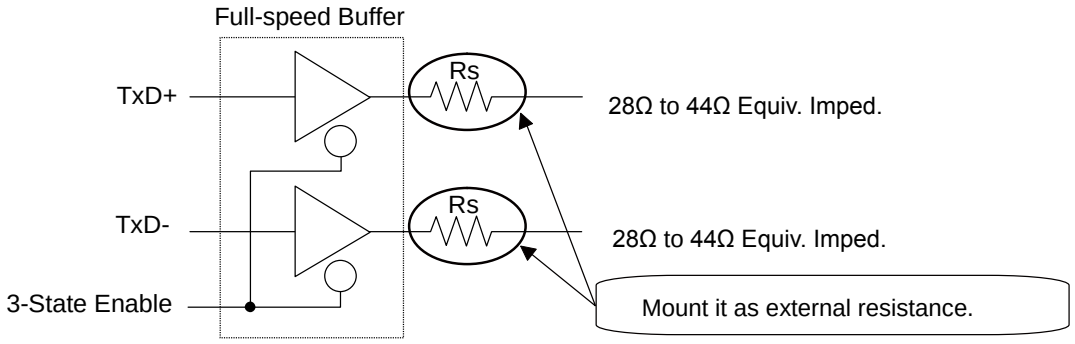


*5: They indicate rising time (Trise) and falling time (Tfall) of the full-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.
For full-speed buffer, Tr/Tf ratio is regulated as within ± 10% to minimize RFI emission.





*6: USB Full-speed connection is performed via twist pair cable shield with 90 Ω ± 15% characteristic impedance (Differential Mode). USB standard defines that output impedance of USB driver must be in range from 28 Ω to 44 Ω. So, discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommendation value 27 Ω) Series resistor Rs.

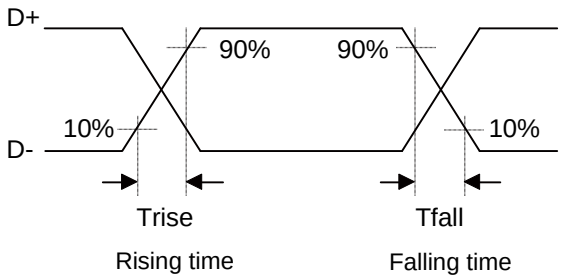


Rs series resistor 25 Ω to 30 Ω

Series resistor of 27 Ω (recommendation value) must be added.

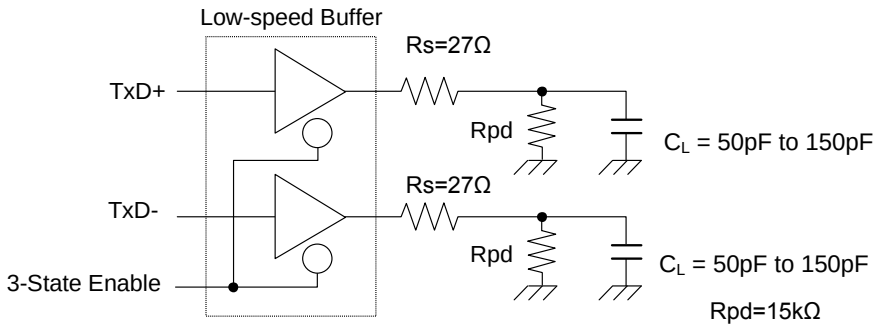
And, use "resistance with an uncertainty of 5% by E24 sequence".

*7: They indicate rising time (Trise) and falling time (Tfall) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.

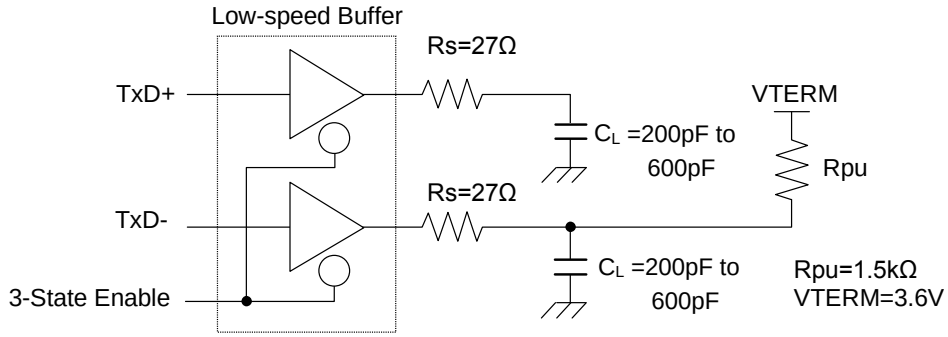


See Low-Speed Load (Compliance Load) for conditions of external load.

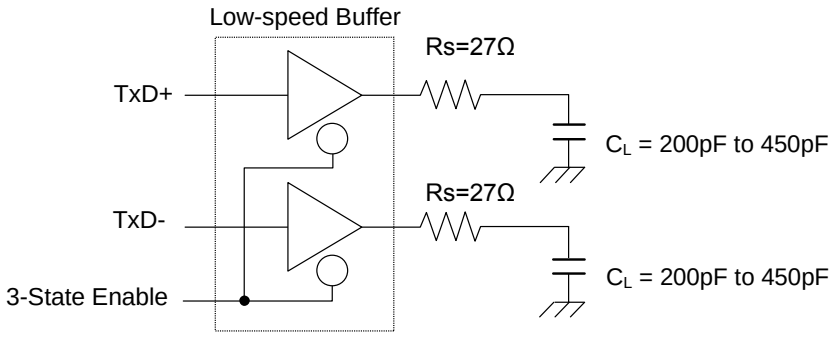
Low-Speed Load (Upstream Port Load) - Reference 1



Low-Speed Load (Downstream Port Load) - Reference 2



Low-Speed Load (Compliance Load)



12.8 Low-Voltage Detection Characteristics

12.8.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.25	2.45	2.65	V	When voltage drops
Released voltage	VDH	-	2.30	2.50	2.70	V	When voltage rises

12.8.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.58	2.8	3.02	V	When voltage drops
Released voltage	VDH		2.67	2.9	3.13	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.76	3.0	3.24	V	When voltage drops
Released voltage	VDH		2.85	3.1	3.34	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	2.94	3.2	3.45	V	When voltage drops
Released voltage	VDH		3.04	3.3	3.56	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.31	3.6	3.88	V	When voltage drops
Released voltage	VDH		3.40	3.7	3.99	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.40	3.7	3.99	V	When voltage drops
Released voltage	VDH		3.50	3.8	4.10	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	3.68	4.0	4.32	V	When voltage drops
Released voltage	VDH		3.77	4.1	4.42	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	3.77	4.1	4.42	V	When voltage drops
Released voltage	VDH		3.86	4.2	4.53	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	3.86	4.2	4.53	V	When voltage drops
Released voltage	VDH		3.96	4.3	4.64	V	When voltage rises
LVD stabilization wait time	T_{LVDW}	-	-	-	4480× t_{CYCP}*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.9 MainFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter		Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	Large Sector	-	0.7	3.7	s	Includes write time prior to internal erase
	Small Sector		0.3	1.1		
Half word (16-bit) write time	Write cycles < 100 times	-	12	100	µs	Not including system-level overhead time
	Write cycles > 100 times			200		
Chip erase time		-	8.0	38.4	s	Includes write time prior to internal erase

Write cycles and data hold time

Erase/Write Cycles (Cycle)	Data Hold Time (Year)
1,000	20 *
10,000	10 *
100,000	5 *

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at +85°C).

12.10 WorkFlash Memory Write/Erase Characteristics

(V_{CC} = 2.7V to 5.5V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.3	1.5	s	Includes write time prior to internal erase
Half word (16-bit) write time	-	20	200	µs	Not including system-level overhead time
Chip erase time	-	1.2	6	s	Includes write time prior to internal erase

Write cycles and data hold time

Erase/Write Cycles (Cycle)	Data Hold Time (Year)
1,000	20 *
10,000	10 *
100,000	5 *

*: This value comes from the technology qualification (using Arrhenius equation to translate high temperature acceleration test result into average temperature value at +85°C).

12.11 Standby Recovery Time

12.11.1 Recovery Cause: Interrupt/WKUP

The time from recovery cause reception of the internal circuit to the program operation start is shown.

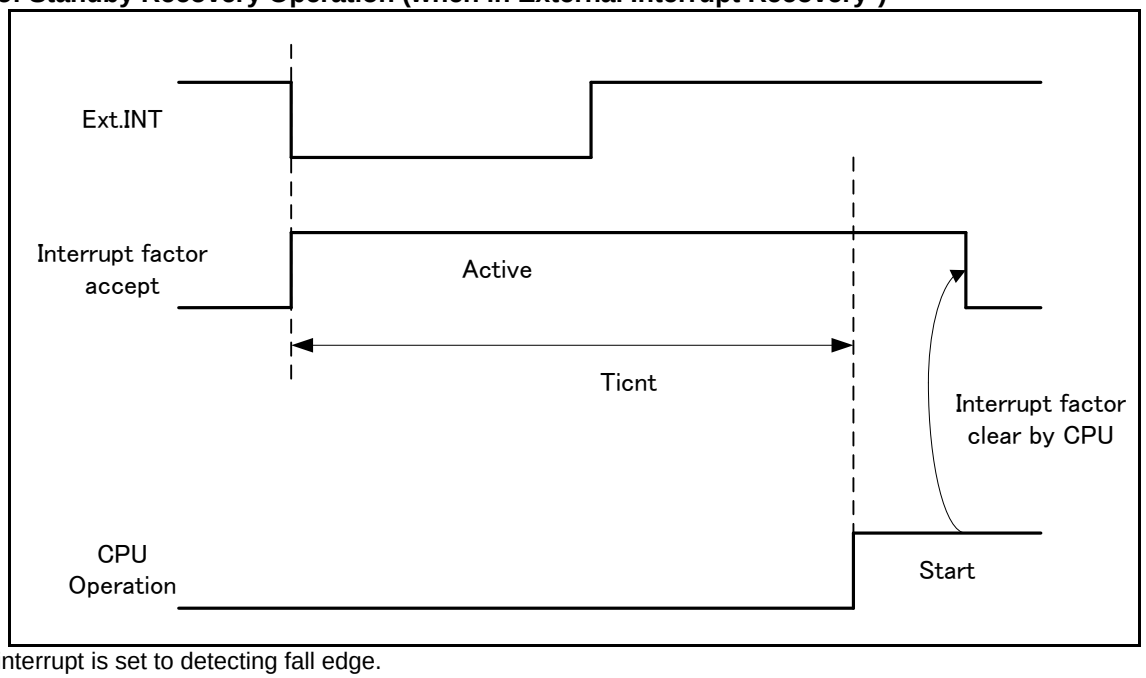
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	Ticnt	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR timer mode		450	900	µs	
Sub timer mode		896	1136	µs	
RTC mode stop mode (High-speed CR /Main/PLL run mode return)		316	581	µs	
RTC mode stop mode (Low-speed CR/sub run mode return)		270	540	µs	
Deep standby RTC mode		365	667	µs	without RAM retention
Deep standby stop mode		365	667	µs	with RAM retention

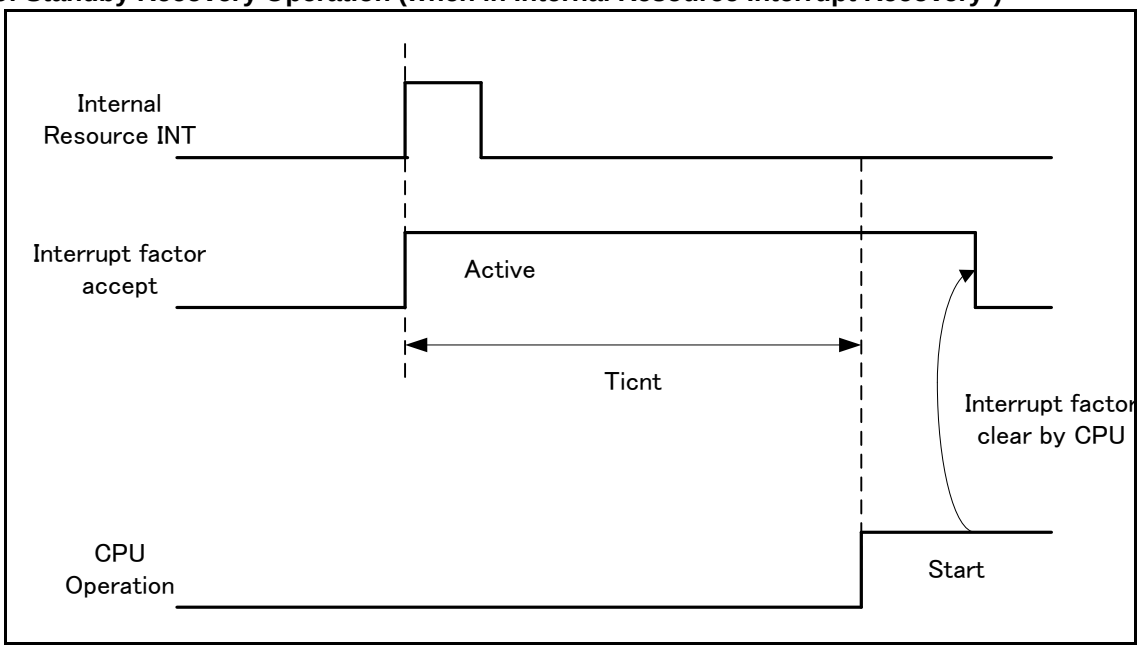
*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in External Interrupt Recovery*)



*: External interrupt is set to detecting fall edge.

Example of Standby Recovery Operation (when in Internal Resource Interrupt Recovery*)



*: Depending on the standby mode, interrupt from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each Low-Power consumption modes.*
  See CHAPTER 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main part (002-04856).
- *When interrupt recoveries, the operation mode that CPU recoveries depend on the state before the Low-Power consumption mode transition. See CHAPTER 6: Low Power Consumption Mode in FM4 Family Peripheral Manual Main part (002-04856).*

12.11.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

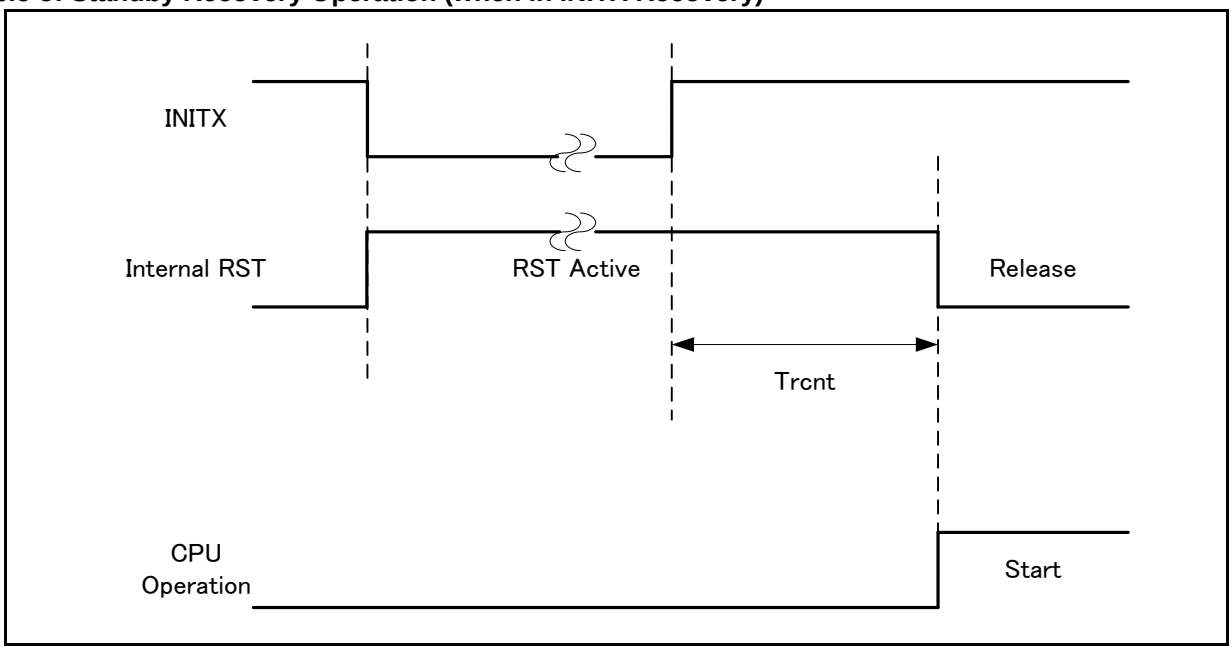
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

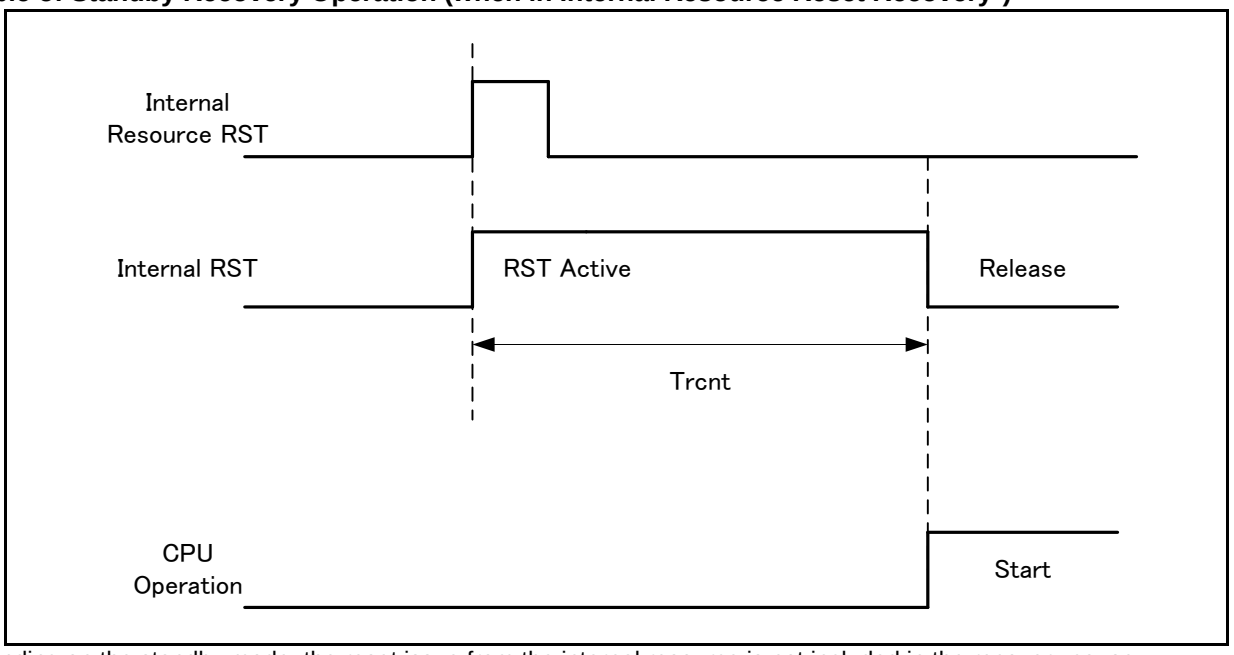
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	Trcnt	155	266	µs	
High-speed CR timer mode Main timer mode PLL timer mode		155	266	µs	
Low-speed CR timer mode		315	567	µs	
Sub timer mode		315	567	µs	
RTC mode Stop mode		315	567	µs	
Deep standby RTC mode Deep standby stop mode		336	667	µs	without RAM retention
			667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)



Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)



*: Depending on the standby mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

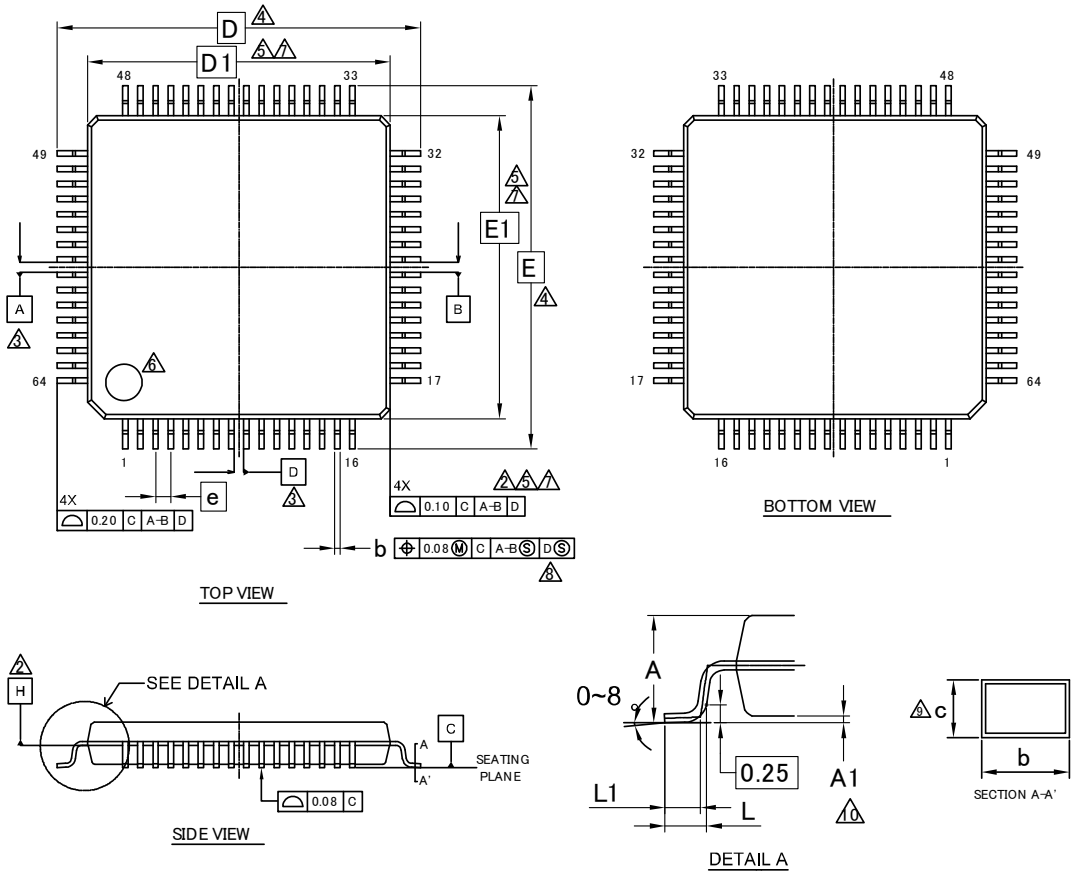
- *The return factor is different in each Low-Power consumption modes.*
  See CHAPTER 6: Low Power Consumption Mode and Operations of Standby Modes in FM4 Family Peripheral Manual Main part (002-04856).
- *The time during the power-on reset/low-voltage detection reset is excluded to the recovery source. See 12.4.7 Power-on Reset Timing in 12.4 AC Characteristics in 12. Electrical Characteristics for the detail on the time during the power-on reset/low-voltage detection reset.*
- *When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.*
- *The internal resource reset means the watchdog reset and the CSV reset.*

13. Ordering Information

Part Number	Package
MB9BF364LPMC1	Plastic・LQFP (0.5mm pitch), 64 pin (LQD064)
MB9BF365LPMC1	
MB9BF366LPMC1	
MB9BF364LPMC	Plastic・LQFP (0.65mm pitch), 64 pin (LQG064)
MB9BF365LPMC	
MB9BF366LPMC	
MB9BF364KPMC	Plastic・LQFP (0.5mm pitch), 48 pin (LQA048)
MB9BF365KPMC	
MB9BF366KPMC	
MB9BF364LQN	Plastic・QFN (0.5mm pitch), 64 pin (VNC064)
MB9BF365LQN	
MB9BF366LQN	
MB9BF364KQN	Plastic・QFN (0.5mm pitch), 48 pin (VNA048)
MB9BF365KQN	
MB9BF366KQN	

14. Package Dimensions

Package Type	Package Code
LQFP 64pin (0.5mm pitch)	LQD064



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.00	——	0.20
b	0.15	——	0.27
c	0.09	——	0.20
D	12.00 BSC.		
D1	10.00 BSC.		
e	0.50 BSC		
E	12.00 BSC.		
E1	10.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

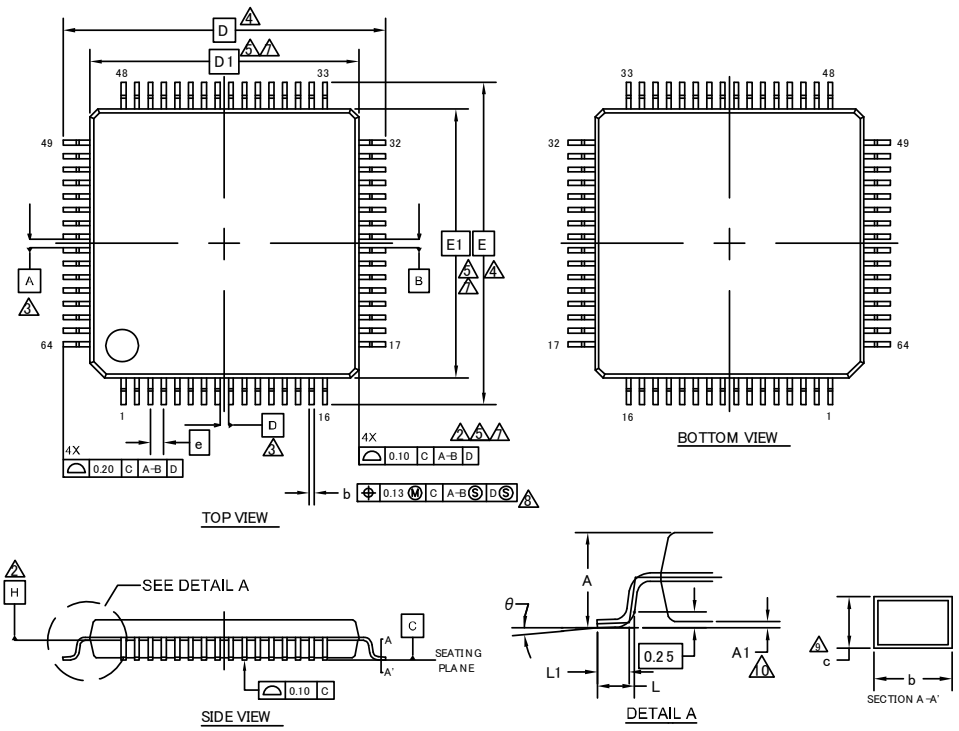
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-11499 **

PACKAGE OUTLINE, 64 LEAD LQFP
10.0X10.0X1.7 MM LQD064 Rev**

Package Type	Package Code
LQFP 64pin (0.65mm pitch)	LQG064



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.00	——	0.20
b	0.27	0.32	0.37
c	0.09	——	0.20
D	14.00 BSC		
D1	12.00 BSC		
e	0.65 BSC		
E	14.00 BSC		
E1	12.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	——	8°

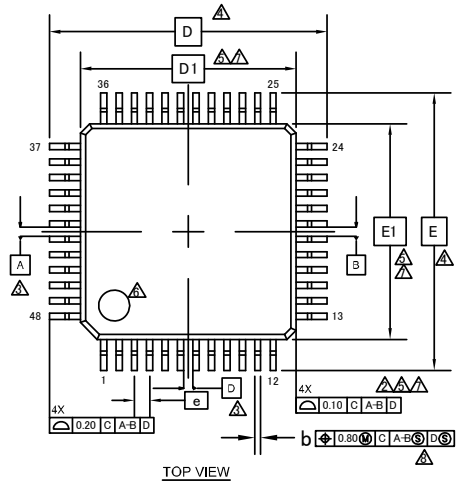
NOTES

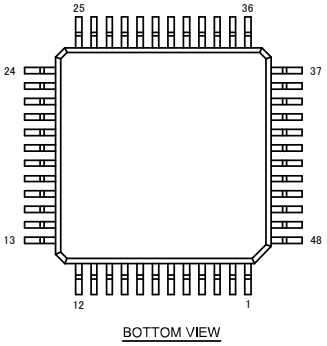
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

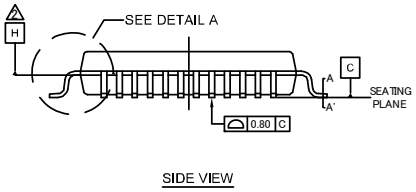
002-13881 **

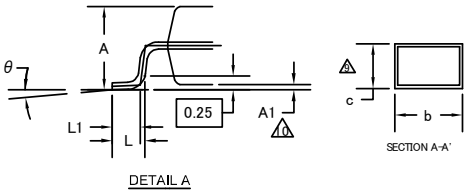
PACKAGE OUTLINE, 64 LEAD LQFP
12.0X12.0X1.7 MM LQG064 REV**

Package Type	Package Code
LQFP 48pin (0.5mm pitch)	LQA048









SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.15	—	0.27
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.50 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

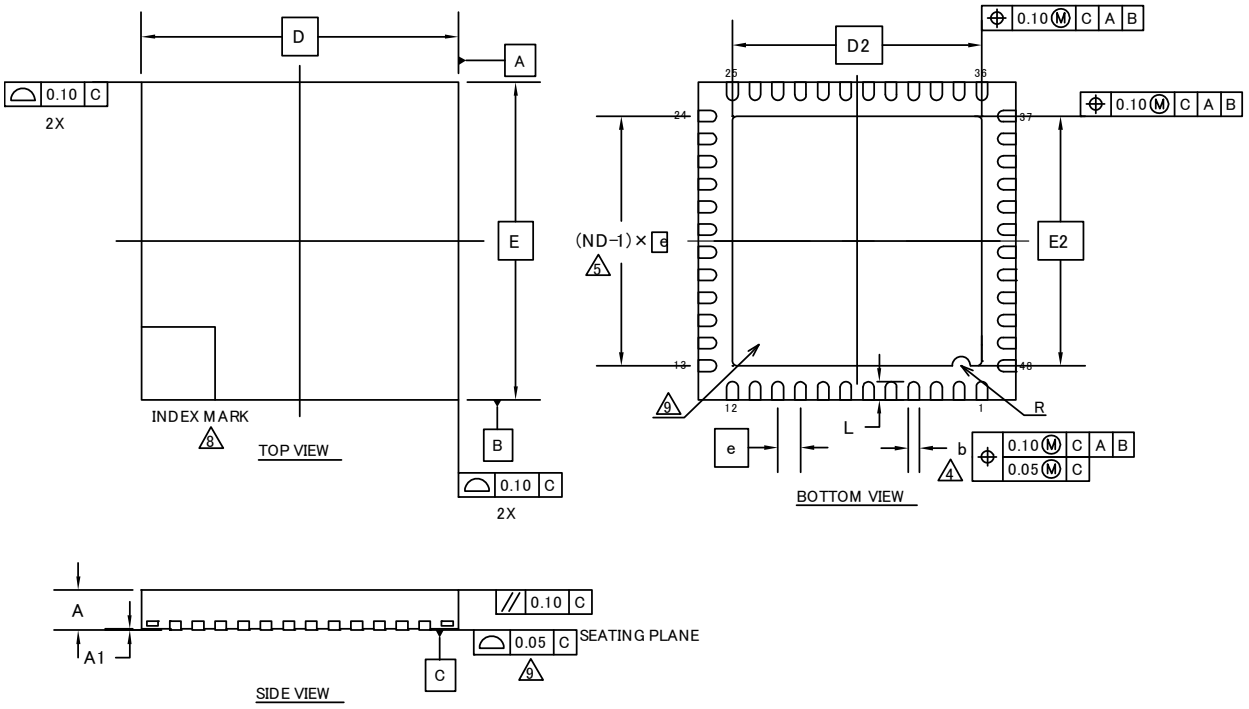
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13731 **

PACKAGE OUTLINE, 48 LEAD LQFP
7.0X7.0X1.7 MM LQA048 REV**

Package Type	Package Code
QFN 64pin (0.5mm pitch)	VNC064



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	0.90
A1	0.00	——	0.05
D	7.00 BSC		
E	7.00 BSC		
b	0.20	0.25	0.30
D2	5.50 BSC		
E2	5.50 BSC		
e	0.50 BSC		
R	0.20 REF		
L	0.35	0.40	0.45

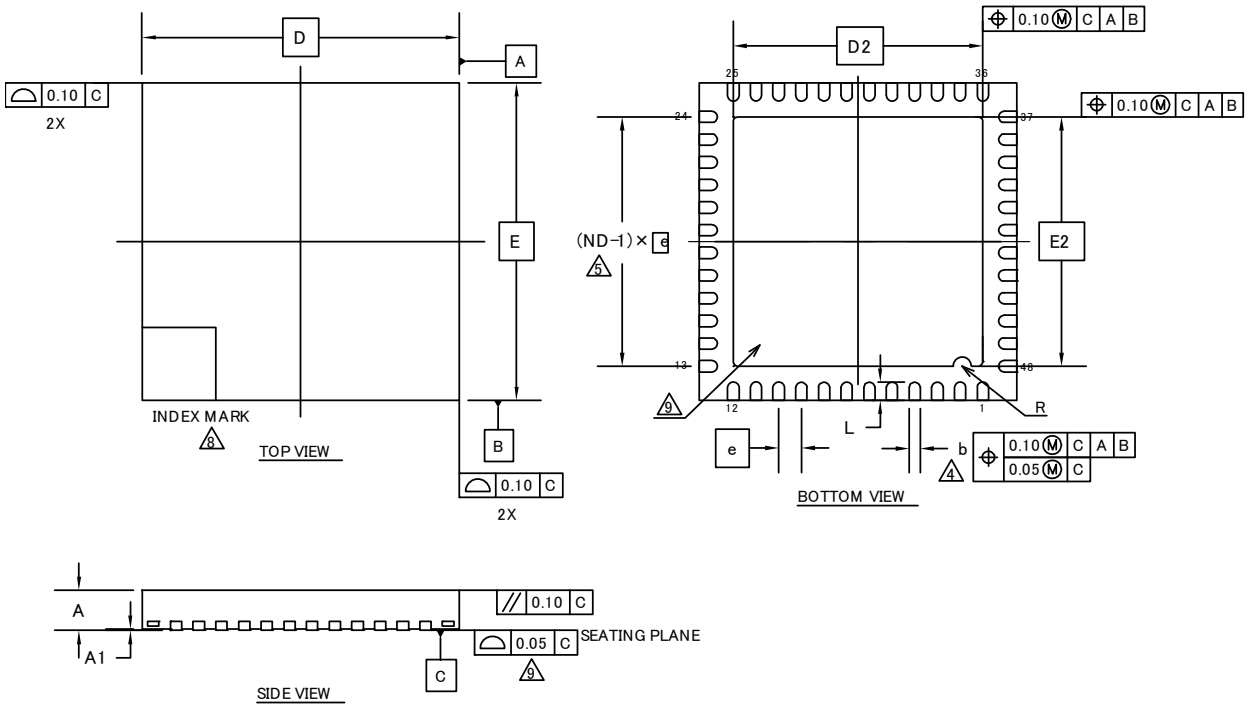
NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. JEDEC SPEC IFICATION NO . REF: N/A

002-13234 **

PACKAGE OUTLINE, 48 LEAD QFN
7.0X7.0X0.9 MM VNA048 5.5X5.5 MM EPAD(SAWN) REV**

Package Type	Package Code
QFN 48pin (0.5mm pitch)	VNA048



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	0.90
A1	0.00	——	0.05
D	7.00 BSC		
E	7.00 BSC		
b	0.20	0.25	0.30
D2	5.50 BSC		
E2	5.50 BSC		
e	0.50 BSC		
R	0.20 REF		
L	0.35	0.40	0.45

NOTE

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING CONFORMS TO ASME Y14.5-1994.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. JEDEC SPECIFICATION NO. REF: N/A

002-15528 **

PACKAGE OUTLINE, 48 LEAD QFN
7.0X7.0X0.9 MM VNA048 5.5X5.5 MM EPAD (SAWN) REV**

15. Major Changes

Spansion Publication Number: DS709-00007

Page	Section	Change Results
-	-	Preliminary → Data Sheet
3	■FEATURES [USB function]	Added the following description : ・The size of each endpoint is according to the follows. - Endpoint 0, 2 to 5 : 64bytes - Endpoint 1 : 256bytes
31 to 34	■I/O CIRCUIT TYPE	Added the following description to Remarks of Type F, G, I, L, M, N : When this pin is used as an I2C pin, the digital output P-ch transistor is always off
35 to 36		Added the following description to Remarks of Type O, P, Q: For I/O setting, refer to VBAT Domain in the PERIPHERAL MANUAL
43	■HANDLING DEVICES ●Handling when using debug pins	Added new section
44	■BLOCK DIAGRAM	Revised the block diagram
57	■ELECTRICAL CHARACTERISTICS 2. Recommended Operating Conditions	Added the note to “AVRH”
		Revised “Table for package thermal resistance and maximum permissible power”
58		Revised “Icc(leakmax)”
60 to 65	■ELECTRICAL CHARACTERISTICS 3. DC Characteristics (1) Current Rating	• Revised the value of TBD • Added the note to “I_{CC}” • Added the note to “I_{CCVBAT}”
70	■ELECTRICAL CHARACTERISTICS 4. AC Characteristics (3) Sub Clock Input Characteristics	Revised the waveform chart : V_{CC} → V_{BAT}
70	■ELECTRICAL CHARACTERISTICS 4. AC Characteristics (3) Built-in CR OscillationCharacteristics	• Revised the value of TBD • Revised the table and the note of “Built-in High-speed CR”
71	■ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4-1) Operating Conditions of Main PLL(In the case of using main clock for input clock of PLL) (4-2)Operating Conditions of USB PLL(In the case of using main clock for input clock of PLL)	• Revised the table and the note
71	■ELECTRICAL CHARACTERISTICS 4. AC Characteristics (4-3) Operating Conditions of Main PLL(In the case of using built-in high-speed CR clock for input clock of main PLL)	• Revised the value of TBD • Revised the table and the note
106	■ELECTRICAL CHARACTERISTICS 5. 12-bit A/D Converter ・Electrical Characteristics for the A/D Converter	• Revised the value of TBD • Revised the condition of the electrical characteristics table • Revised the description of "Reference voltage"
109	■ELECTRICAL CHARACTERISTICS 6. 12-bit D/A Converter ・Electrical Characteristics for the D/A Converter	• Revised the value of TBD • Revised the condition of the electrical characteristics table • Revised the remarks of “IDDA”

Page	Section	Change Results
116	■ELECTRICAL CHARACTERISTICS 11. Standby Recovery Time (1) Recovery cause: Interrupt/WKUP	• Revised the value of TBD • Revised the table of Recovery count time
118	■ELECTRICAL CHARACTERISTICS 11. Standby Recovery Time (2) Recovery cause:Reset	• Revised the value of TBD • Revised the table of Recovery count time

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB9B360L Series 32-Bit Arm® Cortex® - M4F, FM4 Microcontroller
Document Number: 002-04930

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	AKIH	12/25/2013	Migrated to Cypress and assigned document number 002-04930. No change to document contents or format.
*A	5273878	AKIH	05/12/2016	Updated to Cypress format.
*B	5555936	YSKA	12/15/2017	Added an explanation of product category in introduction (Page 1). Changed an explanation from “from 01 to 99” to “from 00 to 99” in Real-Time Clock (RTC) (Page 3) of Features, and Deleted “Second/A day of the week” of interrupt function. Corrected “USB Function" to “USB Device" in the following chapters. Features (Page 1) 1. Product Lineup (Page 7) 4.2 List of Pin Functions (Page 19) Divided an explanation into 64 pin and 48 pin in Power Supply (Page 4) of Features. Changed package code as the following in chapter : 2. Packages (Page 8) 3. Pin Assignment (Page 9 to 12) 12.2 Recommended Operating Conditions (Page 53) 13. Ordering Information (Page 117) 14. Package Dimensions (Page 118 to 122). FTP-48P-M49 -> LQA048, LCC-48P-M73 -> VNA048, FTP-64P-M38 -> LQD064, FTP-64P-M39 -> LQG064, LCC-64P-M24 -> VNC064 Changed 15 pin (Page 15) at LQFP48 from VBAT to VCC in 4.1 List of Pin Numbers. Added 15 pin (Page 27) to VCC of Power at LQFP48, Deleted 15 pin from VBAT of VBAT Power at LQFP48 in 4.2 List of Pin Functions. Added Note for JTAG pin (Page 27) in 4. Pin Description. Added an explanation in Notes on Power-on (Page 39) of 7. Handling Devices. Corrected "total maximum output current" to "total average output current" at ΣIOLAV in 12.1 Absolute Maximum Ratings (Page52). Added Smoothing capacitor to Parameter, and Added remarks *6 in 12.2 Recommended Operating Conditions (Page 53). Changed remark *3 to "When all ports are input and are fixed at "0"." in 12.3.1 Current Rating (Page 57 to 62).

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				In 12.3.1 Current Rating, Added remark *6 to ICCHD, Added remark *7 to ICCRD, Added remark *8/*9 to ICCVBAT/RTC operation, and Added remark *9 to ICCVBAT/RTC stop (Page 62). Added an explanation for 48 pin package in 12.4.2 Sub Clock Input Characteristics (Page 67). Changed Parameter “Power supply rising time (t_{VCCR})” to “Power ramp rate (dV/dt)” in 12.4.8 Power-on Reset Timing, Changed the minimum to 1.3mV/µs, Changed the maximum to 1000mV/µs, and Added remarks and note (Page 69). Deleted setting value “SPI=1” and “MS=0” at using chip select in 12.4.11 UART Timing, and Added “MS bit = 0” and “MS bit = 1” on the Figure (Page 88 to 95). Corrected "Analog port input current" to "Analog port input leak current" in 12.5 12-bit A/D Converter (Page 103). Reflected the following items in "Datasheet Errata for the MB9B360L Series (002-04931)". Added “Pull-up resistor : Approximately 50 kΩ” to remarks in Type I (Page 31) of 5.I/O Circuit Type. Modified S/T of VBAT Pin Status Type and remark *2 in List of VBAT Domain Pin Status (Page 51) of 11.Pin Status in Each CPU State. Added remarks *5 in 12.2 Recommended Operating Conditions (Page 53). Added Frequency stabilization time to Parameter, and Added remarks *2 in Built-in High-speed CR of 12.4.3 Built-in CR Oscillation Characteristics (Page 67). Added Conversion time to Parameter in Electrical Characteristics for the D/A Converter of 12.6 12-bit D/A Converter (Page 106). Revised Recovery Count Time of 12.11.1 Recovery cause: Interrupt/WKUP (Page 113) as follows. - Typical Value of Sub timer mode is 896µs. - Typical Value of RTC mode stop mode (High-speed CR / Main/PLL run mode return) is 316µs. - Typical Value of RTC mode stop mode (Low-speed CR / sub run mode return) is 270µs, and Max Value is 540µs. - Typical Value of Deep standby RTC mode without RAM retention is 365µs. - Typical Value of Deep standby RTC mode with RAM retention is 365µs. Revised Recovery Count Time of 12.11.2 Recovery cause: Reset (Page 115) as follows. - Typical Value of Sleep mode is 155µs. - Typical Value of High-speed CR timer mode is 155µs. - Typical Value of Low-speed CR timer mode is 315µs. - Typical Value of Sub timer mode is 315µs.

Revision	ECN	Orig. of Change	Submission Date	Description of Change
				- Typical Value of RTC mode stop mode is 315µs, Max Value is 567µs. - Typical Value of Deep standby RTC mode without RAM retention is 336µs. - Typical Value of Deep standby RTC mode with RAM retention is 336µs. Modified the Chapter name “12.4.11 UART Timing” to “12.4.11 CSIO/UART Timing”. (Page 72) Added the Baud rate spec in “12.4.11 CSIO/UART Timing”.(Page 72, 74, 76, 78) Modified the expression for “Reference power supply current” from “between AVRH and AVSS” to “AVRH” in chapter 12.5. 12-bit A/D Converter (Page 103) Moved the value(1.0) in “State transition time to operation permission” from minimum to maximum.(Page 103) Modified the expression of Built-in CR in “1. Product Lineup”(Page 7) Modified the mode name of I^2C as follows(Page 2, 100) High-speed mode → Fast-mode, Typical Mode → Standard-mode Modified the typo as below.(Page 72, 74, 76, 78) SCLKx_0 → SCKx_0 Modified typo in the “Recovery Count Time” table in 12.11.1 Recovery cause: Interrupt/WKUP (Page 113) and 12.11.2 Recovery Cause: Reset (Page 115) as follows. Old) Deep standby RTC mode with RAM retention Deep standby stop mode with RAM retention New) Deep standby RTC mode Deep standby stop mode

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