MOSFETs Silicon N-channel MOS (U-MOSⅧ-H)

# **TK72E12N1**

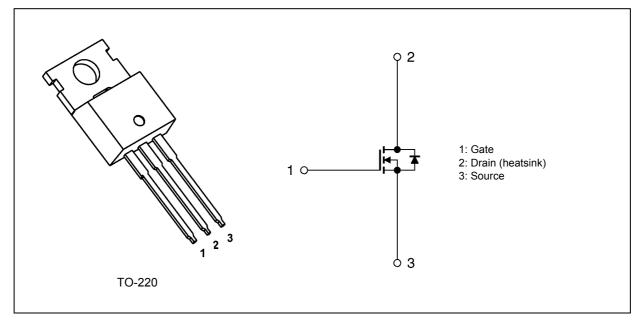
### 1. Applications

• Switching Voltage Regulators

#### 2. Features

- (1) Low drain-source on-resistance:  $R_{DS(ON)} = 3.6 \text{ m}\Omega \text{ (typ.)} (V_{GS} = 10 \text{ V})$
- (2) Low leakage current:  $I_{DSS} = 10 \ \mu A \ (max) \ (V_{DS} = 120 \ V)$
- (3) Enhancement mode:  $V_{th}$  = 2.0 to 4.0 V (V\_{DS} = 10 V,  $I_{D}$  = 1.0 mA)

#### 3. Packaging and Internal Circuit



### 4. Absolute Maximum Ratings (Note) ( $T_a = 25^{\circ}C$ unless otherwise specified)

Characteristics				Rating	Unit
Drain-source voltage			V <sub>DSS</sub>	120	V
Gate-source voltage			V <sub>GSS</sub>	±20	
Drain current (DC)	(Silicon limit)	(Note 1), (Note 2)	I <sub>D</sub>	179	Α
Drain current (DC)		(Note 1), (Note 3)	Ι <sub>D</sub>	72	
Drain current (pulsed)	(t = 1 ms)	(Note 1)	I <sub>DP</sub>	360	
Power dissipation	(T <sub>c</sub> = 25°C)		PD	255	W
Single-pulse avalanche energy		(Note 4)	E <sub>AS</sub>	256	mJ
Avalanche current			I <sub>AR</sub>	72	Α
Channel temperature			T <sub>ch</sub>	150	°C
Storage temperature			T <sub>stg</sub>	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Start of commercial production 2012-07

#### 5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance	R <sub>th(ch-c)</sub>	0.49	°C/W
Channel-to-ambient thermal resistance	R <sub>th(ch-a)</sub>	83.3	

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Limited by silicon chip capability. Package limit is 100 A.

Note 3: Device mounted with heatsink so that  $R_{th(ch-a)}$  becomes 2.77°C/W.

Note 4: V\_DD = 80 V, T\_ch = 25°C (initial), L = 48.3  $\mu H$ , I\_AR = 72 A

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

#### 6. Electrical Characteristics

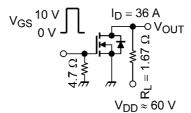
### 6.1. Static Characteristics (T<sub>a</sub> = 25°C unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current	I <sub>GSS</sub>	$V_{GS}$ = ±20 V, $V_{DS}$ = 0 V	_	_	±0.1	μA
Drain cut-off current	I <sub>DSS</sub>	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V	-	—	10	
Drain-source breakdown voltage	V <sub>(BR)DSS</sub>	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = 0 V	120		_	V
Drain-source breakdown voltage (Note 5)	V <sub>(BR)DSX</sub>	I <sub>D</sub> = 10 mA, V <sub>GS</sub> = -20 V	90	_	_	
Gate threshold voltage	V <sub>th</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1.0 mA	2.0	—	4.0	
Drain-source on-resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 36 A	_	3.6	4.4	mΩ

Note 5: If a reverse bias is applied between gate and source, this device enters V<sub>(BR)DSX</sub> mode. Note that the drainsource breakdown voltage is lowered in this mode.

### 6.2. Dynamic Characteristics ( $T_a = 25^{\circ}C$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V, f = 1 MHz	_	8100	_	pF
Reverse transfer capacitance	C <sub>rss</sub>		_	30	—	
Output capacitance	C <sub>oss</sub>		_	1200	—	
Gate resistance	r <sub>g</sub>	—	_	2.4	_	Ω
Switching time (rise time)	tr	See Figure 6.2.1	_	33	—	ns
Switching time (turn-on time)	t <sub>on</sub>		_	64	—	
Switching time (fall time)	t <sub>f</sub>		_	37	_	
Switching time (turn-off time)	t <sub>off</sub>		_	120	_	



 $Duty \le 1\%, \ t_w = 10 \ \mu s$  Fig. 6.2.1 Switching Time Test Circuit

### 6.3. Gate Charge Characteristics ( $T_a = 25^{\circ}C$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Qg	$V_{DD} \approx 96 \text{ V}, \text{ V}_{GS} \text{ = } 10 \text{ V}, \text{ I}_{D} \text{ = } 72 \text{ A}$	—	130	_	nC
Gate-source charge 1	Q <sub>gs1</sub>	]		44	_	
Gate-drain charge	Q <sub>gd</sub>	]	_	34	_	
Gate switch charge	Q <sub>SW</sub>	]		52		

### 6.4. Source-Drain Characteristics ( $T_a = 25^{\circ}C$ unless otherwise specified)

Characteristics		Symbol	Test Condition	Min	Тур.	Max	Unit
Reverse drain current (DC)	(Note 6)	I <sub>DR</sub>	—	—		72	A
Reverse drain current (pulsed)	(Note 6)	I <sub>DRP</sub>	—	_	_	360	
Diode forward voltage		V <sub>DSF</sub>	I <sub>DR</sub> = 72 A, V <sub>GS</sub> = 0 V	_	—	-1.2	V
Reverse recovery time	(Note 7)	t <sub>rr</sub>	I <sub>DR</sub> = 72 A, V <sub>GS</sub> = 0 V	_	110		ns
Reverse recovery charge	(Note 7)	Q <sub>rr</sub>	-dI <sub>DR</sub> /dt = 100 A/µs	_	290		nC

Note 6: Ensure that the channel temperature does not exceed 150°C. Note 7: Ensure that  $V_{DS}$  peak does not exceed  $V_{DSS}$ .

### 7. Marking

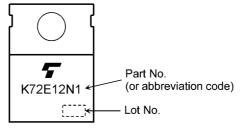
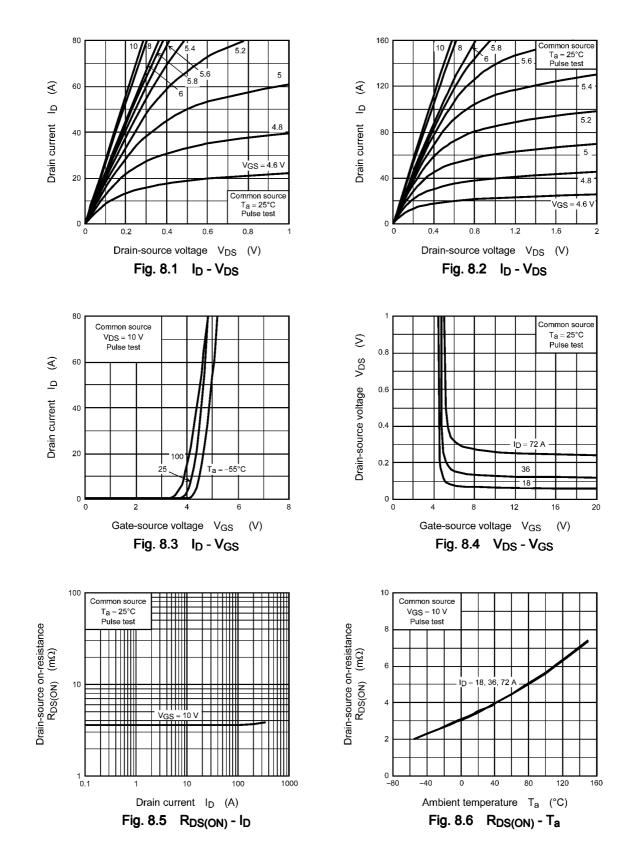
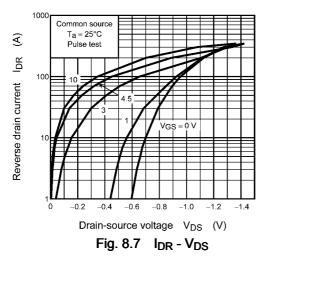
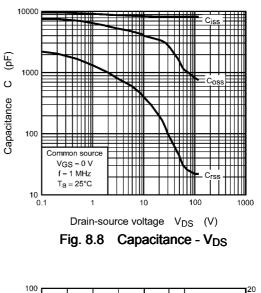


Fig. 7.1 Marking

### 8. Characteristics Curves (Note)







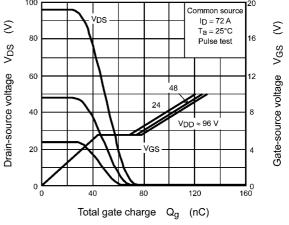
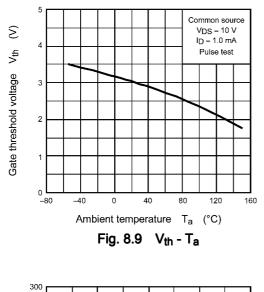
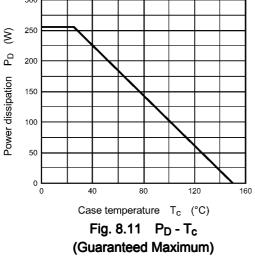
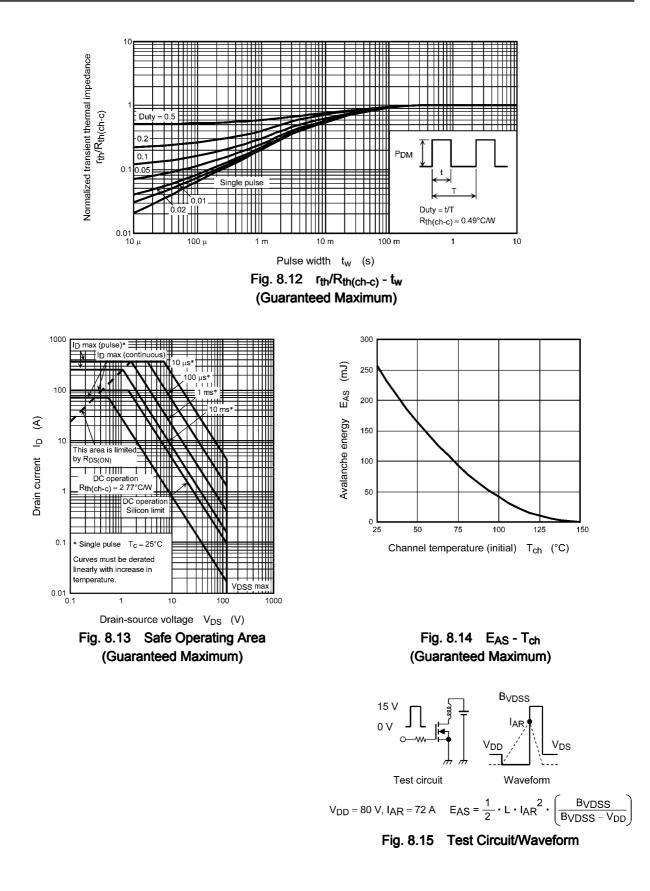


Fig. 8.10 Dynamic Input/Output Characteristics







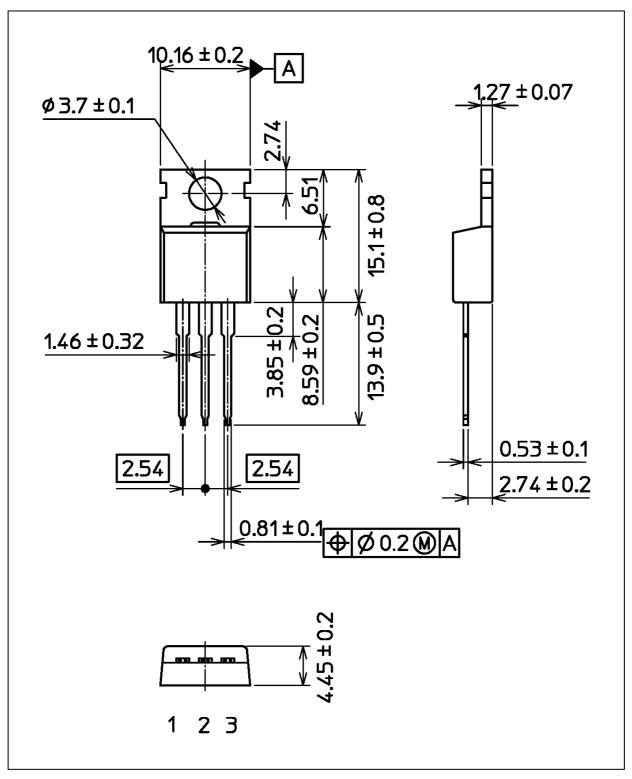
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.



### Package Dimensions

TK72E12N1

Unit: mm



Weight: 1.93 g (typ.)

	Package Name(s)
TOSHIBA: 2-10X1A	
Nickname: TO-220	

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