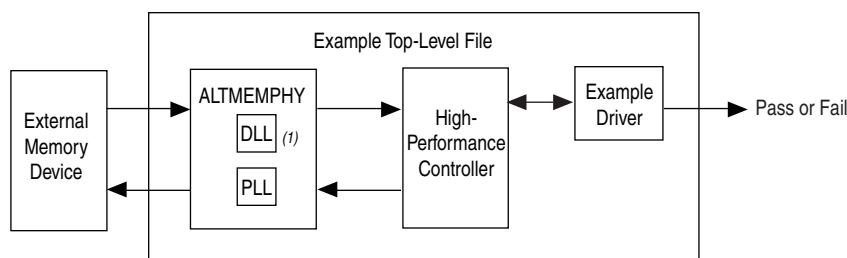


The Altera® DDR, DDR2, and DDR3 SDRAM Controllers with ALTMEMPHY IP provide simplified interfaces to industry-standard DDR, DDR2, and DDR3 SDRAM. The ALTMEMPHY megafunction is an interface between a memory controller and the memory devices, and performs read and write operations to the memory. The DDR, DDR2, and DDR3 SDRAM Controllers with ALTMEMPHY IP work in conjunction with the Altera ALTMEMPHY megafunction.

The DDR and DDR2 SDRAM Controllers with ALTMEMPHY IP and ALTMEMPHY megafunction offer full-rate or half-rate DDR and DDR2 SDRAM interfaces. The DDR3 SDRAM Controller with ALTMEMPHY IP and ALTMEMPHY megafunction support DDR3 SDRAM interfaces in half-rate mode. The DDR, DDR2, and DDR3 SDRAM Controllers with ALTMEMPHY IP offer the high-performance controller II (HPC II), which provides high efficiency and advanced features.

Figure 15–1 shows a system-level diagram including the example top-level file that the DDR, DDR2, or DDR3 SDRAM Controller with ALTMEMPHY IP creates for you.

**Figure 15–1. System-Level Diagram**



**Note to Figure 15–1:**

- (1) When you choose **Instantiate DLL Externally**, delay-locked loop (DLL) is instantiated outside the ALTMEMPHY megafunction.

The MegaWizard™ Plug-In Manager generates an example top-level file, consisting of an example driver, and your DDR, DDR2, or DDR3 SDRAM high-performance controller custom variation. The controller instantiates an instance of the ALTMEMPHY megafunction which in turn instantiates a phase-locked loop (PLL) and DLL. You can also instantiate the DLL outside the ALTMEMPHY megafunction to share the DLL between multiple instances of the ALTMEMPHY megafunction. You cannot share a PLL between multiple instances of the ALTMEMPHY megafunction, but you may share some of the PLL clock outputs between these multiple instances.

The example top-level file is a fully-functional design that you can simulate, synthesize, and use in hardware. The example driver is a self-test module that issues read and write commands to the controller and checks the read data to produce the pass or fail, and test complete signals.

The ALTMEMPHY megafunction creates the datapath between the memory device and the memory controller. The megafunction is available as a stand-alone product or can be used in conjunction with the Altera high-performance memory controller. When using the ALTMEMPHY megafunction as a stand-alone product, use with either custom or third-party controllers.



For new designs, Altera recommends using a UniPHY-based external memory interface, such as the DDR2 and DDR3 SDRAM controllers with UniPHY, QDR II and QDR II+ SRAM controllers with UniPHY, or RLDRAM II controller with UniPHY.

## Release Information

Table 15-1 provides information about this release of the DDR3 SDRAM Controller with ALTMEMPHY IP.

**Table 15-1. Release Information**

| Item           | Description                                                                                 |
|----------------|---------------------------------------------------------------------------------------------|
| Version        | 11.1                                                                                        |
| Release Date   | November 2011                                                                               |
| Ordering Codes | IP-SDRAM/HPDDR (DDR SDRAM HPC)<br>IP-SDRAM/HPDDR2 (DDR2 SDRAM HPC)<br>IP-HPMCII (HPC II)    |
| Product IDs    | 00BE (DDR SDRAM)<br>00BF (DDR2 SDRAM)<br>00C2 (DDR3 SDRAM)<br>00CO (ALTMEMPHY Megafunction) |
| Vendor ID      | 6AF7                                                                                        |

Altera verifies that the current version of the Quartus® II software compiles the previous version of each MegaCore function. The *MegaCore IP Library Release Notes and Errata* report any exceptions to this verification. Altera does not verify compilation with MegaCore function versions older than one release. For information about issues on the DDR, DDR2, or DDR3 SDRAM high-performance controller and the ALTMEMPHY megafunction in a particular Quartus II version, refer to the *Quartus II Software Release Notes*.

## Device Family Support

Table 15-2 defines the device support levels for Altera IP cores.

**Table 15-2. Altera IP Core Device Support Levels**

| FPGA Device Families                                                                                                                                                                                                                                                              | HardCopy Device Families                                                                                                                                                                                                                                                                             |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Preliminary support</b> —The IP core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution. | <b>HardCopy Companion</b> —The IP core is verified with preliminary timing models for the HardCopy companion device. The IP core meets all functional requirements, but might still be undergoing timing analysis for the HardCopy device family. It can be used in production designs with caution. |
| <b>Final support</b> —The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.                                                              | <b>HardCopy Compilation</b> —The IP core is verified with final timing models for the HardCopy device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.                                                                  |

Table 15-3 shows the level of support offered by the DDR, DDR2, and DDR3 SDRAM Controllers with ALTMEMPHY IP for Altera device families.

**Table 15-3. Device Family Support**

| Device Family         | Protocol                                                                         |            |
|-----------------------|----------------------------------------------------------------------------------|------------|
|                       | DDR and DDR2                                                                     | DDR3       |
| Arria® GX             | Final                                                                            | No support |
| Arria II GX           | Final                                                                            | Final      |
| Cyclone® III          | Final                                                                            | No support |
| Cyclone III LS        | Final                                                                            | No support |
| Cyclone IV E          | Final                                                                            | No support |
| Cyclone IV GX         | Final                                                                            | No support |
| HardCopy II           | Refer to the <a href="#">What's New in Altera IP</a> page of the Altera website. | No support |
| Stratix® II           | Final                                                                            | No support |
| Stratix II GX         | Final                                                                            | No support |
| Other device families | No support                                                                       | No support |

## Features

### ALTMEMPHY Megafunction

Table 15-4 summarizes key feature support for the ALTMEMPHY megafunction.

**Table 15-4. ALTMEMPHY Megafunction Feature Support**

| Feature                                                                                                                                     | DDR and DDR2 | DDR3 |
|---------------------------------------------------------------------------------------------------------------------------------------------|--------------|------|
| Support for the Altera PHY Interface (AFI) on all supported devices.                                                                        | ✓            | ✓    |
| Automated initial calibration eliminating complicated read data timing calculations.                                                        | ✓            | ✓    |
| Voltage and temperature (VT) tracking that guarantees maximum stable performance for DDR, DDR2, and DDR3 SDRAM interfaces.                  | ✓            | ✓    |
| Self-contained datapath that makes connection to an Altera controller or a third-party controller independent of the critical timing paths. | ✓            | ✓    |
| Full-rate interface                                                                                                                         | ✓            | —    |
| Half-rate interface                                                                                                                         | ✓            | ✓    |
| Easy-to-use parameter editor                                                                                                                | ✓            | ✓    |

In addition, the ALTMEMPHY megafunction supports DDR3 SDRAM components without leveling:

- The ALTMEMPHY megafunction supports DDR3 SDRAM components without leveling for Arria II GX devices using T-topology for clock, address, and command bus:
  - Supports multiple chip selects.
- The DDR3 SDRAM PHY without leveling  $f_{MAX}$  is 400 MHz for single chip selects.
- No support for data-mask (DM) pins for ×4 DDR3 SDRAM DIMMs or components, so select **No** for **Drive DM pins from FPGA** when using ×4 devices.
- The ALTMEMPHY megafunction supports half-rate DDR3 SDRAM interfaces only.

### High-Performance Controller II

Table 15-5 summarizes key feature support for the DDR, DDR2, and DDR3 SDRAM HPC II.

**Table 15-5. Feature Support (Part 1 of 2)**

| Feature                                                                   | DDR and DDR2 | DDR3 |
|---------------------------------------------------------------------------|--------------|------|
| Half-rate controller                                                      | ✓            | ✓    |
| Support for AFI ALTMEMPHY                                                 | ✓            | ✓    |
| Support for Avalon <sup>®</sup> Memory Mapped (Avalon-MM) local interface | ✓            | ✓    |

**Table 15–5. Feature Support (Part 2 of 2)**

| Feature                                                                                    | DDR and DDR2 | DDR3 |
|--------------------------------------------------------------------------------------------|--------------|------|
| Configurable command look-ahead bank management with in-order reads and writes             | ✓            | ✓    |
| Additive latency                                                                           | ✓            | ✓    |
| Support for arbitrary Avalon burst length                                                  | ✓            | ✓    |
| Built-in flexible memory burst adapter                                                     | ✓            | ✓    |
| Configurable Local-to-Memory address mappings                                              | ✓            | ✓    |
| Optional run-time configuration of size and mode register settings, and memory timing      | ✓            | ✓    |
| Partial array self-refresh (PASR)                                                          | ✓            | ✓    |
| Support for industry-standard DDR3 SDRAM devices                                           |              |      |
| Optional support for self-refresh command                                                  | ✓            | ✓    |
| Optional support for user-controlled power-down command                                    | ✓            | ✓    |
| Optional support for automatic power-down command with programmable time-out               | ✓            | ✓    |
| Optional support for auto-precharge read and auto-precharge write commands                 | ✓            | ✓    |
| Optional support for user-controller refresh                                               | ✓            | ✓    |
| Optional multiple controller clock sharing in SOPC Builder Flow                            |              |      |
| Integrated error correction coding (ECC) function 72-bit                                   | ✓            | ✓    |
| Integrated ECC function, 16, 24, and 40-bit                                                | ✓            | ✓    |
| Support for partial-word write with optional automatic error correction                    | ✓            | ✓    |
| SOPC Builder ready                                                                         |              |      |
| Support for OpenCore Plus evaluation                                                       | ✓            | ✓    |
| IP functional simulation models for use in Altera-supported VHDL and Verilog HDL simulator | ✓            | ✓    |

**Notes to Table 15–5:**

- (1) HPC II supports additive latency values greater or equal to  $t_{RCD}-1$ , in clock cycle unit ( $t_{CK}$ ).
- (2) This feature is not supported with DDR3 SDRAM with leveling.

## Unsupported Features

Table 15-6 summarizes unsupported features for Altera's ALTMEMPHY-based external memory interfaces.

**Table 15-6. Unsupported Features**

| Memory Protocol    | Unsupported Feature                                                                 |
|--------------------|-------------------------------------------------------------------------------------|
| DDR and DDR2 SDRAM | Timing simulation                                                                   |
|                    | Burst length of 2                                                                   |
|                    | Partial burst and unaligned burst in ECC and non-ECC mode when DM pins are disabled |
| DDR3 SDRAM         | Timing simulation                                                                   |
|                    | Partial burst and unaligned burst in ECC and non-ECC mode when DM pins are disabled |
|                    | Stratix III and Stratix IV                                                          |
|                    | DIMM support                                                                        |
|                    | Full-rate interfaces                                                                |

## MegaCore Verification

Altera performs extensive random, directed tests with functional test coverage using industry-standard Denali models to ensure the functionality of the DDR, DDR2, and DDR3 SDRAM Controllers with ALTMEMPHY IP.

## Resource Utilization

This section provides typical resource utilization information for the external memory controllers with ALTMEMPHY for supported device families. This information is provided as a guideline only; for precise resource utilization data, you should generate your IP core and refer to the reports generated by the Quartus II software.

Table 15-7 shows resource utilization data for the ALTMEMPHY megafunction, and the DDR3 high-performance controller II for Arria II GX devices.

**Table 15-7. Resource Utilization in Arria II GX Devices (Part 1 of 2)**

| Protocol            | Memory Width (Bits) | Combinational ALUTs | Logic Registers | Mem ALUTs | M9K Blocks | M144K Blocks | Memory (Bits) |
|---------------------|---------------------|---------------------|-----------------|-----------|------------|--------------|---------------|
| <b>Controller</b>   |                     |                     |                 |           |            |              |               |
| DDR3<br>(Half rate) | 8                   | 1,883               | 1,505           | 10        | 2          | 0            | 4,352         |
|                     | 16                  | 1,893               | 1,505           | 10        | 4          | 0            | 8,704         |
|                     | 64                  | 1,946               | 1,521           | 18        | 15         | 0            | 34,560        |
|                     | 72                  | 1,950               | 1,505           | 10        | 17         | 0            | 39,168        |

**Table 15-7. Resource Utilization in Arria II GX Devices (Part 2 of 2)**

| Protocol              | Memory Width (Bits) | Combinational ALUTs | Logic Registers | Mem ALUTs | M9K Blocks | M144K Blocks | Memory (Bits) |
|-----------------------|---------------------|---------------------|-----------------|-----------|------------|--------------|---------------|
| <b>Controller+PHY</b> |                     |                     |                 |           |            |              |               |
| DDR3 (Half rate)      | 8                   | 3,389               | 2,760           | 12        | 4          | 0            | 4,672         |
|                       | 16                  | 3,457               | 2,856           | 12        | 7          | 0            | 9,280         |
|                       | 64                  | 3,793               | 3,696           | 20        | 24         | 0            | 36,672        |
|                       | 72                  | 3,878               | 3,818           | 12        | 26         | 0            | 41,536        |

Table 15-8 shows resource utilization data for the DDR2 high-performance controller and controller plus PHY, for half-rate and full-rate configurations for Arria II GX devices.

**Table 15-8. DDR2 Resource Utilization in Arria II GX Devices**

| Protocol              | Memory Width (Bits) | Combinational ALUTs | Logic Registers | Mem ALUTs | M9K Blocks | M144K Blocks | Memory (Bits) |
|-----------------------|---------------------|---------------------|-----------------|-----------|------------|--------------|---------------|
| <b>Controller</b>     |                     |                     |                 |           |            |              |               |
| DDR2 (Half rate)      | 8                   | 1,971               | 1,547           | 10        | 2          | 0            | 4,352         |
|                       | 16                  | 1,973               | 1,547           | 10        | 4          | 0            | 8,704         |
|                       | 64                  | 2,028               | 1,563           | 18        | 15         | 0            | 34,560        |
|                       | 72                  | 2,044               | 1,547           | 10        | 17         | 0            | 39,168        |
| DDR2 (Full rate)      | 8                   | 2,007               | 1,565           | 10        | 2          | 0            | 2,176         |
|                       | 16                  | 2,013               | 1,565           | 10        | 2          | 0            | 4,352         |
|                       | 64                  | 2,022               | 1,565           | 10        | 8          | 0            | 17,408        |
|                       | 72                  | 2,025               | 1,565           | 10        | 9          | 0            | 19,584        |
| <b>Controller+PHY</b> |                     |                     |                 |           |            |              |               |
| DDR2 (Half rate)      | 8                   | 3,481               | 2,722           | 12        | 4          | 0            | 4,672         |
|                       | 16                  | 3,545               | 2,862           | 12        | 7          | 0            | 9,280         |
|                       | 64                  | 3,891               | 3,704           | 20        | 24         | 0            | 36,672        |
|                       | 72                  | 3,984               | 3,827           | 12        | 26         | 0            | 41,536        |
| DDR2 (Full rate)      | 8                   | 3,337               | 2,568           | 29        | 2          | 0            | 2,176         |
|                       | 16                  | 3,356               | 2,558           | 11        | 4          | 0            | 4,928         |
|                       | 64                  | 3,423               | 2,836           | 31        | 12         | 0            | 19,200        |
|                       | 72                  | 3,445               | 2,827           | 11        | 14         | 0            | 21,952        |

Table 15-9 shows resource utilization data for the DDR2 high-performance controller and controller plus PHY, for half-rate and full-rate configurations for Cyclone III devices.

**Table 15-9. DDR2 Resource Utilization in Cyclone III Devices**

| Protocol              | Memory Width (Bits) | Logic Registers | Logic Cells | M9K Blocks | Memory (Bits) |
|-----------------------|---------------------|-----------------|-------------|------------|---------------|
| <b>Controller</b>     |                     |                 |             |            |               |
| DDR2<br>(Half rate)   | 8                   | 1,513           | 3,015       | 4          | 4,464         |
|                       | 16                  | 1,513           | 3,034       | 6          | 8,816         |
|                       | 64                  | 1,513           | 3,082       | 18         | 34,928        |
|                       | 72                  | 1,513           | 3,076       | 19         | 39,280        |
| DDR2<br>(Full rate)   | 8                   | 1,531           | 3,059       | 4          | 2,288         |
|                       | 16                  | 1,531           | 3,108       | 4          | 4,464         |
|                       | 64                  | 1,531           | 3,134       | 10         | 17,520        |
|                       | 72                  | 1,531           | 3,119       | 11         | 19,696        |
| <b>Controller+PHY</b> |                     |                 |             |            |               |
| DDR2<br>(Half rate)   | 8                   | 2,737           | 5,131       | 6          | 4,784         |
|                       | 16                  | 2,915           | 5,351       | 9          | 9,392         |
|                       | 64                  | 3,969           | 6,564       | 27         | 37,040        |
|                       | 72                  | 4,143           | 6,786       | 28         | 41,648        |
| DDR2<br>(Full rate)   | 8                   | 2,418           | 4,763       | 6          | 2,576         |
|                       | 16                  | 2,499           | 4,919       | 6          | 5,008         |
|                       | 64                  | 2,957           | 5,505       | 15         | 19,600        |
|                       | 72                  | 3,034           | 5,608       | 16         | 22,032        |

## System Requirements

The DDR3 SDRAM Controller with ALTMEMPHY IP is a part of the MegaCore IP Library, which is distributed with the Quartus II software and downloadable from the Altera website, [www.altera.com](http://www.altera.com).

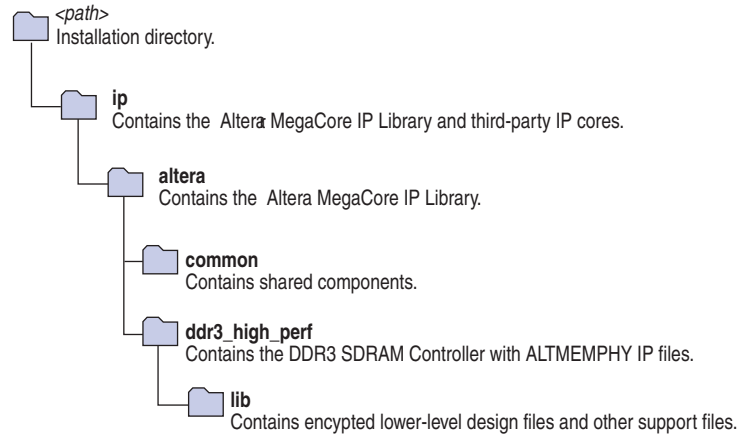


For system requirements and installation instructions, refer to *Altera Software Installation & Licensing*.

## Installation and Licensing

Figure 15-2 shows the directory structure after you install the DDR3 SDRAM Controller with ALTMEMPHY IP, where *<path>* is the installation directory. The default installation directory on Windows is `c:\altera\<version>`; on Linux it is `/opt/altera<version>`.

**Figure 15-2. Directory Structure**



You need a license for the MegaCore function only when you are completely satisfied with its functionality and performance, and want to take your design to production.

To use the DDR3 SDRAM HPC, you can request a license file from the Altera web site at [www.altera.com/licensing](http://www.altera.com/licensing) and install it on your computer. When you request a license file, Altera emails you a **license.dat** file. If you do not have Internet access, contact your local representative.

To use the DDR3 SDRAM HPC II, contact your local sales representative to order a license.

## Free Evaluation

Altera's OpenCore Plus evaluation feature is only applicable to the DDR3 SDRAM HPC. With the OpenCore Plus evaluation feature, you can perform the following actions:

- Simulate the behavior of a megafunction (Altera MegaCore function or AMPP<sup>SM</sup> megafunction) within your system.
- Verify the functionality of your design, as well as evaluate its size and speed quickly and easily.
- Generate time-limited device programming files for designs that include MegaCore functions.
- Program a device and verify your design in hardware.

You need to purchase a license for the megafunction only when you are completely satisfied with its functionality and performance, and want to take your design to production.

## OpenCore Plus Time-Out Behavior

OpenCore Plus hardware evaluation can support the following two modes of operation:

- Untethered—the design runs for a limited time
- Tethered—requires a connection between your board and the host computer. If tethered mode is supported by all megafunctions in a design, the device can operate for a longer time or indefinitely

All megafunctions in a device time-out simultaneously when the most restrictive evaluation time is reached. If there is more than one megafunction in a design, a specific megafunction's time-out behavior may be masked by the time-out behavior of the other megafunctions.



For MegaCore functions, the untethered time-out is 1 hour; the tethered time-out value is indefinite.

Your design stops working after the hardware evaluation time expires and the `local_ready` output goes low.

## Document Revision History

Table 15-10 lists the revision history for this document.

**Table 15-10. Document Revision History**

| Date          | Version | Changes                                                                                                                                                                                      |
|---------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| November 2012 | 1.2     | Changed chapter number from 13 to 15.                                                                                                                                                        |
| June 2012     | 1.1     | Added Feedback icon.                                                                                                                                                                         |
| November 2011 | 1.0     | Combined <a href="#">Release Information</a> , <a href="#">Device Family Support</a> , <a href="#">Features</a> list, and <a href="#">Unsupported Features</a> list for DDR, DDR2, and DDR3. |

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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
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