

## Features

- Fast read access time – 70ns
- Low-power CMOS operation
  - 100µA max standby
  - 30mA max active at 5MHz
- JEDEC standard packages
  - 32-lead PDIP
  - 32-lead PLCC
- 5V ± 10% supply
- High-reliability CMOS technology
  - 2000V ESD protection
  - 200mA latchup immunity
- Rapid programming algorithm – 100µs/byte (typical)
- CMOS- and TTL-compatible inputs and outputs
- Industrial temperature range
- Green (Pb/halide-free) packaging option

## 1. Description

The Atmel® AT27C040 is a low-power, high-performance, 4,194,304-bit, One-Time Programmable, Read-Only Memory (OTP EPROM) organized as 512K by 8 bits. The AT27C040 requires only one 5V power supply in normal Read mode operation. Any byte can be accessed in less than 70ns, eliminating the need for speed reducing wait states on high-performance microprocessor systems.

The Atmel scaled CMOS technology provides low active power consumption and fast programming. Power consumption is typically 8mA in active mode and less than 10µA in standby mode.

The AT27C040 is available in a choice of industry standard, JEDEC-approved, PDIP and PLCC packages. The device features two-line control ( $\overline{CE}$ ,  $\overline{OE}$ ) to eliminate bus contention in high-speed systems.

The AT27C040 has additional features to ensure high quality and efficient production use. The rapid programming algorithm reduces the time required to program the part and guarantees reliable programming. Programming time is typically only 100µs/byte. The integrated product identification code electronically identifies the device and manufacturer. This feature is used by industry standard programming equipment to select the proper programming algorithms and voltages.

## 2. Pin Configurations and Pinouts

Pin Name	Function
V <sub>PP</sub>	Peak to Peak Voltage
A <sub>0</sub> - A <sub>18</sub>	Address Inputs
O <sub>0</sub> - O <sub>7</sub>	Outputs
GND	Ground
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V <sub>CC</sub>	Device Power Supply



## 3. Switching Considerations

Switching between active and standby conditions via the Chip Enable ( $\overline{\text{CE}}$ ) pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device nonconformance. At a minimum, a 0.1 $\mu\text{F}$ , high-frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V<sub>CC</sub> and ground terminals of the device — as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 $\mu\text{F}$  bulk electrolytic capacitor should be utilized, again connected between the V<sub>CC</sub> and ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

## 4. Block Diagram



## 5. Absolute maximum ratings\*

Temperature under bias -55°C to +125°C  
 Storage temperature . . . . . -65°C to +150°C

Voltage on any pin with respect to ground. . . . . -2.0V to +7.0V

Voltage on A<sub>9</sub> with respect to ground . . . . . -2.0V to +14.0V

V<sub>PP</sub> supply voltage with respect to ground. . . . . -2.0V to +14.0V

\*Notice: Stresses beyond those listed under “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## 6. Electrical Characteristics

### 6.1 DC and AC characteristics

Table 6-1. Operating modes

Mode/Pin	$\overline{CE}$	$\overline{OE}$	Ai	V <sub>PP</sub>	Outputs
Read	V <sub>IL</sub>	V <sub>IL</sub>	Ai	X <sup>(1)</sup>	D <sub>OUT</sub>
Output Disable	X	V <sub>IH</sub>	X	X	High Z
Standby	V <sub>IH</sub>	X	X	X	High Z
Rapid Program <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	Ai	V <sub>PP</sub>	D <sub>IN</sub>
PGM Verify	X	V <sub>IL</sub>	Ai	V <sub>PP</sub>	D <sub>OUT</sub>
PGM Inhibit	V <sub>IH</sub>	V <sub>IH</sub>	X	V <sub>PP</sub>	High Z
Product Identification <sup>(4)</sup>	V <sub>IL</sub>	V <sub>IL</sub>	A <sub>9</sub> = V <sub>H</sub> <sup>(3)</sup> A <sub>0</sub> = V <sub>IH</sub> or V <sub>IL</sub> A <sub>1</sub> – A <sub>18</sub> = V <sub>IL</sub>	X	Identification Code

- Notes:
1. X can be V<sub>IL</sub> or V<sub>IH</sub>.
  2. Refer to programming characteristics.
  3. V<sub>H</sub> = 12.0 ± 0.5V.
  4. Two identifier bytes may be selected. All Ai inputs are held low (V<sub>IL</sub>), except A<sub>9</sub>, which is set to V<sub>H</sub>, and A<sub>0</sub>, which is toggled low (V<sub>IL</sub>) to select the manufacturer’s identification byte and high (V<sub>IH</sub>) to select the device code byte.

## 6.2 DC and AC Operating Conditions for Read Operation

	Atmel AT27C040-70	Atmel AT27C040-90
Industrial Operating Temperature (Case)	-40°C to 85°C	-40°C to 85°C
V <sub>CC</sub> Power Supply	5V ± 10%	5V ± 10%

## 6.3 DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0V to V <sub>CC</sub>		±1	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0V to V <sub>CC</sub>		±5	μA
I <sub>PP1</sub> <sup>(2)</sup>	V <sub>PP</sub> <sup>(1)</sup> Read/Standby Current	V <sub>PP</sub> = V <sub>CC</sub>		10	μA
I <sub>SB</sub>	V <sub>CC1</sub> <sup>(1)</sup> Standby Current	I <sub>SB1</sub> (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μA
		I <sub>SB2</sub> (TTL), $\overline{CE} = 2.0$ to V <sub>CC</sub> + 0.5V		1	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current	f = 5MHz, I <sub>OUT</sub> = 0mA, $\overline{CE} = V_{IL}$		30	mA
V <sub>IL</sub>	Input Low Voltage		-0.6	0.8	V
V <sub>IH</sub>	Input High Voltage		2.0	V <sub>CC</sub> + 0.5	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4		V

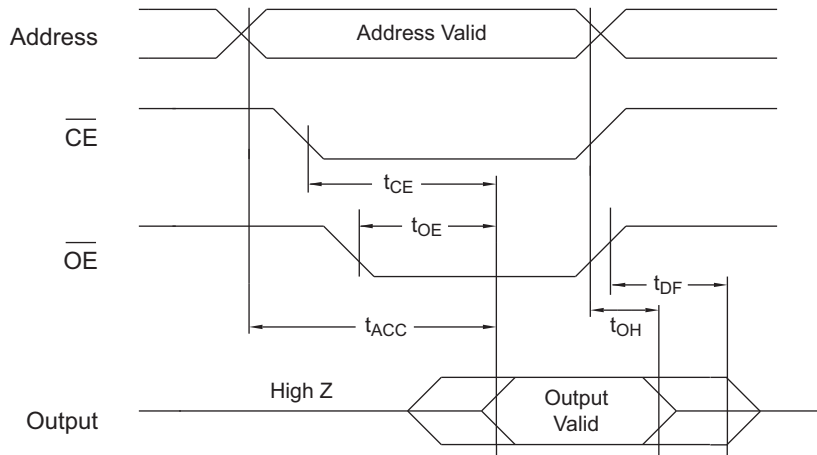
- Notes: 1. V<sub>CC</sub> must be applied simultaneously with or before V<sub>PP</sub>, and removed simultaneously with or after V<sub>PP</sub>.  
 2. V<sub>PP</sub> may be connected directly to V<sub>CC</sub>, except during programming. The supply current would then be the sum of I<sub>CC</sub> and I<sub>PP</sub>.

## 6.4 AC Characteristics for Read Operation

Symbol	Parameter	Condition	Atmel AT27C040				Units
			-70		-90		
			Min	Max	Min	Max	
t <sub>ACC</sub> <sup>(1)</sup>	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		70		90	ns
t <sub>CE</sub> <sup>(1)</sup>	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		70		90	ns
t <sub>OE</sub> <sup>(1)</sup>	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		30		35	ns
t <sub>DF</sub> <sup>(1)</sup>	$\overline{OE}$ or $\overline{CE}$ High to Output Float; whichever occurred first.			20		20	ns
t <sub>OH</sub>	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ ; whichever occurred first.		0		0		ns

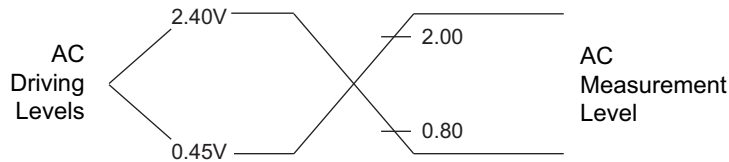
- Note: 1. See AC waveforms for read operation.

**Figure 6-1. AC Waveforms for Read Operation<sup>(1)</sup>**

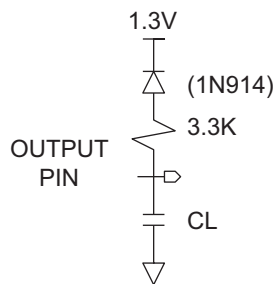


- Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V, unless otherwise specified.
  2.  $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
  3.  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the address is valid without impact on  $t_{ACC}$ .
  4. This parameter is only sampled, and is not 100% tested.
  5. Output float is defined as the point when data is no longer driven.

**Figure 6-2. Input Test Waveforms and Measurement Levels**



**Figure 6-3. Output Test Load**



**Table 6-2. Pin Capacitance**

f = 1MHz, T = 25°C<sup>(1)</sup>

Symbol	Typ	Max	Units	Conditions
$C_{IN}$	4	8	pF	$V_{IN} = 0V$
$C_{OUT}$	8	12	pF	$V_{OUT} = 0V$

- Note:
1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

**Figure 6-4. Programming Waveforms<sup>(1)</sup>**



- Notes:
1. The input timing reference is 0.8V for  $V_{IL}$  and 2.0V for  $V_{IH}$ .
  2.  $t_{OE}$  and  $t_{DFP}$  are characteristics of the device, but must be accommodated by the programmer.
  3. When programming the AT27C040, a 0.1 $\mu$ F capacitor is required across  $V_{PP}$  and ground to suppress spurious voltage transients.

**Table 6-3. DC Programming Characteristics**

$T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $V_{PP} = 13.0 \pm 0.25\text{V}$ .

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
$I_{LI}$	Input Load Current	$V_{IN} = V_{IL}, V_{IH}$		$\pm 10$	$\mu\text{A}$
$V_{IL}$	Input Low Level		-0.6	0.8	V
$V_{IH}$	Input High Level		2.0	$V_{CC} + 0.7$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 2.1\text{mA}$		0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = -400\mu\text{A}$	2.4		V
$I_{CC2}$	$V_{CC}$ Supply Current (Program And Verify)			40	mA
$I_{PP2}$	$V_{PP}$ Supply Current	$\overline{CE} = V_{IL}$		20	mA
$V_{ID}$	$A_9$ Product Identification Voltage		11.5	12.5	V

**Table 6-4. AC Programming Characteristics** $T_A = 25 \pm 5^\circ\text{C}$ ,  $V_{CC} = 6.5 \pm 0.25\text{V}$ ,  $V_{PP} = 13.0 \pm 0.25\text{V}$ 

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Limits		Units
			Min	Max	
$t_{AS}$	Address Setup Time	Input rise and fall times: (10% to 90%) 20ns	2		$\mu\text{s}$
$t_{OES}$	$\overline{OE}$ Setup Time		2		$\mu\text{s}$
$t_{DS}$	Data Setup Time		2		$\mu\text{s}$
$t_{AH}$	Address Hold Time	Input pulse levels: 0.45V to 2.4V	0		$\mu\text{s}$
$t_{DH}$	Data Hold Time		2		$\mu\text{s}$
$t_{DFP}$	$\overline{OE}$ High to Output Float Delay <sup>(2)</sup>		0	130	ns
$t_{VPS}$	$V_{PP}$ Setup Time	Input timing reference level: 0.8V to 2.0V	2		$\mu\text{s}$
$t_{VCS}$	$V_{CC}$ Setup Time		2		$\mu\text{s}$
$t_{PW}$	$\overline{CE}$ Program Pulse Width <sup>(3)</sup>	Output timing reference level: 0.8V to 2.0V	95	105	$\mu\text{s}$
$t_{OE}$	Data Valid from $\overline{OE}$ <sup>(2)</sup>			150	ns
$t_{PRT}$	$V_{PP}$ Pulse Rise Time During Programming		50		ns

- Notes: 1.  $V_{CC}$  must be applied simultaneously with or before  $V_{PP}$  and removed simultaneously with or after  $V_{PP}$ .  
2. This parameter is only sampled, and is not 100% tested. Output float is defined as the point where data is no longer driven. See timing diagram.  
3. Program pulse width tolerance is  $100\mu\text{s} \pm 5\%$ .

**Table 6-5. Atmel AT27C040 Integrated Product Identification Code**

Codes	Pins									Hex Data
	A <sub>0</sub>	O <sub>7</sub>	O <sub>6</sub>	O <sub>5</sub>	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>0</sub>	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

## 7. Rapid programming algorithm

A  $100\mu\text{s}$   $\overline{\text{CE}}$  pulse width is used to program. The address is set to the first location.  $V_{\text{CC}}$  is raised to 6.5V and  $V_{\text{PP}}$  is raised to 13.0V. Each address is first programmed with one  $100\mu\text{s}$   $\overline{\text{CE}}$  pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to ten successive  $100\mu\text{s}$  pulses are applied with a verification after each pulse. If the byte fails to verify after ten pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked.  $V_{\text{PP}}$  is then lowered to 5.0V and  $V_{\text{CC}}$  to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.

Figure 7-1. Rapid Programming Algorithm





## 8. Ordering Information

### Green Package Option (Pb/Halide-free)

Atmel Ordering Code	Package	$t_{ACC}$ (ns)	$I_{CC}$ (mA)		Lead Finish	Operation Range
			Active	Standby		
AT27C040-70JU	32J	70	30	0.1	Matte Tin	Industrial (-40°C to 85°C)
AT27C040-70PU	32P6					
AT27C040-90JU	32J	90	30	0.1	Matte Tin	Industrial (-40°C to 85°C)
AT27C040-90PU	32P6					

Package Type	
32J	32-lead, plastic, J-leaded Chip Carrier (PLCC)
32P6	32-lead, 0.600" wide, plastic, Dual Inline (PDIP)

## 9. Package information

### 9.1 32J — 32-lead PLCC



## 9.2 32P6 — 32-lead PDIP



11/28/11

**Atmel**

Package Drawing Contact:  
packagedrawings@atmel.com

**TITLE**  
32P6, 32-lead, 0.600"/15.24 mm Wide Plastic Dual  
Inline Package (PDIP)

**GPC**  
PLU

**DRAWING NO.**  
32P6

**REV.**  
C

## 10. Revision History

Doc. Rev.	Date	Comments
0189J	10/2012	Update 32P6 package outline drawing. Update template and Atmel logo.
0189I	04/2011	Remove TSOP package. Add lead finish to ordering information.
0189H	12/2007	Datasheet revision.



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