N-Channel 150-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
150	0.052 at V_{GS} = 10 V	25
	0.060 at V_{GS} = 6 V	23

FEATURES

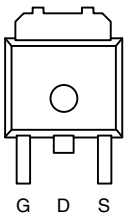
- TrenchFET® Power MOSFET
- 175 °C Junction Temperature
- PWM Optimized
- 100 % R_g Tested
- Compliant to RoHS Directive 2002/95/EC

RoHS COMPLIANT

APPLICATIONS

- Primary Side Switch

TO-252

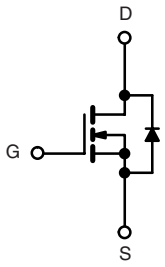


Drain Connected to Tab

Top View

Ordering Information:

SUD25N15-52-E3 (Lead (Pb)- free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-Source Voltage		V_{DS}	150	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 175 °C)[b]	T_C = 25 °C	I_D	25	A
	T_C = 125 °C		14.5	
Pulsed Drain Current		I_{DM}	50	
Continuous Source Current (Diode Conduction)		I_S	25	
Avalanche Current		I_{AR}	25	
Repetitive Avalanche Energy (Duty Cycle ≤ 1 %)	L = 0.1 mH	E_{AR}	31	mJ
Maximum Power Dissipation	T_C = 25 °C	P_D	136[b]	W
	T_A = 25 °C		3[a]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 175	°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	15	18	°C/W
	Steady State		40	50	
Junction-to-Case (Drain)		R_{thJC}	0.85	1.1	

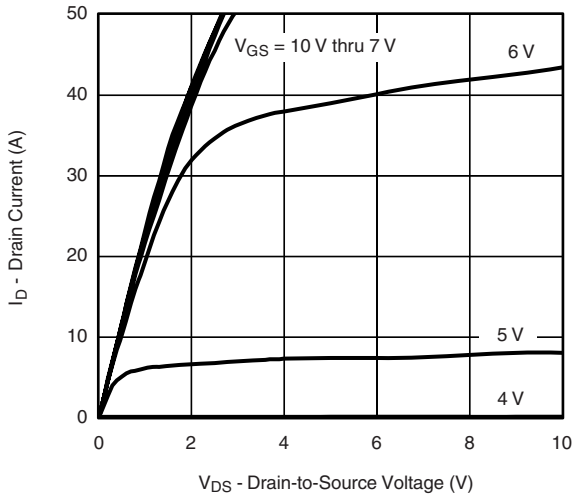
Notes:
a. Surface Mounted on 1" x 1" FR4 board.
b. See SOA curve for voltage derating.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.[a]**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA	150			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2		4	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 150 V, V_{GS} = 0 V			1	µA
		V_{DS} = 150 V, V_{GS} = 0 V, T_J = 125 °C			50	
		V_{DS} = 150 V, V_{GS} = 0 V, T_J = 175 °C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5 A		0.042	0.052	Ω
		V_{GS} = 10 V, I_D = 5 A, T_J = 125 °C			0.109	
		V_{GS} = 10 V, I_D = 5 A, T_J = 175 °C			0.145	
		V_{GS} = 6 V, I_D = 5 A		0.047	0.060	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 25 A		40		S
Dynamic[a]						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		1725		pF
Output Capacitance	C_{oss}			216		
Reverse Transfer Capacitance	C_{rss}			100		
Total Gate Charge[c]	Q_g	V_{DS} = 75 V, V_{GS} = 10 V, I_D = 25 A		33	40	nC
Gate-Source Charge[c]	Q_{gs}			9		
Gate-Drain Charge[c]	Q_{gd}			12		
Gate Resistance	R_g		1		3	Ω
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 50 V, R_L = 3 Ω I_D ≅ 25 A, V_{GEN} = 10 V, R_g = 2.5 Ω		15	25	ns
Rise Time[c]	t_r			70	100	
Turn-Off Delay Time[c]	$t_{d(off)}$			25	40	
Fall Time[c]	t_f			60	90	
Source-Drain Diode Ratings and Characteristics T_C = 25 °C						
Pulsed Current	I_{SM}				50	A
Diode Forward Voltage[b]	V_{SD}	I_F = 25 A, V_{GS} = 0 V		0.9	1.5	V
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 25 A, dI/dt = 100 A/µs		95	140	ns

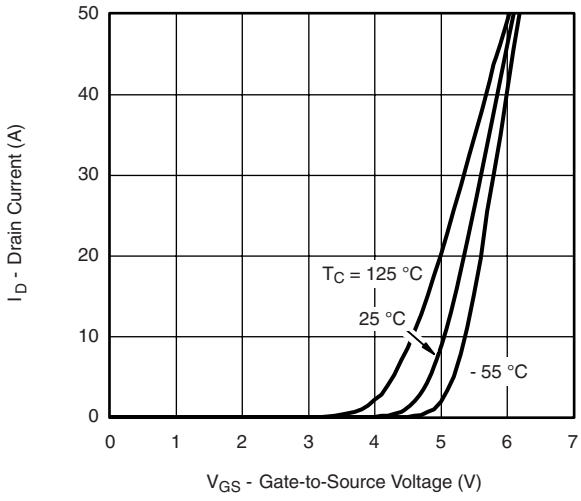
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

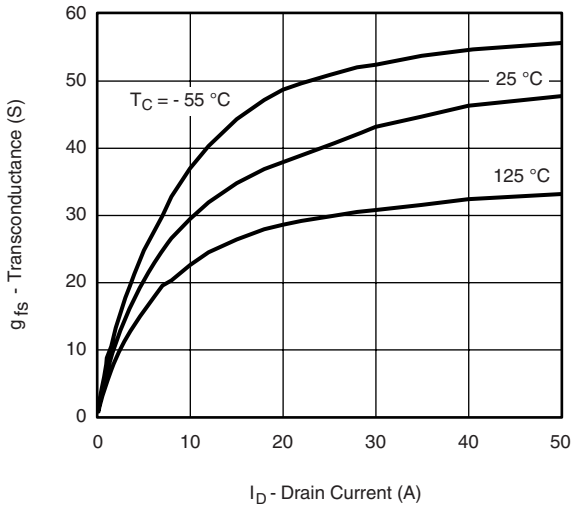
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



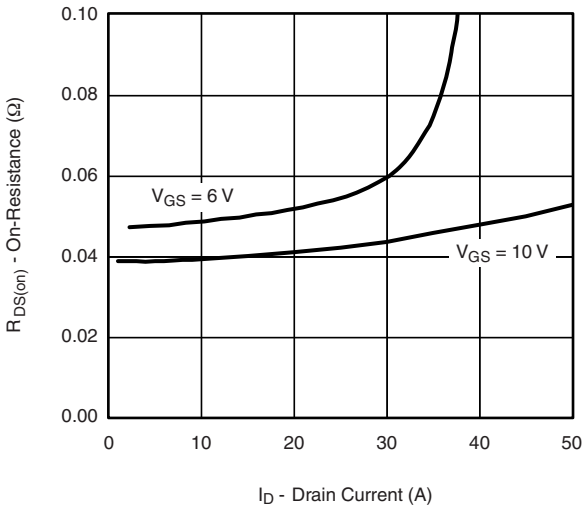
Output Characteristics



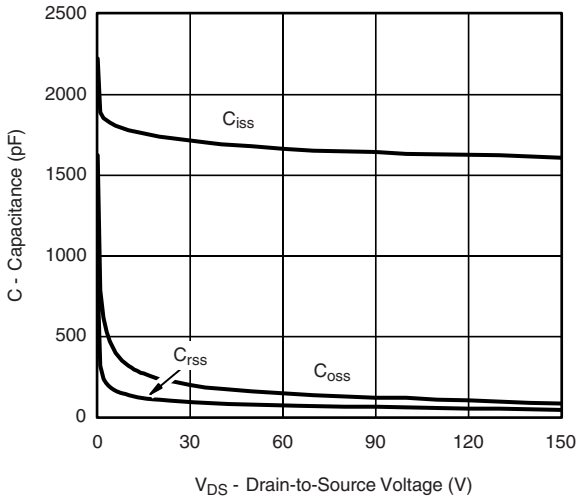
Transfer Characteristics



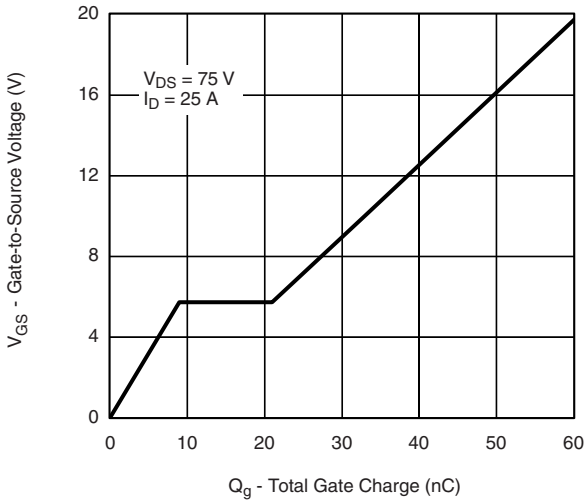
Transconductance



On-Resistance vs. Drain Current

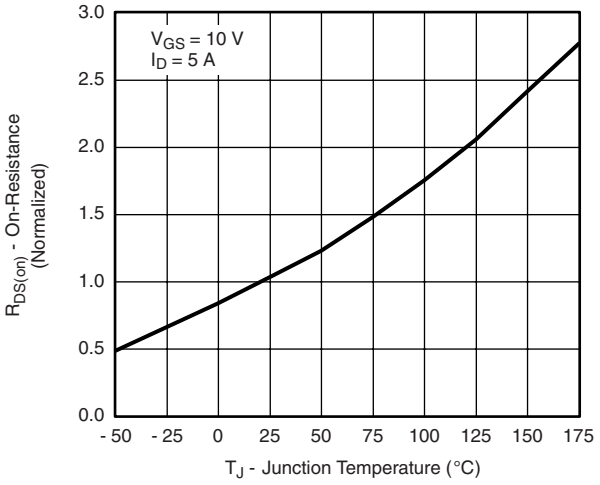


Capacitance

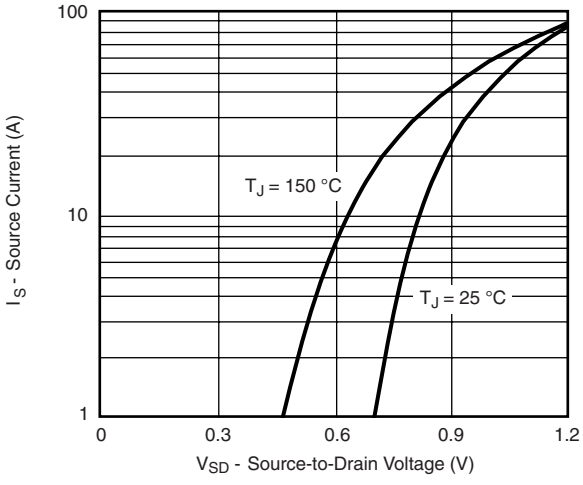


Gate Charge

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

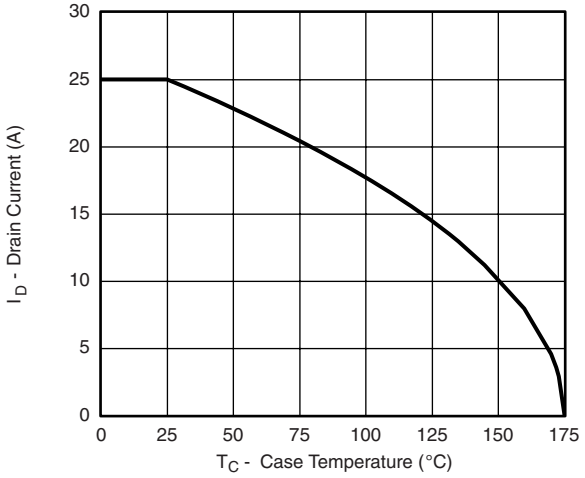


On-Resistance vs. Junction Temperature

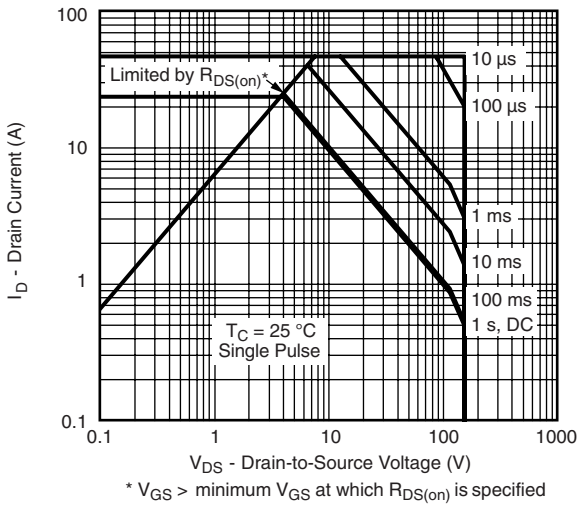


Source-Drain Diode Forward Voltage

THERMAL RATINGS

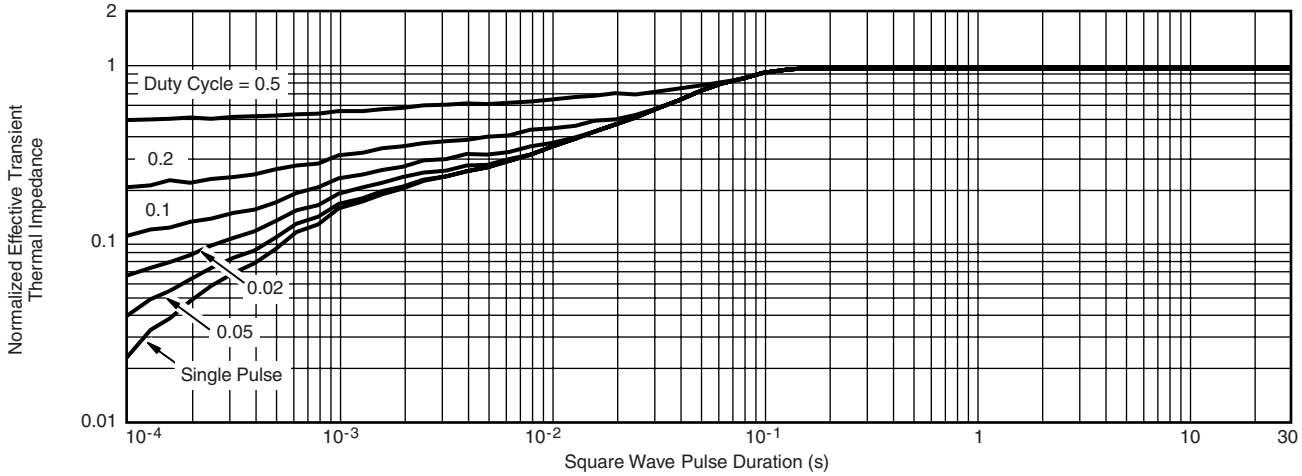


Maximum Avalanche Drain Current vs. Case Temperature



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

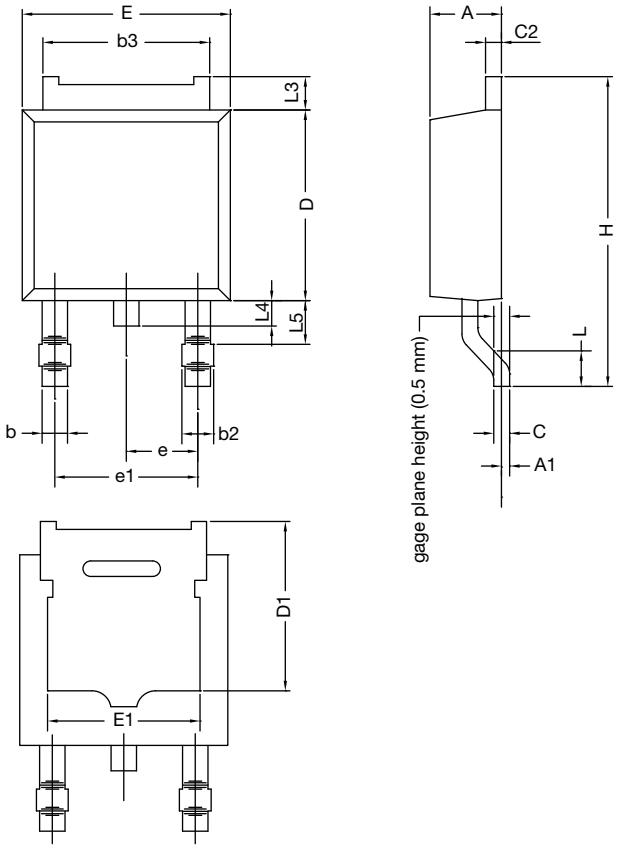
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71768.

TO-252AA CASE OUTLINE



	MILLIMETERS		INCHES	
DIM.	**MIN.**	**MAX.**	**MIN.**	**MAX.**
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347				

Note

- Dimension L3 is for reference only.

For technical questions, contact: pmostechsupport@vishay.com

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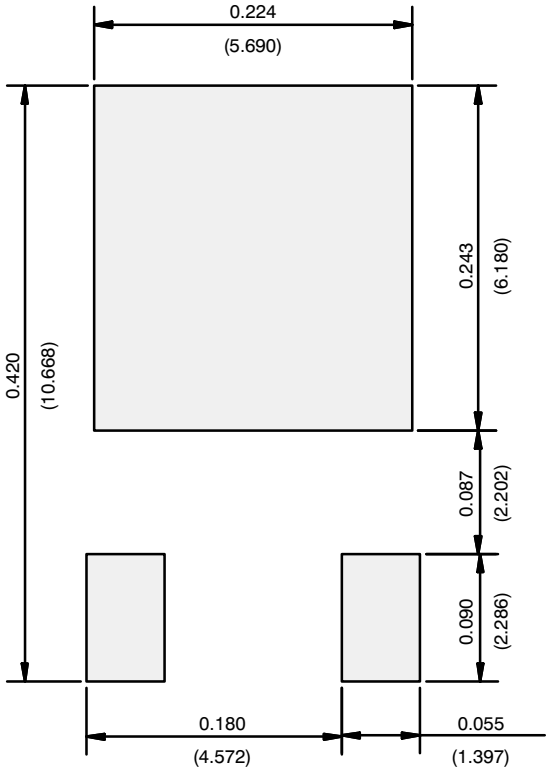
RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

APPLICATION NOTE

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- *Оценку стоимости проекта по компонентам.*
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