SEMTECH
GENNUM PRODUCTS

GS3440

Extended Reach 3G/HD/SD Adaptive Cable Equalizer

Key Features

- SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259 compliant
- Automatic cable equalization
- Multi-standard operation from 125Mb/s to 2.97Gb/s
- Performance optimized for 270Mb/s, 1.485Gb/s and 2.97Gb/s. Typical equalized length of Belden 1694A cable up to:
  - 210m at 2.97Gb/s
  - 300m at 1.485Gb/s
  - 600m at 270Mb/s
- Supports DVB-ASI at 270Mb/s
- Supports MADI at 125Mb/s
- Manual bypass (useful for low data rates with slow rise/fall times)
- Programmable carrier detect with squelch threshold adjustment
- Automatic sleep on loss of signal
  - Sleep mode power <30mW (typical)
- Differential outputs support DC-coupling from 1.2V to 3.3V CML logic
- Option to compensate for 6dB flat attenuation prior to input of device
- Selectable output de-emphasis: 2dB, 4dB and 6dB
- Standard EIA/JEDEC logic control and status signal levels
- Single 3.3V power supply operation
- 169mW power consumption (typical)
- Wide operating temperature range of -40°C to +85°C
- Small footprint QFN package (4mm x 4mm)
  - Footprint compatible with the GS2974A, GS2974B, GS2984 and GS2994
- Pb-free and RoHS compliant

Applications

- SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259 coaxial cable serial digital interfaces

Description

The GS3440 is a high-speed BiCMOS device designed to equalize and restore signals received over 75Ω coaxial cable.

The device is designed to support SMPTE ST 424, SMPTE ST 292 and SMPTE ST 259, and is optimized for performance at 270Mb/s, 1.485Gb/s and 2.97Gb/s.

The GS3440 features DC restoration to compensate for the DC content of SMPTE pathological test patterns.

The Carrier Detect output pin ($\overline{CD}$) indicates whether a valid input signal has been detected. It can be connected directly to the SLEEP pin to enable automatic sleep on loss of carrier.

A voltage programmable threshold, set via the SQ_ADJ pin, forces $\overline{CD}$ high when the input signal amplitude falls below the threshold. This allows the GS3440 to distinguish between low-amplitude SDI signals and noise at the input of the device.

The equalizing and DC restore stages are disengaged and no equalization occurs when the BYPASS pin is HIGH. Setting the BYPASS pin HIGH is useful for signals launched at the signal source with low data rates and/or slow rise/fall times.

The GS3440 features a gain selection pin (GAIN_SEL) which can be used to compensate for 6dB flat attenuation prior to the input of the device.

The differential outputs can be DC-coupled to Gennum reclockers and cable drivers, as well as industry-standard 1.2V, 1.8V, 2.5V and 3.3V CML logic by changing the voltage applied to the VCC_O pin. In general, DC-coupling to any termination voltage between 1.2V and 3.3V is supported.

The GS3440 also features programmable output de-emphasis with three, user-selectable operating levels to support long PCB traces at the output of the device.

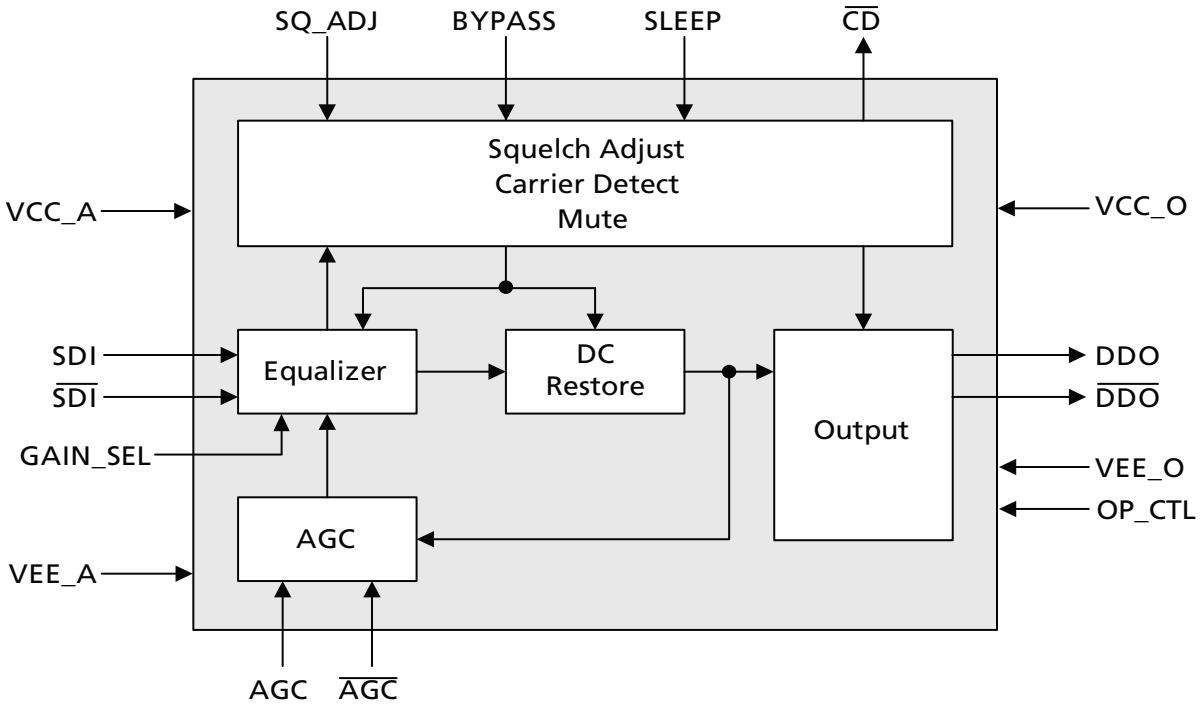
Description (continued)

The device comes in a 16-pin, 4mm x 4mm QFN package and is footprint compatible with Gennum's GS2974A, GS2974B, GS2984 and GS2994 equalizers.

Power consumption of the GS3440 is typically 169mW when DC-coupled at 1.2V.

The GS3440 is Pb-free, and the encapsulation compound does not contain halogenated flame retardant.

This component and all homogeneous subcomponents are RoHS compliant.



GS3440 Functional Block Diagram

Contents

1. Pin Out

1.1 GS3440 Pin Assignment

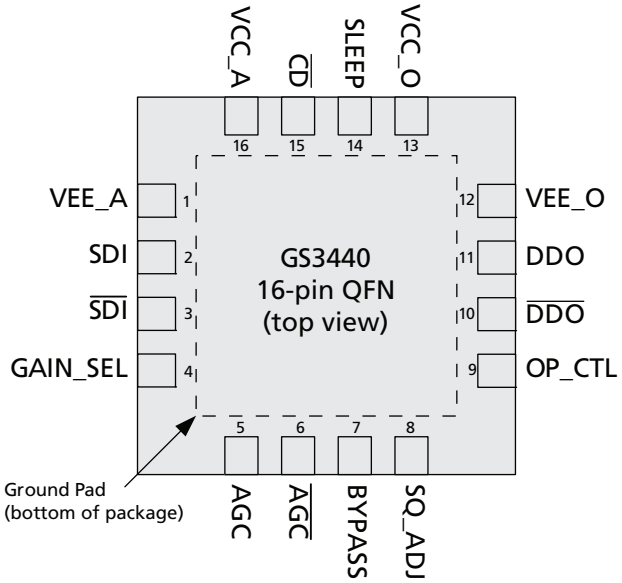


Figure 1-1: GS3440 Pin Out

1.2 GS3440 Pin Descriptions

Table 1-1: GS3440 Pin Descriptions

Pin Number	Name	Timing	Type	Description
1	VEE_A	Analog	Power	Most negative power supply connection for the input buffer, core and control circuits. Connect to GND.
2, 3	SDI, $\overline{SDI}$	Analog	Input	Serial digital differential input.
4	GAIN_SEL	Not Synchronous	Input	Input Sensitivity Control. Signal levels are LVCMOS/LVTTL compatible. This pin is a 2.5V input that is tolerant to 3.3V levels. When HIGH, the device compensates for an additional 6dB of loss across the entire operating band. This pin has an internal pull-down resistor.
5, 6	AGC, $\overline{AGC}$	Analog	–	External AGC capacitor connection.
7	BYPASS	Not Synchronous	Input	Core Bypass Control. Signal levels are LVCMOS/LVTTL compatible. This pin is a 2.5V input that is tolerant to 3.3V levels. Forces the equalizer and DC-restore stages into Bypass mode when HIGH. No equalization occurs in this mode. This pin has an internal pull-down resistor.

Table 1-1: GS3440 Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
8	SQ_ADJ	Analog	Input	Squelch Threshold Adjust. Adjusts the input signal amplitude threshold of the carrier detect function. The serial data output of the device can be muted when the serial data input signal amplitude is too low by connecting the $\overline{CD}$ and OP_CTL pins using a suitable resistor network (see Figure 4-2 and Figure 4-3). This pin has an internal pull-down resistor. NOTE: The SQ_ADJ function is only available when the device is not in auto-sleep mode. Reference Section 4.5 for more detail.
9	OP_CTL	Not Synchronous	Input	Controls the Output Swing, De-emphasis and Mute Features of the DDO/$\overline{DDO}$ outputs. When this pin is connected to GND, the output swing is 800mV with no de-emphasis applied to the output signal. With this pin connected to 2.5V, the output is muted. Intermediate voltages and functions are shown in Table 4-5. These voltages can be achieved as shown in Figure 4-2 and Figure 4-3. This pin has an internal pull-down resistor.
10, 11	$\overline{DDO}$, DDO	Analog	Output	Serial digital differential output.
12	VEE_O	Analog	Power	Most negative power supply connection for the output buffer. Connect to GND.
13	VCC_O	Analog	Power	Most positive power supply connection for the output buffer. Connect to 1.2V - 3.3V DC.
14	SLEEP	Not Synchronous	Input	SLEEP Control. Signal levels are LVCMOS/LVTTL compatible. This pin is a 2.5V input that is tolerant to 3.3V levels. When HIGH the part is powered-down except for the Carrier Detect function. This pin can be connected directly to the $\overline{CD}$ pin to automatically put the device to sleep (low-power operation) on loss of carrier. This pin has an internal pull-down resistor. **NOTE**: When SLEEP is connected to $\overline{CD}$ for automatic power reduction on loss of carrier, the SQ_ADJ pin will not modify the $\overline{CD}$ threshold. The $\overline{CD}$ threshold will revert to the default value used when SQ_ADJ is pulled LOW.
15	$\overline{CD}$	Not Synchronous	Output	Carrier Detect Status Output. Signal levels are LVCMOS/LVTTL compatible. This pin is a 2.5V output. Indicates presence of a good input signal. When the $\overline{CD}$ pin is LOW, a signal has been detected at the input. When this pin is HIGH, this indicates loss of input signal.
16	VCC_A	Analog	Power	Most positive power supply connection for the input buffer, core and control circuits. Connect to +3.3V DC.
–	Center Pad	–	Power	Internally bonded to VEE_A. Connect to GND with at least 5 VIAs.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value
Supply Voltage - Core/Output Driver	-0.5V to +3.6V DC
Input ESD Voltage (HBM)	5kV
Storage Temperature Range (T_s)	-50°C to 125°C
Input Voltage Range (any input)	-0.3 to (V_{CC_A} +0.3)V
Operating Temperature Range	-40°C to +85°C
Solder Reflow Temperature	260°C

NOTE: Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 DC Electrical Characteristics

Table 2-1: DC Electrical Characteristics

V_{CC_A} = 3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage - Core	V_{CC_A}	–	3.135	3.3	3.465	V	–
Supply Voltage - Output Driver	V_{CC_O}	–	1.14	1.2	1.26	V	1
		–	2.375	2.5	2.625	V	1
		–	3.135	3.3	3.465	V	1
Power Consumption	P_D	T_A = 25°C V_{CC_O} = 1.2V ΔV_{DDO} = 400mV	–	169	–	mW	2
		T_A = 25°C V_{CC_O} = 1.2V ΔV_{DDO} = 800mV	–	182	–	mW	2
		T_A = 25°C V_{CC_O} = 3.3V ΔV_{DDO} = 400mV	–	192	–	mW	2
		T_A = 25°C V_{CC_O} = 3.3V ΔV_{DDO} = 800mV	–	225	–	mW	2
Supply Current - Core	I_s	T_A = 25°C	–	49	–	mA	2, 3

Table 2-1: DC Electrical Characteristics (Continued)

V_{CC_A} = 3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Current - Output Driver	$I_{Output\ Driver}$	T_A = 25°C ΔV_{DDO} = 800mV	–	19	–	mA	2
		T_A = 25°C ΔV_{DDO} = 400mV	–	10	–	mA	2
Input Common Mode Voltage	V_{CMIN}	T_A = 25°C	1.62	1.71	1.80	V	–
$\overline{CD}$ Output Voltage	$V_{\overline{CD}(OH)}$	Carrier not present	2.0	–	–	V	–
	$V_{\overline{CD}(OL)}$	Carrier present	–	–	0.4	V	–
Input Voltage - Digital pins	V_{GAIN_SEL} V_{BYPASS} V_{SLEEP}	Minimum to assert	1.7	–	–	V	4
		Maximum to de-assert	–	–	0.7	V	4

NOTES:

1. V_{CC_O} operates from 1.2V through 3.3V (+/-5%).
2. De-emphasis off.
3. An additional 3mA when de-emphasis is enabled.
4. GAIN_SEL, BYPASS, SLEEP pins are 2.5V, but 3.3V tolerant.

2.3 AC Electrical Characteristics

Table 2-2: AC Electrical Characteristics

V_{CC_A} = 3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Serial input data rate	DR_{DDO}	–	125	–	2970	Mb/s	1
Input Voltage Swing	ΔV_{SDI}	T_A =25°C, differential, 270Mb/s and 1.485Gb/s	720	800	950	mV_{p-p}	2
		T_A =25°C, differential, 2.97Gb/s	720	800	880	mV_{p-p}	2
Output Voltage Swing	ΔV_{DDO}	100Ω load, T_A =25°C, differential, OP_CTL set for high swing	–	800	–	mV_{p-p}	–
		100Ω load, T_A =25°C, differential, OP_CTL set for low swing	–	400	–	mV_{p-p}	–

Table 2-2: AC Electrical Characteristics (Continued)

V_{CC_A} = 3.3V ±5%, T_A = -40°C to +85°C, unless otherwise shown

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Output Jitter at Various Cable Lengths and Data Rates	–	2.97Gb/s Belden 1694A: 0-120m	–	–	0.25	UI	3, 4, 5
	–	2.97Gb/s Belden 1694A: 120-160m	–	–	0.3	UI	3, 4, 5
	–	2.97Gb/s Belden 1694A: 160-180m	–	–	0.4	UI	3, 4, 5
	–	2.97Gb/s Belden 1694A: 180-200m	–	–	0.5	UI	3, 4, 5
	–	2.97Gb/s Belden 1694A: 200-210m	–	0.5	–	UI	3, 4, 5
	–	1.485Gb/s Belden 1694A: 0-200m	–	–	0.2	UI	3, 4, 5
	–	1.485Gb/s Belden 1694A: 200-260m	–	–	0.3	UI	3, 4, 5
	–	1.485Gb/s Belden 1694A: 260-300m	–	0.3	–	UI	3, 4, 5
	–	270Mb/s Belden 1694A: 0-300m	–	0.1	0.15	UI	3, 4, 5
	–	270Mb/s Belden 1694A: 300-550m	–	–	0.25	UI	3, 4, 5
Output Rise/Fall time	–	2.97Gb/s & 1.485Gb/s 20% - 80%	–	75	–	ps	–
	–	270Mb/s 20% - 80%	–	150	–	ps	–
Mismatch in rise/fall time	–	–	–	–	30	ps	–
Duty cycle distortion	–	SD/HD/3G	–	–	30	ps	–
Overshoot	–	–	–	–	10	%	–
Input Return Loss	–	5MHz - 1.485GHz	15	–	–	dB	–
	–	1.485GHz - 2.97GHz	10	–	–	dB	–
Input Resistance	–	single-ended	–	1.9	–	kΩ	–
Input Capacitance	–	single-ended	–	1.3	–	pF	–
Output Resistance	–	single-ended	–	50	–	Ω	–

NOTES:

1. Device performance is optimized for standard data rates (SD = 270Mb/s, HD = 1.485Gb/s, 3G = 2.970Gb/s)
2. 0m cable length.
3. All parts are production tested. In order to guarantee jitter over the full range of specification (V_{CC_A} = 3.3V ±5%, T_A = -40°C to +85°C, and 720-880mV launch swing from the SDI cable driver) the recommended applications circuit must be used.
4. Based on validation data using the recommended applications circuit, at V_{CC_A} = 3.3V, T_A = 25°C and 800mV launch swing from the SDI cable driver.
5. GAIN_SEL = 0.

3. Input/Output Circuits

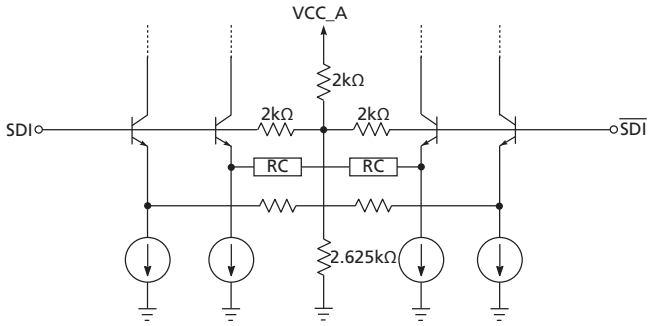


Figure 3-1: Input Circuit

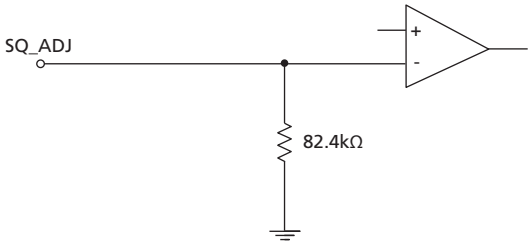


Figure 3-2: SQ_ADJ Circuit

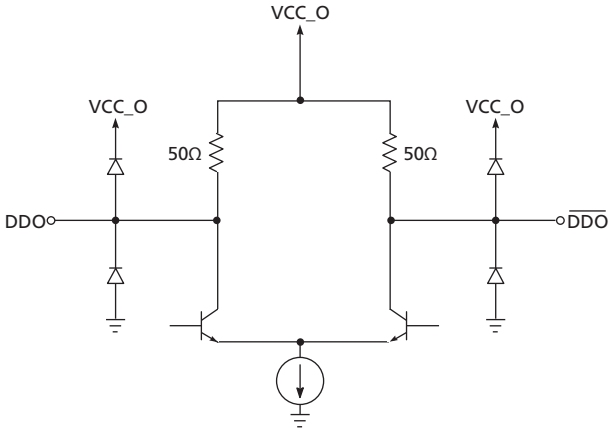


Figure 3-3: Output Circuit

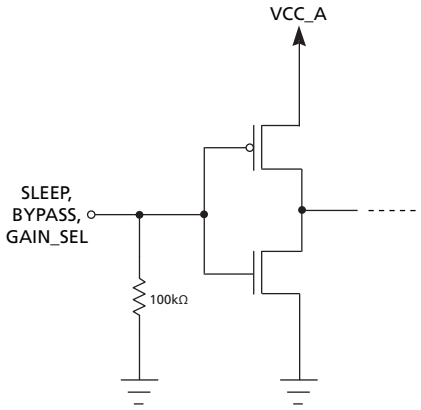


Figure 3-4: SLEEP, BYPASS and GAIN_SEL Circuits

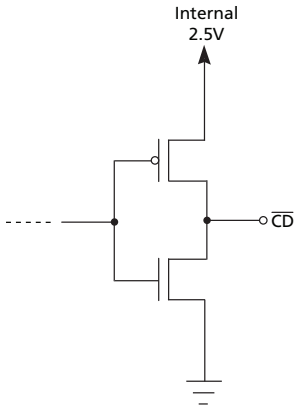


Figure 3-5: $\overline{CD}$ Circuit

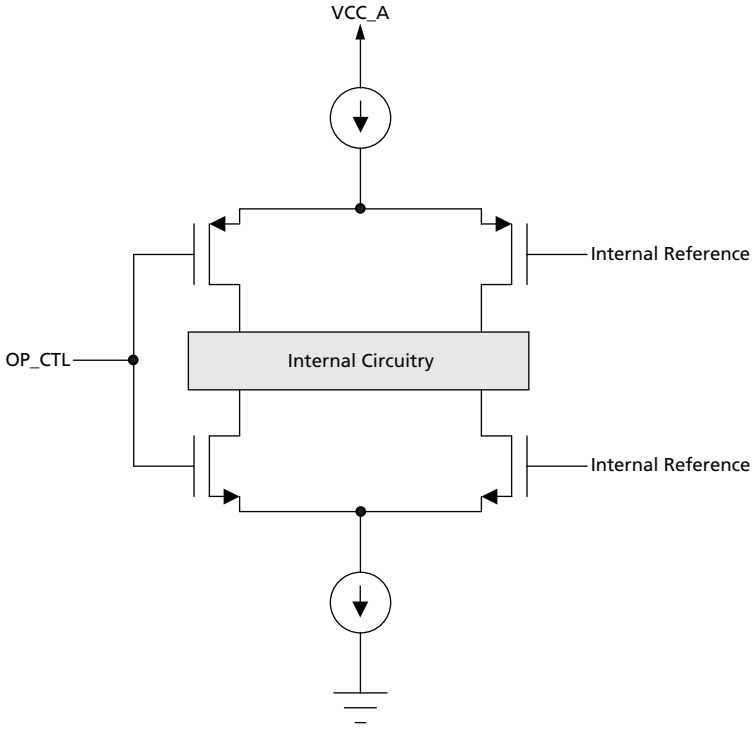


Figure 3-6: OP_CTL

4. Detailed Description

The GS3440 is a high-speed BiCMOS IC designed to equalize serial digital signals.

The GS3440 can equalize 3Gb/s, HD and SD serial digital signals, and will typically equalize up to 210m of Belden 1694A cable at 2.97Gb/s, 300m at 1.485Gb/s, and 600m at 270Mb/s. The GS3440 can be powered from a single +3.3V DC power supply, and is footprint-compatible with Gennum's GS2974A, GS2974B, GS2984, and GS2994 equalizers. When DC coupling the output of a device to a 1.2V CML load, the GS3440 typically consumes 169mW of power.

4.1 Serial Digital Inputs

The received serial data signal can be connected to the input pins (SDI/$\overline{\text{SDI}}$) in either a differential or single-ended configuration. AC-coupling of the inputs is recommended, because the SDI and $\overline{\text{SDI}}$ inputs are internally biased to approximately 1.71V.

4.2 Automatic (Adaptive) Cable Equalization

The input signal passes through a variable gain equalizing stage, whose frequency response closely matches the inverse of the cable (Belden 1694A) loss characteristic. In addition, the variation of the frequency response with control voltage imitates the variation of the inverse cable loss characteristic with cable length ensuring that the correct amount of gain is automatically applied to the input signal for any cable length within the supported ranges.

The equalized signal is DC-restored, effectively restoring the logic threshold of the equalized signal to its correct level independent of shifts due to AC-coupling.

4.3 Differential Digital Data Output

The GS3440 features a differential data output. The digital data output signals (DDO/$\overline{\text{DDO}}$) have a nominal output voltage swing of either 800mV$_{ppd}$ or 400mV$_{ppd}$, as set by the OP_CTL pin. Table 4-1 shows the typical output common mode voltage levels related to the two output swing options and the chosen coupling (DC vs. AC).

Table 4-1: Typical Common Mode Output Voltage Levels

Supply Voltage (VCC_O)	400mV$_{p-p}$ Swing (DC-coupled Output)	400mV$_{p-p}$ Swing (AC-coupled Output)	800mV$_{p-p}$ Swing (DC-coupled Output)	800mV$_{p-p}$ Swing (AC-coupled Output)
3.3V	3.2V	3.1V	3.1V	2.9V
2.5V	2.4V	2.3V	2.3V	2.1V
1.8V	1.7V	1.6V	1.6V	1.4V
1.2V	1.1V	1.0V	1.0V	0.8V

4.4 Programmable Squelch Adjust (SQ_ADJ)

The GS3440 features a programmable Squelch Adjust (SQ_ADJ) threshold.

This feature can be useful in applications where there are multiple input channels using the GS3440 and the maximum gain can be limited to avoid crosstalk.

The SQ_ADJ pin acts to change the threshold of the Carrier Detect ($\overline{CD}$) pin. When the input signal drops below the threshold set by SQ_ADJ, the $\overline{CD}$ pin will be driven HIGH, indicating that there is not a valid input signal. In applications where programmable squelch adjust is not required, the SQ_ADJ pin can be left unconnected.

This feature has been designed for use in applications such as routers, where signal crosstalk and circuit noise cause the equalizer to output erroneous data when no input signal is present. The use of a Carrier Detect function with a fixed internal reference does not solve this problem, since the signal-to-noise ratio on the circuit board could be significantly less than the default signal detection level set by the on-chip reference.

NOTE: When using SQ_ADJ to limit the maximum gain of the GS3440, $\overline{CD}$ should not be connected to SLEEP.

4.5 Carrier Detect, Sleep, and Auto-Sleep

The Carrier Detect output pin ($\overline{CD}$) indicates the presence of a valid signal at the input of the GS3440. When $\overline{CD}$ is LOW, the device has detected a valid input on SDI and $\overline{SDI}$. When $\overline{CD}$ is HIGH, the device has not detected a valid input.

The GS3440 includes a SLEEP input pin, which can be used to put the device into a low-power sleep mode, consuming less than 30mW. In this mode, the outputs are high impedance and will be pulled high by the on-chip termination. Set the SLEEP pin HIGH to place the chip in this low-power state. In this mode, the Carrier Detect output will still function to facilitate the detection of a valid serial input data signal.

Auto-Sleep is enabled by connecting $\overline{CD}$ to SLEEP. When connected, the GS3440 will automatically go into low-power sleep mode when there is a loss of Serial Digital Input signal.

NOTE 1: $\overline{CD}$ will only detect loss of carrier for data rates greater than 19Mb/s.

NOTE 2: If SQ_ADJ is being used to limit the maximum gain of the device, and the maximum cable length is exceeded when BYPASS is set LOW, the $\overline{CD}$ pin will be set HIGH even if a carrier is present.

NOTE 3: If the $\overline{CD}$ pin is connected to the SLEEP pin, SQ_ADJ must be either left open, or connected to ground.

Table 4-2: SLEEP Input Table

SLEEP	Function
0	The GS3440 operates normally
1	The GS3440 enters low-power sleep mode. $\overline{CD}$ output remains valid

Table 4-3: $\overline{CD}$ Output Table

$\overline{CD}$	Input Status
0	Valid Input on SDI, $\overline{SDI}$ pins
1	Input is not valid

4.6 GAIN_SEL

The GS3440 has an option of compensating for 6dB of flat attenuation prior to the equalizer.

Table 4-4: GAIN_SEL Input Table

GAIN_SEL	Function
0	No flat band gain is applied.
1	6dB of flat attenuation will be compensated by the device.

4.7 Adjustable Output Swing, De-Emphasis and Mute

The OP_CTL input pin determines the output swing and de-emphasis settings for DDO and $\overline{DDO}$.

The OP_CTL pin is an analog input, allowing different combinations of output swing, de-emphasis and mute. The possible values are listed in Table 4-5.

Table 4-5: OP_CTL Functions and Levels

Level	Swing	De-emphasis	Mute	Voltage (V)
0	800mV	Off	N	0.000 - 0.083
1	800mV	2dB	N	0.234 - 0.394
2	800mV	4dB	N	0.545 - 0.704
3	800mV	6dB	N	0.856 - 1.015
4	400mV	Off	N	1.166 - 1.333
5	400mV	2dB	N	1.484 - 1.644
6	400mV	4dB	N	1.795 - 1.954
7	400mV	6dB	N	2.106 - 2.265
8	400mV	N/A	Y	2.416 - 2.500

When muted, the output swing is set to 400mV and the outputs are latched.

Automatic muting of the output can be enabled by connecting the $\overline{CD}$ pin to the OP_CTL pin.

If the connection is made directly, as shown in Figure 4-1, the output would be in its default mode (800mV swing with no de-emphasis) when there is signal present.

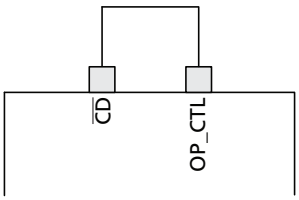


Figure 4-1: Direct Loopback

To enable automatic muting while the output is configured for other settings, a resistor network should be used between $\overline{CD}$ and VCC_A. The intermediate voltages of this resistor ladder can set the output to any one of the nine different settings as shown in Figure 4-2 and Figure 4-3.

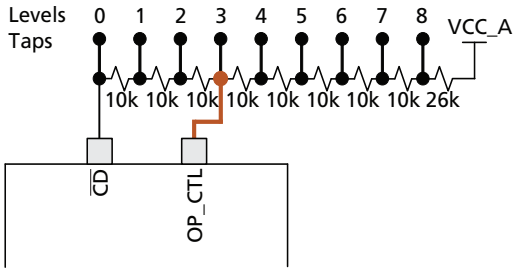


Figure 4-2: Resistor Divider Loopback Example #1 (Function Level 3 from Table 4-5)

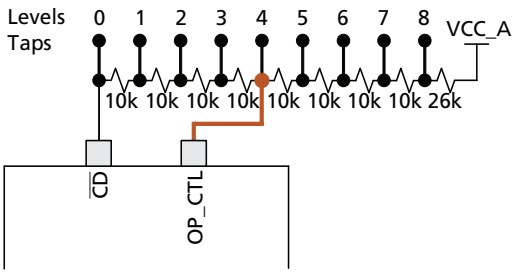


Figure 4-3: Resistor Divider Loopback Example #2 (Function Level 4 from Table 4-5)

In Figure 4-2, the automatic muting of the output is established by connecting node 3 to the OP_CTL pin. In this scenario, the output would be 800mV with 6dB of de-emphasis when there is a signal present.

In Figure 4-3, the OP_CTL pin is connected to node 4. In this scenario, the output would be 400mV with no de-emphasis when there is a signal present.

In both cases, the output would be muted when no carrier is detected.

NOTE: When the device is in SLEEP mode, automatic muting and SQ_ADJ don't function. Asserting the SLEEP pin manually overrides all other functionality.

5. Application Information

5.1 High-Gain Adaptive Cable Equalizers

The GS3440 is a multi-rate adaptive cable equalizer. In order to continue to extend the cable length that the device can support, it is necessary to have high-gain in the equalizer.

A video cable equalizer must provide wide band gain over a range of frequencies in order to accommodate the range of data rates and signal patterns that are present in a SMPTE-compliant serial video stream.

The GS3440 has an increase in gain over the GS2974A at critical HD and 3Gb/s frequencies, and because of this, the GS3440 may be sensitive to signals at the input that the GS2974A will not be sensitive to.

Small levels of signal or noise present at the input pins of the equalizer may cause chatter at the output. In order to prevent this from happening, particular attention must be paid to board layout.

5.2 PCB Layout

Special attention must be paid to component layout when designing Serial Digital Interfaces for HDTV. An FR-4 dielectric can be used, however, controlled impedance transmission lines are required for PCB traces longer than approximately 1cm. Note the following PCB artwork features used to optimize performance:

- PCB trace width for 3Gb/s rate signals is closely matched to SMT component width to minimize reflections due to change in trace impedance.
- High-speed traces are curved to minimize impedance changes.
- Cutouts in the inner layers should be used under the GS3440 input and output components to minimize parasitic capacitance. For more detail on this and other layout recommendations, please refer to 3G-SDI Equalizers Design Guide (genDOC ID: 55280).

5.3 Typical Application Circuit

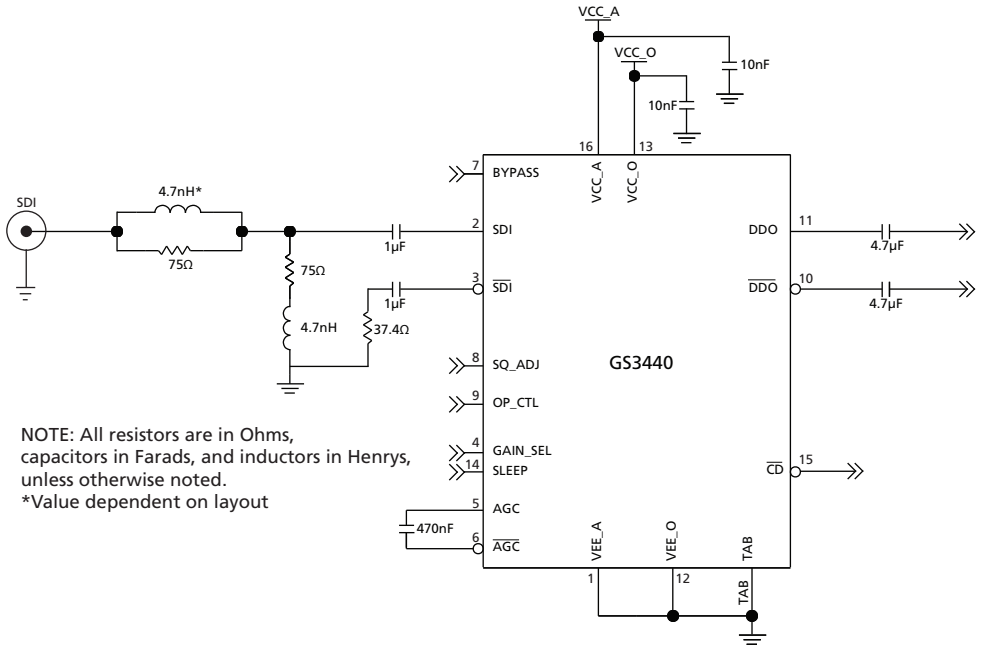
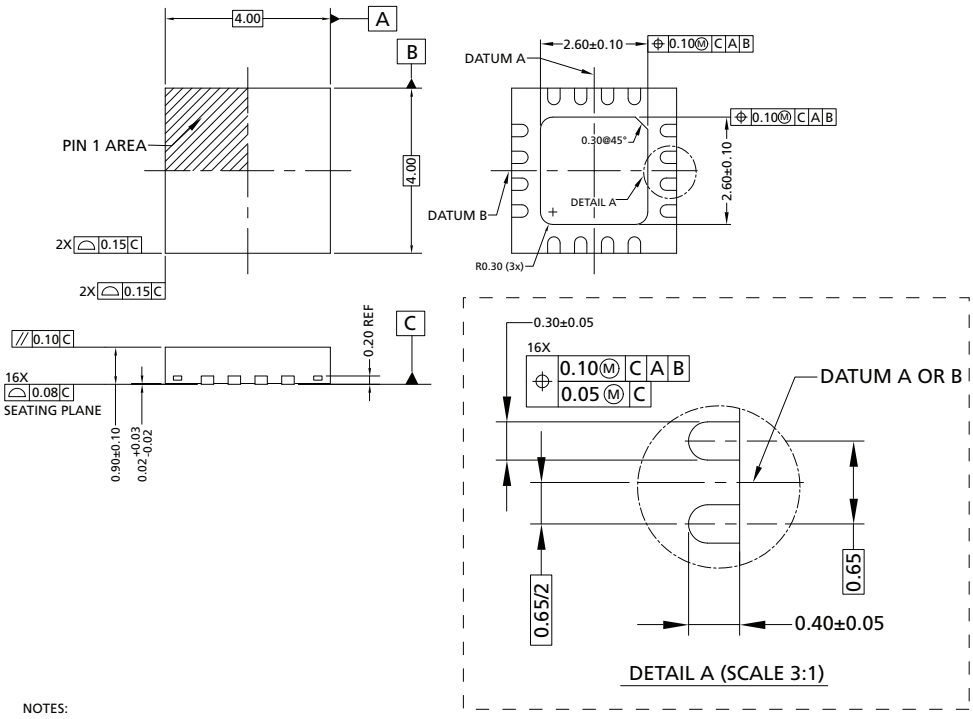


Figure 5-1: GS3440 Typical Application Circuit

6. Package & Ordering Information

6.1 Package Dimensions



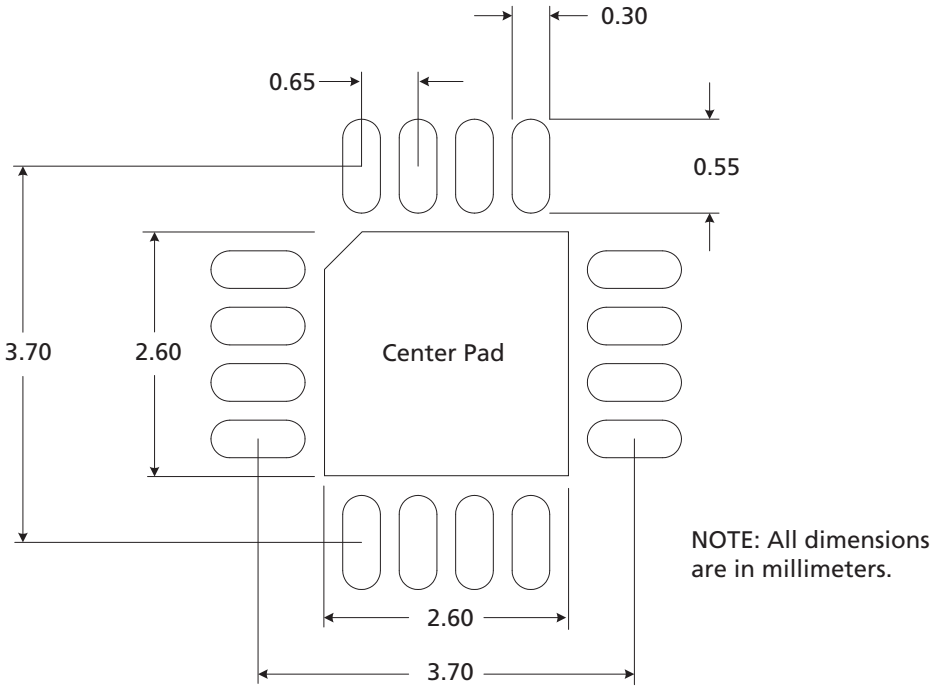
NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5-1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

6.2 Packaging Data

Parameter	Value
Package Type	4mm x 4mm 16-pin QFN
Package Drawing Reference	JEDEC M0220
Moisture Sensitivity Level	1
Junction to Case Thermal Resistance, θ_{j-c}	31.0°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	43.8°C/W
Psi, ψ	11.0°C/W
Pb-free and RoHS compliant	Yes

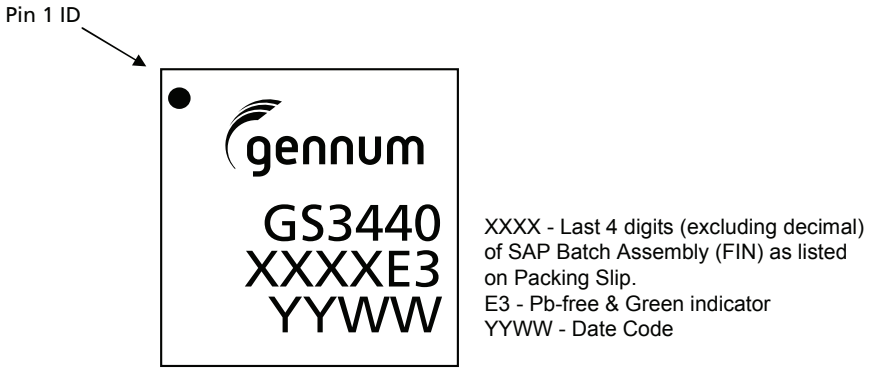
6.3 Recommended PCB Footprint



The Center Pad should be connected to the most negative power supply plane for analog circuitry in the device (VEE_A) by a minimum of 5 vias.

NOTE: Suggested dimensions only. Final dimensions should conform to customer design rules and process optimizations.

6.4 Marking Diagram



6.5 Solder Reflow Profiles

The GS3440 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 6-1.

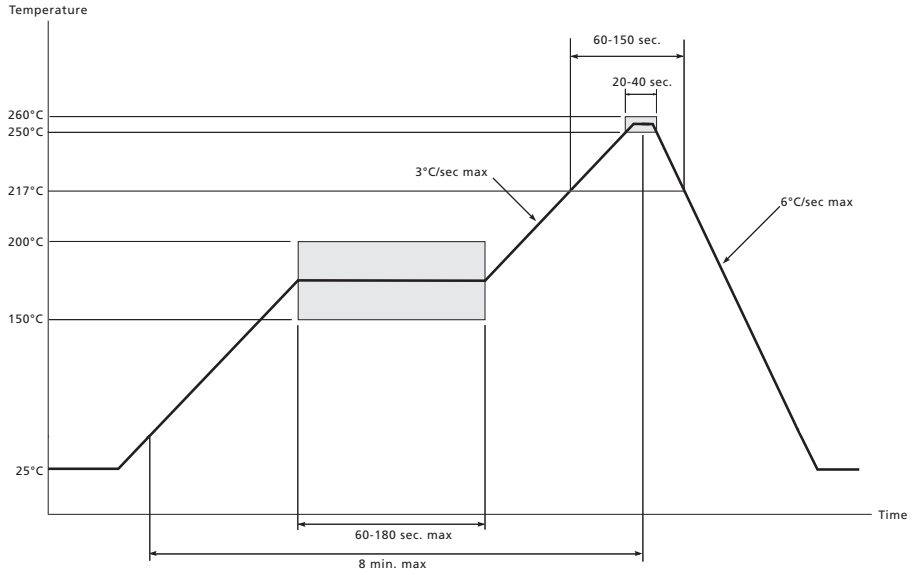


Figure 6-1: Maximum Pb-free Solder Reflow Profile

6.6 Ordering Information

Part Number	Package	Temperature Range
GS3440-INE3	16-pin QFN	-40°C to 85°C
GS3440-INTE3	16-pin QFN Tape & Reel (250pcs)	-40°C to 85°C
GS3440-INTE3Z	16-pin QFN Tape & Reel (2500pcs)	-40°C to 85°C

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
0	158278	–	June 2012	Converted to Preliminary Data Sheet
H	158055	–	May 2012	Updated the description for GAIN_SEL, BYPASS, OP_CTL, SLEEP AND $\overline{CD}$ in Table 1-1. Included additional row with Input Voltage for Digital pins in Table 2-1. Change in text throughout document for clarity
G	157993	–	May 2012	Modifications throughout the document.
F	157289	–	November 2011	Removed the Typical Usages section.
E	157162	–	November 2011	Updated the descriptions for the SQ_ADJ and GAIN_SEL pins in Table 1-1 to indicate that they have internal pull-down resistors.
D	156828	–	August 2011	Updated power and cable reach numbers in Key Features, Description, DC Electrical Characteristics, AC Electrical Characteristics and Detailed Description.
C	156166	–	May 2011	Updated the Power numbers in Table 2-1: DC Electrical Characteristics.
B	156134	–	April 2011	Updated the MSL rating in Packaging Data.
A	155973	–	April 2011	New document.

DOCUMENT IDENTIFICATION
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