SX1255

Low Power Digital I and Q RF Multi-PHY Mode Transceiver

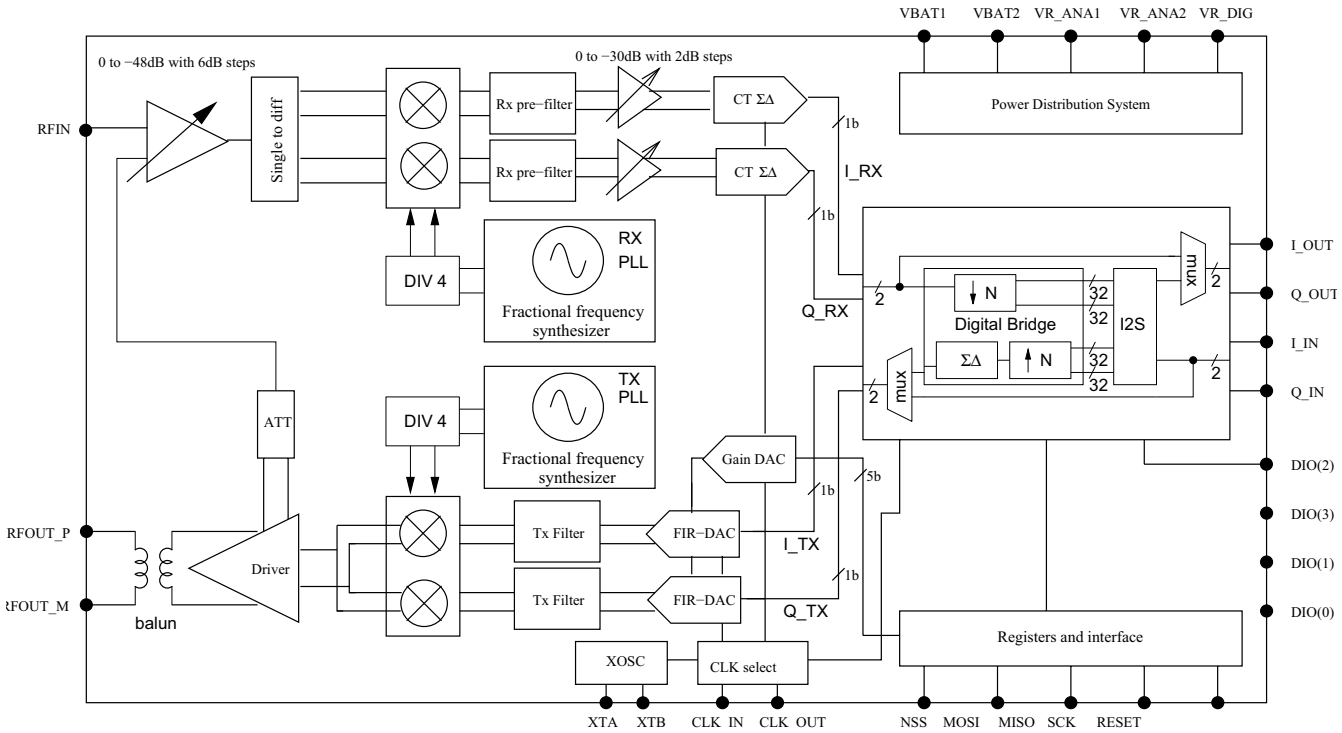


Figure A: SX1255 Block Diagram

General DescripSX1255tion

The SX1255 is a highly integrated RF front-end to digital I and Q modulator/demodulator Multi-PHY mode transceiver capable of supporting multiple constant and non-constant envelope modulation schemes. It is designed to operate over the 400 to 510 MHz worldwide licensed and unlicensed frequency bands. Its highly integrated architecture allows for a minimum of external components whilst maintaining maximum design flexibility. All major RF communication parameters are programmable and most of them can be dynamically set. The SX1255 offers support for both narrow-band and wide-band communication modes without the need to modify external components. The SX1255 is optimized for low power consumption while offering the provision for high RF output power and channelized operation. TrueRF™ technology enables a low-cost external component count whilst still satisfying ETSI, FCC, ARIB and other regulations.

Applications

- IEEE 802.15.4g SUN Multi-PHY Mode Smartgrid
- Cognitive / Software Defined Radio (SDR)

Key Product Features

- Fully flexible I and Q modulator and demodulator
- Half or full-duplex operation
- Bullet proof RX LNA
- Analog TX and RX pre-filtering
- Decimated I&Q signal under I^2S industry format
- Programmable tap TX FIR-DAC filter
- Linear TX amplifier for both constant and non-constant envelope modulation schemes

SX1255Ordering Information

Part Number	Delivery	Minimum Order Quantity
SX1255IWLTRT	MLPQW-32	3'000 pieces
SX1255WS	-	1 wafer

Pb-free, Halogen free, RoHS/WEEE compliant product.

Document Revision History

Version	ECO	Date	Modifications
1.0	011527	February 2013	First datasheet revision
2.0	013161	May 2013	Updated specifications after part characterization
3.0	015891	October 2013	Add wafer sale part number
3.1	041328	March 2018	Migration to the new data sheet template Correction of NSS Hold Time to 50 ns Correction of minor typographical errors

Table of Contents

List of Figures

List of Tables

1. General Description

The SX1255 is a single-chip Zero-IF RF-to-digital front-end transceiver integrated circuit ideally suited for today's high performance multi-PHY mode or SDR ISM band RF applications. The SX1255 has a maximum signal bandwidth of 500 kHz in both transmission and reception and is intended as a high performance, low-cost RF-to-digital converter and provides a generic RF front-end that allows several constant and non-constant envelope modulation schemes to be handled, such as the MR-FSK, MR-OFDM and MR-O-QPSK applications in the 400 - 510 MHz licensed and unlicensed frequency bands.

The SX1255's advanced features set greatly simplifies system design whilst the high level of integration reduces the external BOM to an optional RF power amplifier, and a handful of passive decoupling and matching components. A simple 4-wire 1-bit digital serial interface is provided for the baseband I and Q data streams to a baseband processor.

The SX1255 can operate in both half and full-duplex mode and is compliant with ETSI, FCC and ARIB regulatory requirements. It is available in a MLPQ-W 5 x 5 mm 32 lead package.

1.1 Simplified Block Diagram

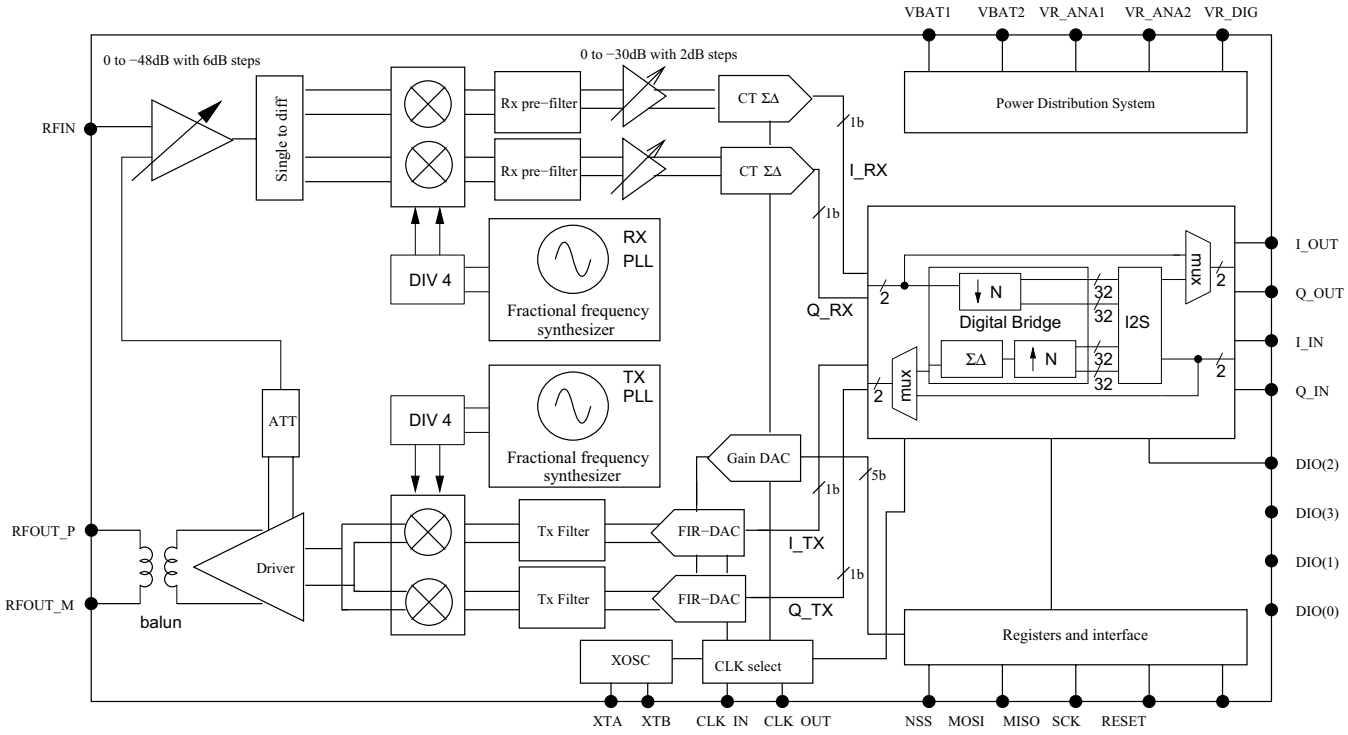


Figure 1-1: SX1255 Block Diagram

1.2 I/O Description

Table 1-1: SX1255 Pinout

Pin Number	Pin Name	Type (I = input O = Ouptut)	Description
0	Ground	-	Exposed Ground pad
1	VR_PA	-	Regulated supply for TX amplifier
2	VBAT1	-	VBAT Supply voltage
3	VR_ANA1	-	Regulated supply for analog TX circuit
4	GND	-	Ground
5	VR_DIG	-	Regulated supply for digital circuit
6	XTA	I/O	Crystal pad
7	GND	-	Ground
8	XTB	I/O	Crystal pad / input for external clock
9	Reset	I/O	Reset
10	CLK_OUT	O	36 MHz digital clock output
11	CLK_IN	I	36 MHz digital clock input (SX1255 used in slave TX mode)
12	Q_IN	I	Digital baseband data input for I (inphase) channel DAC
13	I_IN	I	Digital baseband data input for Q (quadrature) channel DAC
14	Q_OUT	O	Digital baseband data output from I (inphase) channel ADC
15	I_OUT	O	Digital baseband data output from Q (quadrature) channel ADC
16	VBAT2	-	VBAT supply voltage
17	SCK	I	SPI clock
18	MISO	O	Master In Slave Output SPI output
19	MOSI	I	Master Out Slave Input SPI input
20	NSS	I	SPI chip select
21	DIO0	O	Digital I/O, software configured
22	DIO1	O	Digital I/O, software configured
23	DIO2	O	Digital I/O, software configured
24	DIO3	O	Digital I/O, software configured
25	VR_ANA2	-	Regulated supply for analog RX circuit
26	GND	-	Ground
27	RF_IN	I	RX LNA input
28	GND	-	Ground

Table 1-1: SX1255 Pinout

Pin Number	Pin Name	Type (I = input O = Ouptut)	Description
29	RF_ON	O	Differential TX Output, negative node
30	RF_OP	O	Differential TX Output, positive node
31	GND	-	Ground
32	VBAT3	-	VBAT supply for TX amplifier

1.3 Package View

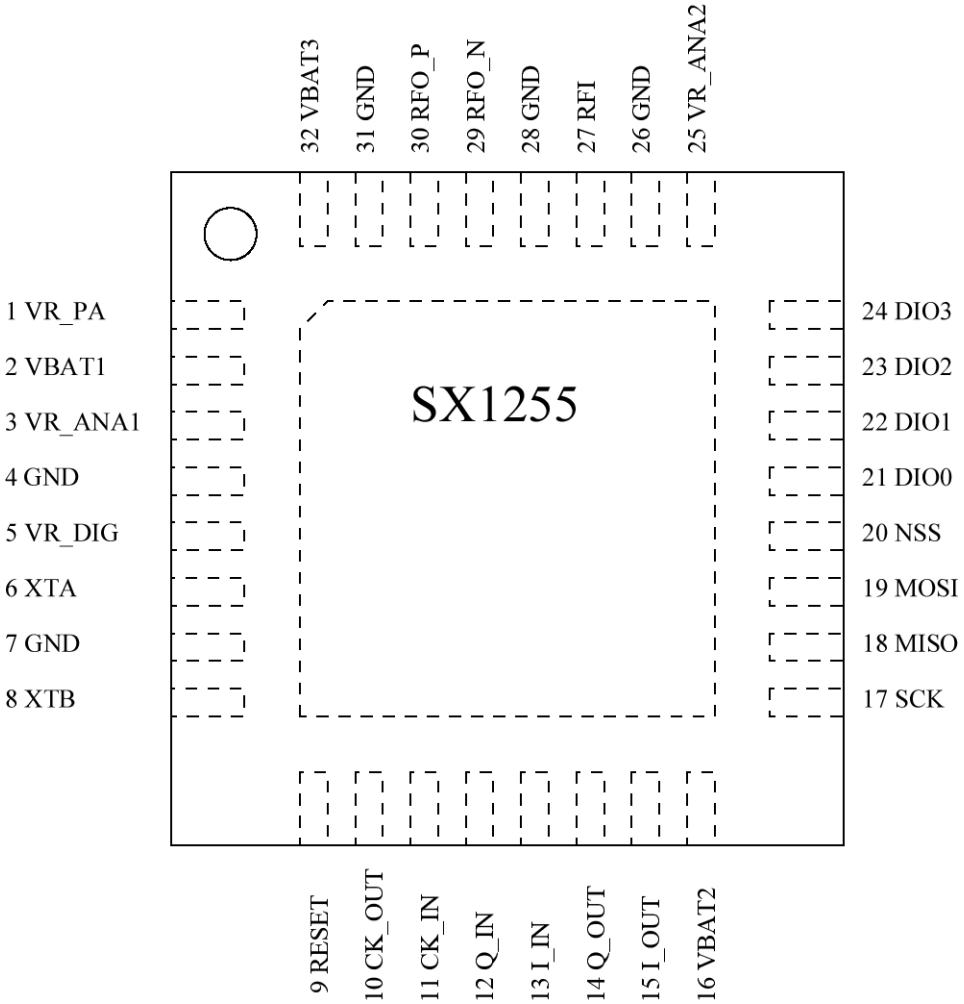


Figure 1-2: SX1255 Top View Pin Location

2. Specifications

2.1 ESD Notice

The SX1255 is a high performance radio frequency device.

- Class 3A of the JEDEC standard JESD22-A114-C (Human Body Model) on all pins
- Class III of the JEDEC standard JESD22-C101-C (Charged Device Model) on all pins

The chip should be handled with all the necessary ESD precautions to avoid any permanent damage.

2.2 Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure.
Exposure to absolute maximum ratings for extended periods may affect device reliability, reducing product life time.

Table 2-1: Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Unit
VDDmr	Supply voltage	-0.5	-	3.9	V
Tmr	Temperature	-55	-	115	°C
Tj	Junction temperature	-	-	125	°C
Pmr	RF input level	-	-	+6	dBm

2.3 Operating Range

Operating ranges define the limits for functional operation and parametric characteristics of the device.
Functionality outside these limits is not guaranteed.

Table 2-2: Operating Range

Symbol	Description	Min	Typ	Max	Unit
VDDop	Supply voltage	2.7	-	3.6	V
Top	Temperature under bias	-40	-	85	°C
Clop	Load capacitance on digital ports	-	-	25	pF
ML	RF Input power	-	-	0	dBm

2.4 Electrical Specifications

The electrical specifications are given with the following conditions unless otherwise specified:

- VBAT_IO = VBAT = 3.3 V, all current consumptions are given for VBAT connected to VBAT_IO
- Temperature = 25 °C
- F_{XOSC} = 36 MHz
- F_{RF} = 434 MHz
- OFDM with 16-QAM
- 3/4 rate coded with 26 active tones (IEEE 802.15.4g MR-OFDM Option 3)
- Output power = -5 dBm (100 ohm differential transmission)
- TXBWANA = 250 kHz
- RXBWANA = 250 kHz
- External baseband RX filter = 150 kHz

2.4.1 Power Consumption Specifications

Table 2-3: Power Consumption Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in sleep mode		-	0.2	1	µA
IDDST	Supply current in standby mode	Crystal oscillator enabled	-	1.15	1.5	mA
IDDRX	Supply current in receive mode	-		18	25	mA
IDDTX	Supply current in transmit mode	RFOutput Power = -5 dBm	-	60	90	mA

2.4.2 Frequency Synthesis Specifications

Table 2-4: Frequency Synthesis Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer frequency range	Programmable	400	-	510	MHz
FXOSC	Crystal oscillator frequency	See Section 5. "Configuration and Status Registers" on page 37	32	36	36.864	MHz
TS_OS	Crystal oscillator wake-up time	from sleep mode	-	300	500	µs
TS_FS	Synthesizer wake-up time	Crystal oscillator enabled	-	50	150	µs
FSTEP	Frequency synthesizer step size	FSTEP = FXOSC / 2^{19}	30.5	34.3	35.16	Hz

2.4.3 Transmitter Front-End Specifications

Table 2-5: Transmitter Front-End Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
FCLK_IN	External clock frequency for TX synthesizer or DAC input clock	SX1255 slave mode	32	-	36.864	MHz
TS_TR	Transmitter wake-up time	Frequency synthesizer enabled	-	120	-	µs
TXPmax	TX maximum output power	Saturated Power	+4	+7	-	dBm
TXP1dB	TX 1 dB compression point	Peak value	+2	+5	-	dBm
TXOIP3	TX output IP3	-5 dBm average output power	+13	+16	-	dBm
PHN	Transmitter phase noise	10 kHz offset from carrier	-	-110	-	dBc/Hz
		100 kHz offset from carrier	-	-108	-	dBc/Hz
		1 MHz offset from carrier	-	-128	-	dBc/Hz
PHNF	Transmitter output noise floor	10 MHz offset from carrier	-128	-135	-	dBc/Hz
PHNID	Transmitter integrated DSB phase noise	Integrated bandwidth from 500 Hz to 125 kHz	-	0.2	1.5	°RMS
TXGM	Transmitter IQ gain mismatch	-	-	0.5	1	dB
TXPM	Transmitter IQ phase mismatch	-	-	1	3	°
TXBWANA	Transmitter analog prefilter BW (SSB)	Programmable	420	-	1700	kHz
XBWANAPrc	Transmitter analog prefilter BW precision	-	-30	-	+30	%
TXBWDIFG	Transmitter FIR-DAC taps	Programmable	24	-	64	-
TXLO	TX LO leakage (before DC offset calibration)	ADC rms input: -10 dBFS	-	-8	-	dBc

2.4.4 Receiver Front-End Specifications

Table 2-6: Receiver Front-End Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
FCLK_IN	External clock frequency for TX synthesizer or DAC input clock	SX1255 slave mode	32	-	36.864	MHz
CLK_INJ	External clock jitter specification	External clock, white noise	-	-	0.01	%
RXNF	Receiver noise figure	Maximum LNA gain	-	4.5	7	dB
		Maximum LNA gain -6 dB	-	6.5	9	dB
		Minimum LNA gain	-	38	40	dB
RXGR	RX gain range	Adjustable in 2 dB steps	-	70	-	dB
IIP3	3rd order input intercept point Unwanted tones are 2 MHz and 3.8 MHz above the LO	Maximum LNA gain	-28	-23	-	dBm
		Maximum LNA gain -6 dB	-21	-16	-	dBm
		Minimum LNA gain	+10	+20	-	dBm
RXGM	Receiver IQ gain mismatch	-	-	0.5	1	dB
RXPM	Receiver IQ phase mismatch	-	-	0.5	3	°
RXBWANA	Receiver analog prefilter BW (SSB)	Programmable	500	-	1500	kHz

2.4.5 SPI Bus Digital Specifications

Table 2-7: Digital I/O Specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high voltage	-	0.8	-	-	VDD
V_{IL}	Input low voltage	-	-	-	0.2	VDD
V_{OH}	Output high voltage	I_{max} = 1 mA	0.9	-	-	VDD
V_{OL}	Output low voltage	I_{max} = -1 mA	-	-	0.1	MHz
F_{SCK}	SCK frequency	-	-	-	10	ns
t_{ch}	SCK high time	-	50	-	-	ns
t_{cl}	SCK low time	-	50	-	-	ns
t_{rise}	SCK rise time	-	-	5	-	ns
t_{fall}	SCK fall time	-	-	5	-	ns
t_{setup}	MOSI set-up time	From MOSI change to SCK rising edge	30	-	-	ns
t_{hold}	MOSI hold time	From SCK rising edge to MOSI change	60	-	-	ns
t_{nsetup}	NSS set-up time	From NSS falling edge to SCK rising edge	30	-	-	ns
t_{nhold}	NSS hold time	From SCK falling edge to NSS rising edge	50	-	-	ns
t_{nhigh}	NSS high time between SPI access	-	20	-	-	ns
t_{data}	Data hold and set-up time	-	25	-	-	ns

3. Circuit Description

3.1 Power Supply Strategy

The SX1255 employs an advanced power distribution scheme (PDS), which provides stable operating characteristics over the full temperature and voltage range of operation.

The SX1255 can be powered from any low-noise voltage source via pins VBAT1, VBAT2 and VBAT3. Decoupling capacitors should be connected, as suggested in the reference design, on VR_PA, VR_DIG, VR_ANA1 and VR_ANA2 pins to ensure a correct operation of the built-in voltage regulators.

3.2 Low Battery Detector

A low battery detector is also included allowing the generation of an interrupt signal in response to passing a programmable threshold adjustable through the register RegLowBat. The interrupt signal can be mapped to the DIO0 pin, through the programmation of RegDioMapping.

3.3 Frequency Synthesizer

The SX1255 incorporates two separate state of the art fractional-N PLLs for the TX and RX circuit blocks.

3.3.1 Reference Oscillator

The crystal oscillator is the main timing reference of the SX1255. It provides the reference source for the transmit and receive frequency synthesizers and as a clock for digital processing.

The XO startup time, TS_OSC, depends on the actual XTAL being connected on pins XTA and XTB. When using the built-in sequencer, the SX1255 optimizes the startup time and automatically triggers the PLL when the XO signal is stable. To manually control the startup time, the user should monitor the signal CLK_OUT which will only be made available on the output buffer when a stable XO oscillation is achieved.

An external crystal controlled source, such as a clipped-sinewave TCXO, clock can be used to replace the crystal oscillator, This external source should be provided on XTB (pin 8) and XTA (pin 6) should be left open, as illustrated in the following figure.

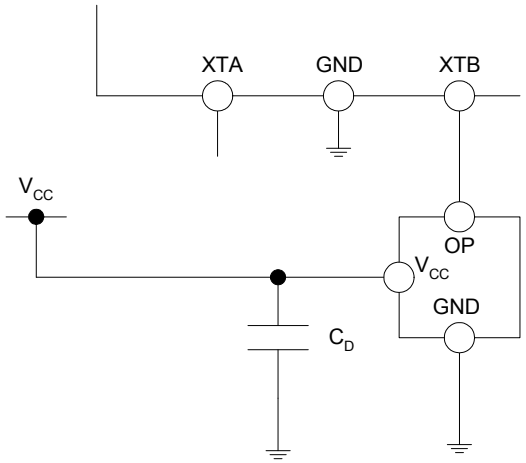


Figure 3-1: TCXO Connection

The peak-peak amplitude of the input signal must never exceed 1.8 V. Please consult your TCXO supplier for an appropriate value of decoupling capacitor, CD. Due to the low jitter requirements required by the receiver digital block it is recommended that only a crystal controlled external frequency source is used.

3.3.2 CLK_OUT Output

For master mode operation the SX1255 provides a system clock output made available at pin CLK_OUT.

3.3.3 PLL Architecture

The SX1255 incorporates two fourth-order type fractional-N sigma-delta PLLs. The PLLs include integrated VCO and programmable bandwidth loop filter, removing the need for any external components. The PLLs are autocalibrating and are capable of fast switching and settling times.

3.3.3.1 VCO

Both TX and RX VCOs operate at twice the RF frequency, with the oscillators centered at 1.9 GHz. This reduces any LO leakage in receive mode, to improve the quadrature precision of the receiver, and to reduce the pulling effects on the VCO during transmission.

The VCO calibration is fully automated, calibration times are fully transparent to the end-user as the processing time is included in the TS_TR and TS_RE specifications.

3.3.3.2 PLL Bandwidth

The bandwidth of the PLL loop filters are independently configurable via the configuration registers TxPllBw and RxPllBw for the modulation schemes supported, as well as fast channel switching and lock times to support FHSS and frequency agile applications, such as AFA.

3.3.3.3 Carrier Frequency and Resolution

Both the TX and RX embed a 19-bit sigma-delta modulator and the frequency resolution, constant over the entire frequency range, is calculated using the following formula:

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$

The RX and RX carrier frequencies are programmed through registers RegFrfRx and RegFrfTx, split across register addresses 0x01 to 0x03 and 0x04 to 0x06, respectively, and are calculated by:

$$F_{RF} = F_{STEP} \times F_{RFXX}(23, 0)$$

where: F_{rfxx} is the integer value of the RegFrfRx or RegFrfTx as defined above.

Note:
As stated above, the F_{rfxx} settings are split across 3 bytes for both the transmitter and receiver frequency synthesizers. A change in the center frequency will only be taken into account when the least significant byte FrfxxLsb in RegFrfxxLsb is written and when exiting SLEEP mode.

3.3.3.4 PLL Lock Time

RX and TX PLL lock times are a function of a number of technical factors, such as synthesized frequency, frequency step, etc. The SX1255 includes an auto-sequencer that manages the start-up sequence of the PLL.

3.3.3.5 Lock Detect Indicator

A lock indication signal for both RX and TX PLLs can be accessed via DIO pins, and is toggled high when the PLL reaches its locking range. Please refer to Table 4-1: "DIO Mapping" on page 28 to map this interrupt to the desired DIO pins.

3.4 Transmitter Analog Front-End Description

The analog front-end of the SX1255 transmitter stage comprises the TX frequency synthesizer, I and Q channel filters, the I/Q mixer and RF amplifier blocks.

3.4.1 Architectural Description

The block diagram of the transmitter front-end block is illustrated below.

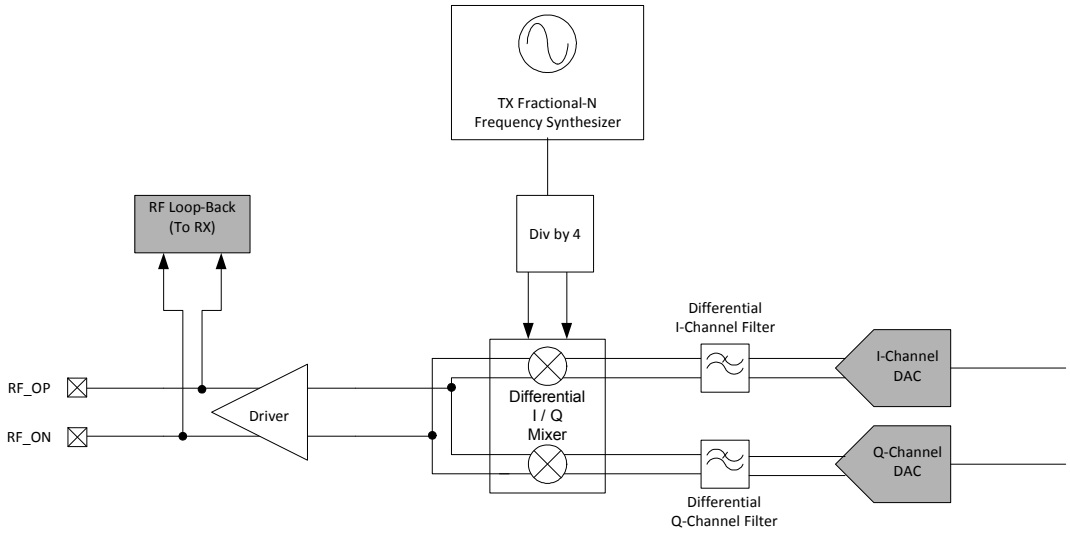


Figure 3-2: SX1255 Transmitter Analog Front-End Block Diagram

3.4.2 TX I / Q Channel Filters

Differential analog I and Q signals input to the TX front-end from the TX FIR DAC are filtered by I and Q channel filters. These filters smooth the reconstructed analog waveforms and remove quantization noise generated by the I and Q channel TX FIR DACs. The filters are unity gain third-order low-pass Butterworth types with programmable bandwidth configured via TxAnaBw.

The 3 dB BW of the analog TX filter BW can be calculated from:

$$BW_{3dB} = \frac{17.15}{(41 - RegTxBWAna(4,0))}$$

The analog filter bandwidth should be set to greater than the signal bandwidth so as to reduce any group delay variations.

The range of programmable TX analog filter bandwidths is tabulated below.

TxAnaBw [Dec]	TxAnaBw [Bin]	SSB Filter BW [kHz]
0	00000	209
1	00001	214
2	00010	220
3	00011	226
4	00100	232
5	00101	238
6	00110	245
7	00111	252
8	01000	260
9	01001	268
10	01010	277
11	01011	286
12	01100	296
13	01101	306
14	01110	318
15	01111	330
16	10000	343
17	10001	357
18	10010	373
19	10011	390
20	10100	408
21	10101	429
22	10110	451
23	10111	476
24	11000	504
25	11001	536
26	11010	572
27	11011	613
28	11100	660
29	11101	715

TxAnaBw [Dec]	TxAnaBw [Bin]	SSB Filter BW [kHz]
30	11110	780
31	11111	858

3.4.3 TX I / Q Up-Conversion Mixers

The TX I / Q mixer block mixes the baseband analog I and Q signals with that from the PLL frequency synthesizer and up converts to the RF carrier frequency. The mixer block includes a highly linear I/ Q mixer stage with programmable gain configurable via configuration register RegTxGain. The modulated RF signal is input to the TX RF amplifier stage.

3.4.4 RF Amplifier

The TX amplifier receives the input signal from the TX mixer and provides two differential outputs. The first output provides the RF_OP and RF_ON signals in TX mode. The second output is used to provide an internal differential signal to the receiver during RX gain calibration. The amplifier provides good linear performance required to meet the peak to average power level variation of OFDM.

The peak output power is +5 dBm, which allows for an average output power of greater than -5 dBm with 10 dB back-off. The output signal is intended to be amplified through a suitable external RF power amplifier to the maximum permissible level allowed by relevant regulatory standards. The optimum load impedance presented RF amplifier is 100 ohms differential.

3.5 Transmitter Digital Baseband Description

The transmitter digital baseband section contains separate I and Q channel digital-to-analog convertors.

3.5.1 Digital-to-Analog Converters

The TX DAC is the first block of the SX1255 transmitter. It accepts the 1-bit I and Q noise shaped 32 Msample/second or 36 MSample/second or I2S datastream from the baseband processor and converts into two analog differential signals. Each TX DAC provides 8-bits of resolution in a 500 kHz bandwidth which corresponds to maximum RF transmitted double-sideband bandwidth of 1 MHz.

A programmable Finite Impulse Response (FIR) filter allows the removal of the digital modulator noise from the external baseband processor. The number of taps implemented by the FIR-DAC and subsequent single-side DAC bandwidth is controlled by the parameter TxDacBw.

TxDacBw [Dec]	TxDacBw [Bin]	No. DAC-FIR Taps	SSB Filter BW [kHz]
0	000	24	
1	001	32	450
2	010	40	
3	011	48	
4	100	56	
5	101	64	290

Examples of the FIR DAC normalized magnitude response are illustrated below.

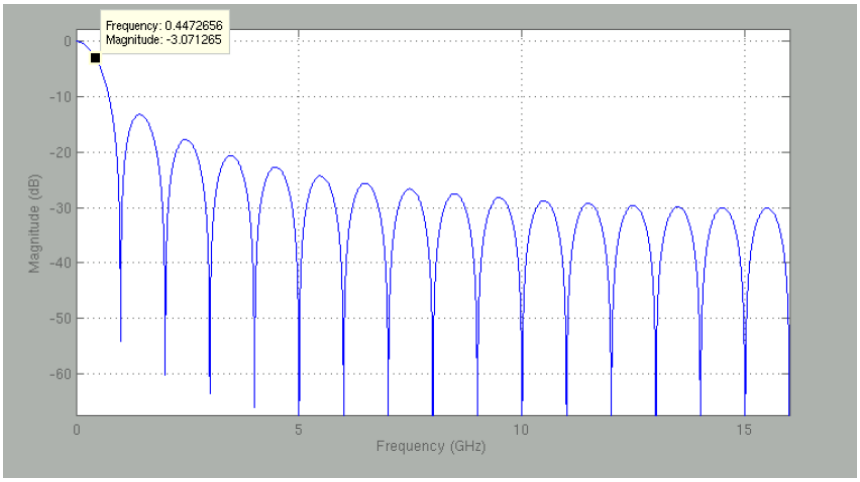


Figure 3-3: FIR-DAC Normalized Magnitude Response with f_S = 32 MHz and N = 32

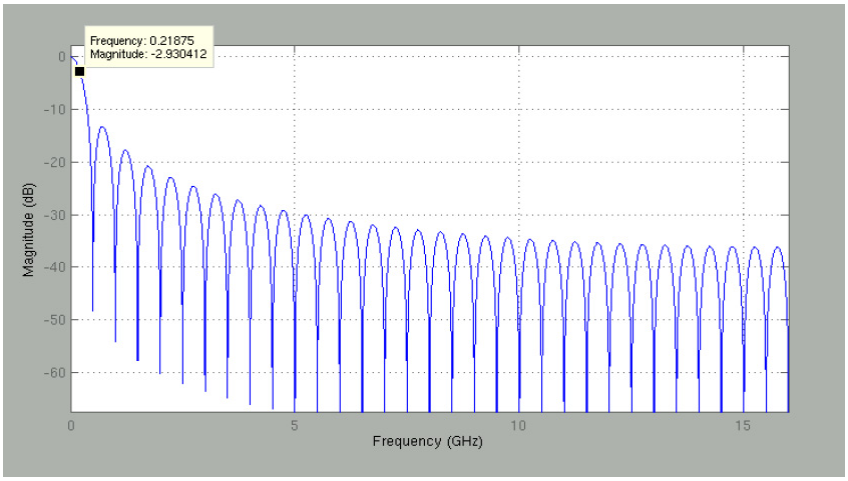


Figure 3-4: FIR-DAC Normalized Magnitude Response with f_S = 32 MHz and N = 64

The DAC 3dB bandwidth is proportional to the sampling frequency fs and inversely proportional to the number of taps N. In the case where f_S = 32 MHz with N = 32 the 3 dB bandwidth is typically 450 kHz. Reducing the bandwidth may be useful to reduce the quantisation noise contribution when the signal bandwidth request is lower, as is illustrated in the case where N = 64, resulting in a 3 dB bandwidth of approximately 290 kHz.

3.6 Receiver Analog Front-End Description

The SX1255 receiver front-end is based upon a zero-IF architecture, ideally suited to handle multiple complex modulation schemes. The RX chain incorporates a programmable gain LNA and single to differential buffer, I / Q mixer, separate I and Q channel analog low-pass filters and programmable baseband amplifiers. The amplified differential analog I and Q outputs are input to two 5th order continuous-time sigma-delta Analog to Digital Converters (ADC) for further signal processing in the digital domain.

3.6.1 Architectural Description

The block diagram of the receiver front-end block is illustrated below.

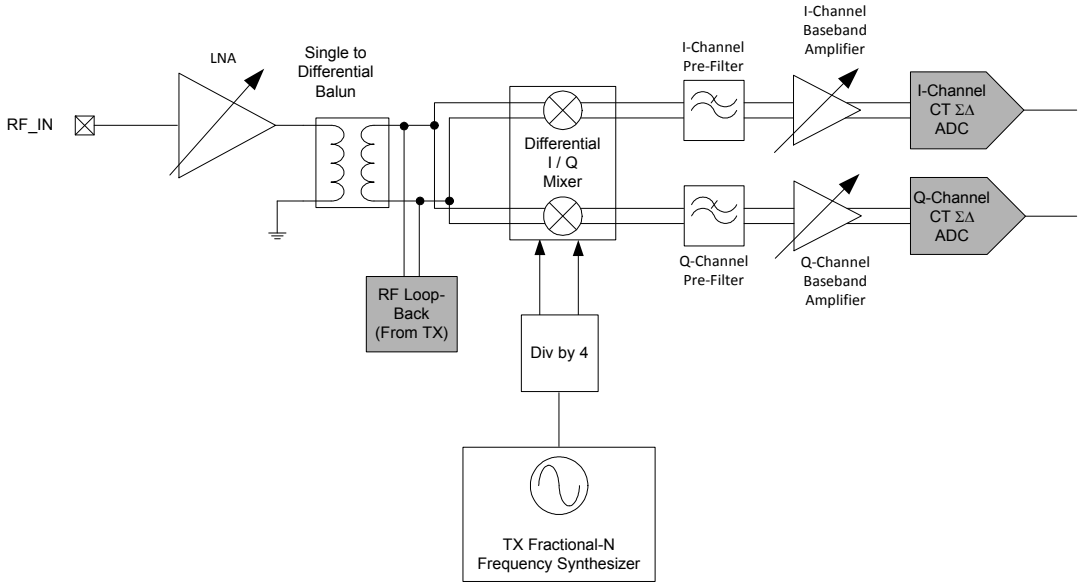


Figure 3-5: SX1255 Receiver Analog Front-End Block Diagram

3.6.2 LNA and Single to Differential Buffer

The LNA uses a common-gate topology, which allows for a flat characteristic over the whole frequency range. It is designed to have an input impedance of 50 Ohms or 200 ohms (as selected with bit LnaZin in RegRxAnaGain). A single to differential buffer is implemented to improve the second order linearity of the receiver.

The LNA gain, including the single-to-differential buffer, is programmable over a 48 dB dynamic range, and gain control can be enabled via an external AGC function.

3.6.3 I /Q Downconversion Quadrature Mixer

The mixer is inserted between output of the RF buffer stage and the input of the I and Q channel analog low-pass filter stages. This block is designed to downconvert the spectrum of the input RF signal to base-band and offers both high IIP2 and IIP3 responses.

3.6.4 Baseband Analog Filters and Amplifiers

The differential I and Q baseband mixer signals are pre-filtered by a programmable 1st order low-pass pre-filter and input to programmable linear baseband amplifiers. The single-sideband 3 dB bandwidth of the pre-filters can be programmed between 500 kHz and 1500 kHz. This additional pre-filtering improves the selectivity of the receiver for complex modulation schemes, such as OFDM.

The amplifier stage gain offers 32 dB of programmable gain, in 2 dB steps, from -24 dB to +6 dB via configuration register RegRxAnaGain while the analog filter bandwidth is programmed via the two least significant bits of configuration register RegRxBw.

3.7 Receiver Digital Baseband

The receiver digital baseband section contains separate I and Q channel continuous time Sigma-Delta analog-to-digital converters to digitize and filter the analog bit stream.

3.7.1 Architectural Block Diagram

The block diagram of the receiver digital baseband is illustrated below.

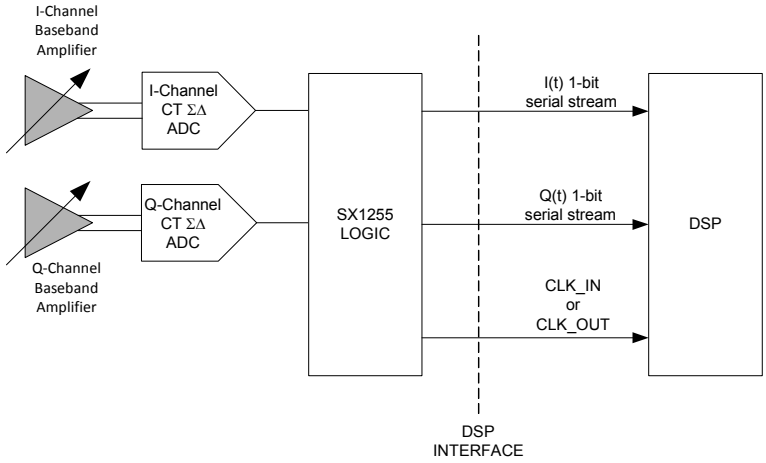


Figure 3-6: SX1255 Digital Receiver Baseband Block Diagram

3.7.2 Analog-to-Digital Converters

The receiver digital baseband consists of separate I and Q channel 5th order continuous-time sigma-delta modulator analog -to-digital converters which sample and digitize the analog baseband I and Q signals output at the analog baseband amplifiers.

The ADC output allows for 13 bits of resolution after decimation and filtering by the external baseband processor within a 500 kHz maximum bandwidth, corresponding to a maximum RF received double sideband bandwidth of 1 MHz.

The ADC output is one bit per channel quadrature bit stream at 32 to 36 MSamples/s or I2S data stream.

3.7.3 Temperature Sensor

The receiver ADC can be used to perform a temperature measurement by digitizing the sensor response. The response of the sensor is -1C / Lsb. Since a CMOS temperature sensor is not accurate by nature, the sensor should be calibrated at ambient temperature for a precise reading.

It takes less than 100 µs for the SX1255 to evaluate the temperature (from setting RxAdcTemp = "1"). The AdcTemp value can be read at Q_OUT. Since there is no on-chip decimation or averaging it is recommmended that data on Q_OUT is externally processed, for example using a simple FFT.

The temperature measurement should be performed with the SX1255 in StandbyEnable Mode (RegMode = 0x01)

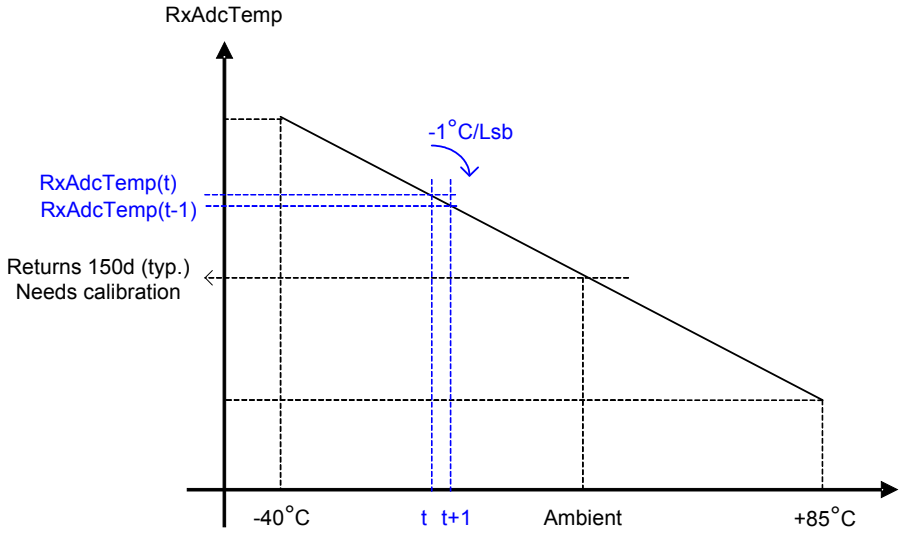


Figure 3-7: Temperature Sensor Response

3.8 Loop-Back

The SX1255 provides mechanisms to both monitor and externally calibrate both the RF transmission path and the I and Q bit streams generated by the external baseband processor.

3.8.1 Digital Loop-Back

The digital loop-back enables the connection of the input and output I and Q baseband bit streams prior to processing by the SX1255. This loop back path enables the validation of the transmitter and receiver baseband processing paths.

3.8.2 RF Loop Back

The RF loop-back path connects the balanced RF output signal of the transmitter driver stage to the output of the differential mixer of the receiver. This path provides a mechanism for the external baseband processor to implement a calibration for the following:

- Receiver I, Q gain mismatch
- Receiver I and Q phase imbalance
- Transmitter I, Q gain mismatch
- Transmitter I and Q phase imbalance
- Transmitter DC offset

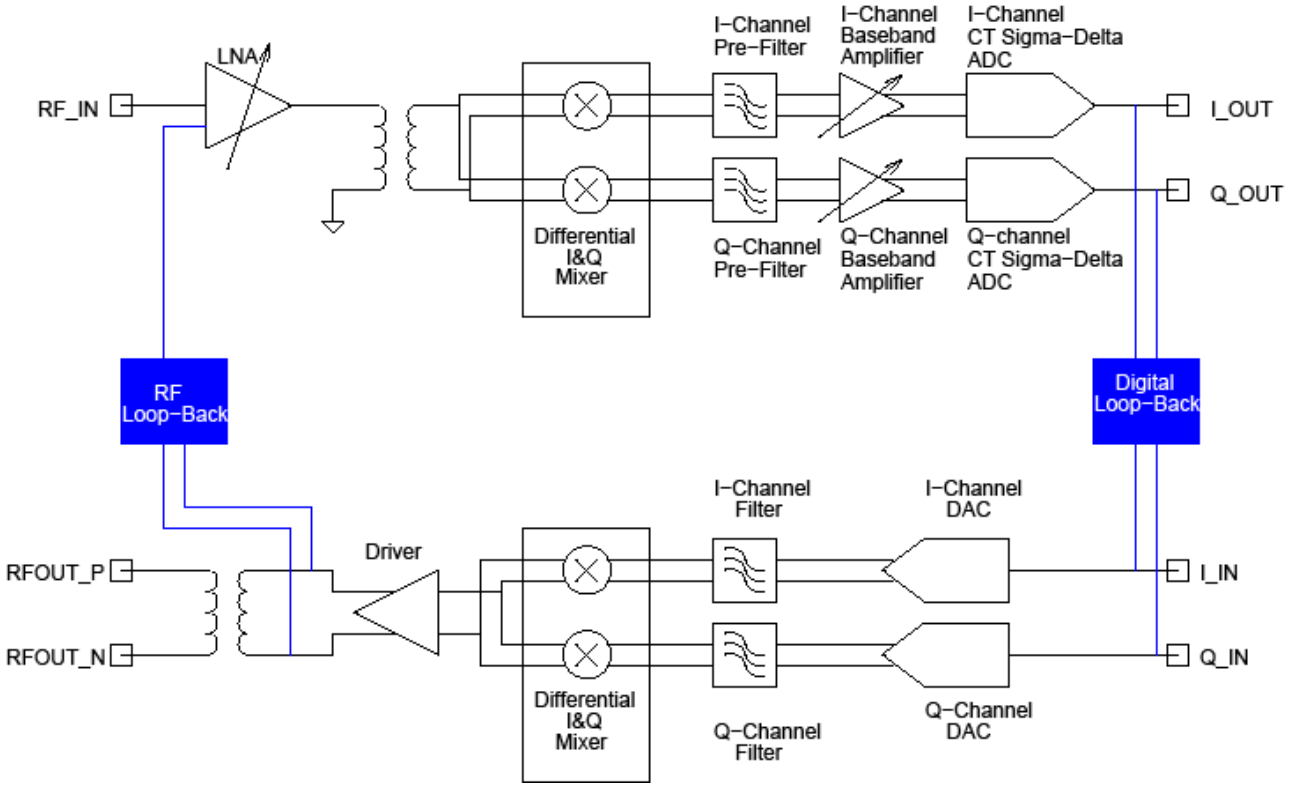


Figure 3-8: Digital and RF Loop-Back Paths

4. Digital Interface

The SX1255 has several operating modes, configuration parameters and internal status indicators. All these operating modes, configuration parameters and status information are stored in internal registers that may be accessed by the external micro-controller via the serial SPI interface.

4.1 SPI Bus Interface

The SPI interface gives access to the configuration register via a synchronous full-duplex protocol corresponding to CPOL = 0 and CPHA = 0 in Motorola/Freescale nomenclature. Only the slave side is implemented.

Two access modes to the registers are provided:

- SINGLE access: an address byte followed by a data byte is sent for a write access whereas an address byte is sent and a read byte is received for the read access. The NSS pin goes low at the begin of the frame and goes high after the data byte.
- BURST access: the address byte is followed by several data bytes. The address is automatically incremented internally between each data byte. This mode is available for both read and write accesses. The NSS pin goes low at the beginning of the frame and stay low between each byte. It goes high only after the last byte transfer.

An example of a typical SPI single access to a register is illustrated below.

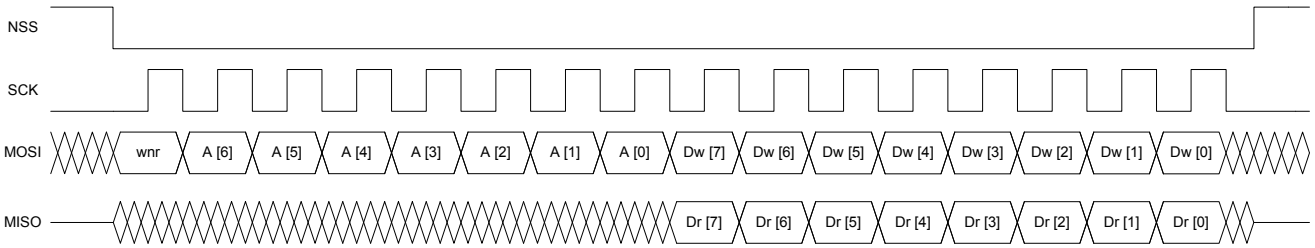


Figure 4-1: SPI Timing Diagram (Single Access)

MOSI is generated by the master on the falling edge of SCK and is sampled by the slave (i.e. this SPI interface) on the rising edge of SCK. MISO is generated by the slave on the falling edge of SCK.

A transfer always starts by the NSS pin going low. MISO is high impedance when NSS is high.

The first byte is the address byte. It is made of:

- wnr bit, which is 1 for write access and 0 for read access
- 7 bits of address, MSB first

The second byte is a data byte, either sent on MOSI by the master in case of a write access, or received by the master on MISO in case of read access. The data byte is transmitted MSB first.

Succeeding bytes may be sent on MOSI (for write access) or received on MISO (for read access) without rising NSS and re-sending the address. The address is then automatically incremented at each new byte received (BURST mode).

The frame ends when NSS goes high. The next frame must start with an address byte. The SINGLE access mode is actually a special case of BURST mode with only 1 data byte transferred. During the write accesses, the byte transferred from the slave to the master on the MISO line is the value of the written register before the write operation.

4.2 Digital IO Pin Mapping

Four general purpose IO pins are available on the SX1255 and their configuration is controlled through the RegDioMapping configuration register.

Table 4-1: DIO Mapping

Mode	DIO MApping	DIO3	DIO2	DIO1	DIO0
Sleep	00	-	-	-	-
	01	-	-	-	-
	10	-	-	-	-
	11	-	-	-	-
Standby	00	-	xosc_ready	-	-
	01	-	-	-	-
	10	-	-	-	-
	11	-	-	-	-
RX	00	pll_lock_rx	-	-	pll_lock_rx
	01	-	-	-	pll_lock_rx
	10	-	-	-	pll_lock_rx
	11	-	-	-	Low Bat
TX	00	pll_lock_tx	-	pll_lock_tx	-
	01	-	-	-	-
	10	-	-	-	-
	11	-	-	-	-

4.3 I and Q interface

There are two main ways of transferring the I and Q signals between the SX1255 and the external digital circuit.

In mode A, the I and Q signals are directly the outputs of the sigma-delta modulator in Rx, and the inputs of the FIR-DAC in Tx. This mode is the one which is implemented in the SX1255 circuit.

In mode B, the I and Q signals are pre- and post-processed by the internal digital bridge. In Rx the I and Q signals are decimated inside the chip and in Tx the I and Q signals are interpolated and $\Sigma\Delta$ modulated internally. In this mode the signals are transferred via an I2S-like protocol working in two possible configurations.

The table below gives the mapping of the pins as a function of the selected mode.

Table 4-2: Mapping of IO Pins Related to the I and Q Transfer

Pins	Mode A	Mode B1	Mode B2
10) CLK_OUT	CLK_OUT	CLK_OUT	CLK_OUT
11) CLK_IN	CLK_IN	Not used	Not used
12) Q_IN	Q_IN	Q_IN	Not used
13) I_IN	I_IN	I_IN	IQ_IN
14) Q_OUT	Q_OUT	Q_OUT	Not used
15) I_OUT	I_OUT	I_OUT	IQ_OUT
23) DIO2	Not used	WS	WS

4.3.1 Mode A

The convention of the I and Q interface for the Rx link in mode A is that the data is delivered on a rising edge of the internal clock, available on CLK_OUT. For the Tx link, the Tx DACs can be used either with the internal clock, available on CLK_OUT for data synchronization (SX1255 master) or with an input clock CLK_IN (SX1255 slave).

The figure below provides the timing diagram for the Tx link in mode A, in the case SX1255 is master:

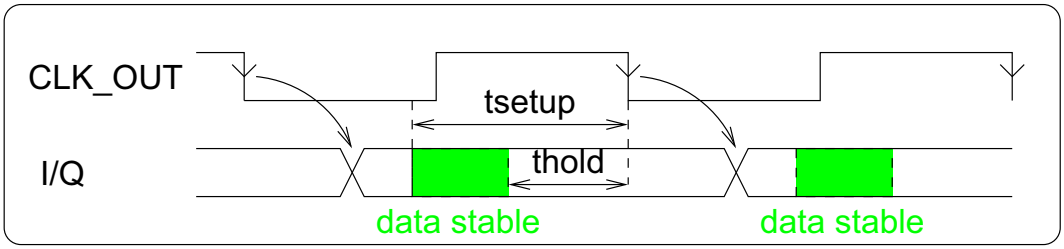


Figure 4-2: Tx timing diagram of I and Q interface in mode A (SX1255 master)

To relax the constraints on the setup and hold time, when SX1255 is used as master, it is recommended to use the **falling edge** of the clock (CLK_OUT) to provide the I&Q bitstreems to the chip. The circuit will sample the data on the next falling edge of the clock.

- tsetup_min = 14 ns
- thold_min = 0 ns

The figure below provides the timing diagram for the Tx link in mode A, in the case SX1255 is slave:

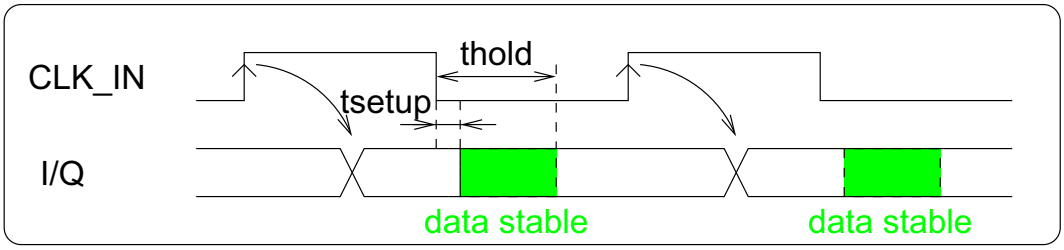


Figure 4-3: Tx timing diagram of I and Q interface in mode A (SX1255 slave)

In the case SX1255 is slave, CLK_IN is provided externally. The I/Q bitstreems should be provided on the **rising edge** of the CLK_IN clock and the circuit will sample the data on the falling edge of the clock.

- tsetup_min = 0 ns
- thold_min = 6 ns

4.3.2 Mode B

In mode B, the I and Q signals are pre- and post-processed by the internal digital bridge. An I2S based interface provides an easy way to transfer parallel I/Q data between the SX1255 and an external baseband chip.

In Rx mode, the serial I/Q data coming from the RF front-end (I_RX/Q_RX) is decimated in the digital bridge to generate parallel I/Q signals at a sampling rate depending on the programmed decimator factor. The I2S interface block is able then to convert this parallel I/Q data (buses i_in_bridge[31:0] / q_in_bridge[31:0]) into one or two I2S serial bitstream(s) and send it to an external baseband signal along with the other I2S signals as defined by the standard.

Similarly, in Tx mode the FIR-DACs are fed by two serial I/Q bitstreems coming from the digital bridge (I_TX/Q_TX). The I2S interface is able to convert the I2S serial data coming from an external baseband chip into parallel I/Q signals (buses i_out_bridge[31:0]/q_out_bridge[31:0]). Then these parallels signals are interpolated and ΣΔ modulated before being fed to the FIR_DACs. The figure below shows the I2S interface in its context in mode B:

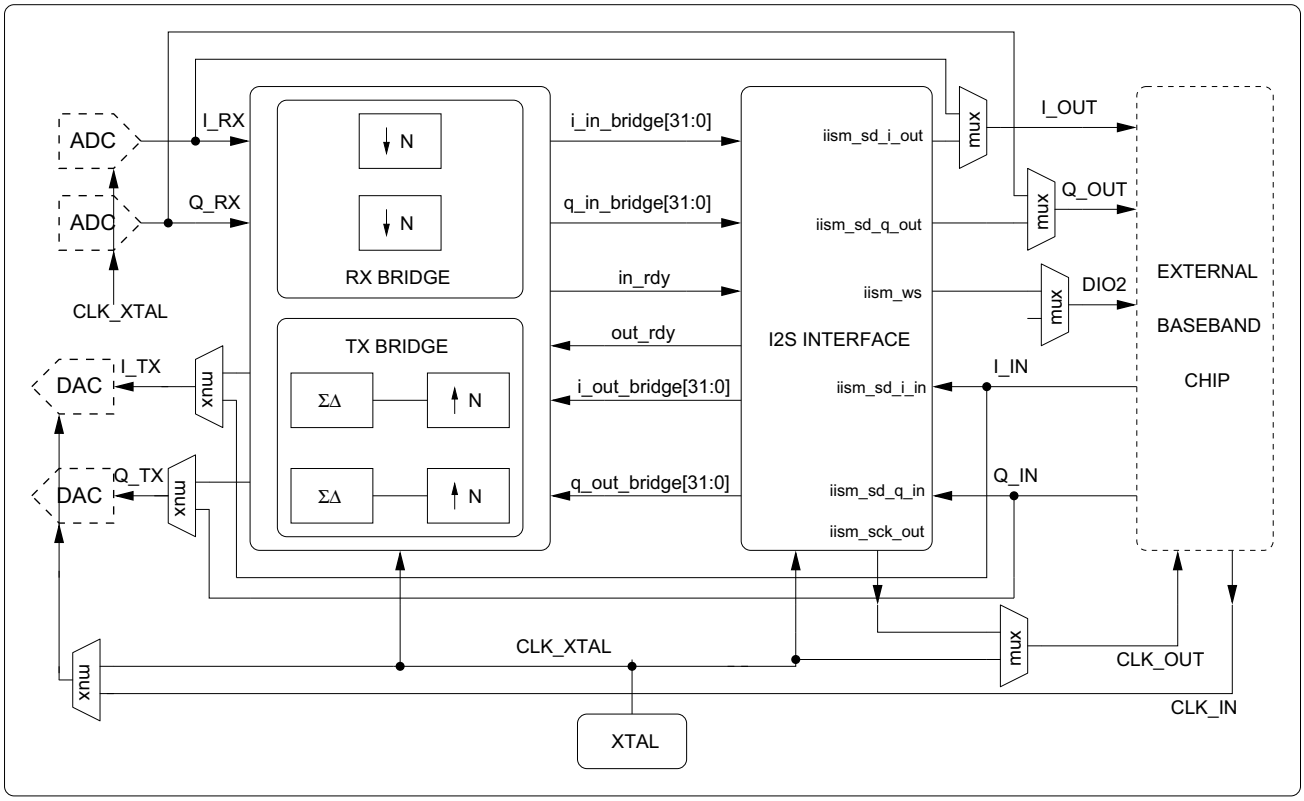


Figure 4-4: The I2S interface block in its context (mux cells are included in PAD_CTL block)

In B mode, the I2S interface is master of the I2S bus. The block generates the usual I2S signal, the clock CLK_OUT, the word select WS (available on DIO2 pin) and one or two serial data. It also samples the serial data coming from the external chip.

Mode B1 is an extension of the I2S format, where the I and Q serial data are not multiplexed on the same line but put or accepted on 2 pins I_OUT/Q_OUT or I_IN/Q_IN respectively in I2S transmitter mode or in I2S receiver mode. In mode B1, the WS frequency corresponds to half of the sampling rate of the parallel I/Q signals.

The figure below shows the timing diagram in B1 mode for samples of 8 bits wide, as an example, actually the number of bits is variable, as explained later on in this document.

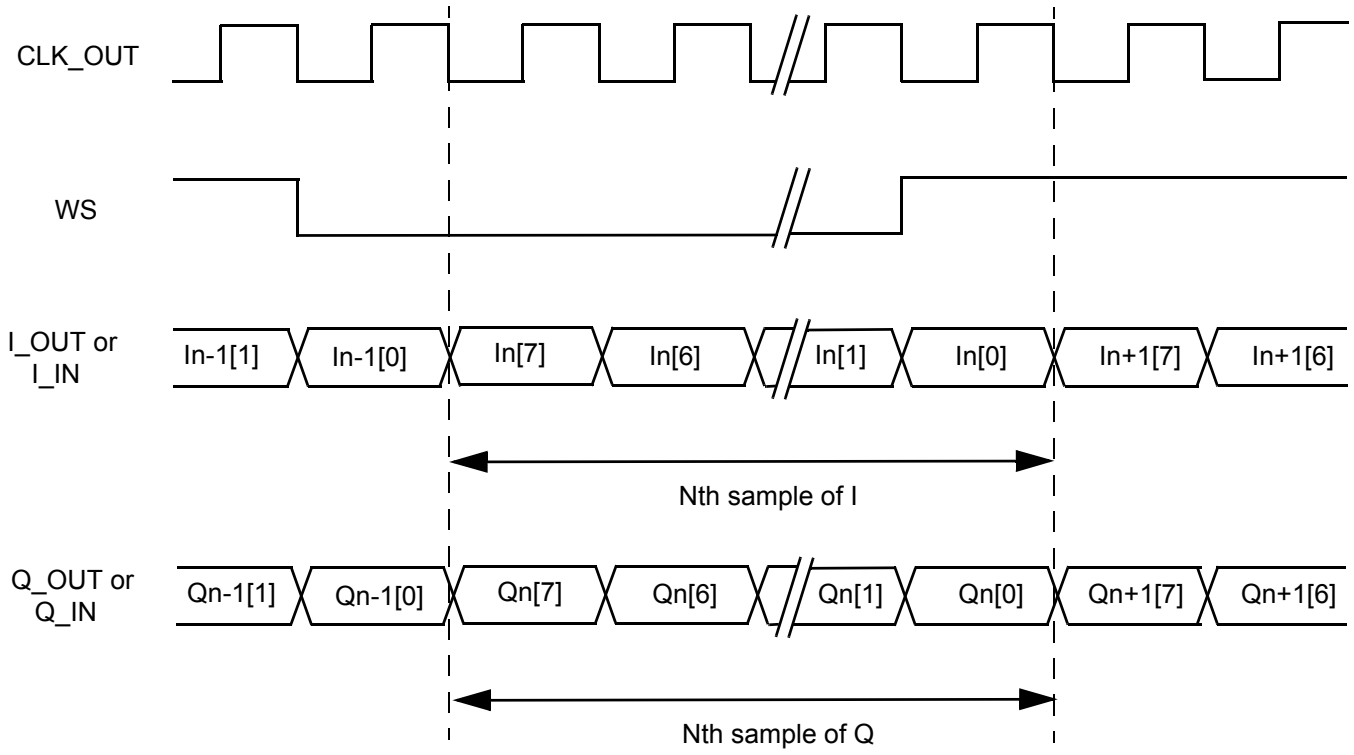


Figure 4-5: Timing diagram of I and Q interfaces in mode B1

Mode B2 is purely I2S compatible and the I/Q serial data is multiplexed on the I_OUT pin (Tx mode) or pin I_IN (Rx mode). Serial data with WS polarity set to “0” corresponds to I signal while WS polarity set to “1” corresponds to Q signal.

The figure below shows an example of timing diagram in B2 mode:

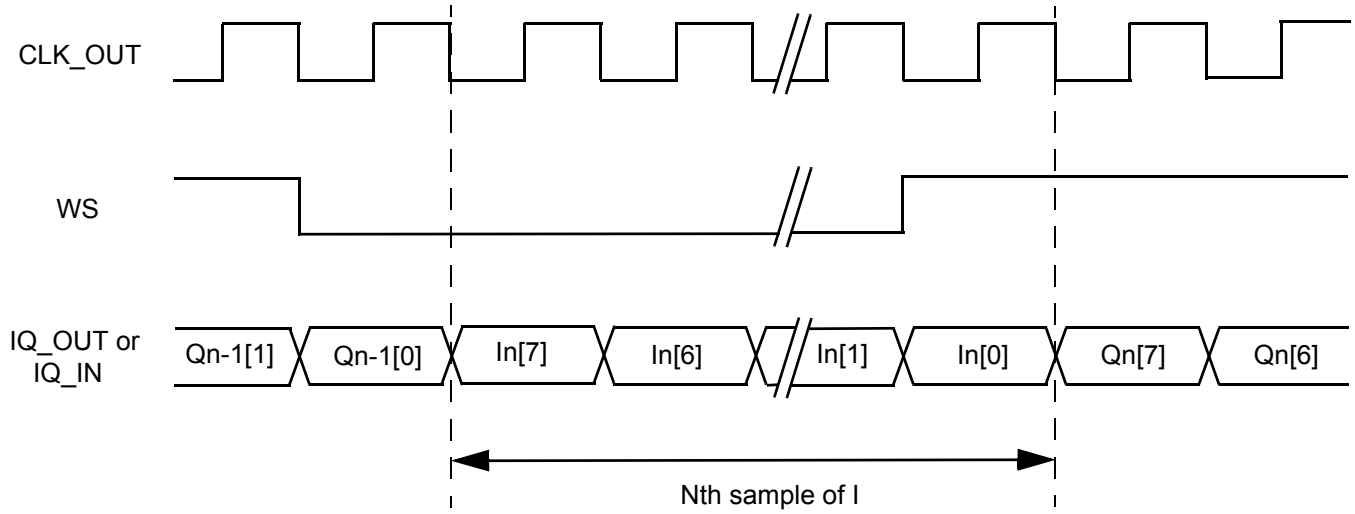


Figure 4-6: Timing diagram of I and Q interfaces in mode B2

In B mode the WS is one CLK_OUT clock period ahead of time.

The digital bridge and the I2S interface are automatically started in Tx and Rx mode as soon as the corresponding modes are activated. Disabled control bits are available in test mode.

The full duplex run is possible, but the user must be aware that in this case input and output I2S frames have the same format, hence the decimator and interpolation factors must be identical.

4.3.3 Parameters

Two main parameters are programmable:

- the decimation/interpolation factor
- the frequency of the output clock CLK_OUT.

The decimation/interpolation factor is programmable on 2 sets of 14 values.The ratios are defined as follows:

$$R = MANTx3^{m}x2^{n}$$

where MANT is 8 for the 1st set and 9 for the 2nd set, m can be 0 or 1, and n is an integer between 0 and 6.

The ratios available and the corresponding sampling rates are given below for 32 MHz, 36.864 MHz and 36 MHz crystals:

Table 4-3: Sampling rates 1st set

Sampling Rates vs Decimation / Interpolation factor [MS/s]	8	16	24	32	48	64	96	128	192	256	384	512	768	1536
32MHz xtal	4	2	1.333	1	0.667	0.5	0.333	0.25	0.167	0.125	0.083	0.063	0.042	0.021
36.864MHz xtal	4.608	2.304	1.536	1.152	0.768	0.576	0.384	0.288	0.192	0.144	0.096	0.072	0.048	0.024

Table 4-4: Sampling rates 2nd set

Sampling Rates vs Decimation / Interpolation factor [MS/s]	9	18	27	36	54	72	108	144	216	288	432	576	864	1728
36MHz xtal	4	2	1.333	1	0.667	0.5	0.333	0.25	0.167	0.125	0.083	0.063	0.042	0.021

Other frequencies between 32 and 36.9 MHz can be used with any decimation factor.

The frequency of the output clock CLK_OUT is equal to the crystal frequency divided by a ratio programmable on several values which are 1, 2, 4, 8, 12, 16, 24, 32 and 48. In IISM test mode, any integer between 1 and 64 can be selected.

The number of bits per sample depends on the decimation/interpolation factor (2 sets of 14 values) as well as the frequency of the CLK_OUT clock (9 possibilities) and the type of B mode. The allowed number of bits is between 8 and 32. In IISM test mode, any number of bits between 4 and 32 can be selected. Less than 4 bits is not possible for implementation reason

In B2 mode, there is a new I/Q sample every period of WS. In B1 mode, there are two I/Q samples every WS period, and the WS frequency is reduced by a factor of 2. This mode allows to allocate twice more bits per I/Q sample.

Only a limited number of parameters combination generate valid I2S frames. Therefore the valid combination are clearly documented and the other ones aborts the I2S interface. The tables below illustrate this statement. Depending on the XTAL/CLK_OUT divider and the decimation/interpolation factor, the number of bits per samples are computed for the 2 predefined sets. Combination with a number of bits higher than 32 and lower than 8 are disabled in functional mode (“NA”) and an error bit is set.

Table 4-5: Number of bits per sample for the 1st set and B1 mode

CLK_OUT/XTAL Decimation/ interpolation factor	1	2	4	8	12	16	24	32	48
8	8	NA	NA	NA	NA	NA	NA	NA	NA
16	16	8	NA	NA	NA	NA	NA	NA	NA
24	24	12	NA	NA	NA	NA	NA	NA	NA
32	32	16	8	NA	NA	NA	NA	NA	NA
48	NA	24	12	NA	NA	NA	NA	NA	NA
64	NA	32	16	8	NA	NA	NA	NA	NA
96	NA	NA	24	12	8	NA	NA	NA	NA
128	NA	NA	32	16	NA	8	NA	NA	NA
192	NA	NA	NA	24	16	12	8	NA	NA
256	NA	NA	NA	32	NA	16	NA	8	NA
384	NA	NA	NA	NA	32	24	16	12	8
512	NA	NA	NA	NA	NA	32	NA	16	NA
768	NA	NA	NA	NA	NA	NA	32	24	16
1536	NA	NA	NA	NA	NA	NA	NA	NA	32

Table 4-6: Number of bits per sample for the 2nd set and B1 mode

CLK_OUT/XTAL Decimation/ interpolation factor	1	2	4	8	12	16	24	32	48
9	9	NA	NA	NA	NA	NA	NA	NA	NA
18	18	9	NA	NA	NA	NA	NA	NA	NA
27	27	NA	NA	NA	NA	NA	NA	NA	NA
36	NA	18	9	NA	NA	NA	NA	NA	NA
54	NA	27	NA	NA	NA	NA	NA	NA	NA
72	NA	NA	18	9	NA	NA	NA	NA	NA
108	NA	NA	27	NA	9	NA	NA	NA	NA
144	NA	NA	NA	18	12	9	NA	NA	NA
216	NA	NA	NA	27	18	NA	9	NA	NA
288	NA	NA	NA	NA	24	18	12	9	NA
432	NA	NA	NA	NA	NA	27	18	NA	9
576	NA	NA	NA	NA	NA	NA	24	18	12
864	NA	NA	NA	NA	NA	NA	NA	27	18
1728	NA	NA	NA	NA	NA	NA	NA	NA	NA

Table 4-7: Number of bits per sample for the 1st set and B2 mode

CLK_OUT/XTAL Decimation/ interpolation factor	1	2	4	8	12	16	24	32	48
8	NA	NA	NA	NA	NA	NA	NA	NA	NA
16	8	NA	NA	NA	NA	NA	NA	NA	NA
24	12	NA	NA	NA	NA	NA	NA	NA	NA
32	16	8	NA	NA	NA	NA	NA	NA	NA
48	24	12	NA	NA	NA	NA	NA	NA	NA
64	32	16	8	NA	NA	NA	NA	NA	NA
96	NA	24	12	NA	NA	NA	NA	NA	NA
128	NA	32	16	8	NA	NA	NA	NA	NA
192	NA	NA	24	12	8	NA	NA	NA	NA
256	NA	NA	32	16	NA	8	NA	NA	NA
384	NA	NA	NA	24	16	12	8	NA	NA
512	NA	NA	NA	32	NA	16	NA	8	NA
768	NA	NA	NA	NA	32	24	16	12	8
1536	NA	NA	NA	NA	NA	NA	32	24	16

Table 4-8: Number of bits per sample for the 2nd set and B2 mode

CLK_OUT/XTAL Decimation/ interpolation factor	1	2	4	8	12	16	24	32	48
9	NA	NA	NA	NA	NA	NA	NA	NA	NA
18	9	NA	NA	NA	NA	NA	NA	NA	NA
27	NA	NA	NA	NA	NA	NA	NA	NA	NA
36	18	9	NA	NA	NA	NA	NA	NA	NA
54	27	NA	NA	NA	NA	NA	NA	NA	NA
72	NA	18	9	NA	NA	NA	NA	NA	NA
108	NA	27	NA	NA	NA	NA	NA	NA	NA
144	NA	NA	18	9	NA	NA	NA	NA	NA
216	NA	NA	27	NA	9	NA	NA	NA	NA
288	NA	NA	NA	18	12	9	NA	NA	NA
432	NA	NA	NA	27	18	NA	9	NA	NA
576	NA	NA	NA	NA	24	18	12	9	NA
864	NA	NA	NA	NA	NA	27	18	NA	9
1728	NA	NA	NA	NA	NA	NA	NA	27	18

The parallel I/Q data bus is expected to be 32-bits wide. Hence, if the number of bits per frame is lower, the I/Q data is truncated, either MSBs or the LSBs are taken, according to a configuration bit, iism_trunc_mode.

5. Configuration and Status Registers

5.1 General Registers

Notes

- Reset values are automatically refreshed at Power on Reset
- DEFAULT values are the Semtech recommended register values, optimizing the device operation
- Registers for which the DEFAULT value differs from the RESET values are denoted by a * in the tables of this section

Table 5-1: General Registers

Name (Address)	Bits	Name	Mode	Reset	Description
Mode (0x00)	7-4	-	r	0x00	unused
	3	driver_enable	rw	0x00	Enables the PA driver
	2	tx_enable	rw	0x00	Enables the complete TX part of the front-end (except the PA)
	1	rx_enable	rw	0x00	Enables the complete RX part of the front-end
	0	ref_enable	rw	0x01	Enables the PDS and the oscillator
FRFH_RX (0x01)	7-0	freq_rf_rx(23:16)	rw	0xC0	MSB of RF RX carrier frequency
FRFM_RX (0x02)	7-0	freq_rf_rx(15:8)	rw	0xE3	MSB of RF RX carrier frequency
FRFL_RX (0x03)	7-0	freq_rf_rx(7:0)	rw	0x8E	LSB of RF RX carrier frequency $f_{RF\_RX} = \frac{F(XOSC) \times freq\_rf\_rx}{2^{20}}$ Resolution is 34.3323 Hz if F_{XOSC} = 36 MHz Default value is 0xC0E38E = 434 MHz The RX RF frequency is taken into account internally only when: - FRFL_RX is written - leaving SLEEP mode (ref_enable 0-1 transition)
FRFH_TX (0x04)	7-0	freq_rf_tx(23:16)	rw	0xC0	MSB of RF TX carrier frequency
FRFM_TX (0x05)	7-0	freq_rf_tx(15:8)	rw	0xE3	MSB of RF TX carrier frequency

Table 5-1: General Registers

Name (Address)	Bits	Name	Mode	Reset	Description
FRFL_TX (0x06)	7-0	freq_rf_tx(7:0)	rw	0x8E	LSB of RF RX carrier frequency $f_{RF\_RX} = \frac{F(XOSC) \times freq\_rf\_tx}{2^{20}}$ Resolution is 34.3323 Hz if F_{XOSC} = 36 MHz Default value is 0xC0E38E = 434 MHz The RX RF frequency is taken into account internally only when: - FRFL_RX is written - leaving SLEEP mode (ref_enable 0-1 transition)
VERSION (0x07)	7-0	chip_version(7:0)	r	0x11	Version code of the chip Bits 7-4 give the fill revision number Bits 3-0 give the metal mask revision number Current value is V1A

5.2 Transmitter Front-End Configuration Registers

Table 5-2: Transmitter Front-End Configuration Registers

Address	Bits	Name	Mode	Reset	Description
TXFE1 (0x08)	7	-	r	0x00	Unused
	6-4	TxDacGain	rw	0x02	DAC gain, programmable in 3 dB steps: 000 = maximum gain - 9 dB 001 = maximum gain - 6 dB 010 = maximum gain - 3 dB 011 = maximum gain (0 dB full scale) 100 and higher: test modes not recommended: 100 => Max gain - 9 dB with test Vref voltage 101 => Max gain - 6 dB with test Vref voltage 110 => Max gain - 3 dB with test Vref voltage 111 => Max gain, 0 dBFS with test Vref voltage
	3-0	TXMixerGain	rw	0x0E *	Mixer gain, programmable in 2 dB steps *Gain ~ -37.5 + 2 x TxMixerGain(3,0))* in dB
TXFE2 (0x09)	7-6	-	r	0x00	unused
	5-3	tx_mixer_tank_cap(2:0)	rw	0x04	Capacitance in parallel with the mixer tank: Cap = 128 * tx_mixer_tank_cap(2:0) [fF]
	2-0	tx_mixer_tank_res(2:0)	rw	0x04 *	Resistance in parallel with the mixer tank: 000 -> 0.95 kΩ 100 -> 2.18 kΩ 001 -> 1.11 kΩ 101 -> 3.24 kΩ 010 -> 1.32 kΩ 110 -> 6.00 kΩ 011 -> 1.65 kΩ 111 -> none => about 64 kΩ
TXFE3 (0x0A)	7	-	r	0x00	unused
	6-5	tx_pll_bw	rw	0x03	Tx PLL bandwidth PLL BW = (rx_pll_bw + 1)*75 KHz
	4-0	tx_filter_bw(4:0)	rw	0x00	Tx analog filter bandwidth DSB: BW_{3dB} = 17.15 / (41 - tx_filter_bw(4:0)) MHz
TXFE4 (0x0B)	7-3	-	rw	0x00	unused
	2-0	tx_dac_bw(2:0)	rw	0x02	Number of taps of FIR-DAC: Actual number of taps = 24 + 8.tx_dac_bw(2:0) max = 64

5.3 Receiver Front-End Configuration Registers

Table 5-3: Receiver Front-End Configuration Registers

Address	Bits	Name	Mode	Reset	Description
RXFE1 (0x0C)	7-5	RxLnaGain(2:0)	rw	0x01	RX LNA gain setting: 000 = not used 001 = G1 = highest gain power - 0 dB 010 = G2 = highest gain power - 6 dB 011 = G3 = highest gain power - 12 dB 100 = G4 = highest gain power - 24 dB 101 = G5 = highest gain power - 36 dB 110 = G6 = highest gain power - 48 dB 111 = not used
	4-1	rx_p-ga_gain(3:0)	rw	0x0F	PGA gain setting: Gain=lowest gain + 2dB * rx_pga_gain
	0	rx_zin_200	rw	0x01	input impedance 0 = 50 Ω 1 = 200 Ω
RXFE2 (0x0D)	7-5	rx_adc_bw(2:0)	rw	0x07	RX ΣΔ ADC bandwidth configuration For BW>400kHz SSB use 0x07 For 200kHz< BW<400kHz SSB use 0x05 For 100kHz<BW<400kHz SSB use 0x02 use 0x01 instead
	4-2	rx_ad-c_trim(2:0)	rw	0x05*	RX ADC trim for 36 MHz reference crystal
	1-0	rx_p-ga_bw(1:0)	rw	0x01	RX analog roofing filter, programmable: 00 = 1500 kHz 01 = 1000 kHz 10 = 750 kHz 11 = 500 kHz
RXFE3 (0x0E)	7-3	-	r	0x00	unused
	2-1	rx_pll_bw(1:0)	rw	0x03	Rx PLL bandwidth PLL BW = (rx_pll_bw + 1)*75 KHz
	0	rx_adc_temp	rw	0x00	sets the RX ADC into temperature measurement mode

5.4 IRC and PIN Mapping Registers

Table 5-4: IRC and PIN Mapping Registers

Address	Bits	Name	Mode	Reset	Description
IO_MAP (0x0F)	7-6	iomap0(1:0)	rw	0x00	Mapping of DIO(0) 00: pll_lock_rx 01 :pll_lock_rx 10: pll_lock_rx 11: eol
	5-4	iomap1(1:0)	rw	0x00	Mapping of DIO(1) 00: pll_lock_tx
	3-2	iomap2(1:0)	rw	0x00	Mapping of DIO(2) 00: xosc_ready
	1-0	iomap3(1:0)	rw	0x00	Mapping of DIO(3) 00: pll_lock_rx in Rx mode & pll_lock_tx in all other modes

5.5 Additional Parameter Configuration Registers

Table 5-5: Additional Parameter Configuration Registers

Address	Bits	Name	Mode	Reset	Description
CK_SEL (0x10)	7-4	-	r	0x00	unused
	3	dig_loopback_en	rw	0x00	Enables the digital loop back mode of the frontend
	2	rf_loopback_en	rw	0x00	Enables the RF loop back mode of the frontend
	1	ckout_enable	rw	0x01	0: output clock disabled on pad CLK_OUT 1: output clock enabled on pad CLK_OUT
	0	ck_select_tx_dac	rw	0x00	0: internal clock (CLK_XTAL) used for Tx DAC 1: external clock (CLK_IN) used for Tx DAC
STAT (0x11)	7-3	-	r	0x00	unused
	3	eol	r	0x00	EOL output signal 0 to VBAT > EOL threshold 1 to VBAT < EOL threshold (battery low)
	2	xosc_ready	rw	0x00	Goes high when the XOSC is ready
	1	pll_lock_rx	r	0x00	Asserted when the Rx PLL is locked
	0	pll_lock_tx	r	0x00	Asserted when the Tx PLL is locked

Table 5-5: Additional Parameter Configuration Registers

Address	Bits	Name	Mode	Reset	Description
IISM (0x12)	7	iism_rx_disable	rw	0x00	disable IISM Rx (during TX mode)
	6	iism_tx_disable	rw	0x00	disable IISM Tx (during RX mode)
	5-4	iism_mode[1:0]	rw	0x00	00 -> mode A 01 -> mode B1 10 -> mode B2 11 -> not used
	3-0	iism_clk_div[3:0]	rw	0x00	XTAL/CLK_OUT division factor 0000 -> 1 0001 -> 2 0010 -> 4 0011 -> 8 0100 -> 12 0101 -> 16 0110 -> 24 0111 -> 32 1000 -> 48 higher values not used
DIG_BRIDGE (0x13)	7	int_dec_mantisse	rw	0x00	interpolation/decimation factor = mant * 3^m * 2^n 0 -> 1st set; mant=8 1 -> 2nd set; mant=9
	6	int_dec_m_parameter	rw	0x00	interpolation/decimation factor = mant * 3^m * 2^n m value
	5-3	int_dec_n_parameter	rw	0x00	interpolation/decimation factor = mant * 3^m * 2^n n value (accepted values 0 to 6)
	2	IISM_truncation	rw	0x00	IISM truncation mode in Rx and Tx 0 -> MSB is truncated, alignement on LSB 1 -> LSB is truncated, alignement on MSB
	1	IISM_status_flag	r	0x00	IISM error status bit when selected factors force IISM off 0 -> no error 1 -> error, IISM off
	0	unused	r	0x00	

6. Application Information

6.1 Crystal Resonator Specification

The specification for the crystal resonator of the reference oscillator circuit block is tabulated below.

Table 6-1: Crystal Resonator Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FXOSC	XTAL Frequency	-	32	-	36.864	MHz
RS	XTAL Series Resistance	-	-	30	140	Ω
C0	XTAL Shunt Capacitance	-	-	2.8	7	pF
CLOAD	External Foot Capacitance	On each pin XTA and XTB	8	16	22	pF

Notes:

- **The initial frequency tolerance, temperature stability and ageing performance should be chosen in accordance with the target operating temperature range and the receiver bandwidth selected**
- **The loading capacitance should be applied externally and adapted to the actual Crystal Cload specification**

6.2 Reset of the Chip

A power-on reset of the SX1255 is automatically triggered at power up. Additionally, a manual reset can be issued by controlling the RESET pin (pin 9).

6.2.1 POR

If the application requires the disconnection of VDD from the SX1255, despite the extremely low Sleep Mode current, the user should wait for 10 ms from of the end of the POR cycle before commencing communications over the SPI bus. Pin 9 (RESET) should be left floating during the POR sequence.

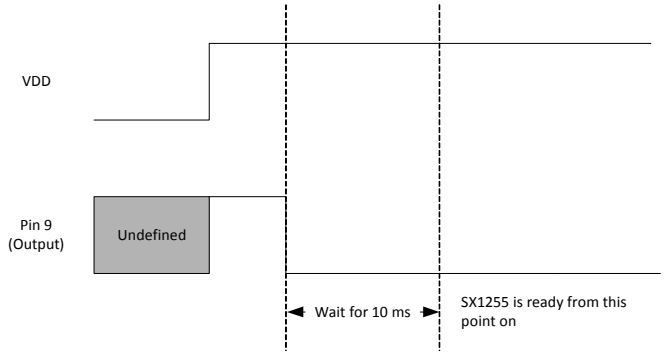


Figure 6-1: POR Timing Diagram

Note that xosc_ready on DIO2 can be used to detect that the chip is ready.

6.2.2 Manual Reset

A manual reset of the SX1255 is possible even for applications in which VDD cannot be physically disconnected. Pin 9 should be pulled high for a hundred microseconds, and then released. The user should then wait for 5 ms before using the chip.

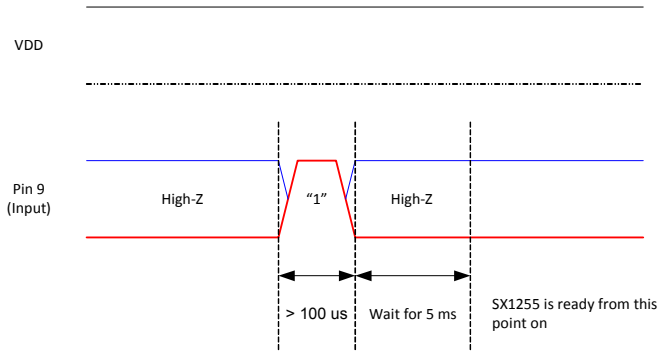


Figure 6-2: Manual Reset Timing Diagram

Note that whilst pin 9 is driven high, an over current consumption of 10 mA may be observed on VDD.

6.2.3 TX Noise Shaper

In order to generate a single TX bit-stream, th 8-bit I and Q signal should be processed by an external third order sigma-delta modulator (implemented within the baseband processor). The noise shaper should be stable for input signals lower than -3dBFS and compatible with SX1255 noise requirements. It is advised that the integrator outputs are saturated to avoid any wraparound of the 2's-complement digital word.

A representative block diagram of a single-bit feed-forward modulator is illustrated below.

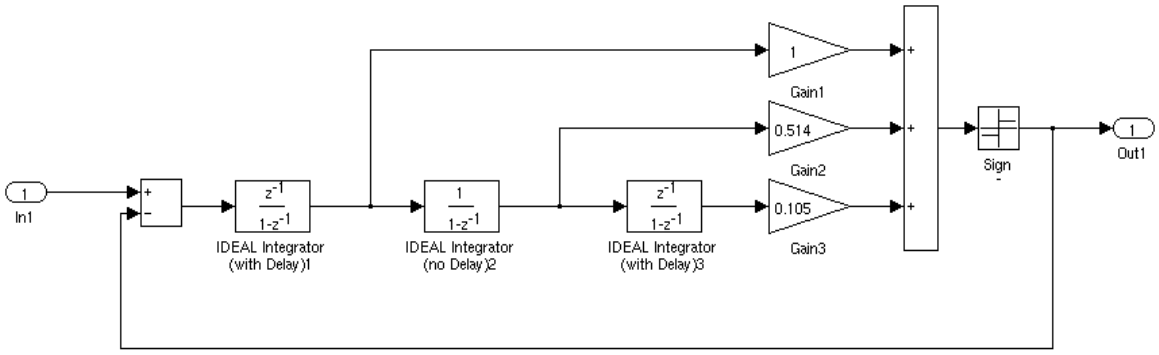


Figure 6-3: Example of a Digital Modulator Implementation

6.3 Application Schematics

Please contact your Semtech representative for evaluation tools, reference designs and design assistance. Note that all schematics shown in this section are full schematics, listing ALL required components, including those required for power supply decoupling.

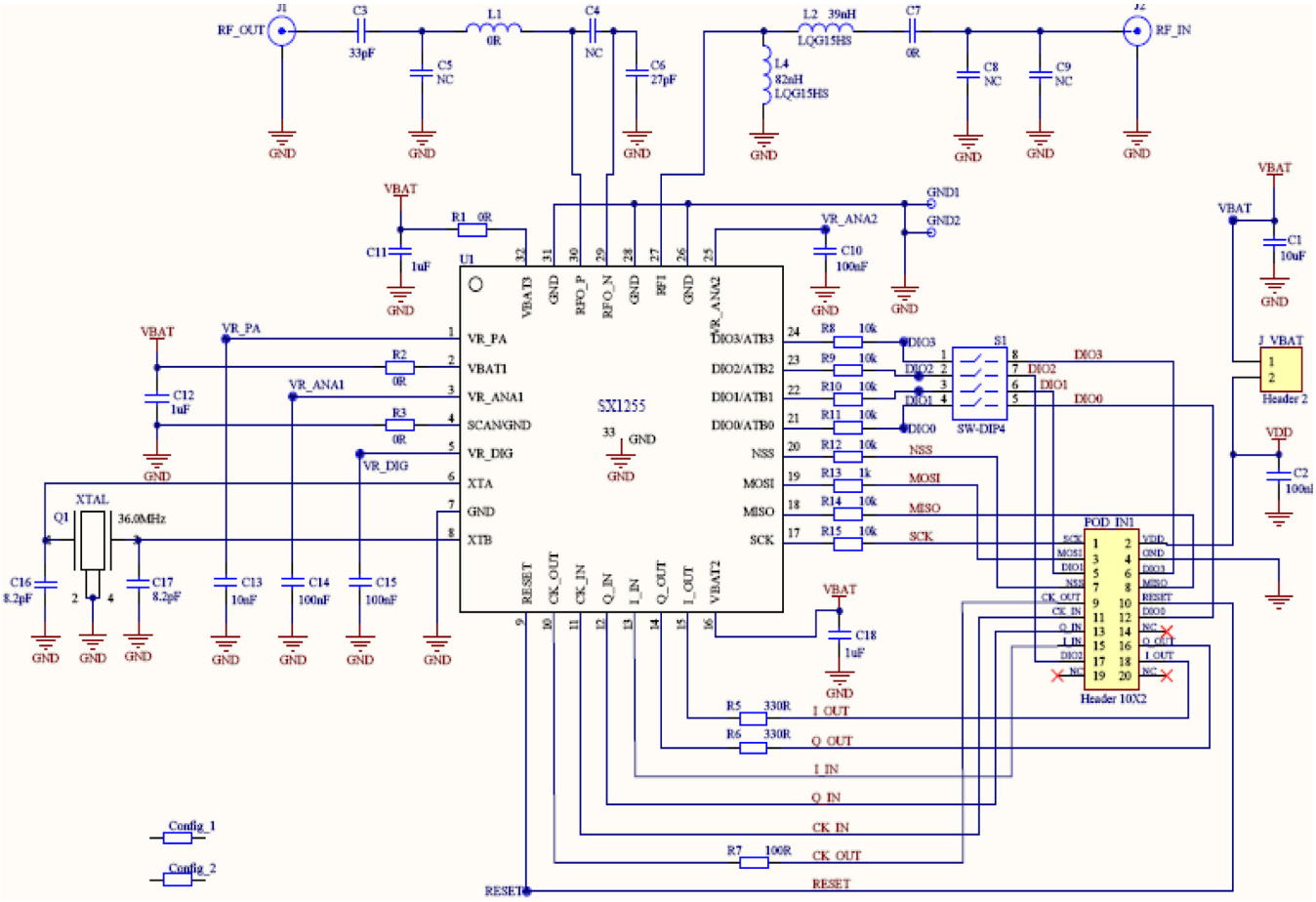


Figure 6-4: Application Schematic of the SX1255

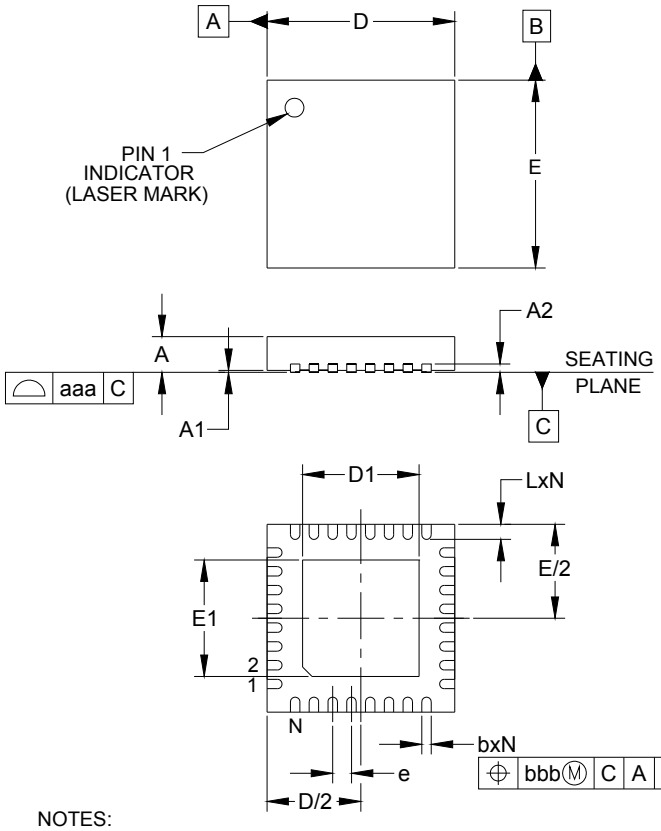
Note:

The application schematic presented here is for information only.

Always refer to the latest reference designs posted on *www.semtech.com*.

7. Packaging Information

7.1 Package Outline Drawing



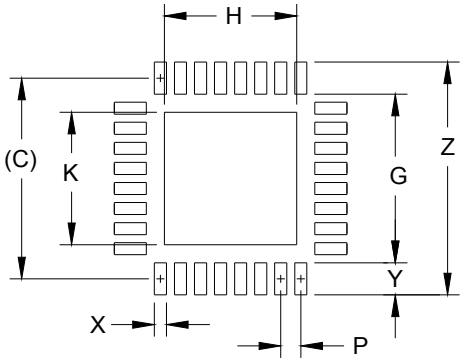
DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.028	.030	.031	0.70	0.75	0.80
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.008	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.118	.122	.126	3.00	3.10	3.20
E	.193	.197	.201	4.90	5.00	5.10
E1	.118	.122	.126	3.00	3.10	3.20
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 7-1: Package Outline Drawing

7.2 Recommended Land Pattern



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.193)	(4.90)
G	.161	4.10
H	.130	3.30
K	.130	3.30
P	.020	0.50
X	.012	0.30
Y	.031	0.80
Z	.224	5.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE-DIMENSIONS APPLY IN BOTH X AND Y DIRECTIONS.

Figure 7-2: Recommended Land Pattern

7.3 Package Marking

Figure 7-3: SX1255 Marking Diagram

Notes:

- yyww refers to the data code
- xxxxxx refers to the lot number

7.4 Thermal Impedance

The thermal impedance of this package is: **Theta ja = 23.8° C/W typ**., calculated from a package in still air, on a 4-layer FR4 JEDEC PCB.

7.5 Tape and Reel Specification

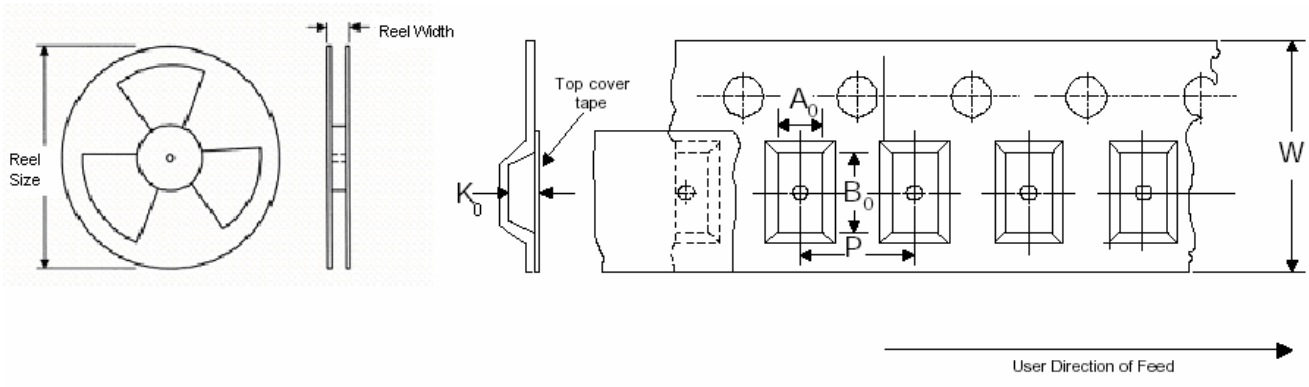


Figure 7-4: Tape and Reel Specification

Table 7-1: Tape and Reel Specification

Carrier Tape (mm)				Reel (mm)				
Tape Width (W)	**Pocket Pitch (P)**	**A_O / B_O**	**K_O**	**Reel Size**	**Reel Width**	**Min. Trailer Length (mm)**	**Min. Leader Length (mm)**	**QTY per Reel**
12 +/- 0.30	8 +/- 0.20	5.25 +/- 0.20	1.10 +/- 0.10	330.2	12.4	400	400	3000

Note: Single sprocket holes

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