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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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### MOS FIELD EFFECT TRANSISTOR

2SK3480

## SWITCHING N-CHANNEL POWER MOS FET

#### **DESCRIPTION**

The 2SK3480 is N-channel MOS Field Effect Transistor designed for high current switching applications.

#### **FEATURES**

• Super low on-state resistance:

 $R_{DS(on)1} = 31 \text{ m}\Omega \text{ MAX. (VGS} = 10 \text{ V, ID} = 25 \text{ A})$   $R_{DS(on)2} = 36 \text{ m}\Omega \text{ MAX. (VGS} = 4.5 \text{ V, ID} = 25 \text{ A})$ 

- Low Ciss: Ciss = 3600 pF TYP.
- Built-in gate protection diode

#### **ORDERING INFORMATION**

PART NUMBER	PACKAGE
2SK3480	TO-220AB
2SK3480-S	TO-262
2SK3480-ZJ	TO-263
2SK3480-Z	TO-220SMD <sup>Note</sup>

**Note** TO-220SMD package is produced only in Japan.

(TO-220AB)

#### ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V)	VDSS	100	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±20	V
Drain Current (DC) (Tc = 25°C)	ID(DC)	±50	Α
Drain Current (pulse) Note1	ID(pulse)	±100	Α
Total Power Dissipation (Tc = 25°C)	P <sub>T1</sub>	84	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.5	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note2	las	34	Α
Single Avalanche Energy Note2	Eas	116	mJ

**Notes 1.** PW  $\leq$  10  $\mu$ s, Duty cycle  $\leq$  1%

**2.** Starting T<sub>ch</sub> = 25°C, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V



(TO-262)



(TO-263, TO-220SMD)

#### THERMAL RESISTANCE

Channel to Case	Rth(ch-C)	1.48	°C/W
Channel to Ambient	Rth(ch-A)	83.3	°C/W



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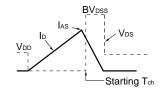


#### **ELECTRICAL CHARACTERISTICS (TA = 25°C)**

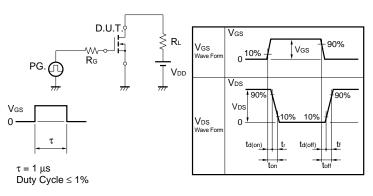
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V			10	μΑ
Gate Leakage Current	Igss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 25 A	17	34		S
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, ID = 25 A		25	31	mΩ
	RDS(on)2	Vgs = 4.5 V, ID = 25 A		27	36	mΩ
Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		3600		pF
Output Capacitance	Coss	V <sub>G</sub> s = 0 V		360		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		190		pF
Turn-on Delay Time	<b>t</b> d(on)	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 25 A		15		ns
Rise Time	<b>t</b> r	V <sub>G</sub> S = 10 V		11		ns
Turn-off Delay Time	t <sub>d(off)</sub>	$R_G = 0 \Omega$		68		ns
Fall Time	<b>t</b> f			6.0		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = 80 V		74		nC
Gate to Source Charge	Qgs	V <sub>G</sub> S = 10 V		10		nC
Gate to Drain Charge	Q <sub>GD</sub>	ID = 50 A		20		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	IF = 50 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	I <sub>F</sub> = 50 A, V <sub>GS</sub> = 0 V		70		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		180		nC

#### TEST CIRCUIT 1 AVALANCHE CAPABILITY

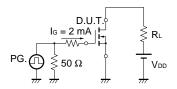
# $\begin{array}{c} \text{D.U.T.} \\ \text{Rg} = 25 \ \Omega \\ \text{Vgs} = 20 \rightarrow 0 \ \text{V} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{PG.} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \\ \text{$\downarrow$} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{$\downarrow$} \\ \text{$$



#### **TEST CIRCUIT 2 SWITCHING TIME**

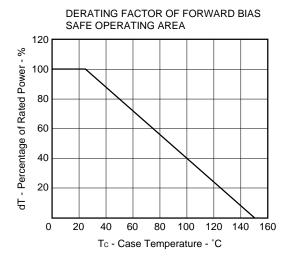


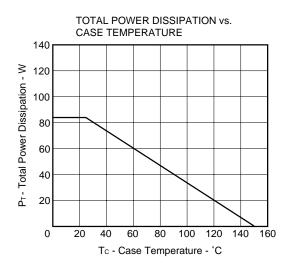
#### **TEST CIRCUIT 3 GATE CHARGE**



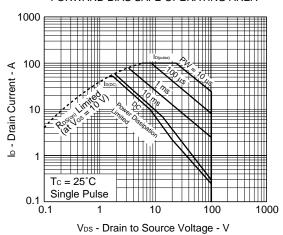


#### TYPICAL CHARACTERISTICS (TA = 25°C)

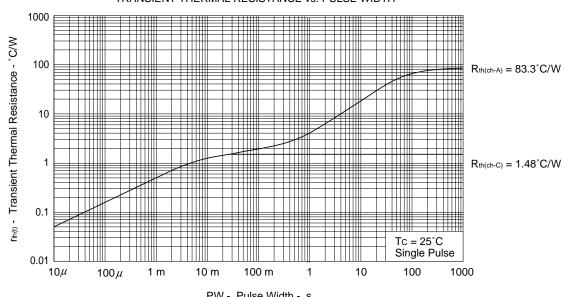




#### FORWARD BIAS SAFE OPERATING AREA



#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

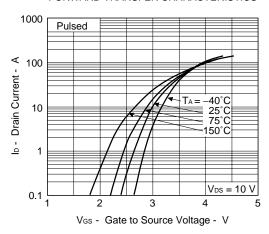


PW - Pulse Width - s

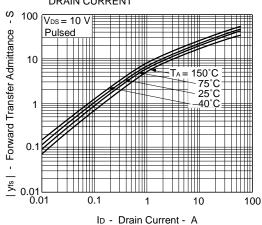
3



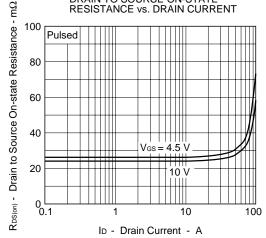
#### FORWARD TRANSFER CHARACTERISTICS



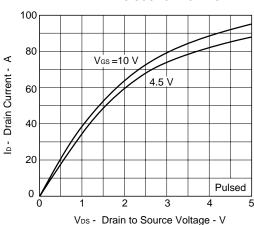
#### FORWARD TRANSFER ADMITTANCE vs. **DRAIN CURRENT**



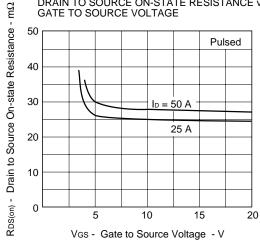
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



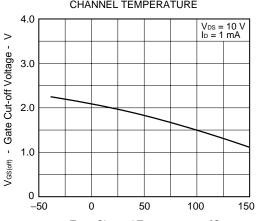
## DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



#### DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

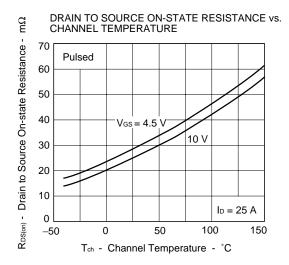


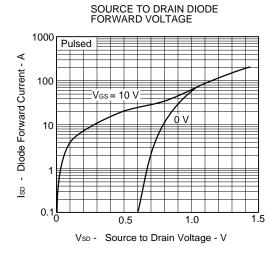
## GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE

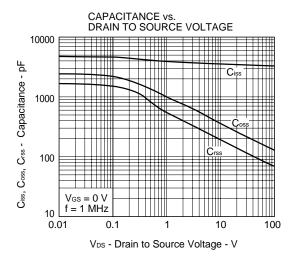


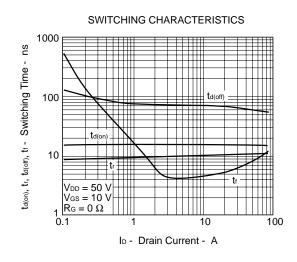
Tch - Channel Temperature - °C

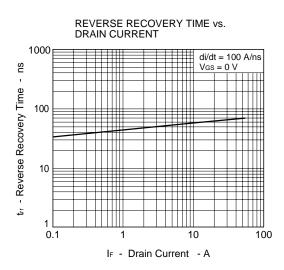


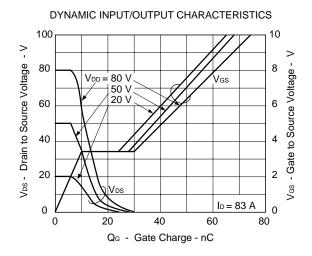


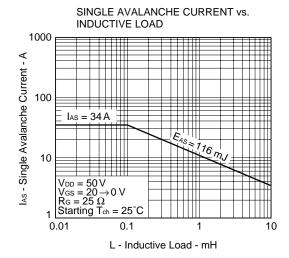


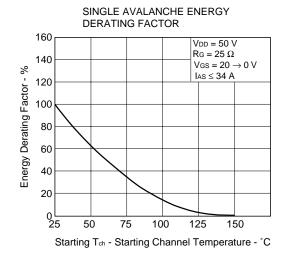








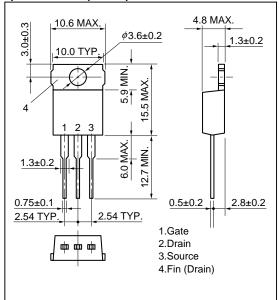




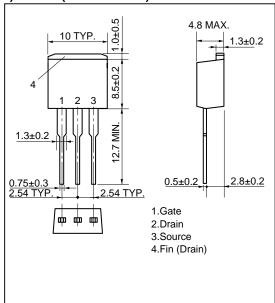


#### PACKAGE DRAWINGS (Unit: mm)

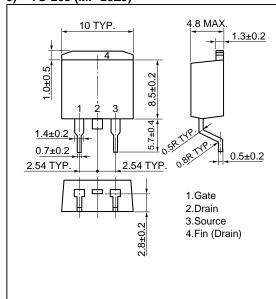
#### 1) TO-220AB(MP-25)



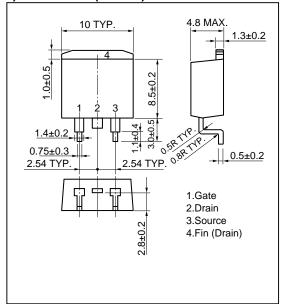
#### 2) TO-262(MP-25 Fin Cut)



#### 3) TO-263 (MP-25ZJ)

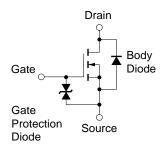


#### 4) TO-220SMD(MP-25Z)<sup>Note</sup>



#### **EQUIVALENT CIRCUIT**

**Note** This package is produced only in Japan.



#### Remark

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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