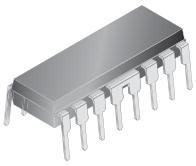
Protected Quad Driver with Fault Detection and Sleep Mode

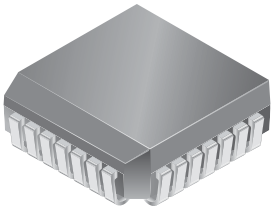
Features and Benefits

- 300 mA output current per channel
- Independent overcurrent protection and thermal limiting for each driver
- Output voltage to 60 V
- Output SOA protection
- Fault-detection circuitry for open or shorted load
- Low quiescent current Sleep Mode
- Integral output flyback/clamp diodes
- TTL- and 5 V CMOS-compatible inputs

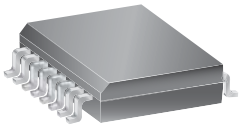
Packages:



Package B, 16-pin DIP with exposed tabs



Package EB, 28-pin PLCC with internally fused pins



Package LB, 16-pin SOIC with internally fused pins

Not to scale

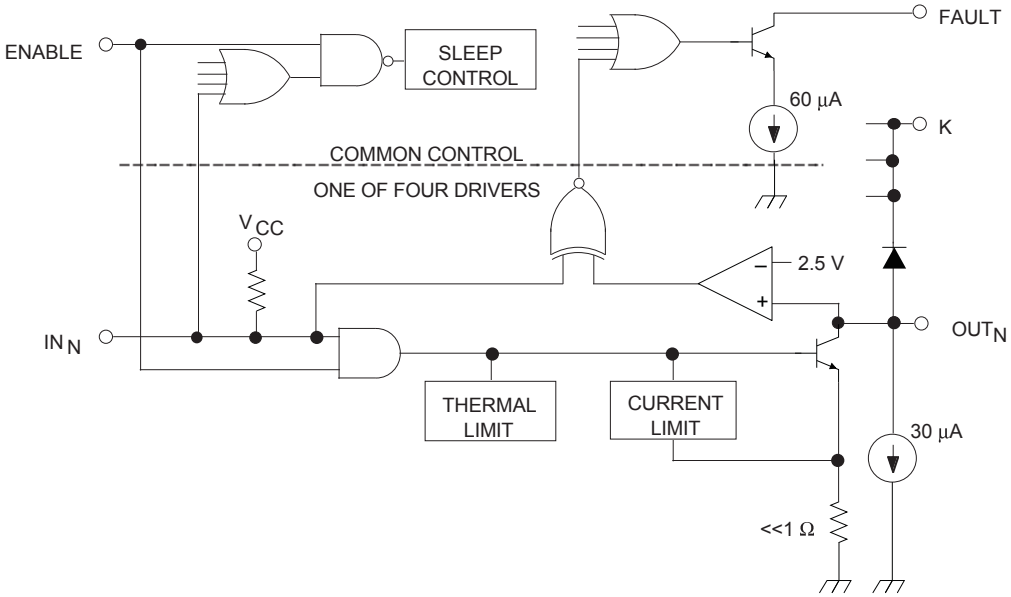
Description

The A2557 has been specifically designed to provide cost-effective solutions to relay-driving applications with up to 300 mA drive current per channel. They may also be used for driving incandescent lamps in applications where turn-on time is not a concern. Each of the four outputs will sink 300 mA in the on state. The outputs have a minimum breakdown voltage of 60 V and a sustaining voltage of 40 V. A low-power Sleep Mode is activated with either ENABLE low or all inputs low. In this mode, the supply current drops to below 100 µA.

Overcurrent protection for each channel has been designed into these devices and is activated at a nominal 500 mA. It protects each output from short circuits with supply voltages up to 32 V. When an output experiences a short circuit, the output current is limited at the 500 mA current clamp. In addition, foldback circuitry decreases the current limit if an excessive voltage is present across the output and assists in keeping the device within its SOA (safe operating area). An exclusive-OR circuit compares the input and output state of each driver. If either a short or open load condition is detected, a single FAULT output is turned on (active low).

Continued on the next page…

Functional Block Diagram



Description (continued)

Continuous or multiple overload conditions causing the channel temperature to reach approximately 165°C will result in an additional linear decrease in the output current of the affected driver. If the fault condition is corrected, the output stage will return to its normal saturated condition.

The packages offer fused leads for enhanced thermal dissipation. Package B is a 16-pin power DIP with exposed tabs, EB is a 28-lead power PLCC, and LB is a 16-lead power wide-body SOIC for surface-mount applications. The lead (Pb) free versions have 100% matte tin leadframe plating.

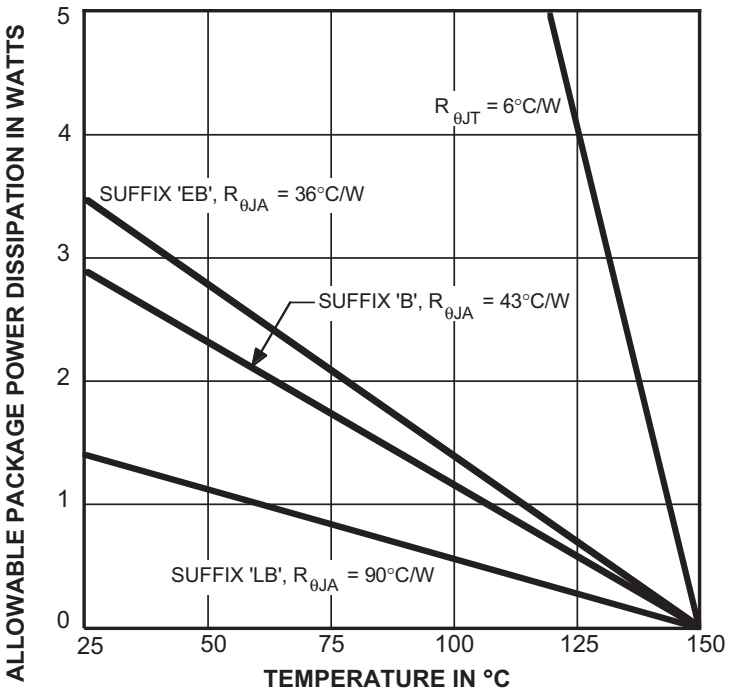
Selection Guide

Part Number	Pb-free	Package	Packing	Ambient Temperature (°C)
~~A2557EB-T*~~	Yes	16-pin DIP, exposed tabs	25 pieces per tube	–40 to 85
~~A2557EEBTR-T*~~	Yes	28-lead PLCC	800 pieces per reel	
~~A2557ELBTR-T*~~	Yes	16-lead SOIC	1000 pieces per reel	
~~A2557KB*~~	–	16-pin DIP, exposed tabs	25 pieces per tube	–40 to 125
~~A2557KB-T*~~	Yes	16-pin DIP, exposed tabs	25 pieces per tube	
~~A2557KEBTR-T*~~	Yes	28-lead PLCC	800 pieces per reel	
~~A2557KLBTR*~~	–	16-lead SOIC	1000 pieces per reel	
A2557KLBTR-T	Yes	16-lead SOIC	1000 pieces per reel	
~~A2557SB-T*~~	Yes	16-pin DIP, exposed tabs	25 pieces per tube	–20 to 85
~~A2557SEBTR-T*~~	Yes	28-lead PLCC	800 pieces per reel	
~~A2557SLBTR-T*~~	Yes	16-lead SOIC	1000 pieces per reel	

*Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: May 4, 2009.

Absolute Maximum Ratings

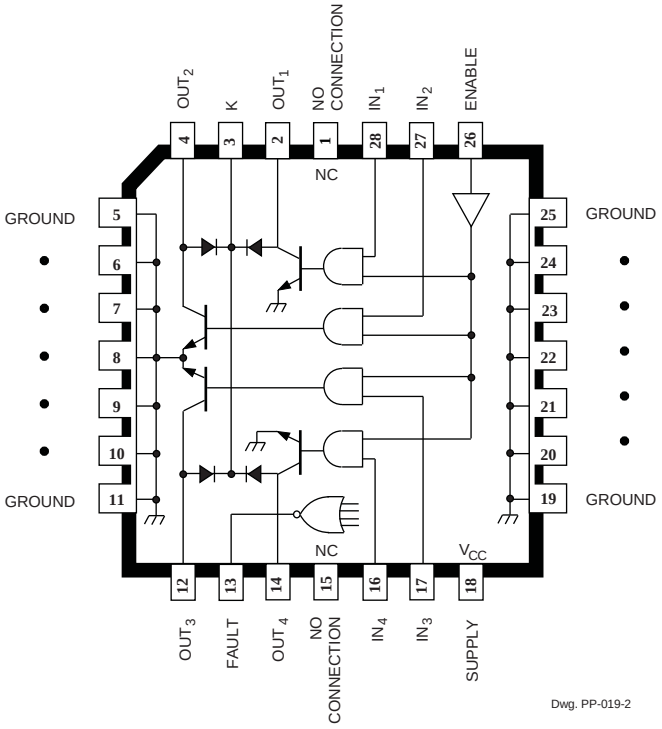
Characteristic	Symbol	Notes	Rating	Units
Logic Supply Voltage	V_{CC}		7.0	V
Input Voltage	V_I or V_{OE}		7.0	V
Output Voltage	V_O		60	V
Overcurrent Protected Output Voltage	$V_{O(OCP)}$		32	V
Output Current	I_O	Outputs current-limited to approximately 500 mA per driver, and T_J limited if higher current is attempted	500	mA
FAULT Output Voltage	V_{FLT}		60	V
Package Power Dissipation	P_D	See graph	–	–
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
		Range K	–40 to 125	ºC
		Range S	–20 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC



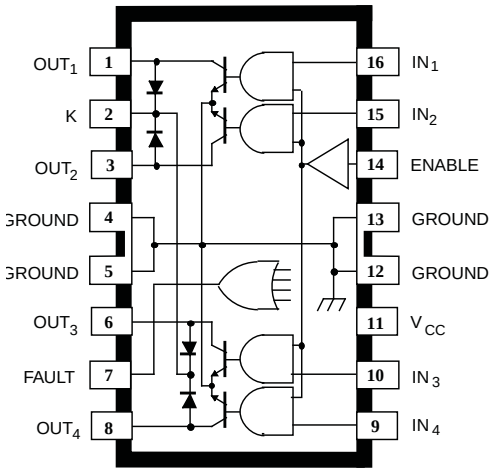
Dwg. GP-004-2B

Pin-out Diagrams

EB (PLCC) Package



B (DIP) and LB (SOIC) Packages



Note that the A2557xB (DIP) and the A2557xLB (SOIC) are electrically identical and share a common terminal number assignment.

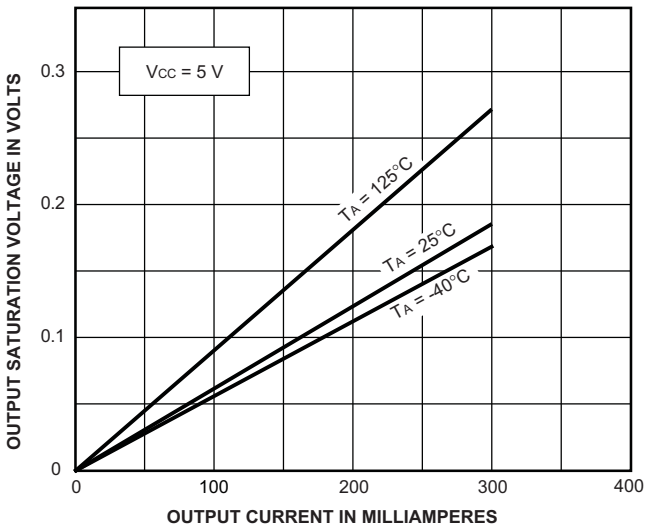
Copyright © 1998, 2002 Allegro MicroSystems, Inc.

ELECTRICAL CHARACTERISTICS over operating temperature range, V_{CC} = 4.75 V to 5.25 V

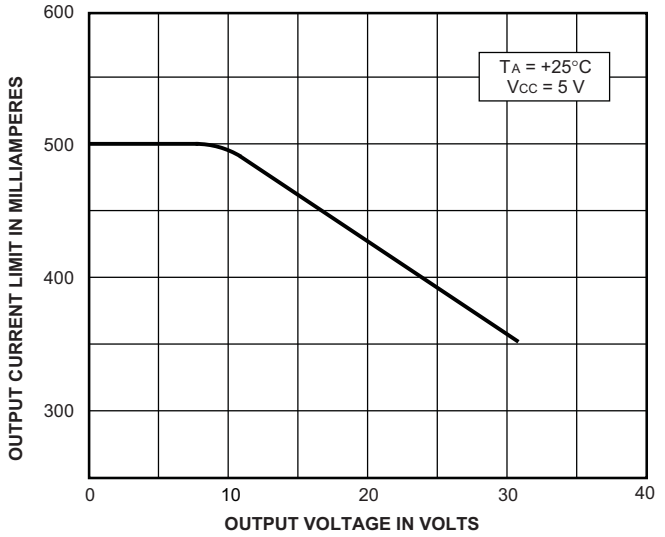
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Output Leakage Current*	I_{CEX}	V_O = 60 V, V_I = 0.8 V, V_{OE} = 2.0 V	—	30	100	μA
		V_O = 60 V, V_I = 2.0 V, V_{OE} = 0.8 V	—	<1.0	100	μA
Output Sustaining Voltage	$V_{O(SUS)}$	I_O = 100 mA, V_I = V_{OE} = 0.8 V, V_{CC} = Open	40	—	—	V
Output Saturation Voltage	$V_{O(SAT)}$	I_O = 100 mA	—	65	200	mV
		I_O = 300 mA	—	180	300	mV
Over-Current Limit	I_{OM}	5 ms PulseTest, V_O = 5.0 V	—	500	—	mA
Input Voltage	V_{IH}	IN_n or ENABLE	2.0	—	—	V
	V_{IL}	IN_n or ENABLE	—	—	0.8	V
Input Current	I_{IH}	IN_n or ENABLE, V_{IH} = 2.0 V	—	—	10	μA
	I_{IL}	IN_n or ENABLE, V_{IL} = 0.8 V	—	—	-10	μA
Fault Output Leakage Current	I_{FLT}	V_{FLT} = 60 V	—	4.0	15	μA
		V_{FLT} = 5 V	—	<1.0	2.0	μA
Fault Output Current	I_{FLT}	V_{FLT} = 5 V, Driver Output Open, V_I = 0.8 V, V_{OE} = 2.0 V	40	60	80	μA
Fault Output Saturation Voltage	$V_{FLT(SAT)}$	I_{FLT} = 30 μA	—	0.1	0.4	V
Clamp Diode Forward Voltage	V_F	I_F = 500 mA	—	1.2	1.7	V
		I_F = 750 mA	—	1.5	2.1	V
Clamp Diode Leakage Current	I_R	V_R = 60 V	—	—	50	μA
Turn-On Delay	t_{PHL}	I_O = 300 mA, 50% V_I to 50% V_O	—	0.6	10	μs
		From Sleep, I_O = 300 mA, 50% V_I to 50% V_O	—	3.0	—	μs
		I_O = 300 mA, 50% V_{OE} to 50% V_O	—	1.3	10	μs
Turn-Off Delay	t_{PLH}	I_O = 300 mA, 50% V_I to 50% V_O	—	2.0	10	μs
		I_O = 300 mA, 50% V_{OE} to 50% V_O	—	1.4	10	μs
Total Supply Current	I_{CC}	All Outputs Off	—	0.075	0.1	mA
		Any One Output On	—	12	20	mA
		Two Outputs On	—	18	30	mA
		Three Outputs On	—	24	40	mA
		All Outputs On	—	30	50	mA
Thermal Limit	T_J		—	165	—	°C

Typical Data is at T_A = +25°C and V_{CC} = 5 V and is for design information only.
Negative current is defined as coming out of (sourcing) the specified terminal.
As used here, -100 is defined as greater than +10 (absolute magnitude convention) and the minimum is implicitly zero.
* Measurement includes output fault-sensing pull-down current.

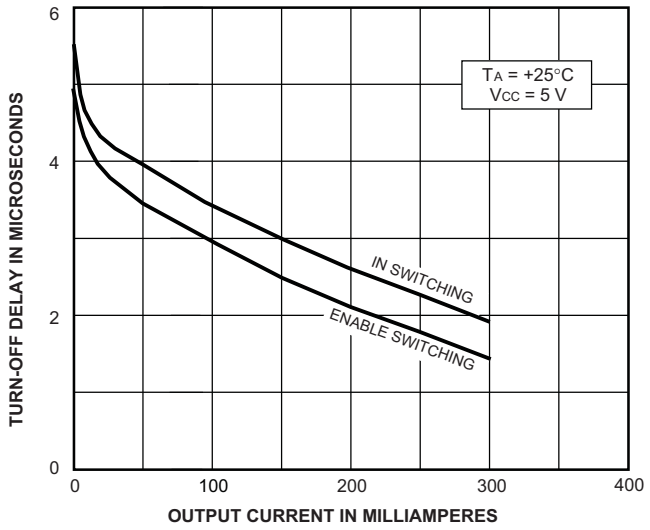
TYPICAL OPERATING CHARACTERISTICS



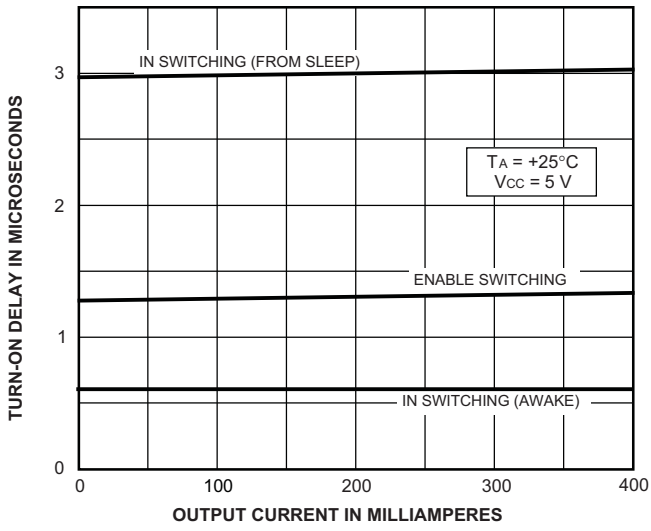
Dwg. GP-064



Dwg. GP-065



Dwg. GP-066



Dwg. GP-066-1

CIRCUIT DESCRIPTION AND APPLICATION

The A2557 low-current quad power drivers provide protected output driver functions, combined with a fault diagnostic scheme, plus an automatic low-current Sleep-Mode function. These devices monitor their outputs for fault (open or shorted) conditions. For each channel the input and output levels are compared. If these are different from the expected levels then a fault condition is flagged by pulling the common FAULT output low.

Status	IN_N	ENABLE	OUT_N	FAULT
Normal Load	H	H	L	H
	L	H	H	H
Sleep Mode	X	L	H	H
	All L	X	H	H
Over-Current or Short to Supply	H	H	R	L
Open Load or Short to Ground	L	H	L	L
Thermal Fault	H	H	H	L
R = Linear drive, current limited.				

The FAULT output is operational only if ENABLE is high. The output state is detected by monitoring the OUT_n terminal using a comparator whose threshold is typically 2.5 V. In order to detect open-circuit outputs, a 30 µA current sink pulls the output below the comparator threshold. To ensure correct fault operation, a minimum load of approximately 1 mA is required. The fault function is disabled when in 'sleep' mode, i.e., FAULT goes high and the 30 µA output sinks are turned off. The FAULT output is a switched current sink of typically 60 µA.

Each channel consists of a TTL/CMOS-compatible logic input gated with a common ENABLE input. A logic high at the input will provide drive to turn on the output npn switch. Each output has a current-limit circuit that limits the output current by detecting the voltage drop across a low-value internal resistor in the emitter of the output switch. If this drop reaches a threshold, then the base drive to the output switch is reduced to maintain constant current in the output.

To keep the device within its safe operating area (SOA) this output current limit is further reduced:

- if the power dissipation in the output device increases the local junction temperature above 165°C (nominal), so as to limit the power dissipation (and hence the local junction temperature). As each channel has its own thermal limit circuitry this provides some independence between the output channels, i.e., one channel can be operating in thermally reduced current limit, while the others can provide full drive capability.
- as a function of the output voltage. Full current limit of 500 mA (nominal) is available up to approximately V_O = 8 V; above this the limit is reduced linearly to about 350 mA at V_O = 32 V. This helps to improve SOA by immediately reducing the peak power pulse into a shorted load at high V_O.

A logic low at the ENABLE input causes all outputs to be switched off regardless of the state of the IN terminals. In addition, the device is put into a low quiescent current 'sleep' mode, reducing I_{CC} below 100 µA. If ENABLE is taken high and any of the inputs go high, the circuit will 'auto-wake-up'. However, if the device is enabled, but all inputs stay low, then the circuit remains in 'sleep' mode.

All outputs have internal flyback diodes, with a common-cathode connection at the K terminal.

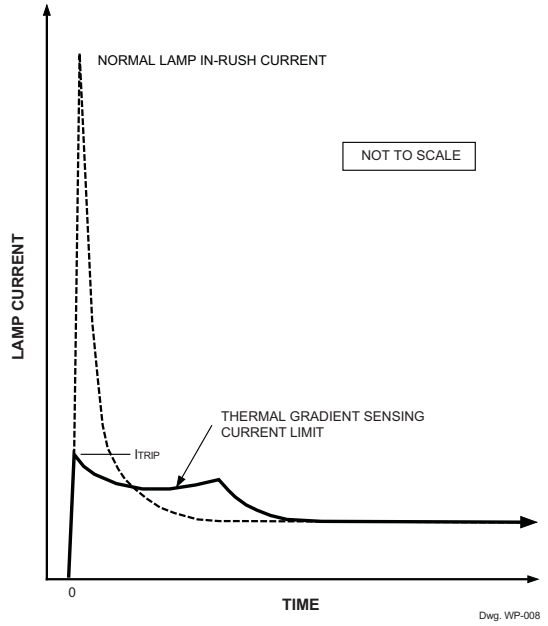
Incandescent lamp driver

High incandescent lamp turn-on (in-rush currents) can contribute to poor lamp reliability and destroy semiconductor lamp drivers. When an incandescent lamp is initially turned on, the cold filament is at minimum resistance and would normally allow a 10x to 12x in-rush current.

Warming (parallel) or current-limiting (series) resistors protect both driver and lamp but use significant power either when the lamp is off or when the lamp is on, respectively. Lamps with steady-state current ratings up to 300 mA can be driven without the need for warming or current-limiting resistors, if lamp turn-on time is not a concern (10s of ms).

With these drivers, during turn-on, the high in-rush current is sensed by the internal sense resistor, drive current to the output stage is reduced, and the output operates in a linear mode with the load current limited to approximately 500 mA. During lamp warmup, the filament resistance increases to its maximum value, the output driver goes into saturation and applies maximum rated voltage to the lamp.

CIRCUIT DESCRIPTION AND APPLICATION (continued)



Inductive load driver

Bifilar (unipolar) stepper motors (and other inductive loads) can be driven directly. The internal diodes prevent damage to the output transistors by suppressing the high-voltage spikes that occur when turning off an inductive load. For rapid current decay (fast turn-off speeds), the use of Zener diodes will raise the flyback voltage and improve performance. However, the peak voltage must not exceed the specified minimum sustaining voltage ($V_{SUPPLY} + V_Z + V_F < V_{O(SUS)}$).

Over-current conditions

In the event of a shorted load, or stalled motor, the load current will attempt to increase. As described above, the drive current to the affected output stage is linearly reduced, causing the output to go linear (limiting the load current to about 500 mA). As the junction temperature of the output stage increases, the thermal-shutdown circuit will shut off the affected output. If the fault condition is corrected, the output driver will return to its normal saturated condition.

Fault diagnostics

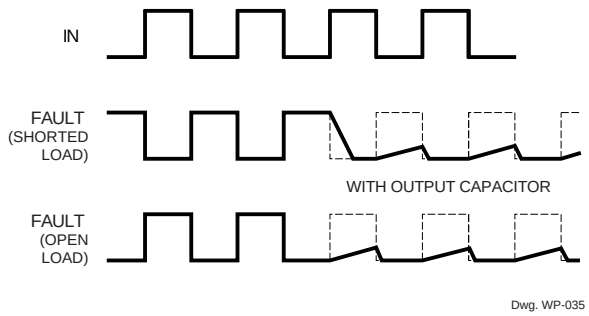
A pull-up resistor or current source is required on the FAULT output. This can be connected to whatever supply level the following circuitry requires (within the specification constraints). For a 5 V supply (i.e., Vcc) 150 kΩ or greater should be used. As the fault diagnostic function is to indicate when the output state is different from the input state for any channel, the FAULT output waveform will obviously produce a pulse waveform following the combined duty-cycle of all channels showing a fault condition. There are therefore two basic approaches to using the function in an application:

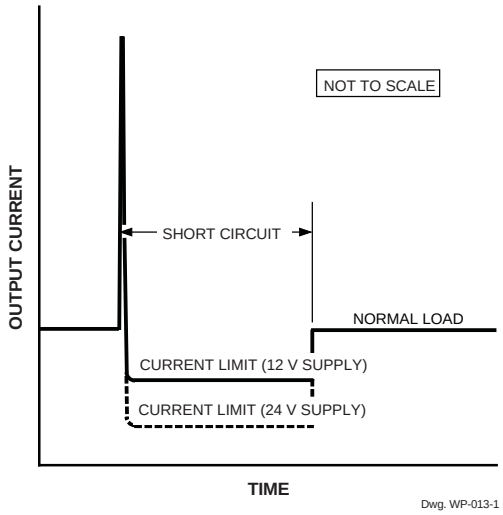
- As an interrupt in a controller-based system. If the system has a microcontroller then a FAULT low causes an interrupt, which then initiates a diagnostic sequence to find the culprit channel. This sequence usually consists of cycling through each channel one at a time, while monitoring the FAULT output. It is then easy to determine which channel has the faulty output and how it is failing (i.e., short to supply, open-circuit or short to ground). The system may then take whatever action is required, but could continue with operation of the remaining 'good' channels while disabling signals to the faulty channel.

- As a simple 'common' fault indication. If there is no controller in the system then the FAULT output can be set to give an indication (via a lamp or LED, etc.) of a fault condition which might be anywhere on the four channels. Because the FAULT output is dependent on the states of the input and output (four possibilities) but will only indicate on two of them, the duty cycle at the FAULT output will reflect the duty cycle at the faulty channel's input (or its inverse, depending upon fault type).

In typical applications (50% duty cycles) a simple solution is to make the pull-up current on the FAULT output much less than the pull-down current (60 µA), and add a capacitor to give a time constant longer than the period of operation. For typical values, the device will produce a continuous dc output level. Component values will need to be adjusted to cope with different conditions.

CIRCUIT DESCRIPTION AND APPLICATION (continued)





Under some conditions it is possible to get spurious glitches on the FAULT output at load turn-on and turn-off transitions:

- Light load turn-off. Under light loading conditions the turn-off delay (see characteristics above) of the output stage increases and may result in a spurious fault output of a few µs (the duration being proportional to the turn-off delay). As it is difficult to define this over all operating conditions, if a particular application would be sensitive to this type of glitch, then it is generally recommended to include a small (about 0.01 µF) smoothing/storage capacitor at the FAULT output.

- Incandescent lamp turn-on. As described above, driving an incandescent filament results in the driver operating in current limit for a period after turn-on. During this period a "fault" condition will be indicated (over current). As discussed above this period can be 10s of ms. To avoid this indication, the capacitor on the FAULT output would need to be increased to provide an appropriate time constant. Alternatively, in a microcontroller-based system, the code could be written to ignore the FAULT condition for an appropriate period after lamp turn on.

Correct FAULT operation cannot be guaranteed with an unconnected output — unused outputs should not be turned on, *or* unused outputs should be pulled high to >2.5 V, *and/or* associated inputs tied low.

Thermal considerations

Device power dissipation can be calculated as:

$P_D = (V_{O1} \times I_{O1} \times \text{duty cycle}_1) + \ldots + (V_{O4} \times I_{O4} \times \text{duty cycle}_4) + (V_{CC} \times I_{CC})$

Note - I_{CC} is also modulated by the duty cycle, but this is a reasonable approximation for most purposes.

This can then be compared against the permitted package power dissipation, using:

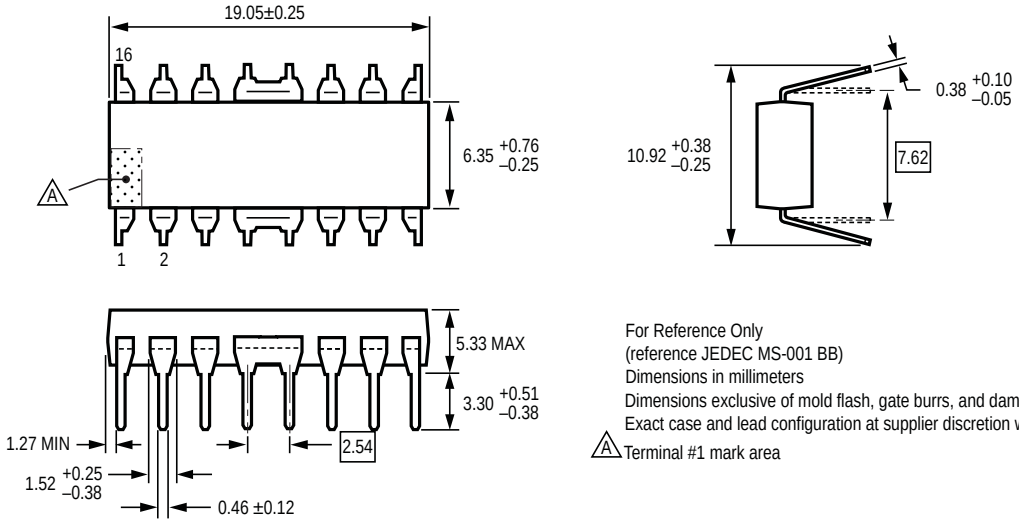
$$\text{Permitted } P_D = (150 - T_A)/R_{\theta JA}$$

where $R_{\theta JA}$ is given as:

28-lead PLCC (part number suffix '–EB') =	36°C/W
16-pin PDIP (part number suffix '–B') =	43°C/W
16-lead SOIC (part number suffix '–LB') =	90°C/W

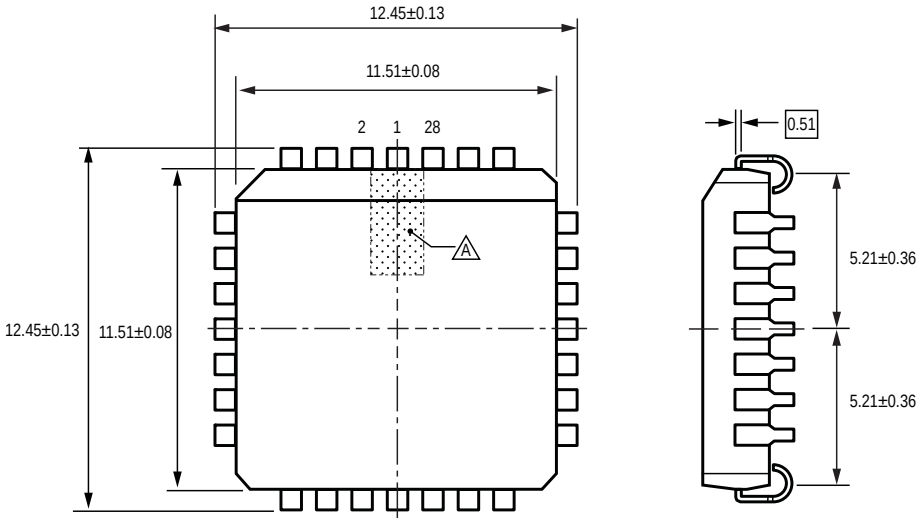
$R_{\theta JA}$ is measured on typical two-sided PCB with minimal copper ground area. Additional information is available on the Allegro website.

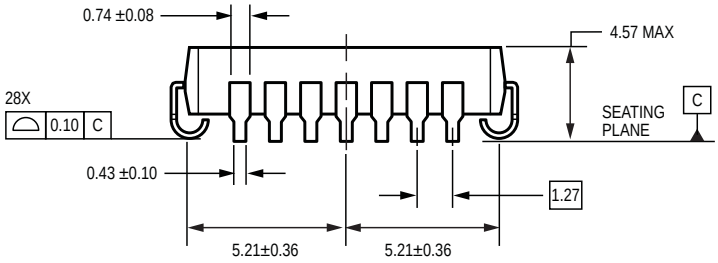
B Package, 16-pin DIP
with internally fused pins 4, 5, 12, and 13 and external thermal tabs



For Reference Only
(reference JEDEC MS-001 BB)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

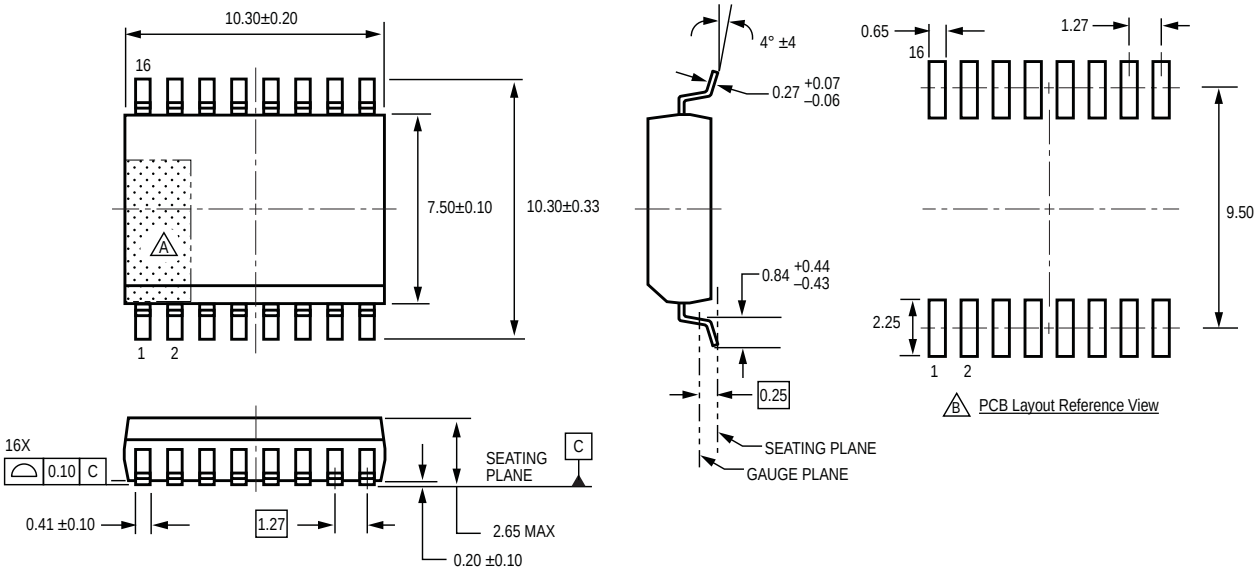
EB Package, 28-pin PLCC
with internally fused pins 5 through 11 and 19 through 25





For Reference Only
(reference JEDEC MS-018 AB)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

LB Package, 16-pin SOIC
with internally fused pins 4 and 5, and 12 and 13



For Reference Only
Pins 4 and 5, and 12 and 13 internally fused
Dimensions in millimeters
(reference JEDEC MS-013 AA)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference pad layout (reference IPC SOIC127P1030X265-16M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

Copyright ©1998-2009, Allegro MicroSystems, Inc.

The products described here are manufactured under one or more U.S. patents or U.S. patents pending.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in life support devices or systems, if a failure of an Allegro product can reasonably be expected to cause the failure of that life support device or system, or to affect the safety or effectiveness of that device or system.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

For the latest version of this document, visit our website:
www.allegromicro.com

ООО «ЛайфЭлектроникс» “LifeElectronics” LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru