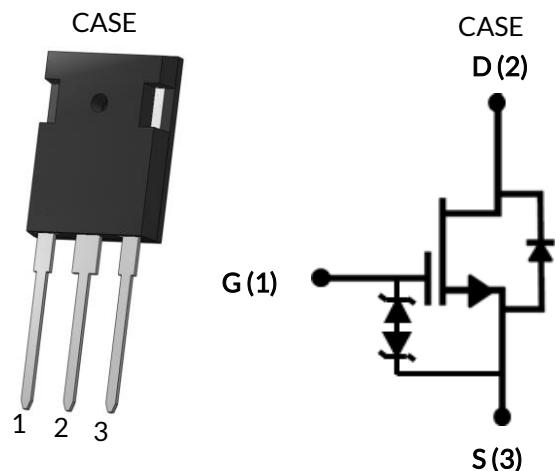


## DATASHEET

# UJ3C065030K3S



Part Number	Package	Marking
UJ3C065030K3S	TO-247-3L	UJ3C065030K3S



## 650V-27mΩ SiC FET

Rev. D, December 2019

### Description

This SiC FET device is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-247-3L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

### Features

- ◆ Typical on-resistance  $R_{DS(on),typ}$  of 27mΩ
- ◆ Maximum operating temperature of 175°C
- ◆ Excellent reverse recovery
- ◆ Low gate charge
- ◆ Low intrinsic capacitance
- ◆ ESD protected, HBM class 2

### Typical applications

- ◆ EV charging
- ◆ PV inverters
- ◆ Switch mode power supplies
- ◆ Power factor correction modules
- ◆ Motor drives
- ◆ Induction heating

## Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	$V_{DS}$		650	V
Gate-source voltage	$V_{GS}$	DC	-25 to +25	V
Continuous drain current <sup>1</sup>	$I_D$	$T_C = 25^\circ C$	85	A
		$T_C = 100^\circ C$	62	A
Pulsed drain current <sup>2</sup>	$I_{DM}$	$T_C = 25^\circ C$	230	A
Single pulsed avalanche energy <sup>3</sup>	$E_{AS}$	$L=15mH, I_{AS} = 4A$	120	mJ
Power dissipation	$P_{tot}$	$T_C = 25^\circ C$	441	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ C$
Operating and storage temperature	$T_J, T_{STG}$		-55 to 175	$^\circ C$
Max. lead temperature for soldering, 1/8" from case for 5 seconds	$T_L$		250	$^\circ C$

1. Limited by  $T_{J,max}$

2. Pulse width  $t_p$  limited by  $T_{J,max}$

3. Starting  $T_J = 25^\circ C$

## Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.26	0.34	$^\circ C/W$

## Electrical Characteristics ( $T_J = +25^\circ\text{C}$ unless otherwise specified)

### Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	$\text{BV}_{\text{DS}}$	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_D=1\text{mA}$	650			V
Total drain leakage current	$\text{I}_{\text{DSS}}$	$\text{V}_{\text{DS}}=650\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{T}_J=25^\circ\text{C}$		6	150	$\mu\text{A}$
		$\text{V}_{\text{DS}}=650\text{V}, \text{V}_{\text{GS}}=0\text{V}, \text{T}_J=175^\circ\text{C}$		30		
Total gate leakage current	$\text{I}_{\text{GSS}}$	$\text{V}_{\text{DS}}=0\text{V}, \text{T}_J=25^\circ\text{C}, \text{V}_{\text{GS}}=-20\text{V} / +20\text{V}$		6	$\pm 20$	$\mu\text{A}$
Drain-source on-resistance	$\text{R}_{\text{DS(on)}}$	$\text{V}_{\text{GS}}=12\text{V}, \text{I}_D=50\text{A}, \text{T}_J=25^\circ\text{C}$		27	35	$\text{m}\Omega$
		$\text{V}_{\text{GS}}=12\text{V}, \text{I}_D=50\text{A}, \text{T}_J=125^\circ\text{C}$		35		
		$\text{V}_{\text{GS}}=12\text{V}, \text{I}_D=50\text{A}, \text{T}_J=175^\circ\text{C}$		43		
Gate threshold voltage	$\text{V}_{\text{G(th)}}$	$\text{V}_{\text{DS}}=5\text{V}, \text{I}_D=10\text{mA}$	4	5	6	V
Gate resistance	$\text{R}_G$	f=1MHz, open drain		4.5		$\Omega$

### Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Diode continuous forward current <sup>1</sup>	$\text{I}_S$	$\text{T}_C=25^\circ\text{C}$			85	A
Diode pulse current <sup>2</sup>	$\text{I}_{\text{S,pulse}}$	$\text{T}_C=25^\circ\text{C}$			230	A
Forward voltage	$\text{V}_{\text{FSD}}$	$\text{V}_{\text{GS}}=0\text{V}, \text{I}_F=20\text{A}, \text{T}_J=25^\circ\text{C}$		1.3	1.4	V
		$\text{V}_{\text{GS}}=0\text{V}, \text{I}_F=20\text{A}, \text{T}_J=175^\circ\text{C}$		1.35		
Reverse recovery charge	$\text{Q}_{\text{rr}}$	$\text{V}_R=400\text{V}, \text{I}_F=50\text{A}, \text{V}_{\text{GS}}=0\text{V}, \text{R}_{\text{G,EXT}}=20\Omega, \text{di/dt}=1550\text{A}/\mu\text{s}, \text{T}_J=150^\circ\text{C}$		400		nC
Reverse recovery time	$\text{t}_{\text{rr}}$			33		ns

## Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	$C_{iss}$	$V_{DS}=100V, V_{GS}=0V$ $f=100kHz$		1500		pF
Output capacitance	$C_{oss}$			320		
Reverse transfer capacitance	$C_{rss}$			2.3		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		230		pF
Effective output capacitance, time related	$C_{oss(tr)}$	$V_{DS}=0V$ to 400V, $V_{GS}=0V$		520		pF
$C_{oss}$ stored energy	$E_{oss}$	$V_{DS}=400V, V_{GS}=0V$		18.5		$\mu J$
Total gate charge	$Q_G$	$V_{DS}=400V, I_D=50A,$ $V_{GS} = -5V$ to 15V		51		nC
Gate-drain charge	$Q_{GD}$			11		
Gate-source charge	$Q_{GS}$			19		
Turn-on delay time	$t_{d(on)}$	$V_{DS}=400V, I_D=50A$ , Gate Driver =-5V to +15V, Turn-on $R_{G,EXT}=1\Omega$ , Turn-off $R_{G,EXT}=20\Omega$ Inductive Load, FWD: UJ3D065030TS, $T_J=150^\circ C$		44		ns
Rise time	$t_r$			26		
Turn-off delay time	$t_{d(off)}$			63		
Fall time	$t_f$			17		
Turn-on energy	$E_{ON}$			657		
Turn-off energy	$E_{OFF}$			330		
Total switching energy	$E_{TOTAL}$			987		$\mu J$

## Typical Performance Diagrams

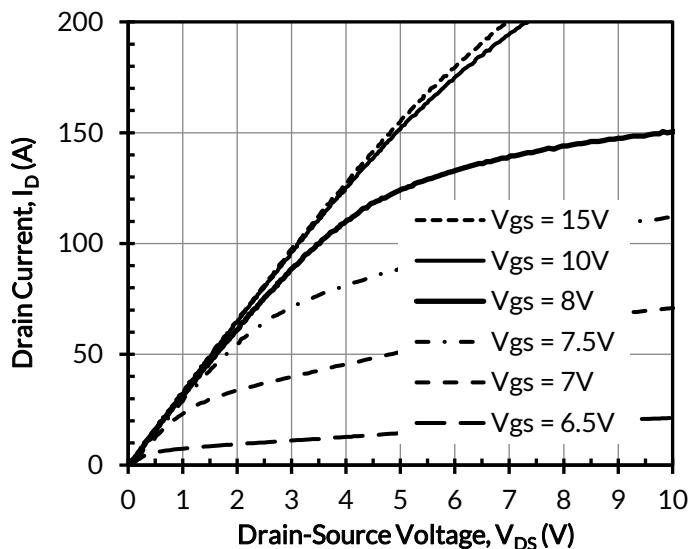


Figure 1. Typical output characteristics at  $T_J = -55^\circ\text{C}$ ,  
 $t_p < 250\mu\text{s}$

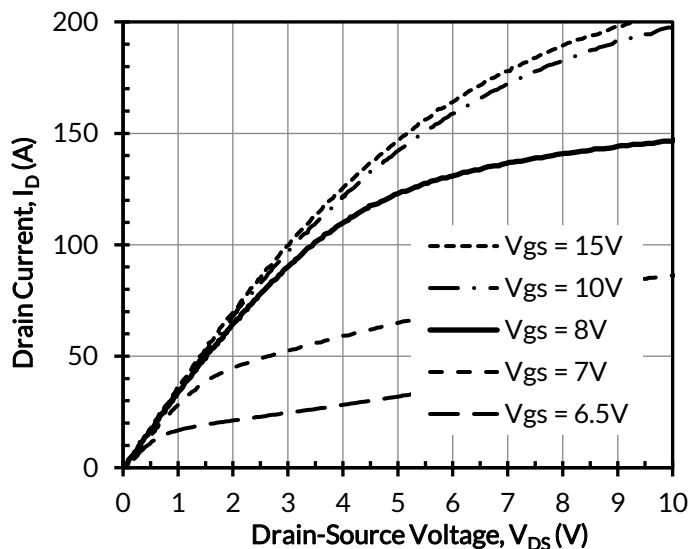


Figure 2. Typical output characteristics at  $T_J = 25^\circ\text{C}$ ,  
 $t_p < 250\mu\text{s}$

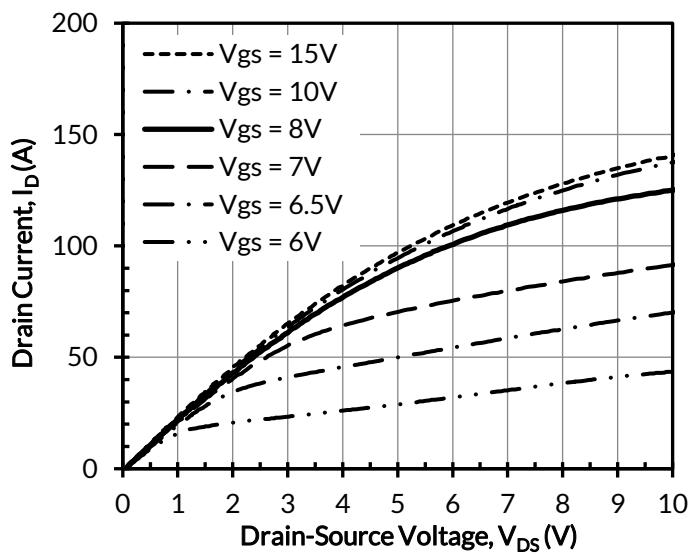


Figure 3. Typical output characteristics at  $T_J = 175^\circ\text{C}$ ,  
 $t_p < 250\mu\text{s}$

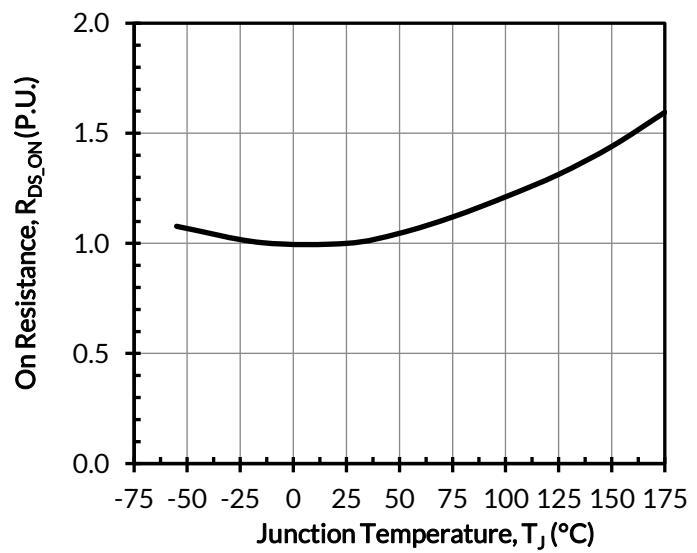


Figure 4. Normalized on-resistance vs. temperature  
at  $V_{GS} = 12\text{V}$  and  $I_D = 50\text{A}$

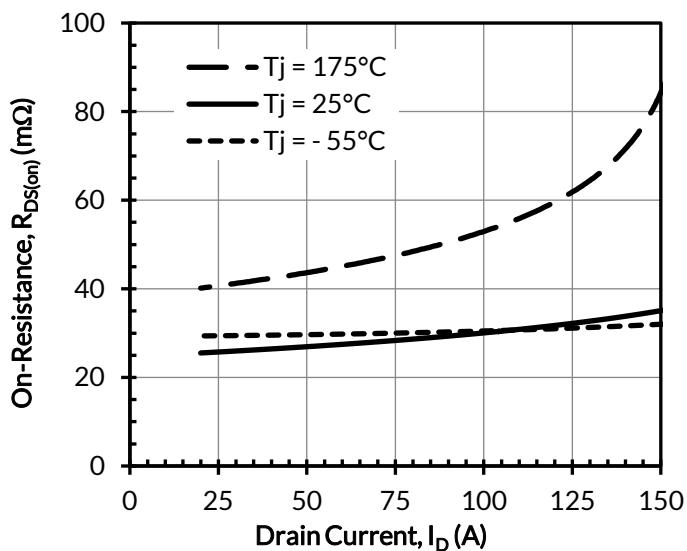


Figure 5. Typical drain-source on-resistances at  $V_{GS} = 12V$

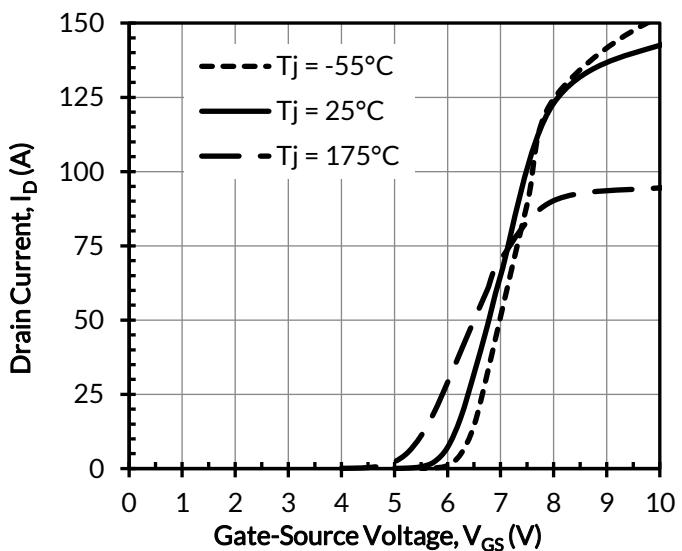


Figure 6. Typical transfer characteristics at  $V_{DS} = 5V$

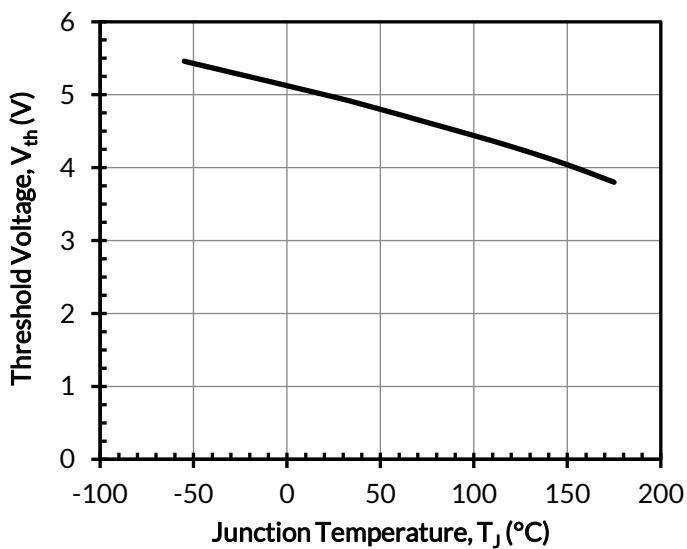


Figure 7. Threshold voltage vs. junction temperature at  $V_{DS} = 5V$  and  $I_D = 10mA$

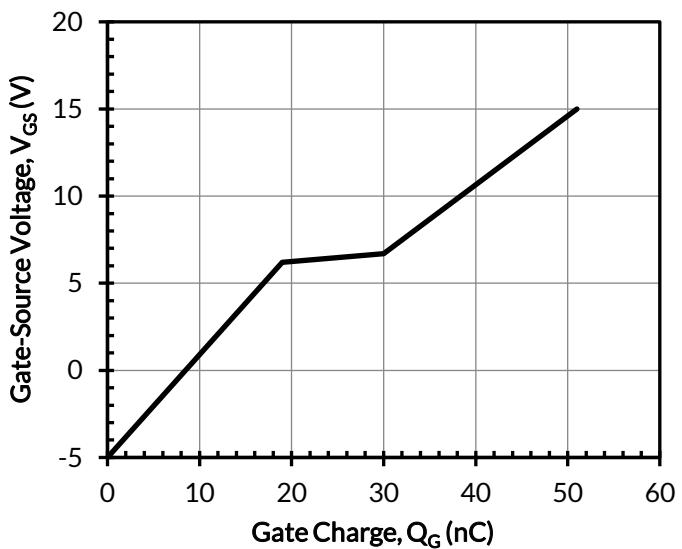


Figure 8. Typical gate charge at  $V_{DS} = 400V$  and  $I_D = 50A$

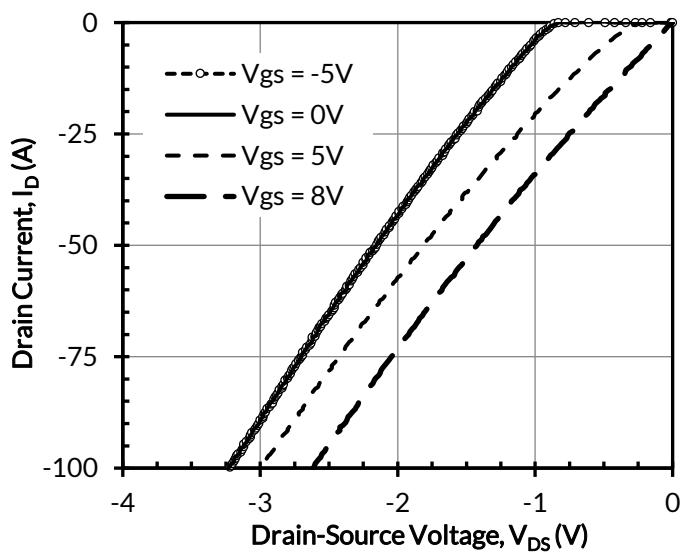


Figure 9. 3rd quadrant characteristics at  $T_J = -55^\circ\text{C}$

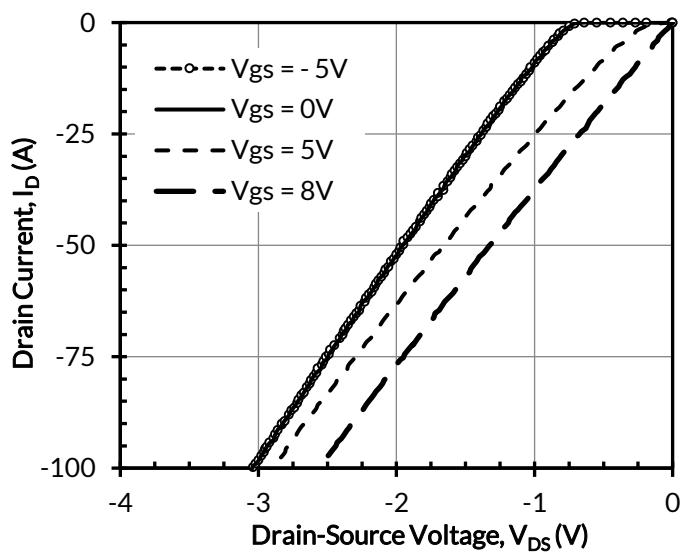


Figure 10. 3rd quadrant characteristics at  $T_J = 25^\circ\text{C}$

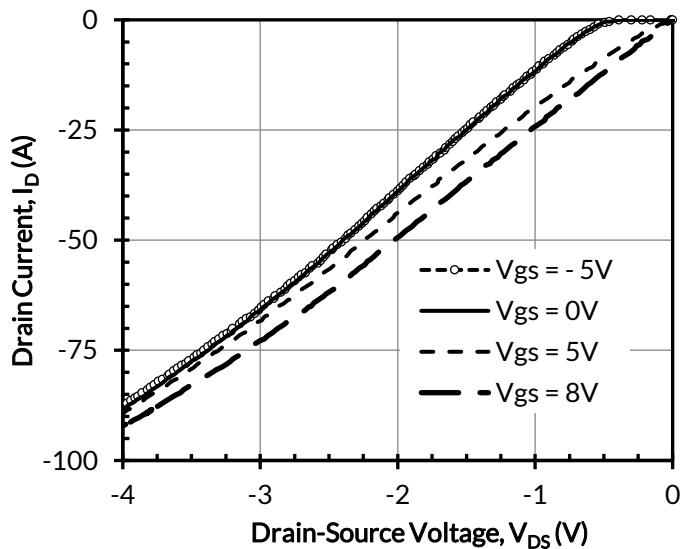


Figure 11. 3rd quadrant characteristics at  $T_J = 175^\circ\text{C}$

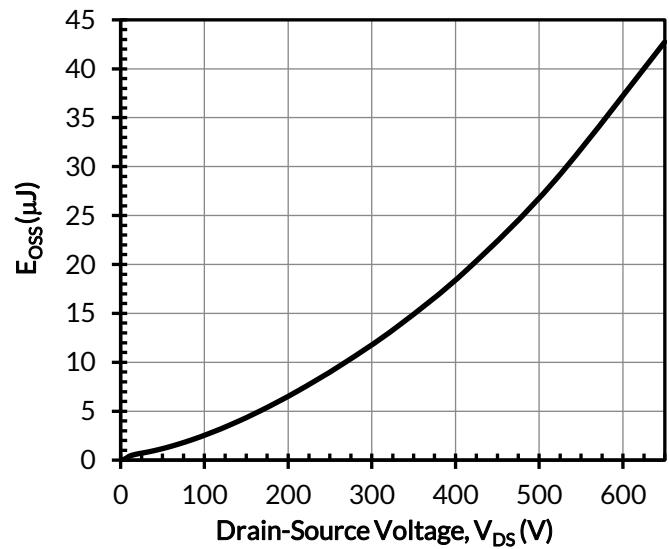


Figure 12. Typical stored energy in  $C_{OSS}$  at  $V_{GS} = 0\text{V}$

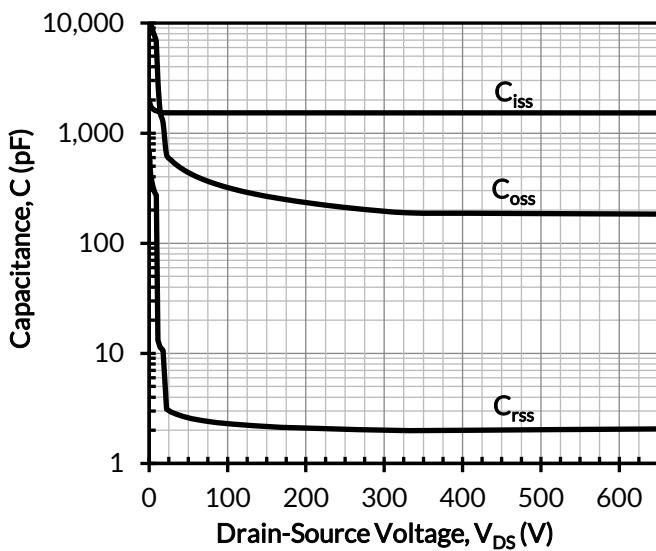


Figure 13. Typical capacitances at  $f = 100\text{kHz}$  and  $V_{GS} = 0\text{V}$

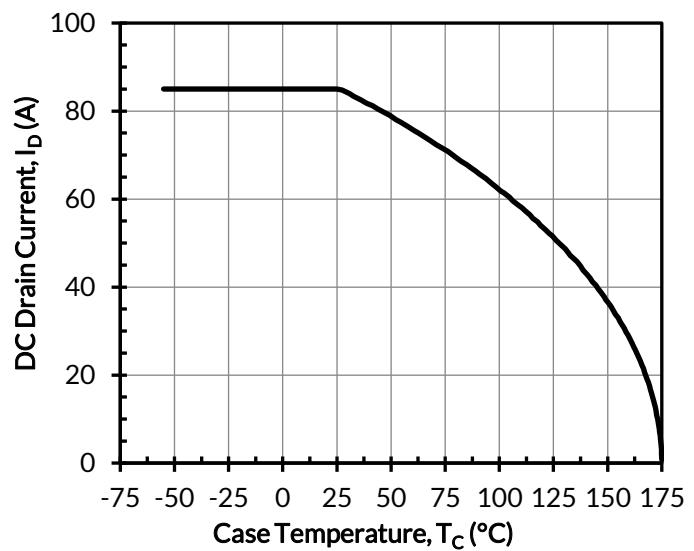


Figure 14. DC drain current derating

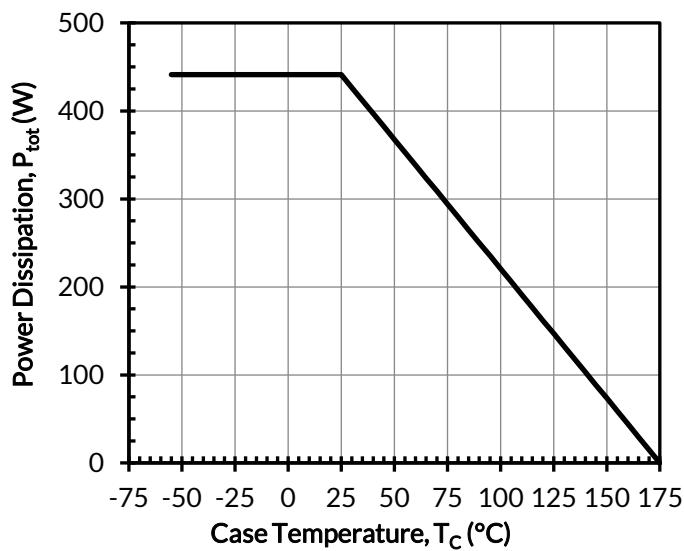


Figure 15. Total power dissipation

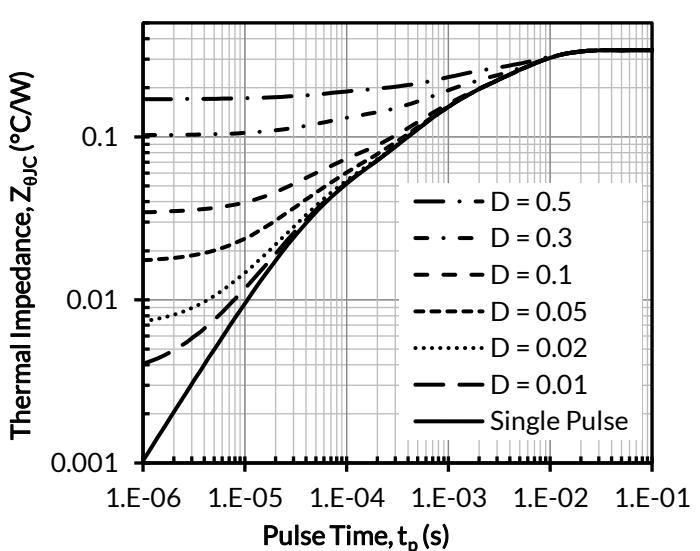


Figure 16. Maximum transient thermal impedance

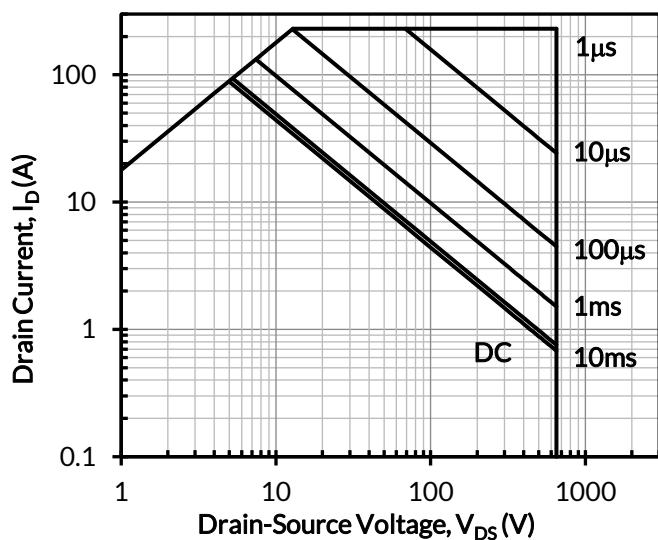


Figure 17. Safe operation area at  $T_C = 25^\circ\text{C}$ ,  $D = 0$ , Parameter  $t_p$

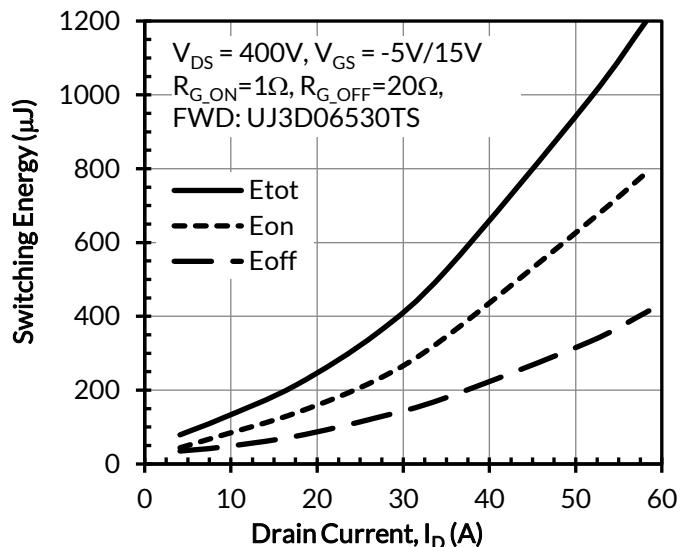


Figure 18. Clamped inductive switching energy vs. drain current at  $T_J = 150^\circ\text{C}$

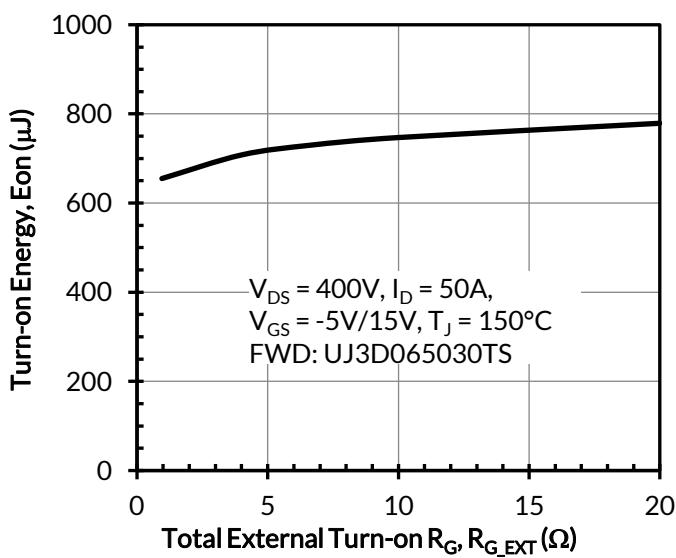


Figure 19. Clamped inductive switching turn-on energy vs.  $R_{G,EXT\_ON}$

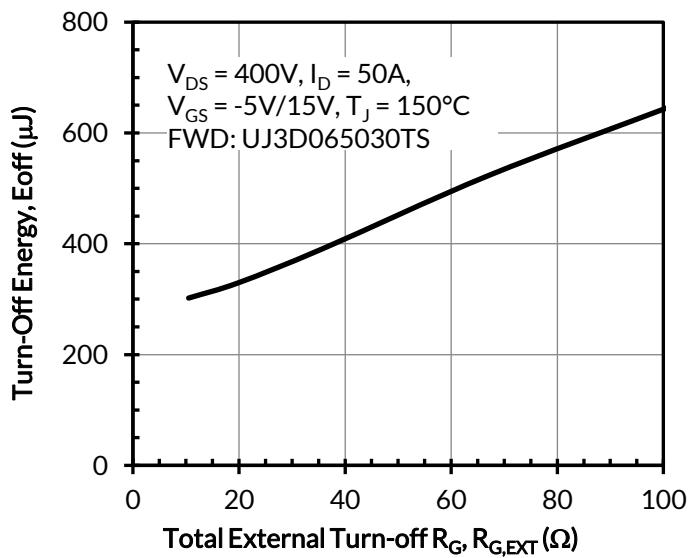


Figure 20. Clamped inductive switching turn-off energy vs.  $R_{G,EXT\_OFF}$

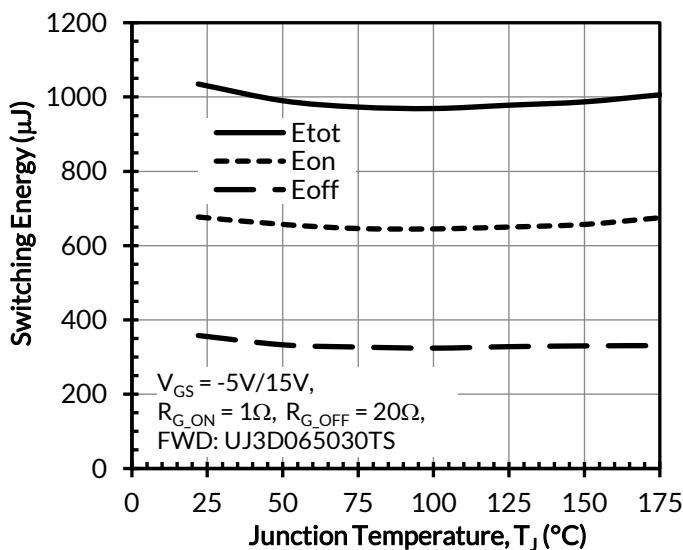


Figure 21. Clamped inductive switching energy vs. junction temperature at  $V_{DS} = 400\text{V}$  and  $I_D = 50\text{A}$

## Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ( $R_{DS(on)}$ ), output capacitance ( $C_{oss}$ ), gate charge ( $Q_G$ ), and reverse recovery charge ( $Q_{rr}$ ) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high  $dv/dt$  and  $di/dt$  rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see [www.unitedsic.com](http://www.unitedsic.com).

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ООО "ЛайфЭлектроникс"

"LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

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С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибуторских договоров

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- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)  
Email: org@lifeelectronics.ru