

Asymmetric Dual N-Channel 30V (D-S) Power MOSFET

FEATURES

- Low $R_{DS(on)}$ to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

APPLICATIONS

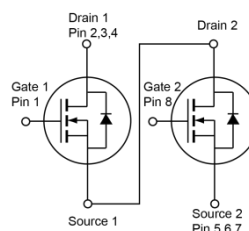
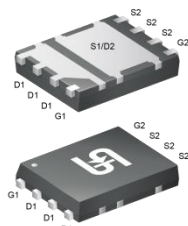
- IPC
- VGA
- NB VCORE

KEY PERFORMANCE PARAMETERS

PARAMETER	TYPE	VALUE	UNIT
V_{DS}	Q1	30	V
	Q2	30	
$R_{DS(on)}$ (max)	Q1	$V_{GS} = 10V$	11.7
		$V_{GS} = 4.5V$	14.9
	Q2	$V_{GS} = 10V$	3.6
		$V_{GS} = 4.5V$	5.5
Q_g	Q1	4.6	nC
	Q2	25	



PDFN56 Asymmetric Dual



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)

PARAMETER	SYMBOL	Q1	Q2	UNIT
Drain-Source Voltage	V_{DS}	30	30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ C$	38	A
		$T_A = 25^\circ C$	10	
Pulsed Drain Current	I_{DM}	152	428	A
Single Pulse Avalanche Current (Note 2)	I_{AS}	16	26	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	38	101	mJ
Total Power Dissipation	P_D	$T_C = 25^\circ C$	30	W
		$T_C = 125^\circ C$	6	
Total Power Dissipation	P_D	$T_A = 25^\circ C$	2.2	W
		$T_A = 125^\circ C$	0.4	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150		$^\circ C$

THERMAL PERFORMANCE

PARAMETER	SYMBOL	LIMIT		UNIT
		Q1	Q2	
Thermal Resistance – Junction to Case	$R_{\theta JC}$	4.2	1.8	$^\circ C/W$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	56	52	

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)							
PARAMETER	CONDITIONS	SYMBOL	TYPE	MIN	TYP	MAX	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	Q1	30	--	--	V
	$V_{GS} = 0V, I_D = 250\mu A$		Q2	30	--	--	
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu A$	$V_{GS(TH)}$	Q1	1.2	1.9	2.5	V
	$V_{GS} = V_{DS}, I_D = 250\mu A$		Q2	1.2	1.6	2.5	
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	Q1	--	--	± 100	nA
	$V_{GS} = \pm 20V, V_{DS} = 0V$		Q2	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 30V$	I_{DSS}	Q1	--	--	1	μA
	$V_{GS} = 0V, V_{DS} = 30V$ $T_J = 125^\circ\text{C}$			--	--	100	
	$V_{GS} = 0V, V_{DS} = 30V$		Q2	--	--	1	
	$V_{GS} = 0V, V_{DS} = 30V$ $T_J = 125^\circ\text{C}$			--	--	100	
Drain-Source On-State Resistance <small>(Note 3)</small>	$V_{GS} = 10V, I_D = 10A$	$R_{DS(on)}$	Q1	--	8.8	11.7	m Ω
	$V_{GS} = 4.5V, I_D = 9A$			--	12.8	14.9	
	$V_{GS} = 10V, I_D = 20A$		Q2	--	2.7	3.6	
	$V_{GS} = 4.5V, I_D = 16A$			--	3.7	5.5	
Forward Transconductance <small>(Note 3)</small>	$V_{DS} = 5V, I_D = 10A$	g_{fs}	Q1	--	27	--	S
	$V_{DS} = 5V, I_D = 20A$		Q2	--	47	--	
Dynamic <small>(Note 4)</small>							
Total Gate Charge	Q1 $V_{DS} = 15V, I_D = 10A$ Q2 $V_{DS} = 15V, I_D = 20A$	$Q_{g(VGS=10V)}$	Q1	--	9.3	--	nC
			Q2	--	49	--	
Total Gate Charge	Q1 $V_{DS} = 15V, I_D = 9A$ Q2 $V_{DS} = 15V, I_D = 16A$	$Q_{g(VGS=4.5V)}$	Q1	--	4.6	--	nC
			Q2	--	25	--	
Gate-Source Charge	$V_{DS} = 15V, I_D = 9A$	Q_{gs}	Q1	--	2.1	--	nC
			Q2	--	7.3	--	
Gate-Drain Charge	$V_{DS} = 15V, I_D = 16A$	Q_{gd}	Q1	--	1.8	--	nC
			Q2	--	12	--	
Input Capacitance	Q1 $V_{GS} = 0V, V_{DS} = 15V$	C_{iss}	Q1	--	555	--	pF
			Q2	--	2550	--	
Output Capacitance	f = 1.0MHz Q2	C_{oss}	Q1	--	142	--	pF
			Q2	--	388	--	
Reverse Transfer Capacitance	$V_{GS} = 0V, V_{DS} = 15V$ f = 1.0MHz	C_{rss}	Q1	--	26	--	pF
			Q2	--	276	--	
Gate Resistance	f = 1.0MHz	R_g	Q1	0.5	1.6	3.2	Ω
			Q2	0.5	1.5	3	

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)							
PARAMETER	CONDITIONS	SYMBOL	TYPE	MIN	TYP	MAX	UNIT
Switching (Note 4)							
Turn-On Delay Time	Q1 $V_{GS} = 10\text{V}, V_{DS} = 15\text{V},$ $I_D = 10\text{A}, R_G = 2\Omega$ Q2 $V_{GS} = 10\text{V}, V_{DS} = 15\text{V},$ $I_D = 20\text{A}, R_G = 2\Omega$	$t_{d(on)}$	Q1	--	4.8	--	ns
			Q2	--	11	--	
Turn-On Rise Time		t_r	Q1	--	65	--	
			Q2	--	79	--	
Turn-Off Delay Time		$t_{d(off)}$	Q1	--	8.2	--	
			Q2	--	32	--	
Turn-Off Fall Time		t_f	Q1	--	14	--	
			Q2	--	49	--	
Source-Drain Diode							
Forward Voltage (Note 3)	$V_{GS} = 0\text{V}, I_S = 10\text{A}$	V_{SD}	Q1	--	--	1.2	V
	$V_{GS} = 0\text{V}, I_S = 20\text{A}$		Q2	--	--	1	
Reverse Recovery Time	Q1 $I_S = 10\text{A}, di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	Q1	--	33	--	ns
			Q2	--	14	--	
Reverse Recovery Charge	Q2 $I_S = 20\text{A}, di/dt = 100\text{A}/\mu\text{s}$	Q_{rr}	Q1	--	19	--	nC
			Q2	--	8	--	

Notes:

- Silicon limited current only.
- Q1 : $L = 0.3\text{mH}, V_{GS} = 10\text{V}, V_{DD} = 30\text{V}, R_G = 25\Omega, I_{AS} = 16\text{A}$, Starting $T_J = 25^\circ\text{C}$
 Q2 : $L = 0.3\text{mH}, V_{GS} = 10\text{V}, V_{DD} = 30\text{V}, R_G = 25\Omega, I_{AS} = 26\text{A}$, Starting $T_J = 25^\circ\text{C}$
- Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

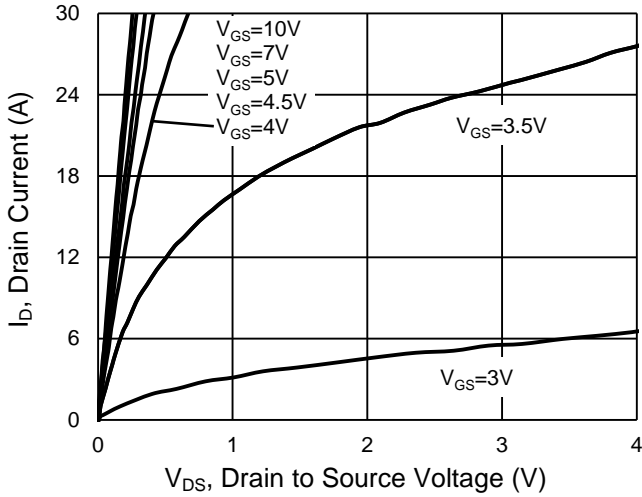
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM5055DCR RLG	PDFN56 Asymmetric Dual	2,500pcs / 13" Reel

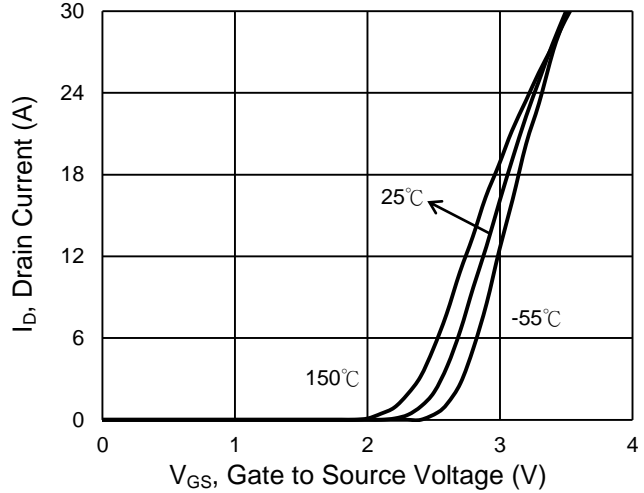
CHARACTERISTICS CURVES (Q1)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

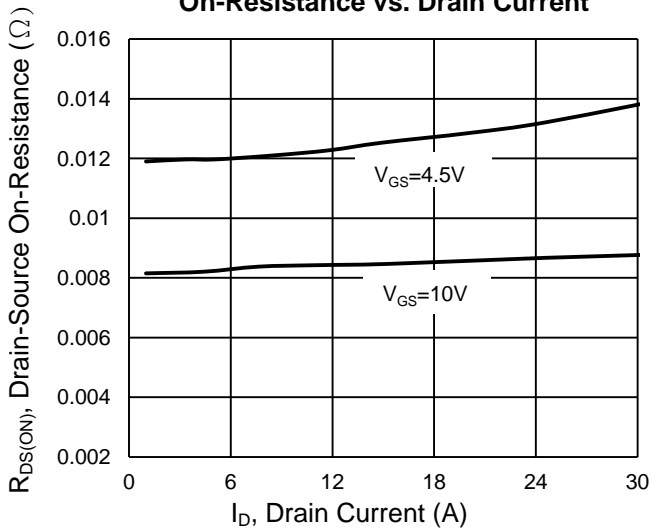
Output Characteristics



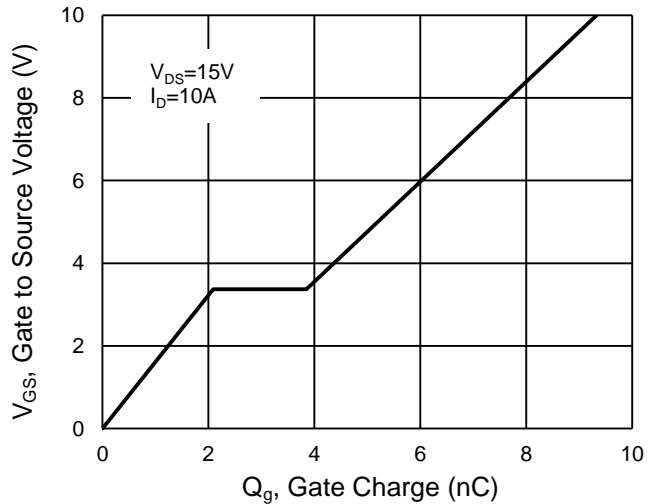
Transfer Characteristics



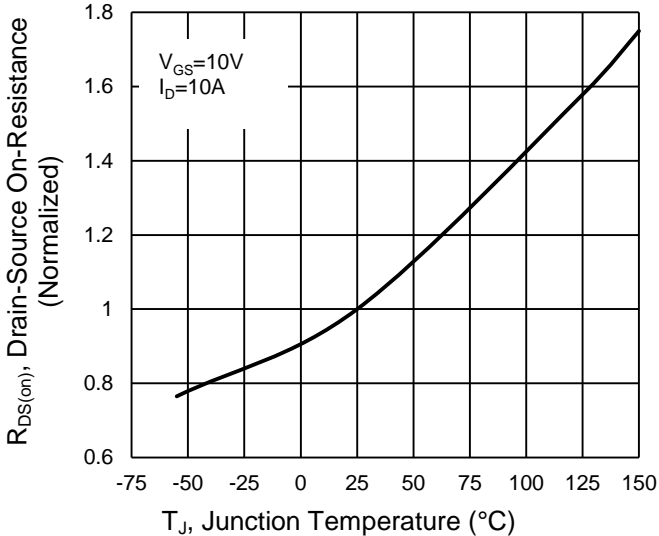
On-Resistance vs. Drain Current



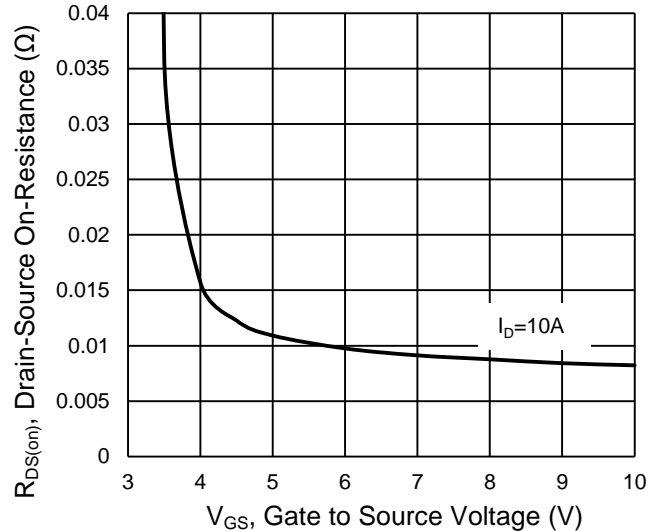
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature

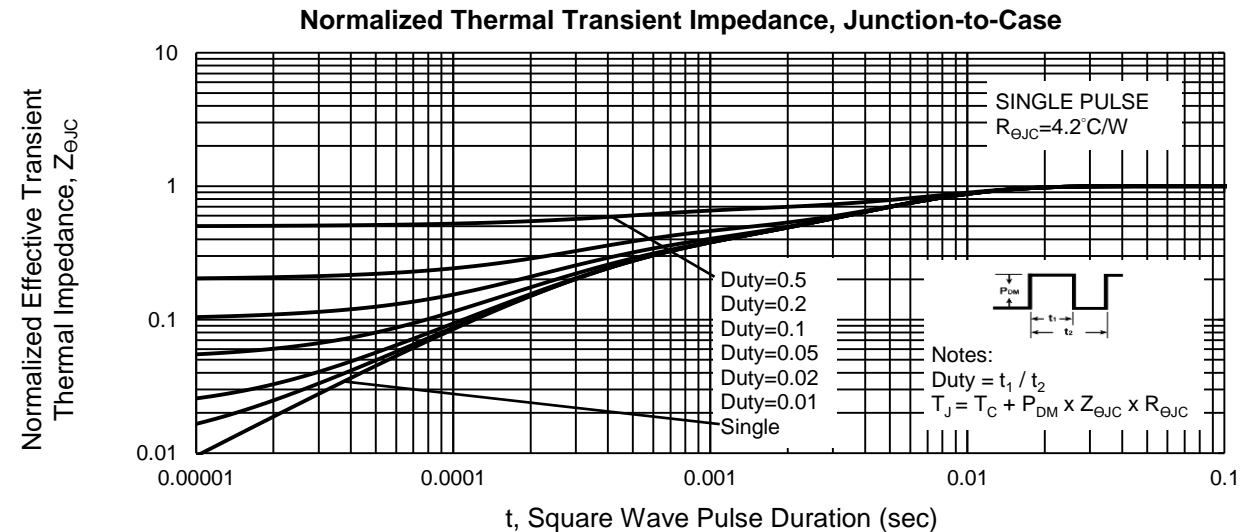
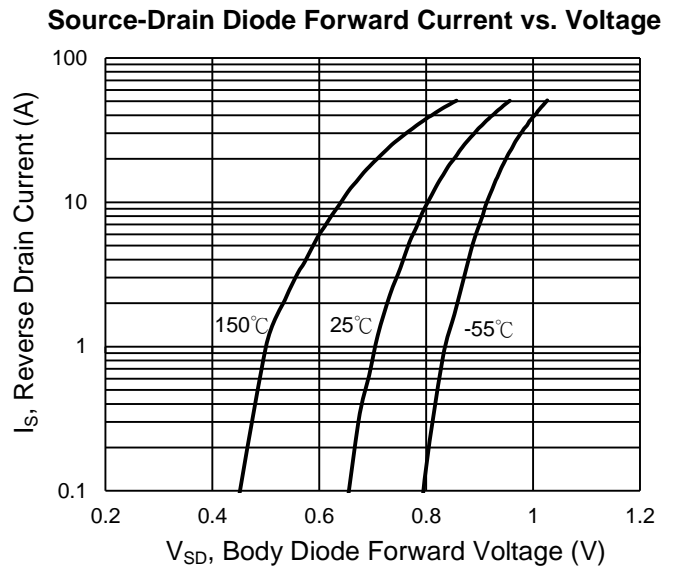
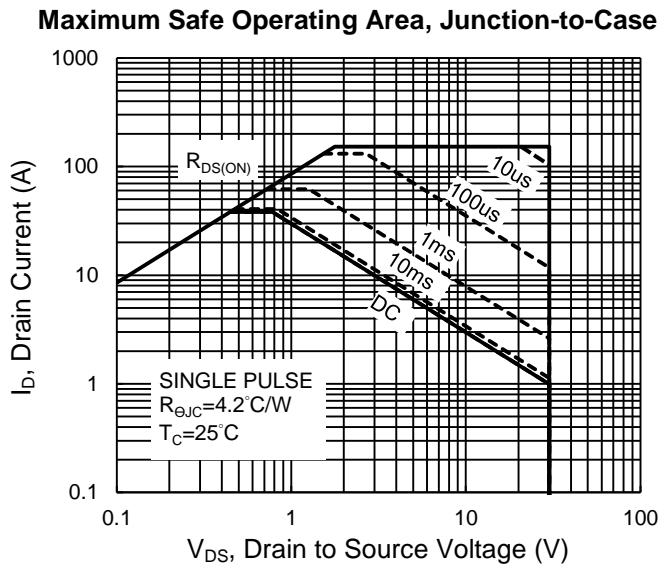
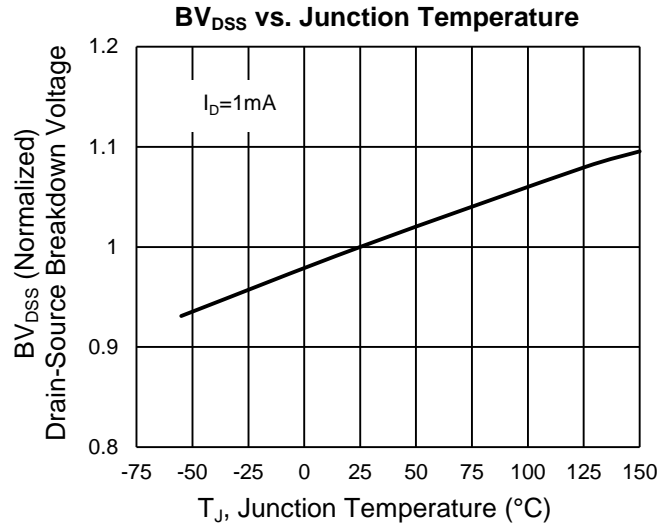
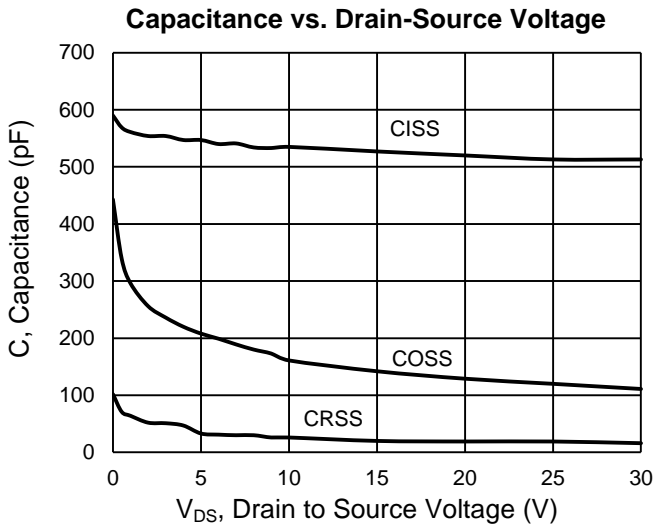


On-Resistance vs. Gate-Source Voltage



CHARACTERISTICS CURVES (Q1)

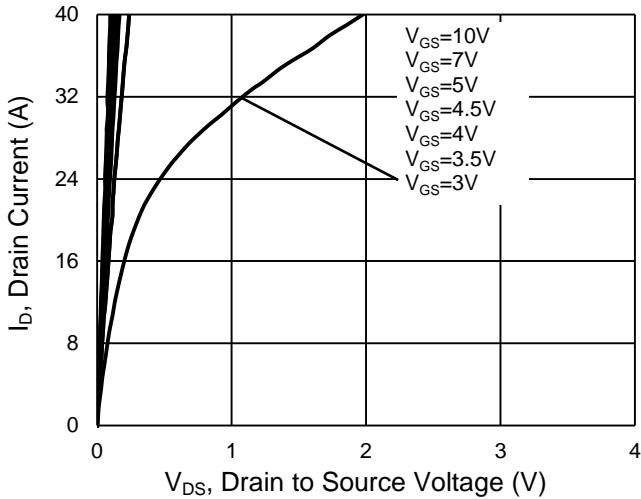
($T_A = 25^\circ\text{C}$ unless otherwise noted)



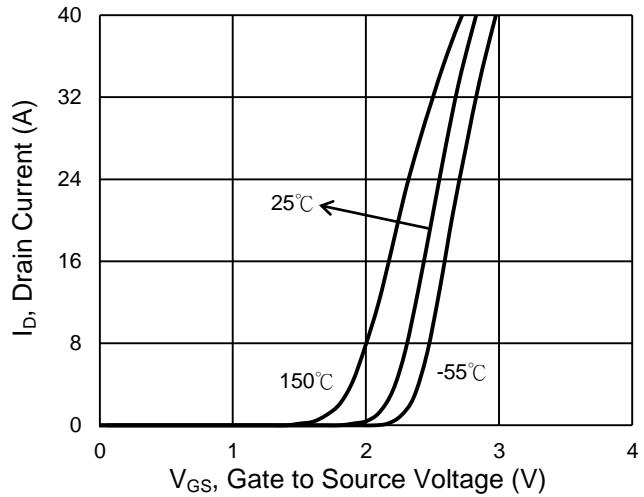
CHARACTERISTICS CURVES (Q2)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

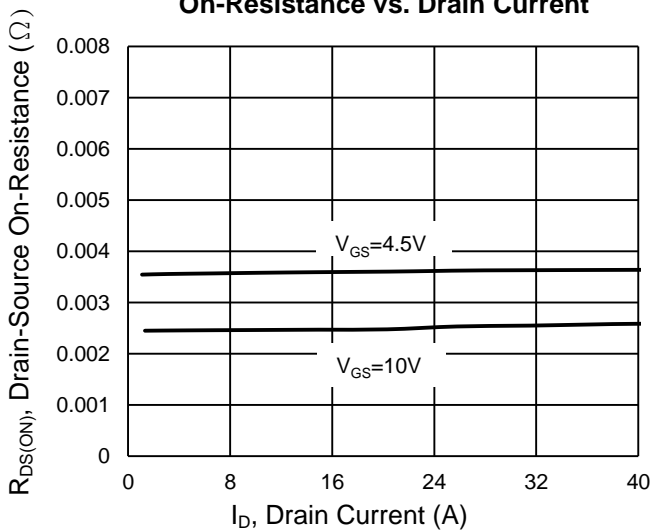
Output Characteristics



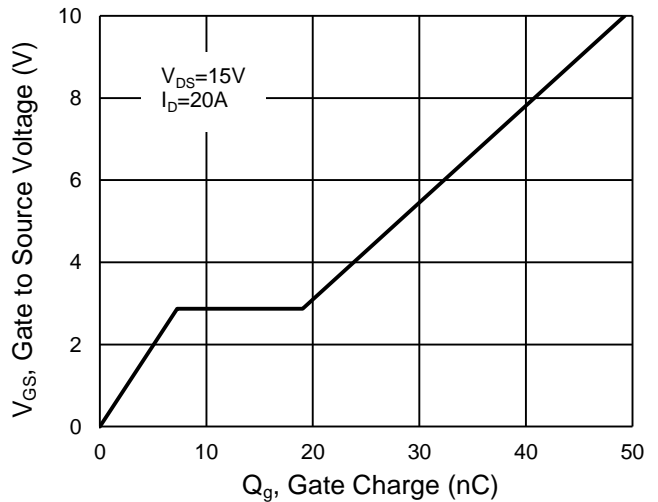
Transfer Characteristics



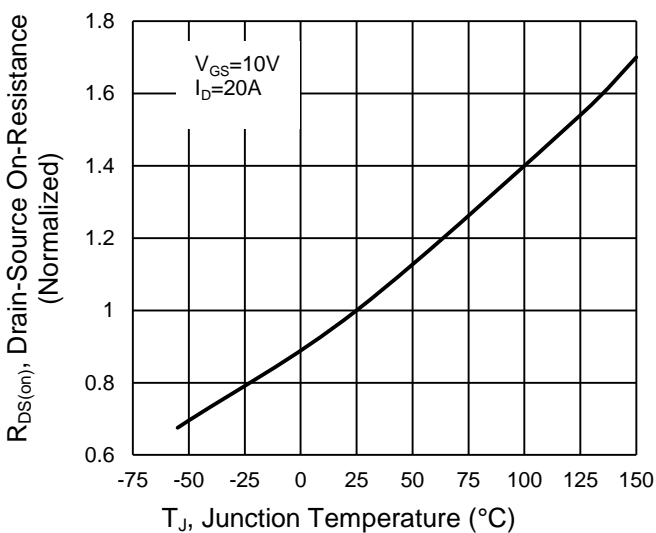
On-Resistance vs. Drain Current



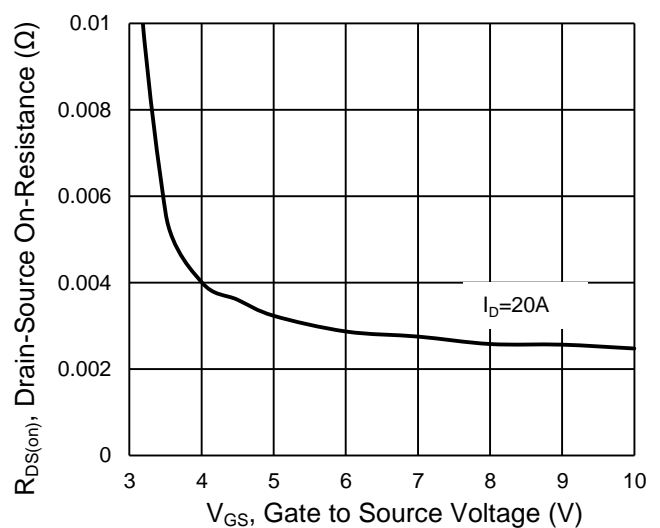
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature

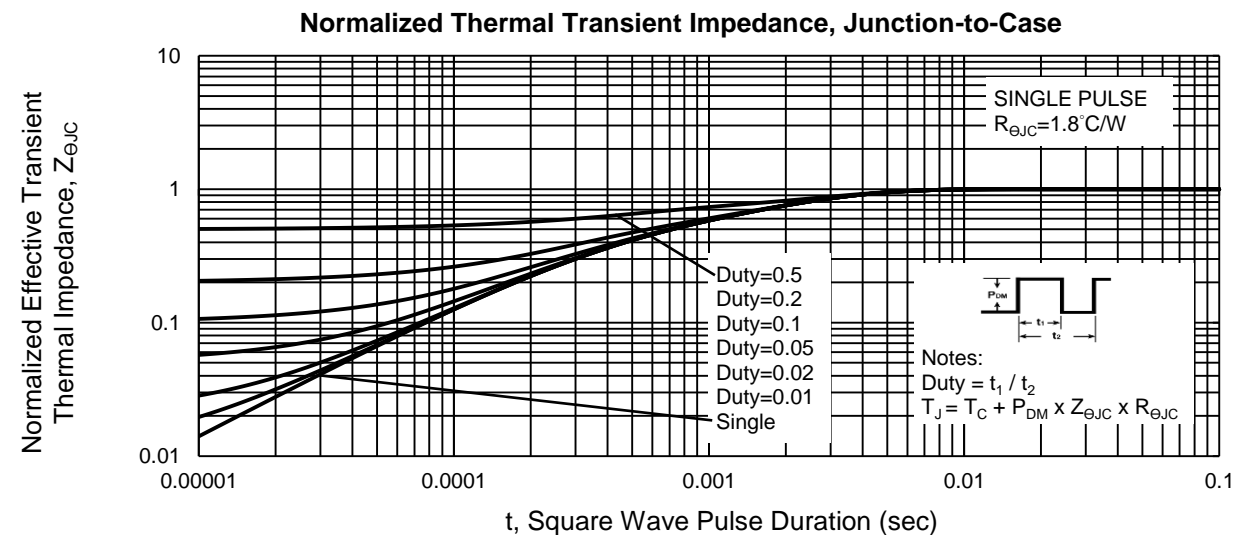
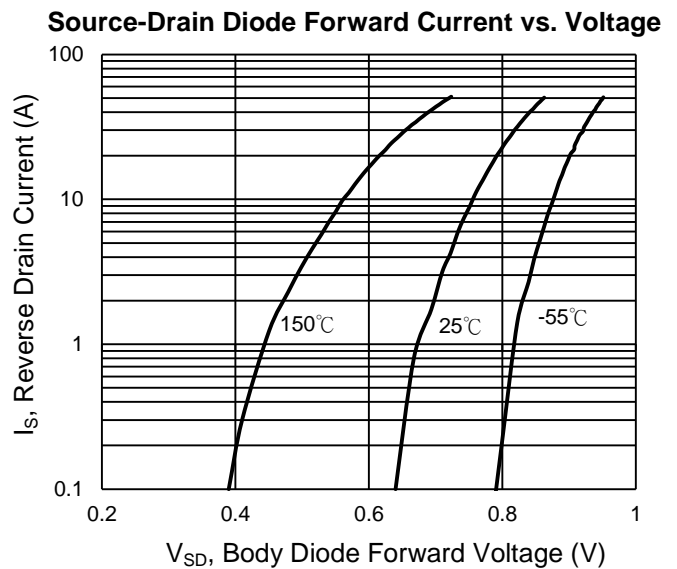
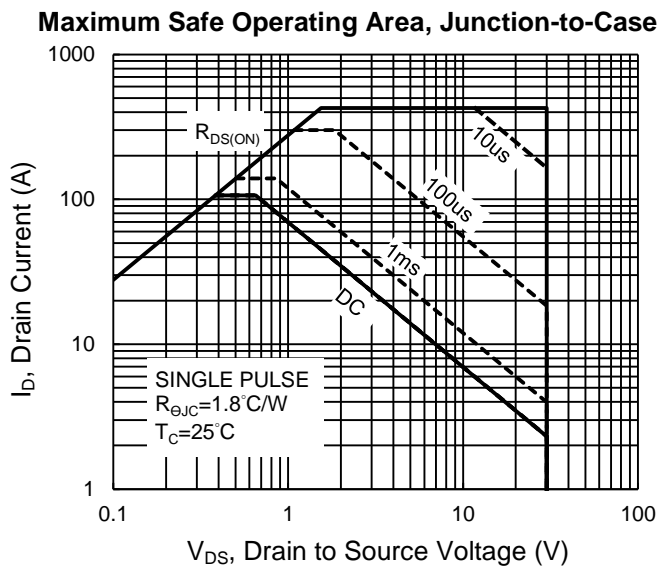
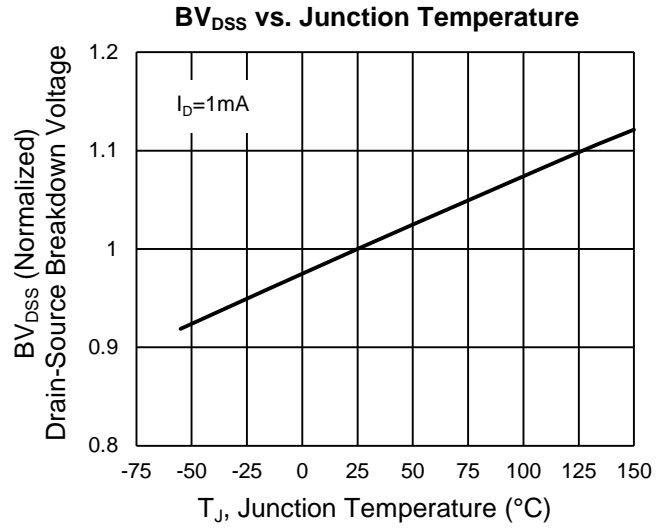
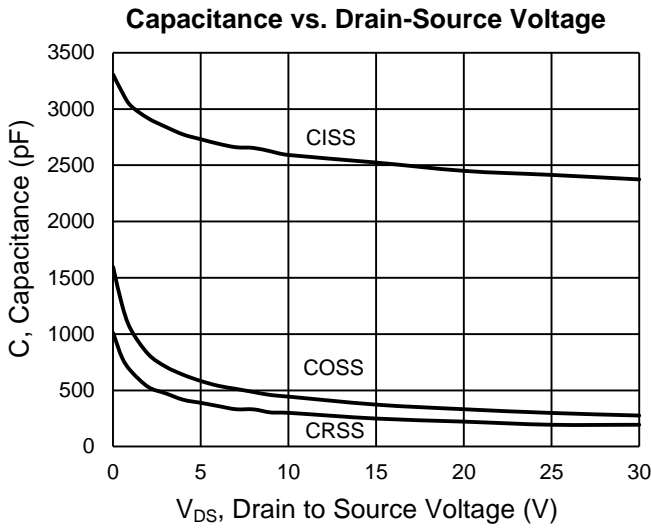


On-Resistance vs. Gate-Source Voltage



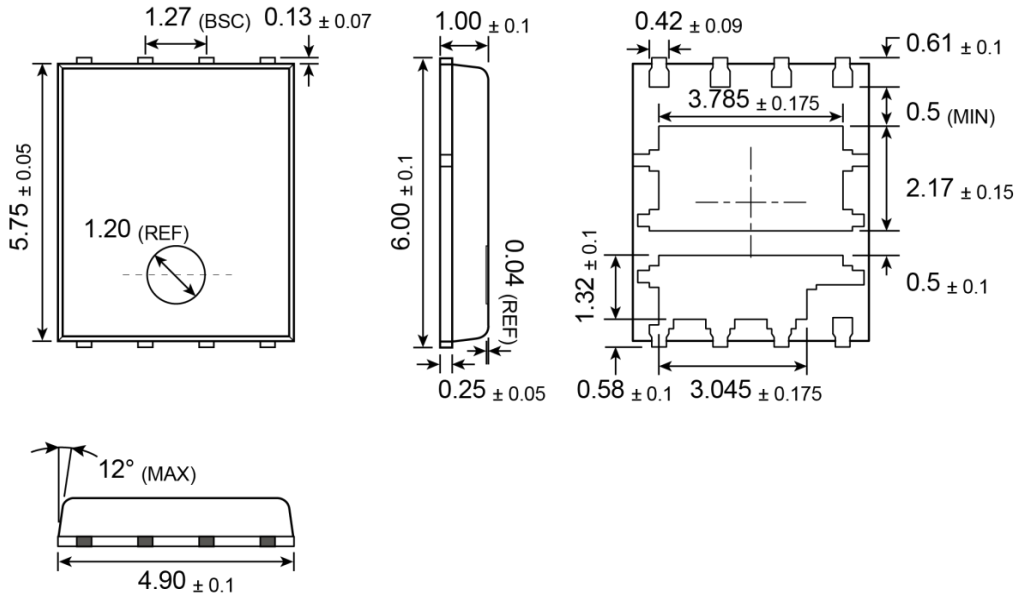
CHARACTERISTICS CURVES (Q2)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

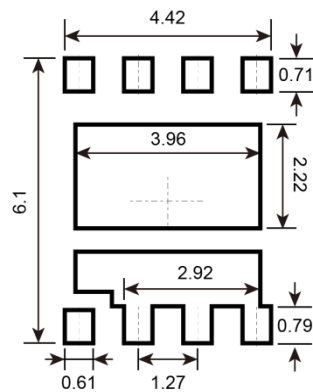


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

PDFN56 Asymmetric Dual



SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

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