MAX1737

Stand-Alone Switch-Mode Lithium-Ion Battery-Charger Controller

General Description

The MAX1737 is a switch-mode lithium-ion (Li+) battery charger that charges one to four cells. It provides a regulated charging current and a regulated voltage with only a ±0.8% total voltage error at the battery terminals. The external N-channel switch and synchronous rectifier provide high efficiency over a wide input voltage range. A built-in safety timer automatically terminates charging once the adjustable time limit has been reached.

The MAX1737 regulates the voltage set point and charging current using two loops that work together to transition smoothly between voltage and current regulation. An additional control loop monitors the total current drawn from the input source to prevent overload of the input supply, allowing the use of a low-cost wall adapter.

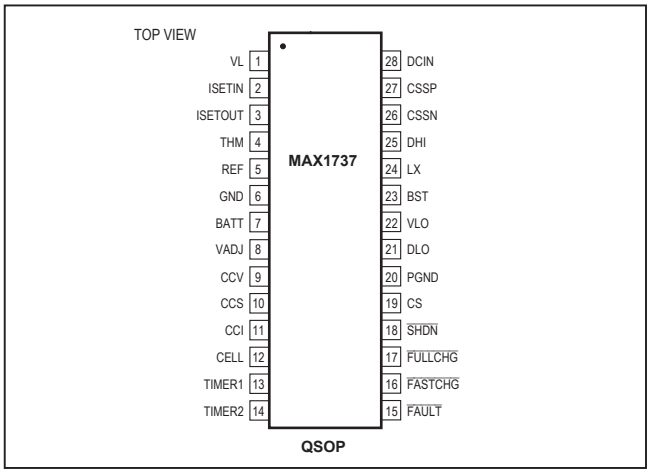
The per-cell battery voltage regulation limit is set between +4.0V and +4.4V and can be set from one to four by pin strapping. Battery temperature is monitored by an external thermistor to prevent charging if the battery temperature is outside the acceptable range.

The MAX1737 is available in a space-saving 28-pin QSOP package. Use the evaluation kit (MAX1737EVKIT) to help reduce design time.

Applications

- Notebook Computers
- Hand-Held Instruments
- Li+ Battery Packs
- Desktop Cradle Chargers

Pin Configuration



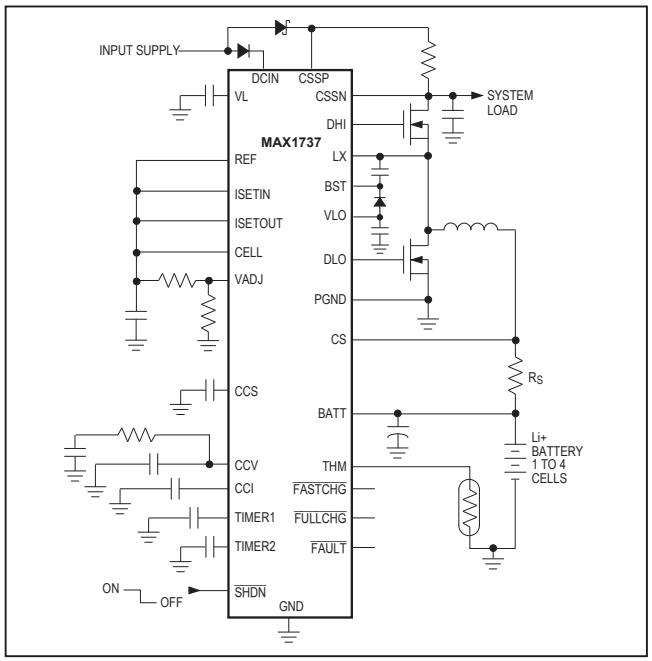
Features

- Stand-Alone Charger for Up to Four Li+ Cells
- ±0.8% Accurate Battery Regulation Voltage
- Low Dropout: 98% Duty Cycle
- Safely Precharges Near-Dead Cells
- Continuous Voltage and Temperature Monitoring
- <1µA Shutdown Battery Current
- Input Voltage Up to +28V
- Safety Timer Prevents Overcharging
- Input Current Limiting
- Space-Saving 28-Pin QSOP
- 300kHz PWM Oscillator Reduces Noise
- 90% Conversion Efficiency

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1737EEI	-40°C to +85°C	28 QSOP

Typical Operating Circuit



maxim integrated™

Absolute Maximum Ratings

CSSP, CSSN, DCIN to GND ..... -0.3V to +30V
BST, DHI to GND ..... -0.3V to +36V
BST to LX ..... -0.3V to +6V
DHI to LX ..... -0.3V to ((BST - LX) + 0.3V)
LX to GND ..... -0.3V to (CSSN + 0.3V)
$\overline{FULLCHG}$, $\overline{FASTCHG}$, $\overline{FAULT}$ to GND ..... -0.3V to +30V
VL, VLO, $\overline{SHDN}$, CELL, TIMER1, TIMER2, CCI, CCS, CCV, REF, ISETIN, ISETOUT, VADJ, THM to GND ..... -0.3V to +6V
DLO to GND ..... -0.3V to (VLO + 0.3V)
BATT, CS to GND ..... -0.3V to +20V
PGND to GND, CSSP to CSSN ..... -0.3V to +0.3V
VL to VLO ..... -0.3V to +0.3V
VL Source Current 50mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 10.8mW/°C above +70°C) 860mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(Circuit of Figure 1, V_{DCIN} = V_{CSSN} = V_{CSSP} = +18V, $\overline{SHDN}$ = VL, CELL = GND, V_{BATT} = V_{CS} = +4.2V, V_{VADJ} = V_{REF} / 2, ISETIN = ISETOUT = REF, R_{THM} = 10kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE						
DCIN Input Voltage Range			6		28	V
DCIN Quiescent Supply Current	6.0V < V_{DCIN} < 28V			5	7	mA
DCIN to BATT Undervoltage Threshold, DCIN Falling			0.05		0.155	V
DCIN to BATT Undervoltage Threshold, DCIN Rising			0.19		0.40	V
VL Output Voltage	6.0V < V_{DCIN} < 28V		5.10	5.40	5.70	V
VL Output Load Regulation	I_{VL} = 0 to 15mA			44	65	mV
REF Output Voltage			4.179	4.20	4.221	V
REF Line Regulation	6V < V_{DCIN} < 28V			2	6	mV
REF Load Regulation	I_{REF} = 0 to 1mA			6	14	mV
SWITCHING REGULATOR						
PWM Oscillator Frequency	V_{BATT} = 15V, CELL = VL		270	300	330	kHz
LX Maximum Duty Cycle	In dropout f_{OSC} / 4, V_{CCV} = 2.4V, V_{BATT} = 15V, CELL = VL		97	98		%
CSSN + CSSP Off-State Leakage	V_{CSSN} = V_{CSSP} = V_{DCIN} = 28V, SHDN = GND			2	10	µA
DHI, DLO On-Resistance					7	Ω
LX Leakage	LX = V_{DCIN} = 28V, $\overline{SHDN}$ = GND			0.1	10	µA
BATT, CS Input Current	$\overline{SHDN}$ = GND, V_{BATT} = 19V			0.1	5	µA
	CELL = $\overline{SHDN}$ = VL, V_{BATT} = 17V			225	500	
BATT, CS Input Voltage Range			0		19	V
Battery Regulation Voltage (V_{BATTR})	CELL = float, GND, VL, or REF (Note 1)		4.167	4.2	4.233	V/cell
Absolute Voltage Accuracy	Not including VADJ resistor tolerances		-0.8		+0.8	%
	With 1% VADJ resistors		-1		+1	
Battery Regulation Voltage Adjustment Range	V_{CCV} = 2V	V_{VADJ} = GND	3.948	3.979	4.010	V/cell
		V_{VADJ} = REF	4.386	4.421	4.453	

Electrical Characteristics (continued)

(Circuit of Figure 1, V_{DCIN} = V_{CSSN} = V_{CSSP} = +18V, $\overline{SHDN}$ = VL, CELL = GND, V_{BATT} = V_{CS} = +4.2V, V_{VADJ} = V_{REF} / 2, ISETIN = ISETOUT = REF, R_{THM} = 10kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ERROR AMPLIFIERS					
CCV Amplifier Transconductance (Note 2)	4.15V < V_{BATT} < 4.25V, V_{CCV} = 2V	0.39	0.584	0.80	mS
CCV Amplifier Maximum Output Current	3.5V < V_{BATT} < 5V, V_{CCV} = 2V	±50			µA
CS to BATT Current-Sense Voltage	$V_{ISETOUT}$ = V_{REF} / 5	30	40	50	mV
CS to BATT Full-Scale Current-Sense Voltage	V_{BATT} = 3V to 17V, CELL = GND or VL	185	200	215	mV
CS to BATT Current-Sense Voltage When in Prequalification State	V_{BATT} < 2.4V per cell	5	10	15	mV
CS to BATT Hard Current-Limit Voltage		355	385	415	mV
CSSP to CSSN Current-Sense Voltage	6V < V_{CSSP} < 28V, V_{ISETIN} = V_{REF} / 5, V_{CCS} = 2V	10	20	30	mV
CSSP to CSSN Full-Scale Current-Sense Voltage	6V < V_{CSSP} < 28V, V_{CCS} = 2V	90	105	115	mV
CCI Amplifier Transconductance	V_{CCI} = 2V	0.6	1	1.4	mS
CCI Amplifier Output Current	V_{CS} - V_{BATT} = 0, 400mV	±100			µA
CCS Amplifier Transconductance	I_{SET} = REF, V_{CCS} = 2V	1.2	2	2.6	mS
CCS Amplifier Output Current	V_{CSSP} - V_{CSSN} = 0, 200mV	±100			µA
CCI, CCS Clamp Voltage with Respect to CCV		25		200	mV
CCV Clamp Voltage with Respect to CCI, CCS		25		200	mV
STATE MACHINE					
THM Trip-Threshold Voltage	THM low-temperature or high-temperature current	1.386	1.4	1.414	V
THM Low-Temperature Current	V_{THM} = 1.4V	46.2	49	51.5	µA
THM High-Temperature Current	V_{THM} = 1.4V	344	353	362	µA
THM COLD Threshold Resistance (Note 3)	Combines THM low-temperature current and THM rising threshold, V_{TRT}/I_{TLTC}	26.92	28.70	30.59	kΩ
THM HOT Threshold Resistance (Note 3)	Combines THM high-temperature current and THM rising threshold, V_{TRT}/I_{THTC}	3.819	3.964	4.115	kΩ
BATT Undervoltage Threshold (Note 4)		2.4	2.5	2.6	V/cell
BATT Overvoltage Threshold (Note 5)		4.55	4.67	4.8	V/cell
BATT Charge Current Full-Charge Termination Threshold CS-BATT (Note 6)		35	44	55	mV
BATT Recharge Voltage Threshold (Note 7)		94	95	96	% of V_{BATTR}
TIMER1, TIMER2 Oscillation Frequency		2.1	2.33	2.6	kHz
Prequalification Timer		6.25	7.5	8.75	min
Fast-Charge Timer		81	90	100	min
Full-Charge Timer		81	90	100	Min

Electrical Characteristics (continued)

(Circuit of Figure 1, V_{DCIN} = V_{CSSN} = V_{CSSP} = +18V, $\overline{SHDN}$ = VL, CELL = GND, V_{BATT} = V_{CS} = +4.2V, V_{VADJ} = V_{REF} / 2, ISETIN = ISETOUT = REF, R_{THM} = 10kΩ, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Top-Off Timer		40.5	45	49.8	Min
Temperature Measurement Frequency	1nF on TIMER1 and TIMER2	0.98	1.12	1.32	Hz
CONTROL INPUTS/OUTPUTS					
$\overline{SHDN}$ Input Voltage High		1.4			V
$\overline{SHDN}$ Input Voltage Low (Note 8)				0.6	V
VADJ, ISETIN, ISETOUT Input Voltage Range		0		V_{REF}	V
VADJ, ISETIN, ISETOUT Input Bias Current	V_{VADJ}, V_{ISETIN}, $V_{ISETOUT}$ = 0 or 4.2V	-50		50	nA
$\overline{SHDN}$ Input Bias Current	$\overline{SHDN}$ = GND or VL	-1		1	µA
CELL Input Bias Current		-5		5	µA
ISETIN Adjustment Range		V_{REF}/5		V_{REF}	V
ISETOUT Adjustment Range		V_{REF}/5		V_{REF}	V
ISETOUT Voltage for I_{CHG} = 0		150	220	300	mV
CELL Input Voltage	For 1 cell	0		0.5	V
	For 2 cells	1.5		2.5	
	For 3 cells	V_{REF} - 0.3		V_{REF} + 0.3	
	For 4 cells	V_{VL} - 0.4		V_{VL}	
$\overline{FASTCHG}$, $\overline{FULLCHG}$, $\overline{FAULT}$ Output Low Voltage	I_{SINK} = 5mA			0.5	V
$\overline{FASTCHG}$, $\overline{FULLCHG}$, $\overline{FAULT}$ Output High Leakage	$\overline{FASTCHG}$, $\overline{FULLCHG}$, $\overline{FAULT}$ = 28V; $\overline{SHDN}$ = GND			1	µA

Electrical Characteristics

(Circuit of Figure 1, V_{DCIN} = V_{CSSN} = V_{CSSP} = +18V, $\overline{SHDN}$ = VL, CELL = GND, V_{BATT} = V_{CS} = +4.2V, V_{VADJ} = V_{REF} / 2, ISETIN = ISETOUT = REF, R_{THM} = 10kΩ, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 9)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE					
DCIN Input Voltage Range		6		28	V
VL Output Voltage	6.0V < V_{DCIN} < 28V	5.1		5.7	V
REF Output Voltage		4.166		4.242	V
REF Line Regulation	6V < V_{DCIN} < 28V			6	mV
SWITCHING REGULATOR					
PWM Oscillator Frequency	V_{BATT} = 15V, CELL = VL	260		340	kHz
DHI, DLO On-Resistance				7	Ω
BATT, CS Input Voltage Range		0		19	V
Battery Regulation Voltage (V_{BATTR})	CELL = float, GND, VL, or REF	4.158		4.242	V/cell
Absolute Voltage Accuracy	Not including V_{ADJ} resistor tolerances	-1		+1	%
ERROR AMPLIFIERS					
CS to BATT Current-Sense Voltage	$V_{ISETOUT}$ = V_{REF}/5	25		55	mV
CS to BATT Full-Scale Current-Sense Voltage	V_{BATT} = 3V to 17V, CELL = GND or VL	180		220	mV
CS to BATT Current-Sense Voltage When in Prequalification State	V_{BATT} < 2.4V per cell	3		17	mV
CS to BATT Hard Current-Limit Voltage		350		420	mV
CSSP to CSSN Current-Sense Voltage	6V < V_{CSSP} < 28V, V_{ISETIN} = V_{REF} / 5, V_{CCS} = 2V	5		35	mV
CSSP to CSSN Full-Scale Current-Sense Voltage	6V < V_{CSSP} < 28V, V_{CCS} = 2V	85		115	mV
STATE MACHINE					
THM Trip-Threshold Voltage	THM low-temperature or high-temperature current	1.386		1.414	V
THM Low-Temperature Current	V_{THM} = 1.4V	46.2		51.5	µA
THM COLD Threshold Resistance (Note 3)	Combines THM low-temperature current and THM rising threshold, V_{TRT}/I_{TLTC}	26.92		30.59	kΩ
BATT Undervoltage Threshold (Note 4)		2.4		2.6	V/cell
BATT Overvoltage Threshold (Note 5)		4.55		4.8	V/cell
BATT Charge Current Full-Charge Termination Threshold CS-BATT (Note 6)		35		55	mV
Temperature Measurement Frequency	1nF on TIMER1 and TIMER2	0.93		1.37	Hz

Electrical Characteristics (continued)

(Circuit of Figure 1, V_{DCIN} = V_{CSSN} = V_{CSSP} = +18V, $\overline{SHDN}$ = VL, CELL = GND, V_{BATT} = V_{CS} = +4.2V, V_{VADJ} = V_{REF} / 2, ISETIN = ISETOUT = REF, R_{THM} = 10kΩ, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 9)

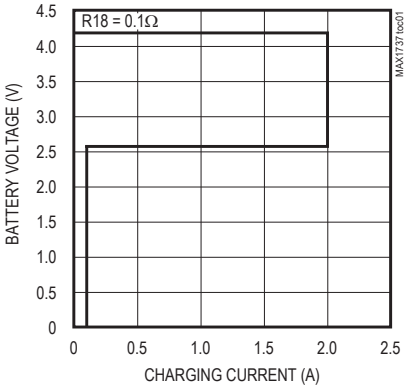
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROL INPUTS/OUTPUTS					
$\overline{SHDN}$ Input Voltage High		1.4			V
$\overline{SHDN}$ Input Voltage Low (Note 8)				0.6	V

Note 1: Battery Regulation Voltage = Number of Cells × (3.979V + 0.10526 × V_{VADJ}).
Note 2: This transconductance is for one cell. Divide by number of cells to determine actual transconductance.
Note 3: See *Thermistor* section.
Note 4: Below this threshold, the charger reverts to prequalification mode and I_{CHG} is reduced to about 5% of full scale.
Note 5: Above this threshold, the charger returns to reset.
Note 6: After full-charge state is complete and peak inductor current falls below this threshold, $\overline{FULLCHG}$ output switches high Battery charging continues until top-off timeout occurs.
Note 7: After charging is complete, when BATT voltage falls below this threshold, a new charging cycle is initiated.
Note 8: In shutdown, charging ceases and battery drain current drops to 5µA (max), but internal IC bias current remains on.
Note 9: Specifications to -40°C are guaranteed by design and not production tested.

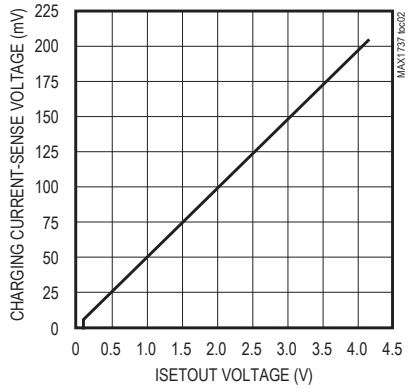
Typical Operating Characteristics

(Circuit of Figure 1, V_{DCIN} = +18V, ISETIN = ISETOUT = REF, $V_{VADJ} = V_{REF} / 2$, T_A = +25°C, unless otherwise noted.)

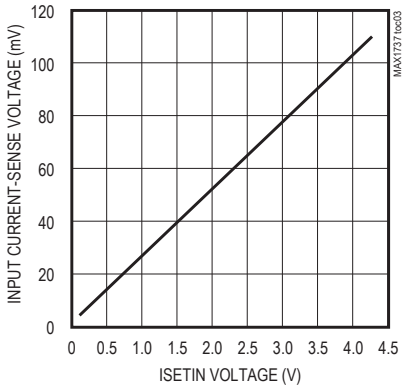
BATTERY VOLTAGE vs. CHARGING CURRENT



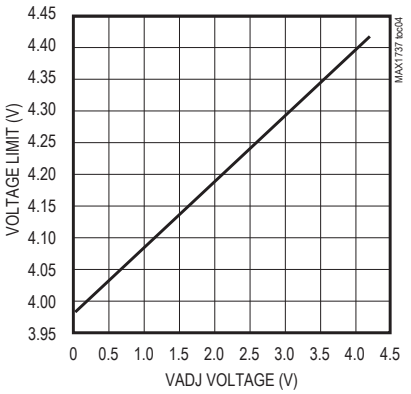
CHARGING CURRENT-SENSE VOLTAGE vs. ISETOUT VOLTAGE



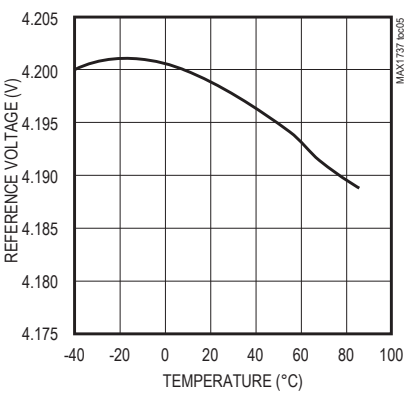
INPUT CURRENT-SENSE VOLTAGE vs. ISETIN VOLTAGE



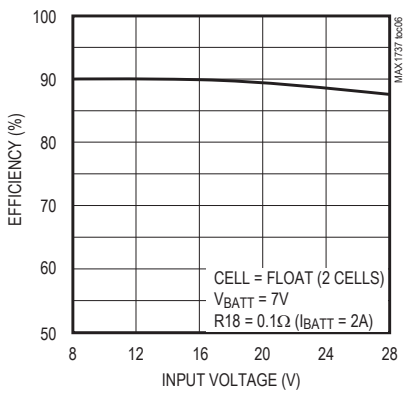
VOLTAGE LIMIT vs. VADJ VOLTAGE



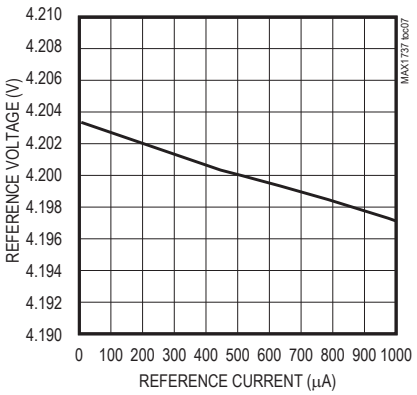
REFERENCE VOLTAGE vs. TEMPERATURE



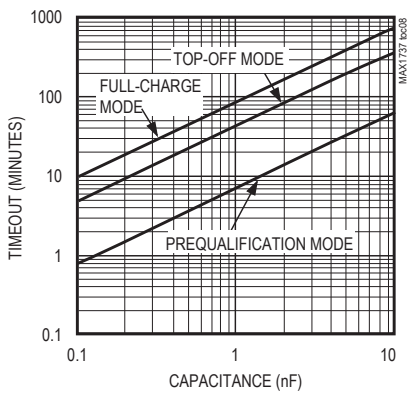
EFFICIENCY vs. INPUT VOLTAGE



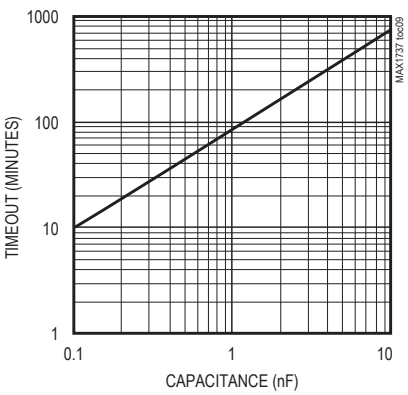
REFERENCE LOAD REGULATION



TIMEOUT vs. TIMER1 CAPACITANCE



FAST-CHARGE TIMEOUT vs. TIMER2 CAPACITANCE



Pin Description

PIN	NAME	FUNCTION
1	VL	Chip Power Supply. Output of the 5.4V linear regulator from DCIN. Bypass VL to GND with a 2.2µF or larger ceramic capacitor.
2	ISETIN	Input Current Limit Adjust. Use a voltage-divider to set the voltage between 0 and V_{REF}. See *Input Current Regulator* section.
3	ISETOUT	Battery Charging Current Adjust. Use a voltage-divider to set the voltage between 0 and V_{REF}. See *Charging Current Regulator* section.
4	THM	Thermistor Input. Connect a thermistor from THM to GND to set a qualification temperature range. If unused, connect a 10kΩresistor from THM to ground. See *Thermistor* section.
5	REF	4.2V Reference Voltage Output. Bypass REF to GND with a 1µF or larger ceramic capacitor.
6	GND	Analog Ground
7	BATT	Battery Voltage-Sense Input and Current-Sense Negative Input
8	VADJ	Voltage Adjust. Use a voltage-divider to set the VADJ voltage between 0 and V_{REF} to adjust the battery regulation voltage by ±5%. See *Setting the Voltage Limit* section.
9	CCV	Voltage Regulation Loop Compensation Point
10	CCS	Input Source Current Regulation Compensation Point
11	CCI	Battery-Current Regulation Loop Compensation Point
12	CELL	Cell-Count Programming Input. See Table 2
13	TIMER1	Timer 1 Adjustment. Connect a capacitor from TIMER1 to GND to set the prequalification, full-charge, and top-off times. See *Timers* section.
14	TIMER2	Timer 2 Adjustment. Connect a capacitor from TIMER2 to GND to set the fast-charge time. See *Timers* section.
15	$\overline{\text{FAULT}}$	Charge Fault Indicator. Open-drain output pulls low when charging terminates abnormally (Table 1).
16	$\overline{\text{FASTCHG}}$	Fast-Charge Indicator. Open-drain output pulls low when charging with constant current.
17	$\overline{\text{FULLCHG}}$	Full-Charge Indicator. Open-drain output pulls low when charging with constant voltage in full-charge state.
18	SHDN	Shutdown Input. Drive $\overline{\text{SHDN}}$ low to disable charging. Connect $\overline{\text{SHDN}}$ to VL for normal operation.
19	CS	Battery Current-Sense Positive Input. See *Charging Current Regulator* section.
20	PGND	Power Ground
21	DLO	Synchronous-Rectifier MOSFET Gate-Drive Output
22	VLO	Synchronous-Rectifier MOSFET Gate-Drive Bias. Bypass VLO to PGND with a 0.1µF capacitor.
23	BST	High-Side MOSFET Gate Drive Bias. Connect a 0.1µF or greater capacitor from BST and LX.
24	LX	Power Inductor Switching Node. Connect LX to the high-side MOSFET source.
25	DHI	High-Side MOSFET Gate-Drive Output
26	CSSN	Source Current-Sense Negative Input. See *Input Current Regulator* section.
27	CSSP	Source Current-Sense Positive Input. See *Input Current Regulator* section.
28	DCIN	Power-Supply Input. DCIN is the input supply for the VL regulator. Bypass DCIN to GND with a 0.1µF capacitor. Also used for the source undervoltage sensing.

Detailed Description

The MAX1737 includes all of the functions necessary to charge between one and four series Li+ battery cells. It includes a high-efficiency synchronous-rectified step-down DC-DC converter that controls charging voltage and current. It also includes input source-current limiting, battery temperature monitoring, battery undervoltage precharging, battery fault indication, and a state machine with timers for charge termination.

The DC-DC converter uses an external dual N-channel MOSFET as a switch and a synchronous rectifier to convert the input voltage to the charging current or voltage. The typical application circuit is shown in Figure 1. Figure 2 shows a typical charging sequence and Figure 3 shows the block diagram. Charging current is set by the voltage at ISETOUT and the voltage across R18. The battery voltage is measured at the BATT pin. The battery regulation voltage is set to 4.2V per cell and can be adjusted ±5% by changing the voltage at the VADJ pin. By limiting the adjust range, the voltage

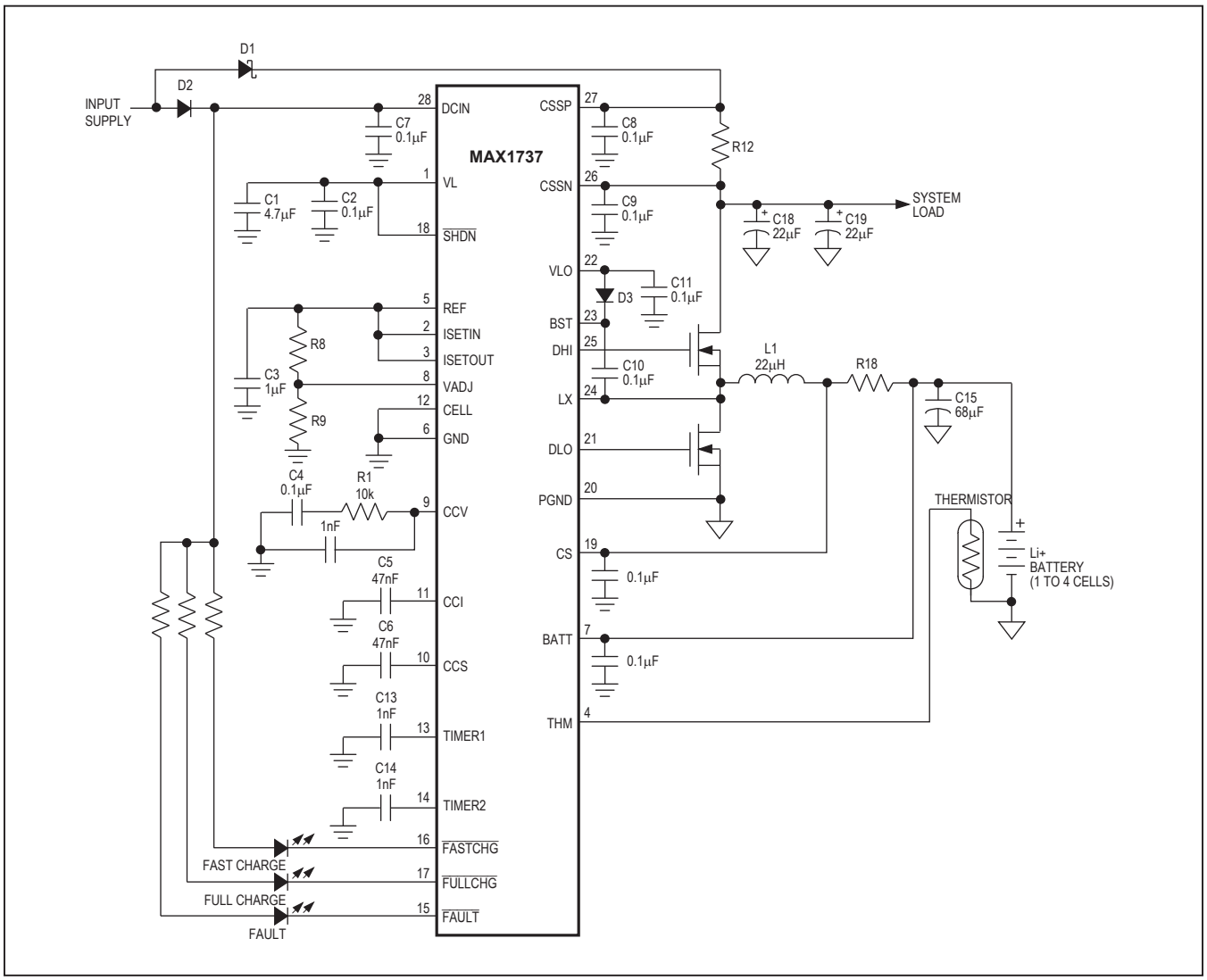


Figure 1. Typical Application Circuit

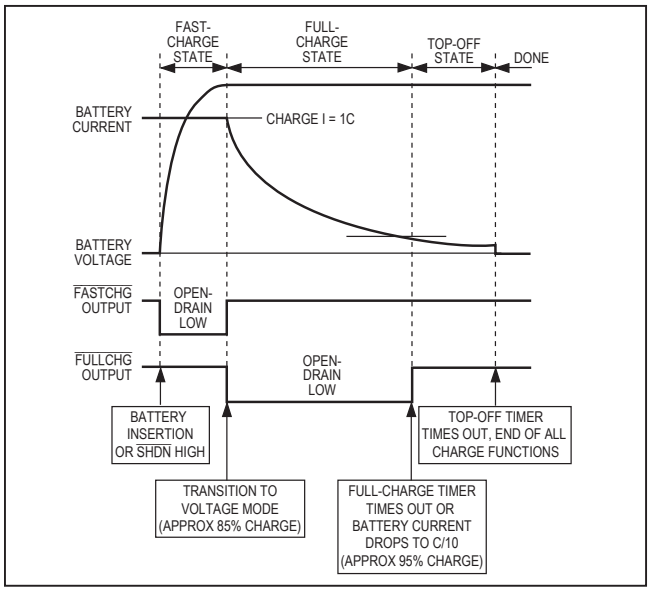


Figure 2. Charge State and Indicator Output Timing for a Typical Charging Sequence

accuracy is better than 1% while using 1% setting resistors.

The MAX1737 includes a state machine that controls the charging algorithm. Figure 4 shows the state diagram. Table 1 lists the charging state conditions. When power is applied or $\overline{SHDN}$ is driven high, the part goes into the reset state where the timers are reset to zero to prepare for charging. From the reset state, it enters the prequalification state. In this state, 1/20 of the fast-charge current charges the battery, and the battery temperature and voltage are measured. If the voltage is above the undervoltage threshold and the temperature is within the limits, then it will enter the fast-charge state. If the battery voltage does not rise above the undervoltage threshold before the prequalification timer expires, the charging terminates and the $\overline{FAULT}$ output goes low. The prequalification time is set by the TIMER1 capacitor (C_{TIMER1}). If the battery is outside the temperature limits, charging and the timer are suspended. Once the temperature is back within limits, charging and the timer resume.

In the fast-charge state, the $\overline{FASTCHG}$ output goes low, and the batteries charge with a constant current (see the *Charging Current Regulator* section). If the battery voltage reaches the voltage limit before the fast timer expires, the part enters the full-charge state. If the fast-charge timer expires before the voltage limit is reached, charging terminates with a fault indication. The fast-charge time limit is set by the TIMER2 capacitor (C_{TIMER2}). If the battery temperature is outside the limits, charging pauses and the timers are suspended until the temperature returns to within the limits.

In the full-charge state, the $\overline{FULLCHG}$ output goes low and the batteries charge at a constant voltage (see the *Voltage Regulator* section). When the charging current drops below 10% of the charging current limit, or if the full-charge timer expires, the state machine enters the top-off state. In the top-off state, the batteries continue to charge at a constant voltage until the top-off timer expires, at which time it enters the done state. In the done state, charging stops until the battery voltage drops below the recharge-voltage threshold. It then enters the reset state to start the charging process again. In the full-charge or the top-off state, if the battery temperature is outside the limits, charging pauses and the timers are suspended until the battery temperature returns to within limits.

Voltage Regulator

Li+ batteries require a high-accuracy voltage limit while charging. The MAX1737 uses a high-accuracy voltage regulator (±0.8%) to limit the charging voltage. The battery regulation voltage is nominally set to 4.2V per cell and can be adjusted ±5% by setting the voltage at the VADJ pin between reference voltage and ground. By limiting the adjust range of the regulation voltage, an overall voltage accuracy of better than 1% is maintained while using 1% resistors. CELL sets the cell count from one to four series cells (see *Setting the Battery Regulation Voltage* section).

An internal error amplifier (GMV) maintains voltage regulation (Figure 3). The GMV amplifier is compensated at CCV. The component values shown in Figure 1 provide suitable performance for most applications. Individual compensation of the voltage regulation and current regulation loops allows for optimal compensation of each.

Charging Current Regulator

The charging current-limit regulator limits the charging current. The current is sensed by measuring the voltage across the current-sense resistor (R18, Figure 1) placed between the BATT and CS pins. The voltage on the ISETOUT pin also controls the charging current. Full-scale charging current is achieved by connecting ISETOUT to REF. In this case, the full-scale current-sense voltage is 200mV from CS to BATT.

When choosing the charging current-sense resistor, note that the voltage drop across this resistor causes further power loss, reducing efficiency. However, adjusting ISETOUT to reduce the voltage across the

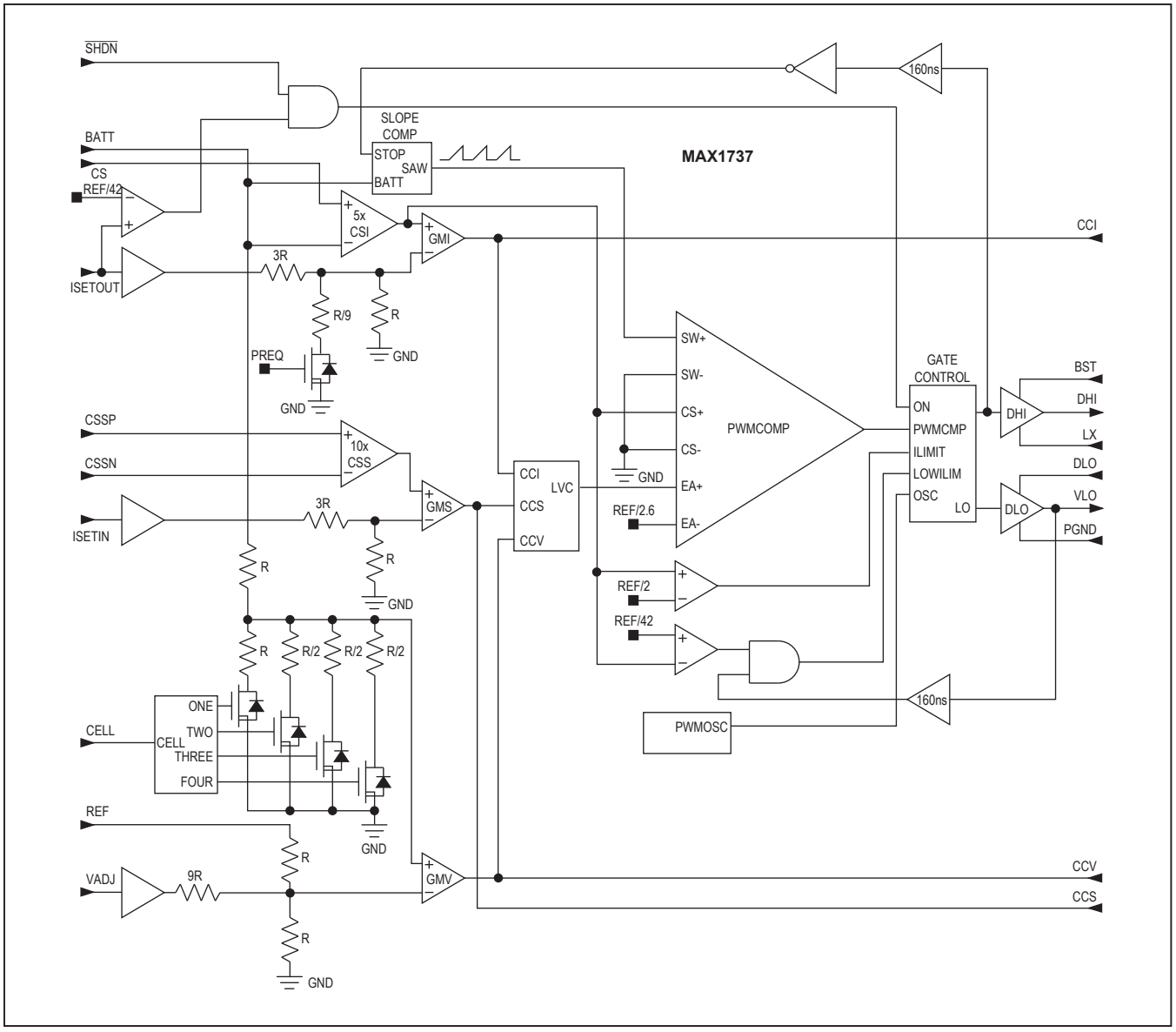


Figure 3. PWM Controller Block Diagram

current-sense resistor may degrade accuracy due to the input offset of the current-sense amplifier.

The charging-current error amplifier (GMI) is compensated at CCI. A 47nF capacitor at CCI provides suitable performance for most applications.

Input Current Regulator

The total input current (from a wall cube or other DC source) is the sum of system supply current plus the battery-charging current. The input current regulator limits the source current by reducing charging current when input current exceeds the set input current limit. System current normally fluctuates as portions of the system are powered up or put to sleep. Without input

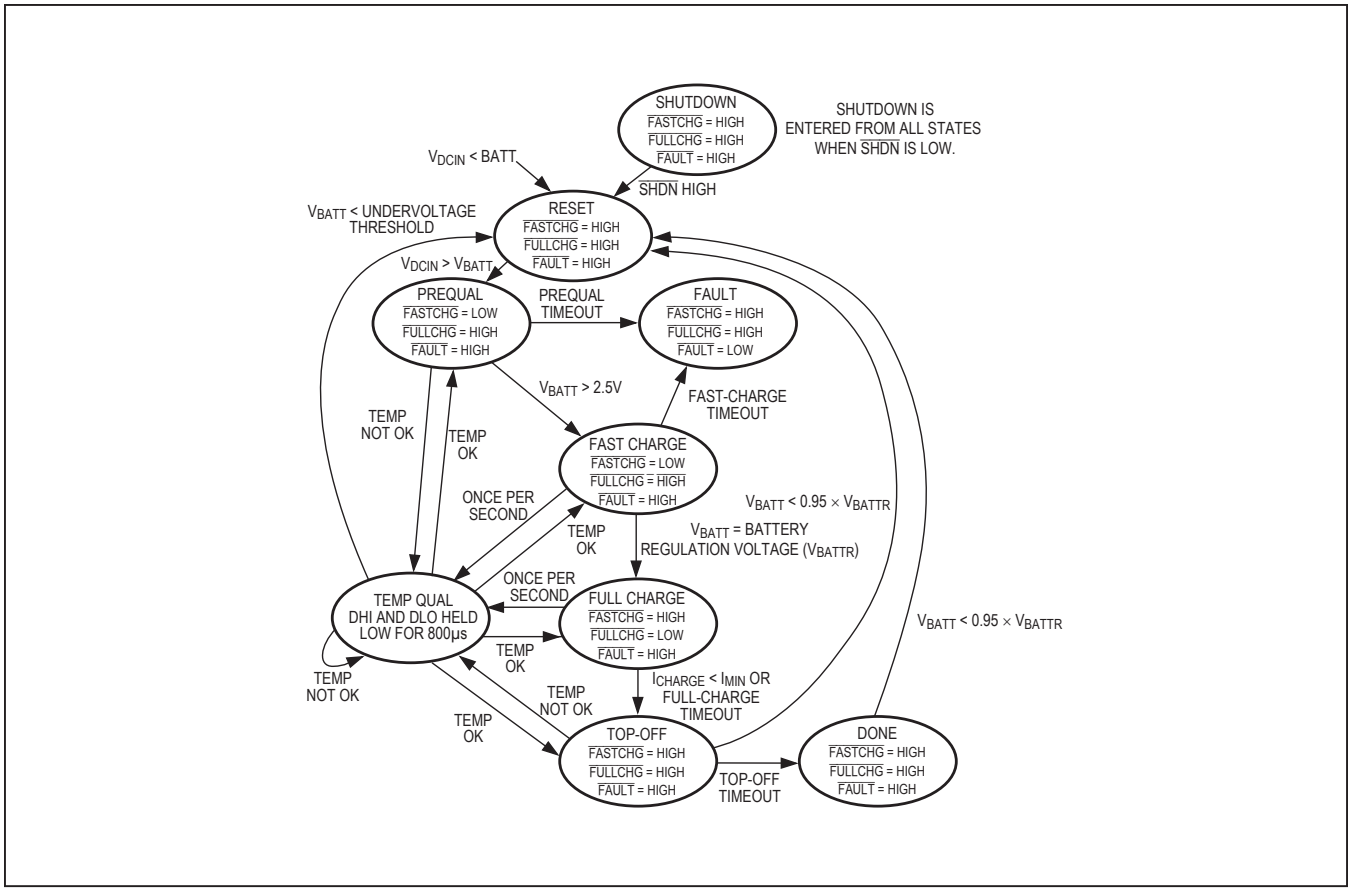


Figure 4. State Diagram

current regulation, the input source must be able to supply the maximum system current plus the maximum charger input current. By using the input current limiter, the current capability of the AC wall adapter may be lowered, reducing system cost.

Input current is measured through an external sense resistor at CSSP and CSSN. The voltage at ISETIN also adjusts the input current limit. Full-scale input current is achieved when ISETIN is connected to REF, setting the full-scale current-sense voltage to 100mV.

When choosing the input current-sense resistor, note that the voltage drop across this resistor adds to the power loss, reducing efficiency. Reducing the voltage across the current-sense resistor may degrade input current limit accuracy due to the input offset of the input current-sense amplifier.

The input current error amplifier (GMS) is compensated at CCS. A 47nF capacitor at CCS provides suitable performance for most applications.

PWM Controller

The PWM controller drives the external MOSFETs to control the charging current or voltage. The input to the PWM controller is the lowest of CCI, CCV, or CCS. An internal clamp limits the noncontrolling signals to within 200mV of the controlling signal to prevent delay when switching between regulation loops.

Table 1. Charging State Conditions

STATE	ENTRY CONDITIONS	STATE CONDITIONS
Reset	From initial power on **or** From done state if battery voltage < recharge voltage threshold **or** V_{DCIN} - V_{BATT} < 100mV or V_{BATT} > battery overvoltage threshold	Timers reset, charging current = 0, $\overline{FASTCHG}$ = high, $\overline{FULLCHG}$ = high, $\overline{FAULT}$ = high
Prequalification	From reset state if input power, reference, and internal bias are within limits	Battery voltage ≤ undervoltage threshold, charging current = C/20, timeout = 7.5min typ (C_{TIMER1} = 1nF), $\overline{FASTCHG}$ = low, $\overline{FULLCHG}$ = high, $\overline{FAULT}$ = high
Fast Charge (Constant Current)	From prequalification state if battery voltage > undervoltage threshold	Undervoltage threshold ≤ battery voltage ≤ battery regulation voltage, charging current = current limit, timeout = 90min typ (C_{TIMER2} = 1nF), $\overline{FASTCHG}$ = low, $\overline{FULLCHG}$ = high, $\overline{FAULT}$ = high
Full Charge (Constant Voltage)	From fast-charge state if battery Voltage = battery regulation voltage	Battery voltage = battery regulation voltage, charging current ≤ current limit, timeout = 90min typ (C_{TIMER1} = 1nF), $\overline{FASTCHG}$ = high, $\overline{FULLCHG}$ = low, $\overline{FAULT}$ = high
Top-Off (Constant Voltage)	From full-charge state if full-charge timer expires **or** charging current ≤ 10% of current limit	Battery voltage = battery regulation voltage, charging current ≤ 10% of current limit, timeout = 45min typ (C_{TIMER1} = 1nF), $\overline{FASTCHG}$ = high, $\overline{FULLCHG}$ = high, $\overline{FAULT}$ = high
Done	From top-off state if top-off timer expires	Recharge voltage threshold ≤ battery voltage ≤ battery regulation voltage, charging current = 0, $\overline{FASTCHG}$ = high, $\overline{FULLCHG}$ = high, $\overline{FAULT}$ = high
Over/Under Temperature	From fast-charge state or full-charge state if battery temperature is outside of limits	Charge current = 0, timers suspended, $\overline{FASTCHG}$ = no change, $\overline{FULLCHG}$ = no change, FAULT = no change
Fault	From prequalification state if prequalification timer expires **or** From fast-charge state if fast-charge timer expires	Charging current = 0, $\overline{FASTCHG}$ = high, $\overline{FULLCHG}$ = high, $\overline{FAULT}$ = low

The current-mode PWM controller uses the inductor current to regulate the output voltage or current, simplifying stabilization of the regulation loops. Separate compensation of the regulation circuits allows each to be optimally stabilized. Internal slope compensation is included, ensuring stable operation over a wide range of duty cycles.

The controller drives an external N-channel MOSFET switch and a synchronous rectifier to step the input voltage down to the battery voltage. A bootstrap capacitor drives the high-side MOSFET gate to a voltage higher than the input source voltage. This capacitor (between BST and LX) is charged through a diode from VLO when the synchronous rectifier is on. The high-side MOSFET gate is driven from BST, supplying sufficient voltage to fully drive the MOSFET gate even when its source is near the input voltage. The synchronous rectifier is driven from DLO to behave like a diode, but with a smaller voltage drop for improved efficiency.

A built-in dead time (50ns typ) between switch and synchronous rectifier turn-on and turn-off prevents crowbar currents (currents that flow from the input voltage to ground due to both the MOSFET switch and synchronous rectifier being on simultaneously). This dead time may allow the body diode of the synchronous rectifier to conduct. If this happens, the resulting forward voltage and diode recovery time will cause a small loss of efficiency and increased power dissipation in the synchronous rectifier. To prevent the body diode from conducting, place an optional Schottky rectifier in parallel with the drain and source of the synchronous rectifier. The internal current-sense circuit turns off the synchronous rectifier when the inductor current drops to zero.

Timers

The MAX1737 includes safety timers to terminate charging and to ensure that faulty batteries are not charged indefinitely. TIMER1 and TIMER2 set the timeout periods.

TIMER1 controls the maximum prequalification time, maximum full-charge time, and the top-off time. TIMER2 controls the maximum fast-charge time. The timers are set by external capacitors. The typical times of 7.5 minutes for prequalification, 90 minutes for full charge, 45 minutes for top-off, and 90 minutes for fast charge are set by using a 1nF capacitor on TIMER1 and TIMER2 (Figure 1). The timers cannot be disabled.

Charge Monitoring Outputs

$\overline{\text{FASTCHG}}$, $\overline{\text{FULLCHG}}$, and $\overline{\text{FAULT}}$ are open-drain outputs that can be used as LED drivers. $\overline{\text{FASTCHG}}$ indicates the battery is being fast charged. $\overline{\text{FULLCHG}}$ indicates the charger has completed the fast-charge cycle (approximately 85% charge) and is operating in voltage mode. The $\overline{\text{FASTCHG}}$ and $\overline{\text{FULLCHG}}$ outputs can be tied together to indicate charging (see Figure 2). $\overline{\text{FAULT}}$ indicates the charger has detected a charging fault and that charging has terminated. The charger can be brought out of the FAULT condition by removing and reapplying the input power, or by pulling $\overline{\text{SHDN}}$ low.

Thermistor

The intent of THM is to inhibit fast-charging the cell when it is too cold or too hot (+2.5°C ≤ T_{OK} ≤ +47.5°C), using an external thermistor. THM time multiplexes two sense currents to test for both hot and cold qualification. The thermistor should be 10kΩ at +25°C and have a negative temperature coefficient (NTC); the THM pin expects 3.97kΩ at +47.5°C and 28.7kΩ at +2.5°C. Connect the thermistor between THM and GND. If no temperature qualification is desired, replace the thermistor with a 10kΩ resistor. Thermistors by Philips/BCcomponents (2322-640-63103), Cornerstone Sensors (T101D103-CA), and Fenwal Electronics (140-103LAG-RB1) work well. Charging pauses briefly (DHI and DLO are held Low for 800µs) to allow accurate temperature measurement . The battery voltage will have an undershoot when DHI and DLO stop switching during the temperature measurement. The battery voltage will have an overshoot when DHI and DLO resume switching after the temperature measurement.

Shutdown

When $\overline{\text{SHDN}}$ is pulled low, the MAX1737 enters the shutdown mode and charging is stopped. In shutdown, the internal resistive voltage-divider is removed from BATT to reduce the current drain on the battery to less than 1µA. DHI and DLO are low. However, the internal linear regulator (VLO) and the reference (REF) remain on. The status outputs $\overline{\text{FASTCHG}}$, $\overline{\text{FULLCHG}}$, and $\overline{\text{FAULT}}$ are high impedance. When exiting shutdown mode, the MAX1737 goes back to the power-on reset state, which resets the timers and begins a new charge cycle.

Source Undervoltage Shutdown (Dropout)

If the voltage on DCIN drops within 100mV of the voltage on BATT, the charger resets.

Table 2. Cell-Count Programming

CELL	CELL COUNT (N)
GND	1
Float	2
REF	3
VL	4

Design Procedure

Setting the Battery Regulation Voltage

VADJ sets the per-cell voltage limit. To set the VADJ voltage, use a resistor-divider from REF to GND. A GND-to-VREF change at VADJ results in a ±5% change in the battery limit voltage. Since the full VADJ range results in only a 10% change on the battery regulation voltage, the resistor-divider's accuracy need not be as high as the output voltage accuracy. Using 1% resistors for the voltage-dividers results in no more than 0.1% degradation in output voltage accuracy. VADJ is internally buffered so that high-value resistors can be used. Set V_{VADJ} by choosing a value less than 100kΩ for R8 and R9 (Figure 1) from VADJ to GND. The per-cell battery termination voltage is a function of the battery chemistry and construction; thus, consult the battery manufacturer to determine this voltage. Once the per-cell voltage limit battery regulation voltage is determined, the VADJ voltage is calculated by the equation:

$$V_{ADJ} = \left(\frac{9.5 \times V_{BATTR}}{N}\right) - (9.0 \times V_{REF})$$

where V_{BATTR} is N x the cell voltage. CELL is the programming input for selecting cell count N. Table 2 shows how CELL is connected to charge one to four cells.

Setting the Charging Current Limit

A resistor-divider from REF to GND sets the voltage at ISETOUT ($V_{ISETOUT}$). This voltage determines the charging current during the current-regulation fast-charge mode. The full-scale charging current (IFSI) is set by the current-sense resistor (R18, Figure 1) between CS and BATT. The full-scale current is IFSI = 0.2V / R18.

The charging current I_{CHG} is therefore:

$$I_{CHG} = I_{FSI}\frac{V_{ISETOUT}}{V_{REF}}$$

In choosing the current-sense resistor, note that the drop across this resistor causes further power loss, reducing efficiency. However, too low a value may degrade the accuracy of the charging current.

Setting the Input Current Limit

A resistor-divider from REF to GND can set the voltage at ISETIN (V_{ISETIN}). This sets the maximum source current allowed at any time during charging. The source current (I_{FSS}) is set by the current-sense resistor (R12, Figure 1) between CSSP and CSSN. The full-scale source current is I_{FSS} = 0.1V / R12.

The input current limit (I_{IN}) is therefore:

$$I_{IN} = I_{FSS}\frac{V_{ISETIN}}{V_{REF}}$$

Set ISETIN to REF to get the full-scale current limit. Short CSSP and CSSN to DCIN if the input source current limit is not used.

In choosing the current-sense resistor, note that the drop across this resistor causes further power loss, reducing efficiency. However, too low a resistor value may degrade input current limit accuracy.

Inductor Selection

The inductor value may be changed to achieve more or less ripple current. The higher the inductance, the lower the ripple current will be; however, as the physical size is kept the same, higher inductance typically will result in higher series resistance and lower saturation current. A good trade-off is to choose the inductor so that the ripple current is approximately 30% to 50% of the DC average charging current. The ratio of ripple current to DC charging current (LIR) can be used to calculate the optimal inductor value:

$$L = \frac{V_{BATT}(V_{DCIN(MAX)} - V_{BATT})}{V_{DCIN(MAX)} \times f \times I_{CHG} \times LIR}$$

where f is the switching frequency (300kHz).

The peak inductor current is given by:

$$I_{PEAK} = I_{CHG}\left(1 + \frac{LIR}{2}\right)$$

Capacitor Selection

The input capacitor absorbs the switching current from the charger input and prevents that current from circulating through the source, typically an AC wall cube. Thus, the input capacitor must be able to handle the input RMS current. Typically, at high charging currents, the converter will operate in continuous conduction (the inductor current does not go to 0). In this case, the RMS current of the input capacitor may be approximated by the equation:

$$I_{CIN} \approx I_{CHG}\sqrt{D - D^2}$$

where I_{CIN} = the input capacitor RMS current, D = PWM converter duty ratio (typically V_{BATT}/V_{DCIN}), and I_{CHG} = battery charging current.

The maximum RMS input current occurs at 50% duty cycle, so the worst-case input ripple current is 0.5 × I_{CHG}. If the input to output voltage ratio is such that the PWM controller will never work at 50% duty cycle, then the worst-case capacitor current will occur where the duty cycle is nearest 50%.

The impedance of the input capacitor is critical to preventing AC currents from flowing back into the wall cube. This requirement varies depending on the wall cube's impedance and the requirements of any conducted or radiated EMI specifications that must be met. Aluminum electrolytic capacitors are generally the least costly, but are usually a poor choice for portable devices due to their large size and low equivalent series resistance (ESR). Tantalum capacitors are better in most cases, as are high-value ceramic capacitors. For equivalent size and voltage rating, tantalum capacitors will have higher capacitance and ESR than ceramic capacitors. This makes it more critical to consider RMS current and power dissipation when using tantalum capacitors.

The output filter capacitor is used to absorb the inductor ripple current. The output capacitor impedance must be significantly less than that of the battery to ensure that it will absorb the ripple current. Both the capacitance and ESR rating of the capacitor are important for its effectiveness as a filter and to ensure stability of the PWM circuit. The minimum output capacitance for stability is:

$$C_{OUT} > \frac{V_{REF}\left(1+\frac{V_{BATT}}{V_{DCIN(MIN)}}\right)}{V_{BATT} \times f \times R_{CS}}$$

where C_{OUT} is the total output capacitance, V_{REF} is the reference voltage (4.2V), V_{BATT} is the maximum battery voltage (typically 4.2V per cell), and $V_{DCIN(MIN)}$ is the minimum source input voltage.

The maximum output capacitor ESR allowed for stability is:

$$R_{ESR} < \frac{R_{CS} \times V_{BATT}}{V_{REF}}$$

where R_{ESR} is the output capacitor ESR and R_{CS} is the current-sense resistor from CS to BATT.

Setting the Timers

The MAX1737 contains four timers: a prequalification timer, fast-charge timer, full-charge timer, and top-off timer. Connecting a capacitor from TIMER1 to GND and TIMER2 to GND sets the timer periods. The TIMER1 input controls the prequalification, full-charge, and top-off times, while TIMER2 controls fast-charge timeout. The typical timeouts for a 1C charge rate are set to 7.5 minutes for the prequalification timer, 90 minutes for the fast-charge timer, 90 minutes for the full-charge timer, and 45 minutes for the top-off timer by connecting a 1nF capacitor to TIMER1 and TIMER2. Each timer period is directly proportional to the capacitance at the corresponding pin. See the *Typical Operating Characteristics*.

Compensation

Each of the three regulation loops—the input current limit, the charging current limit, and the charging voltage limit—can be compensated separately using the CCS, CCI, and CCV pins, respectively.

The charge-current loop error amp output is brought out at CCI. Likewise, the source-current error amplifier output is brought out at CCS; 47nF capacitors to ground at CCI and CCS compensate the current loops in most charger designs. Raising the value of these capacitors reduces the bandwidth of these loops.

The voltage-regulating loop error amp output is brought out at CCV. Compensate this loop by connecting a capacitor in parallel with a series resistor-capacitor (RC) from CCV to GND. Recommended values are shown in Figure 1.

Applications Information

MOSFET Selection

The MAX1737 uses a dual N-channel external power MOSFET switch to convert the input voltage to the charging current or voltage. The MOSFET must be selected to meet the efficiency and power-dissipation requirements of the charging circuit, as well as the temperature rise of the MOSFETs. The MOSFET characteristics that affect the power dissipation are the drain-source on-resistance ($R_{DS(ON)}$) and the gate charge. In general, these are inversely proportional.

To determine the MOSFET power dissipation, the operating duty cycle must first be calculated. When the charger is operating at higher currents, the inductor current will be continuous (the inductor current will not drop to 0A) and, in this case, the high-side MOSFET duty cycle (D) can be approximated by the equation:

$$D \approx \frac{V_{BATT}}{V_{DCIN}}$$

and the synchronous-rectifier MOSFET duty cycle (D′) will be 1 - D or:

$$D' \approx \frac{V_{DCIN} - V_{BATT}}{V_{DCIN}}$$

For the high-side switch, the worst-case power dissipation due to on-resistance occurs at the minimum source voltage $V_{DCIN(MIN)}$ and the maximum battery voltage $V_{BATT(MAX)}$, and can be approximated by the equation:

$$P_R \approx \frac{V_{BATT(MAX)}}{V_{DCIN(MIN)}} \times R_{DS(ON)} \times I_{CHG}2$$

The transition loss can be approximated by the equation:

$$P_T \approx \frac{V_{DCIN} \times I_{CHG} \times f \times t_{TR}}{3}$$

where tTR is the MOSFET transition time. So the total power dissipation of the high-side switch is P_{TOT} = PR + PT.

The worst-case synchronous-rectifier power occurs at the minimum battery voltage $V_{BATT(MIN)}$ and the maximum source voltage $V_{DC(MAX)}$, and can be approximated by:

$$P_{DL} \approx \frac{V_{DCIN(MAX)} - V_{BATT(MIN)}}{V_{DCIN(MAX)}} \times R_{DS(ON)} \times I_{CHG}2$$

There is a brief dead time where both the high-side switch and synchronous rectifier are off. This prevents crowbar currents that flow directly from the source voltage to ground. During the dead time, the inductor current will turn on the synchronous-rectifier MOSFET body diode, which may degrade efficiency. To prevent this, connect a Schottky rectifier across the drain source of the synchronous rectifier to stop the body diode from conducting. The Schottky rectifier may be omitted, typically degrading the efficiency by approximately 1% to 2%, causing a corresponding increase in the low-side synchronous-rectifier power dissipation.

VL and REF Bypassing

The MAX1737 uses an internal linear regulator to drop the input voltage down to 5.4V, which powers the internal circuitry. The output of the linear regulator is the VL pin. The internal linear regulator may also be used to power external circuitry as long as the maximum current and power dissipation of the linear regulator are not exceeded. The synchronous-rectifier MOSFET gate driver (DLO) is powered from VLO. An internal 12Ω resistor from VL to VLO provides the DC current to power the gate driver. Bypass VLO to PGND with a 0.1µF or greater capacitor.

A 4.7µF bypass capacitor is required at VL to ensure that the regulator is stable. A 1µF bypass capacitor is also required between REF and GND to ensure that the internal 4.2V reference is stable. In both cases use a low-ESR ceramic capacitor.

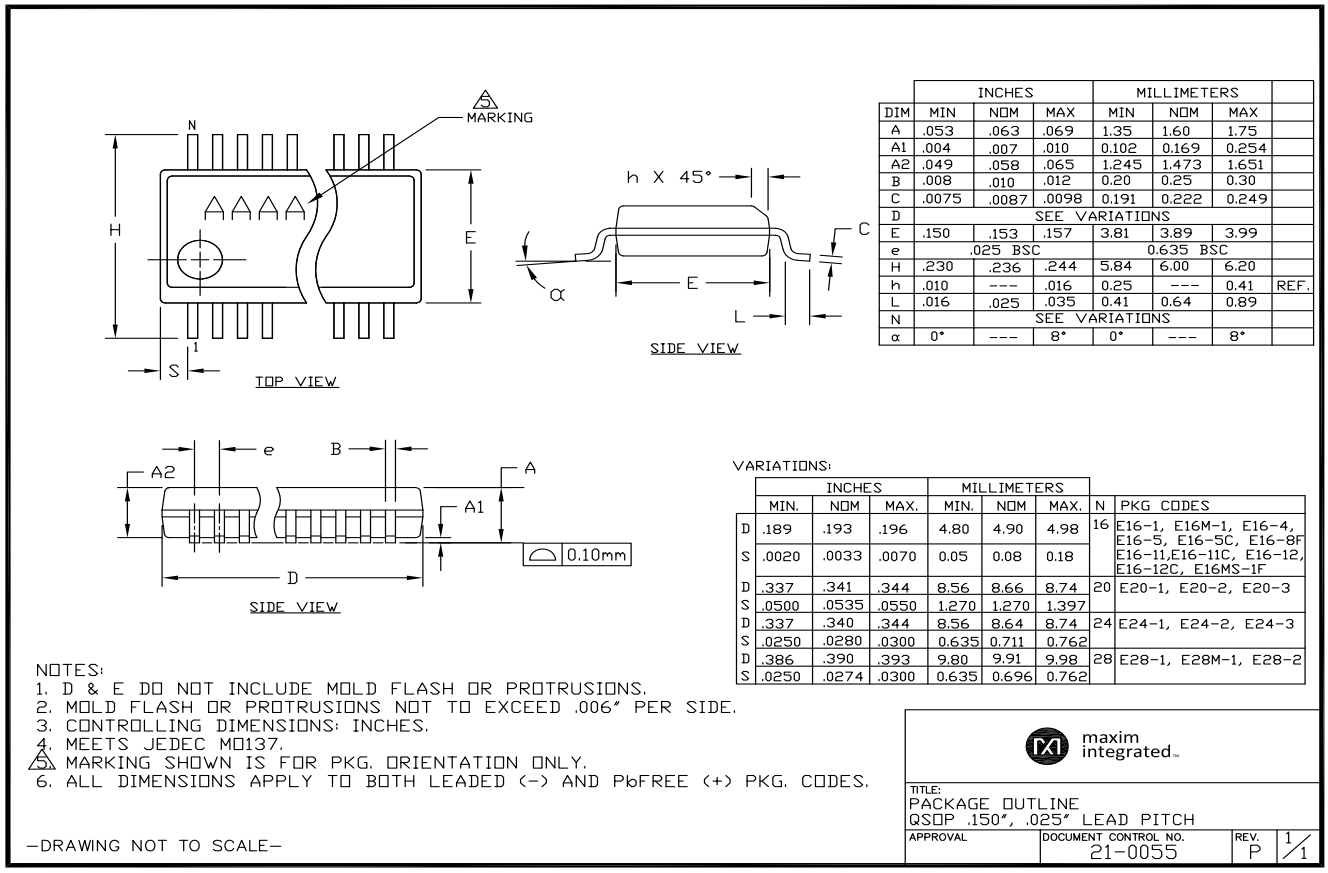
Chip Information

TRANSISTOR COUNT: 5978

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
28 QSOP	E28+1	21-0055	90-0173



DIM	INCHES MIN	INCHES NOM	INCHES MAX	MILLIMETERS MIN	MILLIMETERS NOM	MILLIMETERS MAX	
A	.053	.063	.069	1.35	1.60	1.75	
A1	.004	.007	.010	0.102	0.169	0.254	
A2	.049	.058	.065	1.245	1.473	1.651	
B	.008	.010	.012	0.20	0.25	0.30	
C	.0075	.0087	.0098	0.191	0.222	0.249	
D	SEE VARIATIONS						
E	.150	.153	.157	3.81	3.89	3.99	
e	.025 BSC			0.635 BSC			
H	.230	.236	.244	5.84	6.00	6.20	
h	.010	---	.016	0.25	---	0.41	REF.
L	.016	.025	.035	0.41	0.64	0.89	
N	SEE VARIATIONS						
α	0°	---	8°	0°	---	8°	

VARIATIONS:

	INCHES MIN.	INCHES NOM	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS NOM	MILLIMETERS MAX.	N	PKG CODES
D	.189	.193	.196	4.80	4.90	4.98	16	E16-1, E16M-1, E16-4, E16-5, E16-5C, E16-8F E16-11,E16-11C, E16-12, E16-12C, E16MS-1F
S	.0020	.0033	.0070	0.05	0.08	0.18		
D	.337	.341	.344	8.56	8.66	8.74	20	E20-1, E20-2, E20-3
S	.0500	.0535	.0550	1.270	1.270	1.397		
D	.337	.340	.344	8.56	8.64	8.74	24	E24-1, E24-2, E24-3
S	.0250	.0280	.0300	0.635	0.711	0.762		
D	.386	.390	.393	9.80	9.91	9.98	28	E28-1, E28M-1, E28-2
S	.0250	.0274	.0300	0.635	0.696	0.762		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. CONTROLLING DIMENSIONS: INCHES.
4. MEETS JEDEC MO137.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

maxim integrated

TITLE:
PACKAGE OUTLINE
QSOP .150", .025" LEAD PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0055	P	1/1

Note: *The MAX1737EEI is a 28-pin QSOP and does not have a heat slug.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
4	5/09	Initial release	1, 9, 18
5	7/17	Replaced Figure 4 and added information to *Thermistor* section	12, 14

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- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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