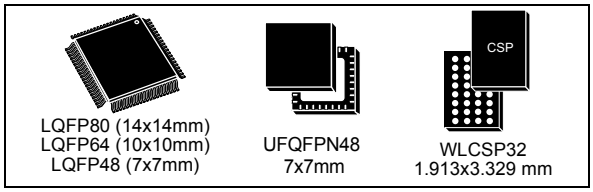
# STM8L151x6/8 STM8L152x6/8

## 8-bit ultra-low-power MCU, up to 64-KB Flash, 2-KB data EEPROM, RTC, LCD, timers, USARTs, I2C, SPIs, ADC, DAC, comparators

**Datasheet - production data**

## Features

- Operating conditions
  - Operating power supply: 1.65 to 3.6 V (without BOR), 1.8 to 3.6 V (with BOR)
  - Temp. range: -40 to 85, 105 or 125 °C
- Low-power features
  - 5 low-power modes: Wait, Low-power run (5.9 µA), Low-power wait (3 µA), Active-halt with full RTC (1.4 µA), Halt (400 nA)
  - Consumption: 200 µA/MHz+330 µA
  - Fast wake up from Halt mode (4.7 µs)
  - Ultra low leakage per I/0: 50 nA
- Advanced STM8 core
  - Harvard architecture and 3-stage pipeline
  - Max freq: 16 MHz, 16 CISC MIPS peak
  - Up to 40 external interrupt sources
- Reset and supply management
  - Low-power, ultra safe BOR reset with five programmable thresholds
  - Ultra-low-power POR/PDR
  - Programmable voltage detector (PVD)
- Clock management
  - 32 kHz and 1-16 MHz crystal oscillators
  - Internal 16 MHz factory-trimmed RC and 38 kHz low consumption RC
  - Clock security system
- Low-power RTC
  - BCD calendar with alarm interrupt
  - Digital calibration with +/- 0.5ppm accuracy
  - Advanced anti-tamper detection
- LCD: 8x40 or 4x44 w/ step-up converter
- DMA
  - 4 ch. for ADC, DACs, SPIs, I$^2$C, USARTs, Timers, 1 ch. for memory-to-memory
- 2x12-bit DAC (dual mode) with output buffer
- 12-bit ADC up to 1 Msps/28 channels
  - Temp. sensor and internal ref. voltage




LQFP80 (14x14mm)
LQFP64 (10x10mm)
LQFP48 (7x7mm)

UFQFPN48
7x7mm

WLCSP32
1.913x3.329 mm

- Memories
  - Up to 64-Kbytes of Flash memory with up to 2 Kbytes of data EEPROM with ECC and RWW
  - Flexible write/read protection modes
  - Up to 4 Kbytes of RAM
- 2 ultra-low-power comparators
  - 1 with fixed threshold and 1 rail to rail
  - Wake up capability
- Timers
  - Three 16-bit timers with 2 channels (IC, OC, PWM), quadrature encoder
  - One 16-bit advanced control timer with 3 channels, supporting motor control
  - One 8-bit timer with 7-bit prescaler
  - One window, one independent watchdog
  - Beeper timer with 1, 2 or 4 kHz frequencies
- Communication interfaces
  - Two synchronous serial interface (SPI)
  - Fast I$^2$C 400 kHz SMBus and PMBus
  - Three USARTs (ISO 7816 interface + IrDA)
- Up to 67 I/Os, all mappable on interrupt vectors
- Up to 16 capacitive sensing channels supporting touchkey, proximity, linear touch and rotary touch sensors
- Fast on-chip programming and non-intrusive debugging with SWIM, Bootloader using USART
- 96-bit unique ID



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**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM8L151x6/8 | STM8L151R6, STM8L151C8, STM8L151M8, STM8L151R8 |
| STM8L152x6/8 | STM8L152R6, STM8L152C8, STM8L152K8, STM8L152M8, STM8L152R8 |

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# 1 Introduction

This document describes the features, pinout, mechanical data and ordering information for: devices.

- **High-density STM8L15xxx devices:** STM8L151x8 and STM8L152x8 microcontrollers with a Flash memory density of 64 Kbyte.
- **Medium+ density STM8L15xxx devices**: STM8L151R6 and STM8L152R6 microcontrollers with Flash memory density of 32 Kbyte.

For further details on the STMicroelectronics ultra-low-power family please refer to *Section 2.3: Ultra-low-power continuum on page 13*.

For detailed information on device operation and registers, refer to the reference manual (RM0031).

For information on to the Flash program memory and data EEPROM, refer to the programming manual (PM0054).

For information on the debug module and SWIM (single wire interface module), refer to the STM8 SWIM communication protocol and debug module user manual (UM0470).

For information on the STM8 core, refer to the STM8 CPU programming manual (PM0044).

# 2 Description

The high-density and medium+ density STM8L15xx6/8 ultra-low-power devices feature an enhanced STM8 CPU core providing increased processing power (up to 16 MIPS at 16 MHz) while maintaining the advantages of a CISC architecture with improved code density, a 24-bit linear addressing space and an optimized architecture for low-power operations.

The family includes an integrated debug module with a hardware interface (SWIM) which allows non-intrusive in-application debugging and ultrafast Flash programming.

All high-density and medium+ density STM8L15xx6/8 microcontrollers feature embedded data EEPROM and low-power low-voltage single-supply program Flash memory.

The devices incorporate an extensive range of enhanced I/Os and peripherals, a 12-bit ADC, two DACs, two comparators, a real-time clock, four 16-bit timers, one 8-bit timer, as well as standard communication interfaces such as two SPIs, an $I^2C$ interface, and three USARTs. A 8x40 or 4x44-segment LCD is available on the STM8L152x8 devices. The modular design of the peripheral set allows the same peripherals to be found in different ST microcontroller families including 32-bit families. This makes any transition to a different family very easy, and simplified even more by the use of a common set of development tools.

## 2.1 STM8L ultra-low-power 8-bit family benefits

High-density and medium+ density STM8L15xx6/8 devices are part of the STM8L ultra-low-power family providing the following benefits:

- Integrated system
  - Up to 64 Kbyte of high-density embedded Flash program memory
  - Up to 2 Kbyte of data EEPROM
  - Up to 4 Kbyte of RAM
  - Internal high-speed and low-power low speed RC.
  - Embedded reset
- ultra-low-power consumption
  - 1 µA in Active-halt mode
  - Clock gated system and optimized power management
  - Capability to execute from RAM for Low-power wait mode and Low-power run mode
- Advanced features
  - Up to 16 MIPS at 16 MHz CPU clock frequency
  - Direct memory access (DMA) for memory-to-memory or peripheral-to-memory access.
- Short development cycles
  - Application scalability across a common family product architecture with compatible pinout, memory map and modular peripherals.
  - Wide choice of development tools

STM8L ultra-low-power microcontrollers can operate either from 1.8 to 3.6 V (down to 1.65 V at power-down) or from 1.65 to 3.6 V. They are available in the -40 to +85 °C and -40 to +125 °C temperature ranges.

These features make the STM8L ultra-low-power microcontroller families suitable for a wide range of applications:

- Medical and handheld equipment
- Application control and user interface
- PC peripherals, gaming, GPS and sport equipment
- Alarm systems, wired and wireless sensors
- Metering

The devices are offered in five different packages from 32 to 80 pins. Different sets of peripherals are included depending on the device. Refer to *Section 3* for an overview of the complete range of peripherals proposed in this family.

All STM8L ultra-low-power products are based on the same architecture with the same memory mapping and a coherent pinout.

*Figure 1* shows the block diagram of the High-density and medium+ density STM8L15xx6/8 families.

## 2.2 Device overview

**Table 2. High-density and medium+ density STM8L15xx6/8 low power device features and peripheral counts**

| Features | | STM8L15xC8 | STM8L15xK8 | STM8L15xR8 | STM8L15xM8 | STM8L15xR6 |
|---|---|---|---|---|---|---|
| Flash (Kbyte) | | 64 | 64 | 64 | 64 | 32 |
| Data EEPROM (Kbyte) | | 2 | 2 | 2 | 2 | 1 |
| RAM (Kbyte) | | 4 | 4 | 4 | 4 | 2 |
| LCD | | 8x24 or 4x28(1) | 4x15(1) | 8x36 or 4x40(1) | 8x40 or 4x44(1) | 8x36 or 4x40(1) |
| Timers | Basic | 1 (8-bit) | 1 (8-bit) | 1 (8-bit) | 1 (8-bit) | 1 (8-bit) |
| | General purpose | 3 (16-bit) | 3 (16-bit) | 3 (16-bit) | 3 (16-bit) | 3 (16-bit) |
| | Advanced control | 1 (16-bit) | 1 (16-bit) | 1 (16-bit) | 1 (16-bit) | 1 (16-bit) |
| Communication interfaces | SPI | 2 | 1 | 2 | 2 | 2 |
| | I2C | 1 | 1 | 1 | 1 | 1 |
| | USART | 3 | 2 | 3 | 3 | 3 |
| GPIOs | | 41(2) | 28(2) | 54(2) | 68(2) | 54(2) |
| 12-bit synchronized ADC (number of channels) | | 1 (25) | 1 (18) | 1 (28) | 1 (28) | 1 (28) |
| 12-Bit DAC<br>Number of channels | | 2<br>2 | 1<br>1 | 2<br>2 | 2<br>2 | 2<br>2 |
| Comparators (COMP1/COMP2) | | 2 | 2 | 2 | 2 | 2 |
| Others | | RTC, window watchdog, independent watchdog, 16-MHz and 38-kHz internal RC, 1- to 16-MHz and 32-kHz external oscillator | | | | |
| CPU frequency | | 16 MHz | | | | |
| Operating voltage | | 1.8 to 3.6 V (down to 1.65 V at power-down) with BOR<br>1.65 to 3.6 V without BOR | | | | |
| Operating temperature | | –40 to +85 °C / –40 to +105 °C / –40 to +125 °C | | | | |
| Packages | | UFQFPN48<br>LQFP48 | WLCSP32 | LQFP64 | LQFP80 | LQFP64 |

1. STM8L152x6/8 versions only.
2. The number of GPIOs given in this table includes the NRST/PA1 pin but the application can use the NRST/PA1 pin as general purpose output only (PA1).

## 2.3 Ultra-low-power continuum

The ultra-low-power STM8L151x6/8, STM8L152x6/8 and STM8L162x8 are fully pin-to-pin, software and feature compatible. Besides the full compatibility within the family, the devices are part of STMicroelectronics microcontrollers ultra-low-power strategy which also includes STM8L101 line, STM8L151/152 lines, and STM8L162 line. The STM8L and STM32L families allow a continuum of performance, peripherals, system architecture, and features.

They are all based on STMicroelectronics 0.13 µm ultra low-leakage process.

*Note: 1 The STM8L151xx and STM8L152xx are pin-to-pin compatible with STM8L101xx devices.*

*2 The STM32L family is pin-to-pin compatible with the general purpose STM32F family. Please refer to STM32Lxxxxx documentation for more information on these devices.*

### Performance

All families incorporate highly energy-efficient cores with both Harvard architecture and pipelined execution: advanced STM8 core for STM8L families and ARM® Cortex®-M3 core for STM32L family. In addition specific care for the design architecture has been taken to optimize the mA/DMIPS and mA/MHz ratios.

This allows the ultra-low-power performance to range from 5 up to 33.3 DMIPs.

### Shared peripherals

STM8L15xx6/8 and STM32Lxxxxx share identical peripherals which ensure a very easy migration from one family to another:

- Analog peripherals: ADC1, DAC1/DAC2, and comparators COMP1/COMP2
- Digital peripherals: RTC and some communication interfaces

### Common system strategy

To offer flexibility and optimize performance, the STM8L15xx6/8 and STM32Lxxxxx devices use a common architecture:

- Same power supply range from 1.65 to 3.6 V. For STM8L101xx and medium-density STM8L15xxx, the power supply must be above 1.8 V at power-on, and go below 1.65 V at power-down.
- Architecture optimized to reach ultra low consumption both in low-power modes and Run mode
- Fast startup strategy from low-power modes
- Flexible system clock
- Ultra safe reset: same reset strategy for both STM8L15xx6/8 and STM32Lxxxxx including power-on reset, power-down reset, brownout reset and programmable voltage detector.

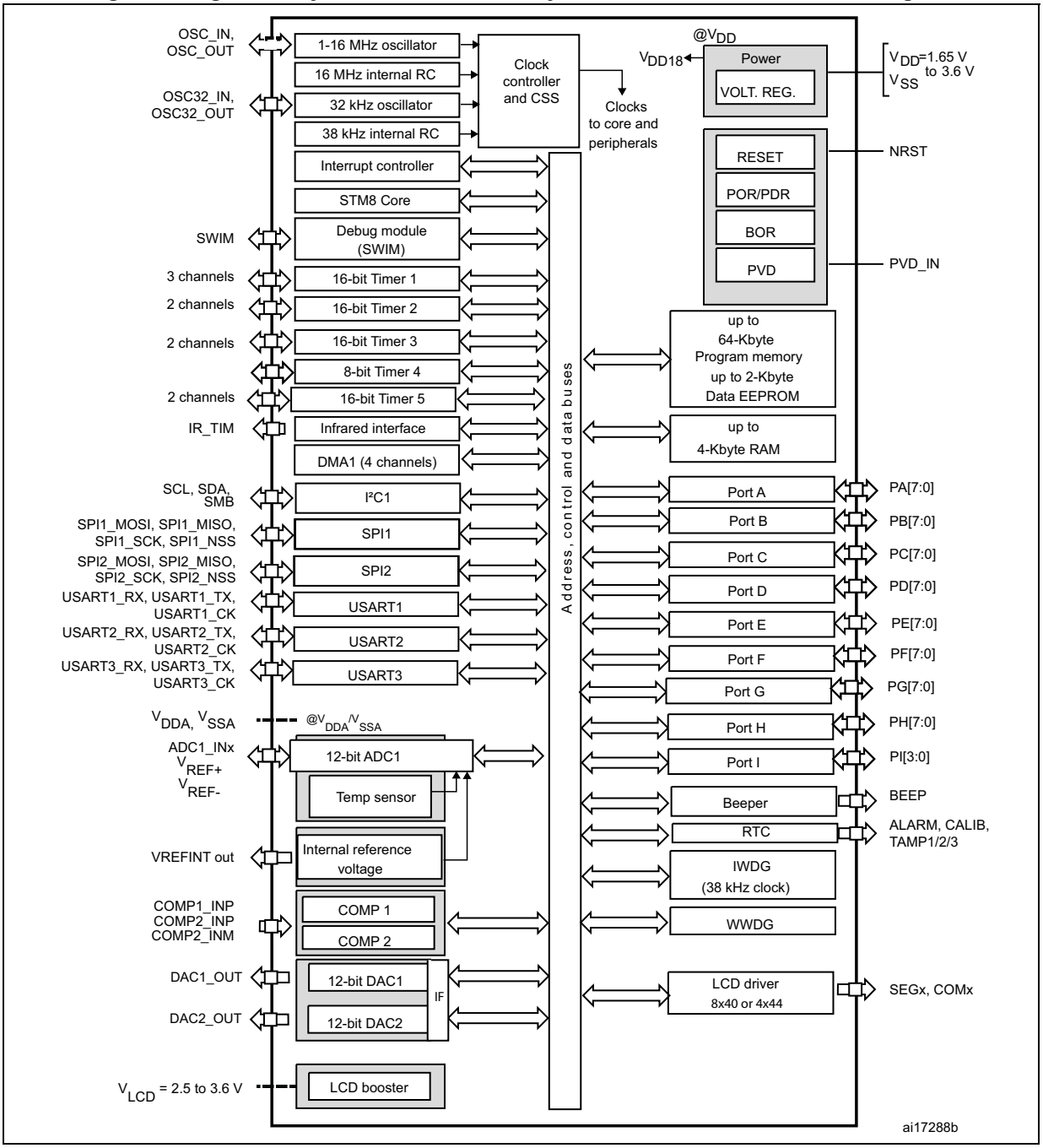
### Features

STMicroelectronics ultra-low-power continuum also lies in feature compatibility:

- More than 10 packages with pin counts from 20 to 100 pins and size down to 3 x 3 mm
- Memory density ranging from 4 to 128 Kbyte

# 3 Functional overview

**Figure 1. High-density and medium+ density STM8L15xx6/8 device block diagram**




1. **Legend**:
   AF: alternate function
   ADC: Analog-to-digital converter
   BOR: Brownout reset
   DMA: Direct memory access
   DAC: Digital-to-analog converter
   I²C: Inter-integrated circuit multimaster interface
   IWDG: Independent watchdog

LCD: Liquid crystal display
POR/PDR: Power on reset / power-down reset
RTC: Real-time clock
SPI: Serial peripheral interface
SWIM: Single wire interface module
USART: Universal synchronous asynchronous receiver transmitter
WWDG: Window watchdog

## 3.1 Low-power modes

The high-density and medium+ density STM8L15xx6/8 devices support five low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Wait mode**: CPU clock is stopped, but selected peripherals keep running. An internal or external interrupt or a Reset can be used to exit the microcontroller from Wait mode (WFE or WFI mode).
- **Low-power run mode**: The CPU and the selected peripherals are running. Execution is done from RAM with a low speed oscillator (LSI or LSE). Flash memory and data EEPROM are stopped and the voltage regulator is configured in ultra-low-power mode. The microcontroller enters Low-power run mode by software and can exit from this mode by software or by a reset.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Low-power wait mode:** This mode is entered when executing a Wait for event in Low-power run mode. It is similar to Low-power run mode except that the CPU clock is stopped. The wakeup from this mode is triggered by a Reset or by an internal or external event (peripheral event generated by the timers, serial interfaces, DMA controller (DMA1), comparators and I/O ports). When the wakeup is triggered by an event, the system goes back to Low-power run mode.
  All interrupts must be masked. They cannot be used to exit the microcontroller from this mode.
- **Active-halt mode**: CPU and peripheral clocks are stopped, except RTC. The wakeup can be triggered by RTC interrupts, external interrupts or reset.
- **Halt mode**: CPU and peripheral clocks are stopped, the device remains powered on. The RAM content is preserved. The wakeup is triggered by an external interrupt or reset. A few peripherals have also a wakeup from Halt capability. Switching off the internal reference voltage reduces power consumption. Through software configuration it is also possible to wake up the device without waiting for the internal reference voltage wakeup time to have a fast wakeup time of 5 µs.

## 3.2 Central processing unit STM8

### 3.2.1 Advanced STM8 Core

The 8-bit STM8 core is designed for code efficiency and performance with an Harvard architecture and a 3-stage pipeline.

It contains 6 internal registers which are directly addressable in each execution context, 20 addressing modes including indexed indirect and relative addressing, and 80 instructions.

#### Architecture and registers

- Harvard architecture
- 3-stage pipeline
- 32-bit wide program memory bus - single cycle fetching most instructions
- X and Y 16-bit index registers - enabling indexed addressing modes with or without offset and read-modify-write type data manipulations
- 8-bit accumulator
- 24-bit program counter - 16 Mbyte linear memory space
- 16-bit stack pointer - access to a 64 Kbyte level stack
- 8-bit condition code register - 7 condition flags for the result of the last instruction

#### Addressing

- 20 addressing modes
- Indexed indirect addressing mode for lookup tables located anywhere in the address space
- Stack pointer relative addressing mode for local variables and parameter passing

#### Instruction set

- 80 instructions with 2-byte average instruction size
- Standard data movement and logic/arithmetic functions
- 8-bit by 8-bit multiplication
- 16-bit by 8-bit and 16-bit by 16-bit division
- Bit manipulation
- Data transfer between stack and accumulator (push/pop) with direct stack access
- Data transfer using the X and Y registers or direct memory-to-memory transfers

### 3.2.2 Interrupt controller

The high-density and medium+ density STM8L15xx6/8x devices feature a nested vectored interrupt controller:

- Nested interrupts with 3 software priority levels
- 32 interrupt vectors with hardware priority
- Up to 40 external interrupt sources on 11 vectors
- Trap and reset interrupts

## 3.3 Reset and supply management

### 3.3.1 Power supply scheme

The device requires a 1.65 V to 3.6 V operating supply voltage ($V_{DD}$). The external power supply pins must be connected as follows:

- $V_{SS1}$, $V_{DD1}$, $V_{SS2}$, $V_{DD2}$, $V_{SS3}$, $V_{DD3}$, $V_{SS4}$, $V_{DD4}$= 1.65 to 3.6 V: external power supply for I/Os and for the internal regulator. Provided externally through $V_{DD}$ pins, the corresponding ground pin is $V_{SS}$. $V_{SS1}$/$V_{SS2}$/$V_{SS3}$/$V_{SS4}$ and $V_{DD1}$/$V_{DD2}$/$V_{DD3}$/$V_{DD4}$ must not be left unconnected.
- $V_{SSA}$, $V_{DDA}$ = 1.65 to 3.6 V: external power supplies for analog peripherals (minimum voltage to be applied to $V_{DDA}$ is 1.8 V when the ADC1 is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{REF+}$, $V_{REF-}$ (for ADC1): external reference voltage for ADC1. Must be provided externally through $V_{REF+}$ and $V_{REF-}$ pin.
- $V_{REF+}$ (for DAC1/2): external voltage reference for DAC1 and DAC2 must be provided externally through $V_{REF+}$.

### 3.3.2 Power supply supervisor

The device has an integrated ZEROPOWER power-on reset (POR)/power-down reset (PDR). For the device sales types without the “D” option (see *Section 11: Ordering information*), it is coupled with a brownout reset (BOR) circuitry. It that case the device operates between 1.8 and 3.6 V, BOR is always active and ensures proper operation starting from 1.8 V. After the 1.8 V BOR threshold is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently (in which case, the $V_{DD}$ min. value at power-down is 1.65 V).

Five BOR thresholds are available through option bytes, starting from 1.8 V to 3 V. To reduce the power consumption in Halt mode, it is possible to automatically switch off the internal reference voltage (and consequently the BOR) in Halt mode. The device remains in reset state when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$ or $V_{BOR}$, without the need for any external reset circuit.

*Note: For device sales types with the “D” option (see Section 11: Ordering information) BOR is permanently disabled and the device operates between 1.65 and 3.6 V. In this case it is not possible to enable BOR through the option bytes.*

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}$/$V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. This PVD offers 7 different levels between 1.85 V and 3.05 V, chosen by software, with a step around 200 mV. An interrupt can be generated when $V_{DD}$/$V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}$/$V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

### 3.3.3 Voltage regulator

The high-density and medium+ density STM8L15xx6/8 devices embed an internal voltage regulator for generating the 1.8 V power supply for the core and peripherals.

This regulator has two different modes:

- Main voltage regulator mode (MVR) for Run, Wait for interrupt (WFI) and Wait for event (WFE) modes.
- Low-power voltage regulator mode (LPVR) for Halt, Active-halt, Low-power run and Low-power wait modes.

When entering Halt or Active-halt modes, the system automatically switches from the MVR to the LPVR in order to reduce current consumption.

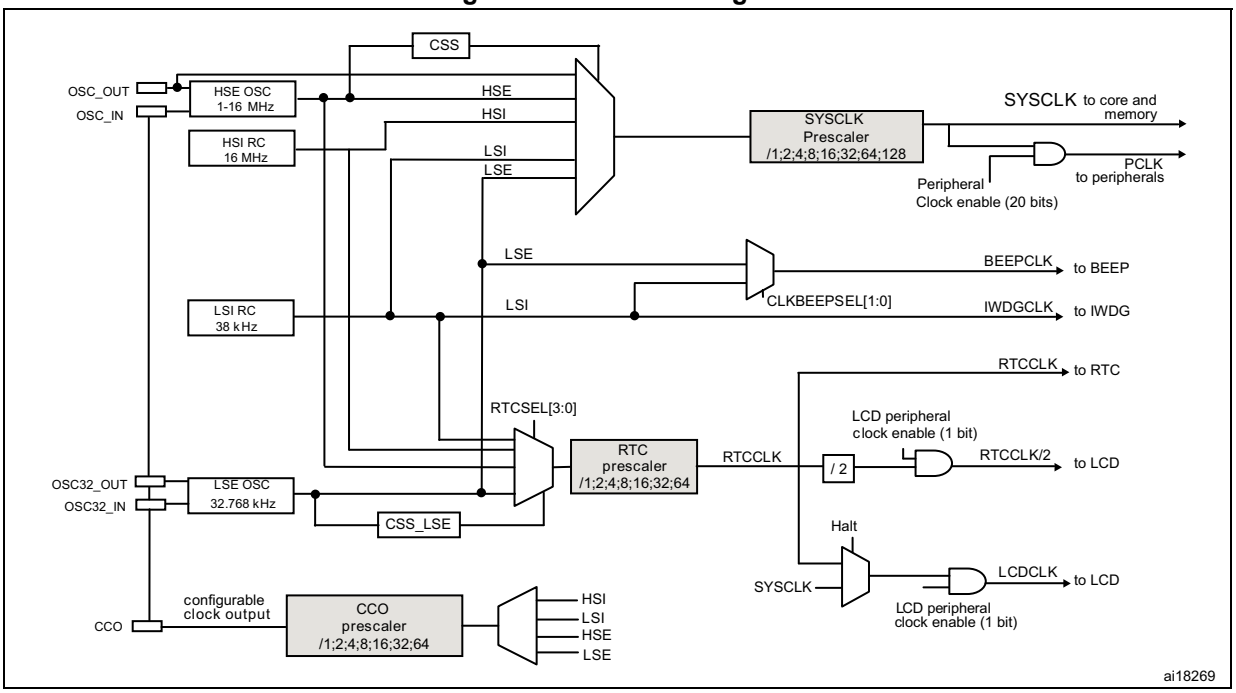
## 3.4 Clock management

The clock controller distributes the system clock (SYSCLK) coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

### Features

- **Clock prescaler:** to get the best compromise between speed and current consumption the clock frequency to the CPU and peripherals can be adjusted by a programmable prescaler
- **Safe clock switching:** Clock sources can be changed safely on the fly in run mode through a configuration register.
- **Clock management:** To reduce power consumption, the clock controller can stop the clock to the core, individual peripherals or memory.
- **System clock sources:** 4 different clock sources can be used to drive the system clock:
  - 1-16 MHz High speed external crystal (HSE)
  - 16 MHz High speed internal RC oscillator (HSI)
  - 32.768 Low speed external crystal (LSE) available on STM8L151xx and STM8L152xx devices
  - 38 kHz Low speed internal RC (LSI)
- **RTC and LCD clock sources:** the above four sources can be chosen to clock the RTC and the LCD, whatever the system clock.
- **Startup clock:** After reset, the microcontroller restarts by default with an internal 2 MHz clock (HSI/8). The prescaler ratio and clock source can be changed by the application program as soon as the code execution starts.
- **Clock security system (CSS):** This feature can be enabled by software. If a HSE clock failure occurs, the system clock is automatically switched to HSI.
- **Configurable main clock output (CCO):** This outputs an external clock for use by the application.

**Figure 2. Clock tree diagram**




## 3.5 Low-power real-time clock

The real-time clock (RTC) is only available on STM8L151xx and STM8L152xx devices.

The real-time clock (RTC) is an independent binary coded decimal (BCD) timer/counter.

Six byte locations contain the second, minute, hour (12/24 hour), week day, date, month, year, in BCD (binary coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day months are made automatically. The subsecond field can also be read in binary format.

The calendar can be corrected from 1 to 32767 RTC clock pulses. This allows to make a synchronization to a master clock.

The RTC offers a digital calibration which allows an accuracy of +/-0.5 ppm.

It provides a programmable alarm and programmable periodic interrupts with wakeup from Halt capability.

- Periodic wakeup time using the 32.768 kHz LSE with the lowest resolution (of 61 µs) is from min. 122 µs to max. 3.9 s. With a different resolution, the wakeup time can reach 36 hours
- Periodic alarms based on the calendar can also be generated from LSE period to every year

A clock security system detects a failure on LSE, and can provide an interrupt with wakeup capability. The RTC clock can automatically switch to LSI in case of LSE failure.

The RTC also provides 3 anti-tamper detection pins. This detection embeds a programmable filter and can wakeup the MCU.

## 3.6 LCD (Liquid crystal display)

The LCD is only available on STM8L152x6/8 devices.

The liquid crystal display drives up to 8 common terminals and up to 40 segment terminals to drive up to 320 pixels. It can also be configured to drive up to 4 common and 44 segments (up to 176 pixels).

- Internal step-up converter to guarantee contrast control whatever $V_{DD}$.
- Static 1/2, 1/3, 1/4, 1/8 duty supported.
- Static 1/2, 1/3, 1/4 bias supported.
- Phase inversion to reduce power consumption and EMI.
- Up to 8 pixels which can programmed to blink.
- The LCD controller can operate in Halt mode.

*Note: Unnecessary segments and common pins can be used as general I/O pins.*

## 3.7 Memories

The high-density and medium+ density STM8L15xx6/8 devices have the following main features:

- Up to 4 Kbyte of RAM
- The non-volatile memory is divided into three arrays:
  - Up to 64 Kbyte of medium-density embedded Flash program memory
  - Up to 2 Kbyte of Data EEPROM
  - Option bytes.

The EEPROM embeds the error correction code (ECC) feature. It supports the read-while-write (RWW): it is possible to execute the code from the program matrix while programming/erasing the data matrix.

The option byte protects part of the Flash program memory from write and readout piracy.

## 3.8 DMA

A 4-channel direct memory access controller (DMA1) offers a memory-to-memory and peripherals-from/to-memory transfer capability. The 4 channels are shared between the following IPs with DMA capability: ADC1, DAC1,DAC2, I2C1, SPI1, SPI2, USART1, USART2, USART3, and the 5 Timers.

## 3.9 Analog-to-digital converter

- 12-bit analog-to-digital converter (ADC1) with 28 channels (including 4 fast channel), temperature sensor and internal reference voltage
- Conversion time down to 1 µs with $f_{SYSCLK}$= 16 MHz
- Programmable resolution
- Programmable sampling time
- Single and continuous mode of conversion
- Scan capability: automatic conversion performed on a selected group of analog inputs
- Analog watchdog: interrupt generation when the converted voltage is outside the programmed threshold
- Triggered by timer

*Note: ADC1 can be served by DMA1.*

## 3.10 Digital-to-analog converter

- 12-bit DAC with 2 buffered outputs (two digital signals can be converted into two analog voltage signal outputs)
- Synchronized update capability using timers
- DMA capability for each channel
- External triggers for conversion
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channels with independent or simultaneous conversions
- Input reference voltage $V_{REF+}$ for better resolution

*Note: DAC can be served by DMA1.*

## 3.11 Ultra-low-power comparators

The high-density and medium+ density STM8L15xx6/8 devices embed two comparators (COMP1 and COMP2) sharing the same current bias and voltage reference. The voltage reference can be internal or external (coming from an I/O).

- One comparator with fixed threshold (COMP1).
- One comparator rail to rail with fast or slow mode (COMP2). The threshold can be one of the following:
  - DAC output
  - External I/O
  - Internal reference voltage or internal reference voltage submultiple (1/4, 1/2, 3/4)

The two comparators can be used together to offer a window function. They can wake up from Halt mode.

## 3.12 System configuration controller and routing interface

The system configuration controller provides the capability to remap some alternate functions on different I/O ports. TIM4 and ADC1 DMA channels can also be remapped.

The highly flexible routing interface allows application software to control the routing of different I/Os to the TIM1 timer input captures. It also controls the routing of internal analog signals to ADC1, COMP1, COMP2, DAC1 and the internal reference voltage $V_{REFINT}$. It also provides a set of registers for efficiently managing the charge transfer acquisition sequence (see *Section 3.13: Touch sensing*).

## 3.13 Touch sensing

The high-density and medium+ density STM8L15xx6/8 devices provide a simple solution for adding capacitive sensing functionality to any application. Capacitive sensing technology is able to detect finger presence near an electrode which is protected from direct touch by a dielectric (for example glass or plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the electrode capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. In the high-density and medium+ density STM8L15xx6/8 devices, the acquisition sequence is managed by software and it involves analog I/O groups and the routing interface.

Reliable touch sensing solution can be quickly and easily implemented using the free STM8 touch sensing firmware library.

## 3.14 Timers

The high-density and medium+ density STM8L15xx6/8 devices contain one advanced control timer (TIM1), three 16-bit general purpose timers (TIM2,TIM3 and TIM5) and one 8-bit basic timer (TIM4).

All the timers can be served by DMA1.

*Table 3* compares the features of the advanced control, general-purpose and basic timers.

**Table 3. Timer feature comparison**

| Timer | Counter resolution | Counter type | Prescaler factor | DMA1 request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|
| TIM1 | 16-bit | up/down | Any integer from 1 to 65536 | Yes | 3 + 1 | 3 |
| TIM2 | | | Any power of 2 from 1 to 128 | | 2 | None |
| TIM3 | | | | | | |
| TIM5 | | | | | | |
| TIM4 | 8-bit | up | Any power of 2 from 1 to 32768 | | 0 | |

### 3.14.1 16-bit advanced control timer (TIM1)

This is a high-end timer designed for a wide range of control applications. With its complementary outputs, dead-time control and center-aligned PWM capability, the field of applications is extended to motor control, lighting and half-bridge driver.

- 16-bit up, down and up/down autoreload counter with 16-bit prescaler
- 3 independent capture/compare channels (CAPCOM) configurable as input capture, output compare, PWM generation (edge and center aligned mode) and single pulse mode output
- 1 additional capture/compare channel which is not connected to an external I/O
- Synchronization module to control the timer with external signals
- Break input to force timer outputs into a defined state
- 3 complementary outputs with adjustable dead time
- Encoder mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)

### 3.14.2 16-bit general purpose timers (TIM2, TIM3, TIM5)

- 16-bit autoreload (AR) up/down-counter
- 7-bit prescaler adjustable to fixed power of 2 ratios (1…128)
- 2 individually configurable capture/compare channels
- PWM mode
- Interrupt capability on various events (capture, compare, overflow, break, trigger)
- Synchronization with other timers or external signals (external clock, reset, trigger and enable)

### 3.14.3 8-bit basic timer (TIM4)

The 8-bit timer consists of an 8-bit up auto-reload counter driven by a programmable prescaler. It can be used for timebase generation with interrupt generation on timer overflow or for DAC trigger generation.

## 3.15 Watchdog timers

The watchdog system is based on two independent timers providing maximum security to the applications.

### 3.15.1 Window watchdog timer

The window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interferences or by unexpected logical conditions, which cause the application program to abandon its normal sequence.

### 3.15.2 Independent watchdog timer

The independent watchdog peripheral (IWDG) can be used to resolve processor malfunctions due to hardware or software failures.

It is clocked by the internal LSI RC clock source, and thus stays active even in case of a CPU clock failure.

## 3.16 Beeper

The beeper function outputs a signal on the BEEP pin for sound generation. The signal is in the range of 1, 2 or 4 kHz.

## 3.17 Communication interfaces

### 3.17.1 SPI

The serial peripheral interfaces (SPI1 and SPI2) provide half/ full duplex synchronous serial communication with external devices.

- Maximum speed: 8 Mbit/s ($f_{SYSCLK}/2$) both for master and slave
- Full duplex synchronous transfers
- Simplex synchronous transfers on 2 lines with a possible bidirectional data line
- Master or slave operation - selectable by hardware or software
- Hardware CRC calculation
- Slave/master selection input pin

*Note: SPI1 and SPI2 can be served by the DMA1 Controller.*

### 3.17.2 $I^2C$

The $I^2C$ bus interface (I2C1) provides multi-master capability, and controls all I²C bus-specific sequencing, protocol, arbitration and timing.

- Master, slave and multi-master capability
- Standard mode up to 100 kHz and fast speed modes up to 400 kHz.
- 7-bit and 10-bit addressing modes.
- SMBus 2.0 and PMBus support
- Hardware CRC calculation

*Note: $I^2C1$ can be served by the DMA1 Controller.*

### 3.17.3 USART

The USART interfaces (USART1, USART2 and USART3) allow full duplex, asynchronous communications with external devices requiring an industry standard NRZ asynchronous serial data format. It offers a very wide range of baud rates.

- 1 Mbit/s full duplex SCI
- SPI1 emulation
- High precision baud rate generator
- Smartcard emulation
- IrDA SIR encoder decoder
- Single wire half duplex mode

*Note: USART1, USART2 and USART3 can be served by the DMA1 Controller.*

## 3.18 Infrared (IR) interface

The high-density and medium+ density STM8L15xx6/8 devices contain an infrared interface which can be used with an IR LED for remote control functions. Two timer output compare channels are used to generate the infrared remote control signals.

## 3.19 Development support

### Development tools

Development tools for the STM8 microcontrollers include:

- The STice emulation system offering tracing and code profiling
- The STVD high-level language debugger including C compiler, assembler and integrated development environment
- The STVP Flash programming software

The STM8 also comes with starter kits, evaluation boards and low-cost in-circuit debugging/programming tools.

### Single wire data interface (SWIM) and debug module

The debug module with its single wire data interface (SWIM) permits non-intrusive real-time in-circuit debugging and fast memory programming.

The Single wire interface is used for direct access to the debugging module and memory programming. The interface can be activated in all device operation modes.

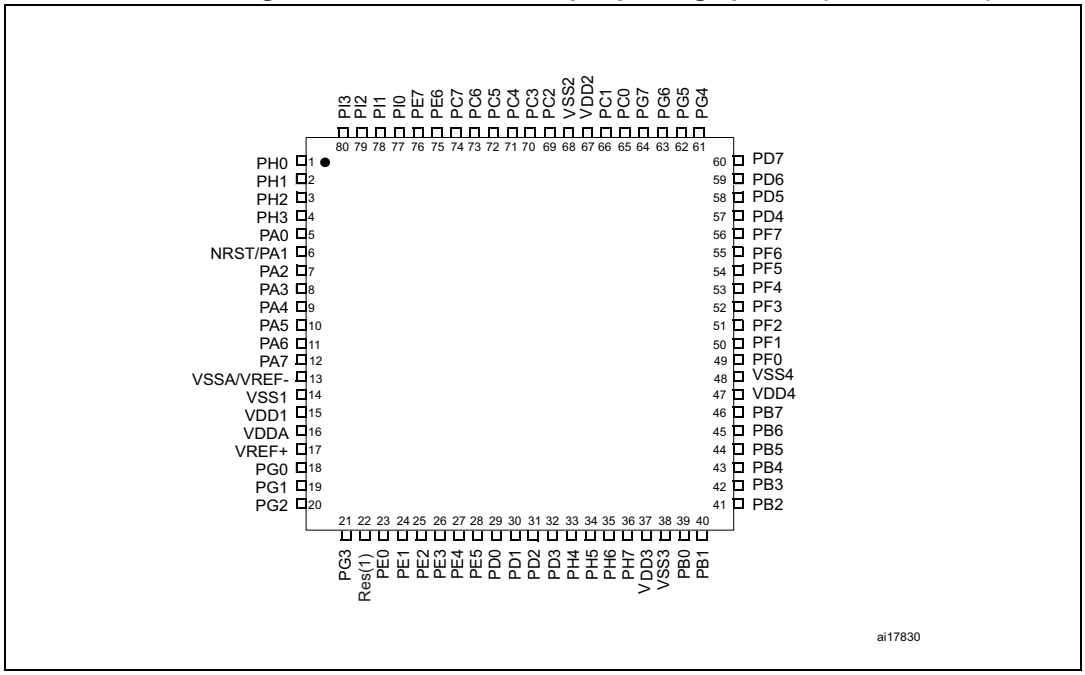
The non-intrusive debugging module features a performance close to a full-featured emulator. Beside memory and peripherals, CPU operation can also be monitored in real-time by means of shadow registers.

### Bootloader

A bootloader is available to reprogram the Flash memory using the USART1, USART2, USART3 (USARTs in asynchronous mode), SPI1 or SPI2 interfaces. The reference document for the bootloader is *UM0560: STM8 bootloader user manual*.

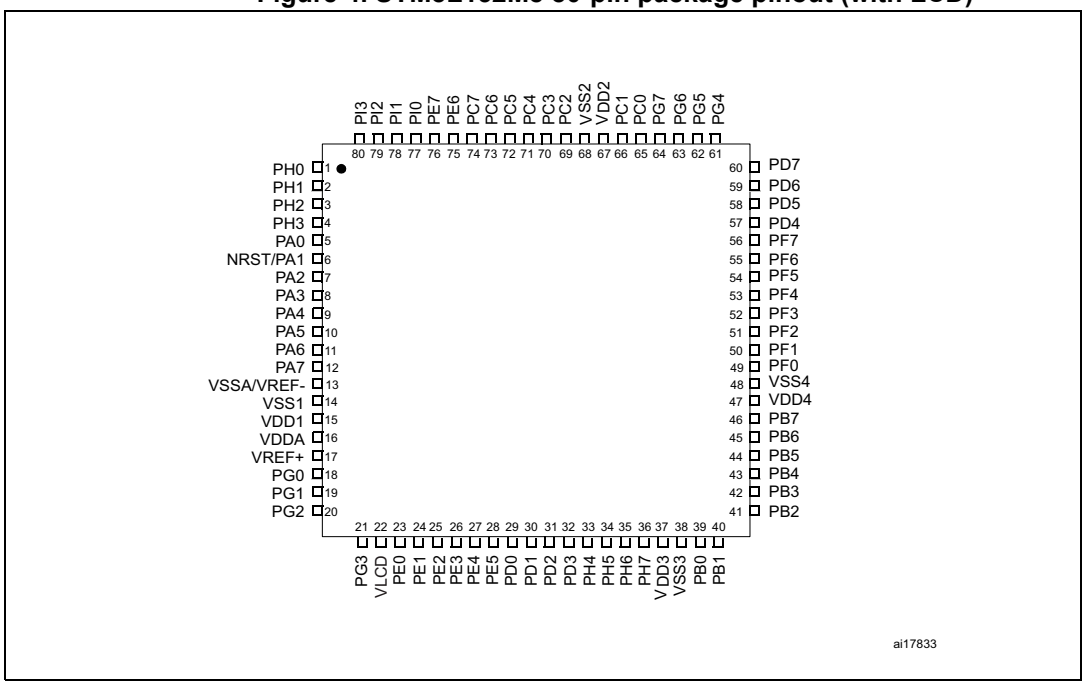
# 4 Pin description

**Figure 3. STM8L151M8 80-pin package pinout (without LCD)**



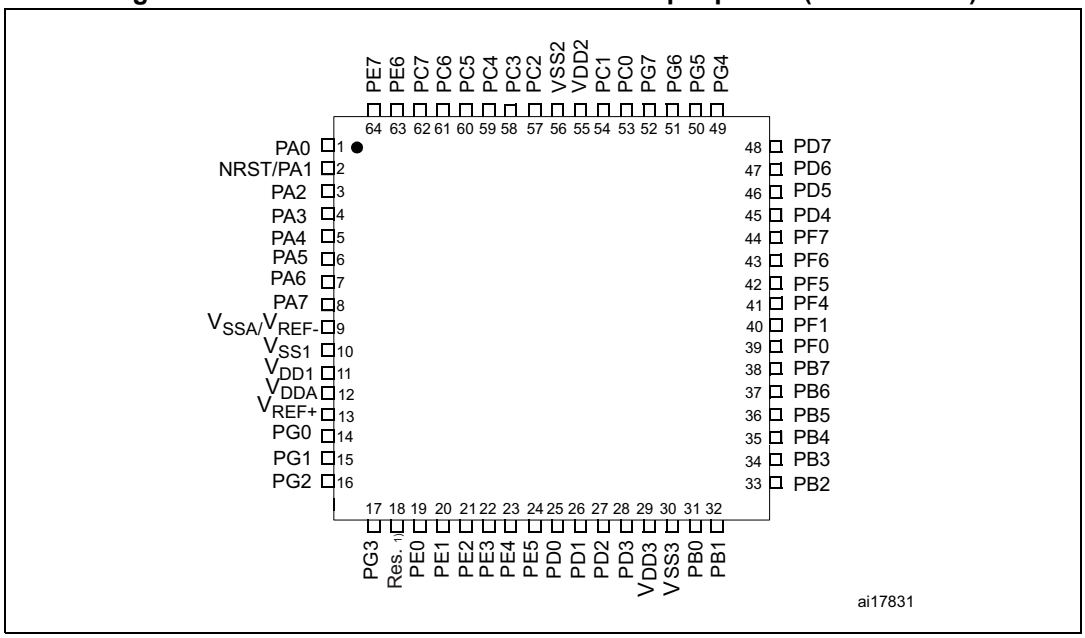

1. Pin 22 is reserved and must be tied to $V_{DD}$.
2. The above figure shows the package top view.

**Figure 4. STM8L152M8 80-pin package pinout (with LCD)**



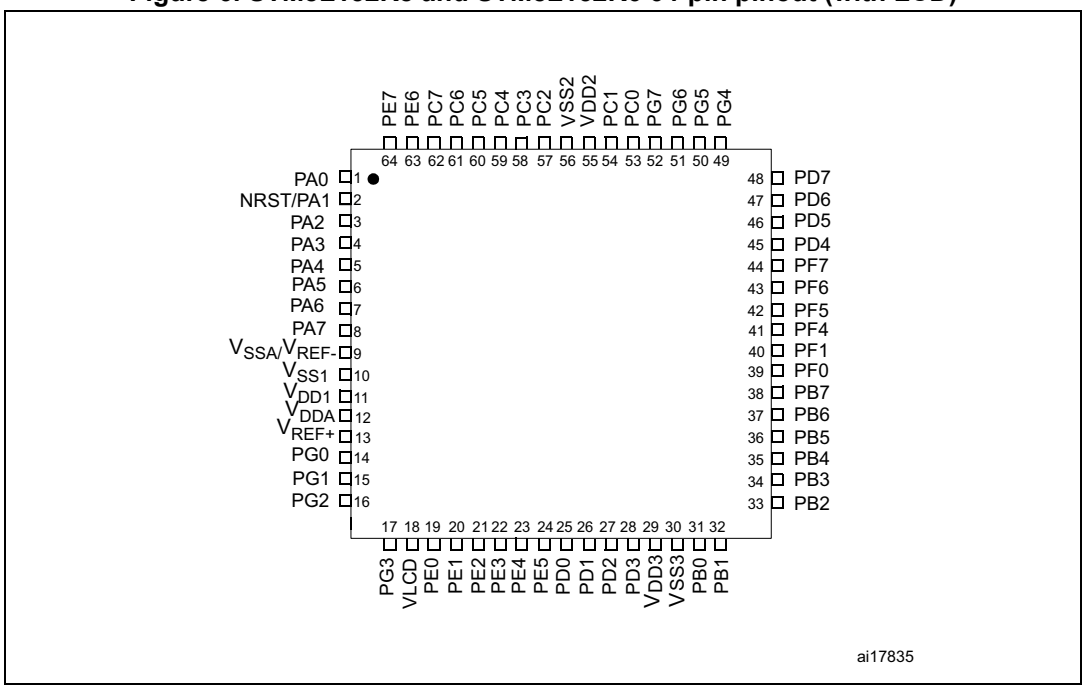

1. The above figure shows the package top view.

**Figure 5. STM8L151R8 and STM8L151R6 64-pin pinout (without LCD)**



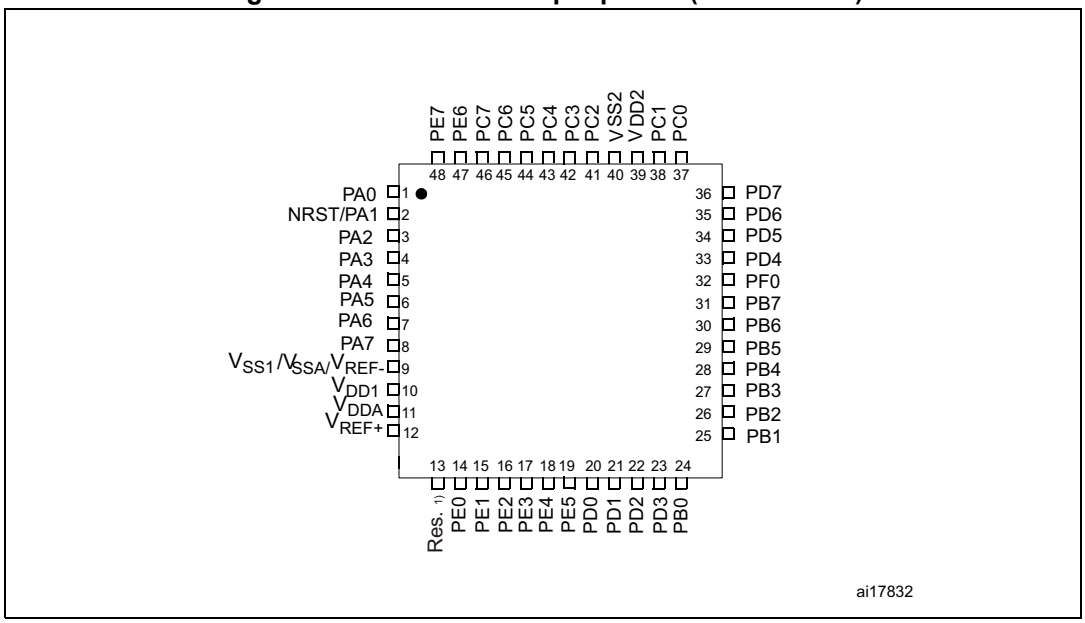

1. Pin 18 is reserved and must be tied to $V_{DD}$.
2. The above figure shows the package top view.

**Figure 6. STM8L152R8 and STM8L152R6 64-pin pinout (with LCD)**



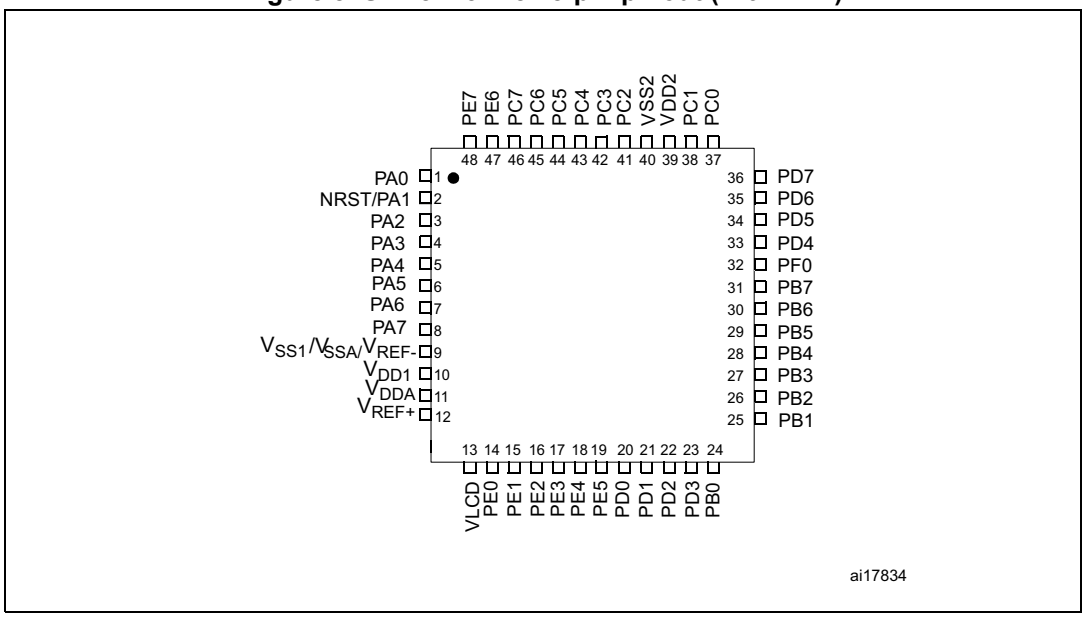

1. The above figure shows the package top view.

**Figure 7. STM8L151C8 48-pin pinout (without LCD)**



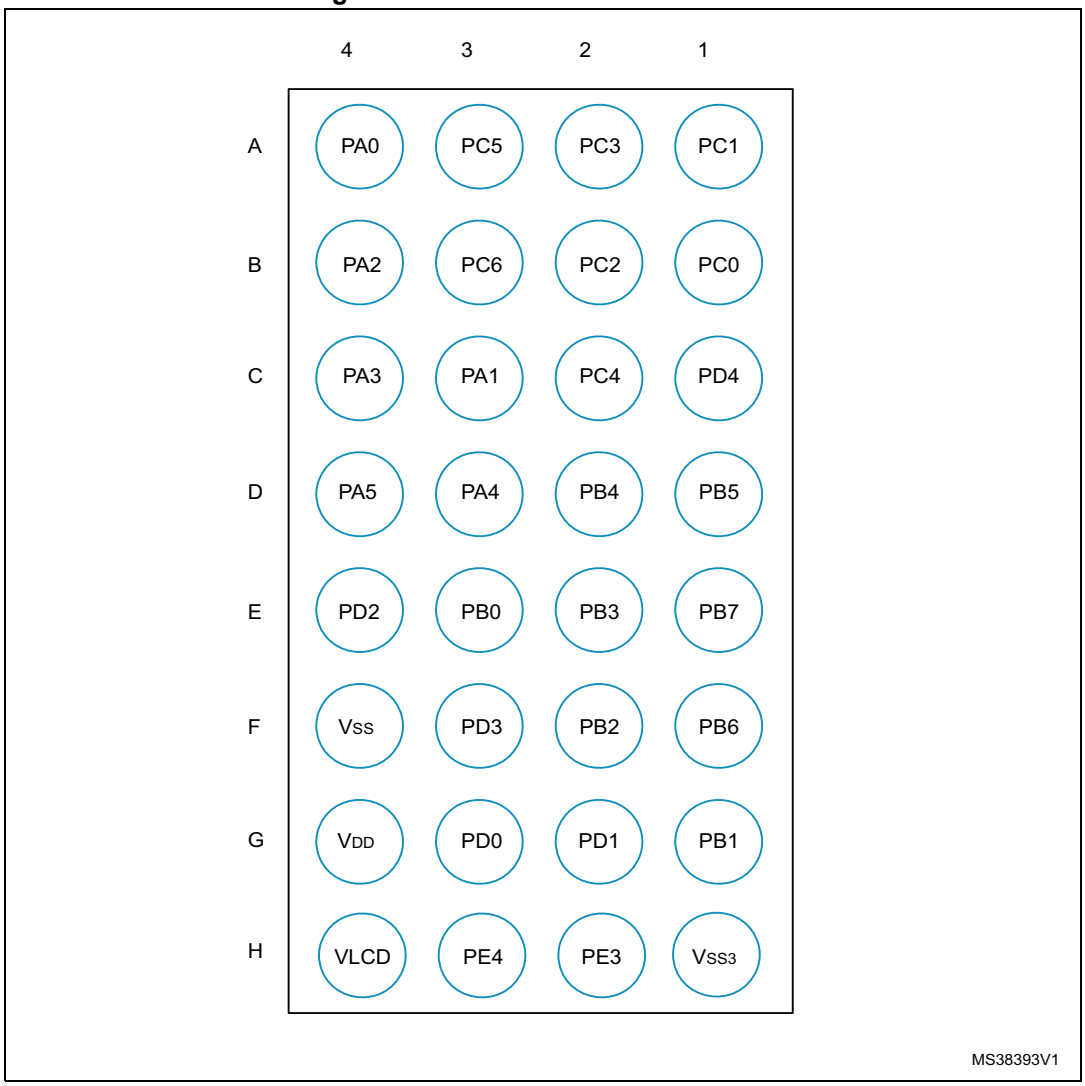

1. Pin 13 is reserved and must be tied to $V_{DD}$.
2. The above figure shows the package top view.

**Figure 8. STM8L152C8 48-pin pinout (with LCD)**




1. The above figure shows the package top view.

**Figure 9. STM8L152K8 32-ball ballout**




**Warning:** **For the 32-pin STM8L152K8 devices, some active I/O pins are not bonded out of the package. Effectively, all ports available on 48-pin devices must be considered as active ports also for 32-pin devices - see *Table 5: High-density and medium+ density STM8L15x pin description* for more details. To avoid spurious effects, users have to configure active ports as input pull-up. A small increase in consumption (typ. < 300 µA) may occur during the power up and reset phase until these ports are properly configured.**

**Table 4. Legend/abbreviation**

| | | |
|---|---|---|
| **Type** | I= input, O = output, S = power supply | |
| **Level** | FT: Five-volt tolerant | |
| | Output | HS = high sink/source (20 mA) |
| **Port and control configuration** | Input | float = floating, wpu = weak pull-up |
| | Output | T = true open drain, OD = open drain, PP = push pull |
| **Reset state** | Bold X (pin state after reset release).<br>Unless otherwise specified, the pin state is the same during the reset phase (i.e. “under reset”) and after internal reset release (i.e. at reset state). | |

**Table 5. High-density and medium+ density STM8L15x pin description**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | UFQFPN48 and LQFP48 | WLCSP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 1 | - | - | - | PH0/LCD SEG 36 (3) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port H0** | LCD segment 36 |
| 2 | - | - | - | PH1/LCD SEG 37 (3) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port H1** | LCD segment 37 |
| 3 | - | - | - | PH2/LCD SEG 38 (3) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port H2** | LCD segment 38 |
| 4 | - | - | - | PH3/LCD SEG 39 (3) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port H3** | LCD segment 39 |
| 6 | 2 | 2 | C3 | NRST/PA1(1) | I/O | - | - | **X** | | HS | - | X | **Reset** | PA1 |
| 7 | 3 | 3 | B4 | PA2/OSC_IN/ *[USART1_TX](2)/ [SPI1_MISO]* (2) | I/O | - | **X** | X | X | HS | X | X | **Port A2** | HSE oscillator input / *[USART1 transmit] / [SPI1 master in- slave out] /* |
| 8 | 4 | 4 | C4 | PA3/OSC_OUT/ *[USART1_RX](2)/[ SPI1_MOSI](2)* | I/O | - | **X** | X | X | HS | X | X | **Port A3** | HSE oscillator output / *[USART1 receive]/ [SPI1 master out/slave in]/* |
| 9 | 5 | 5 | D3 | PA4/TIM2_BKIN/ *[TIM2_ETR](2)* LCD_COM0(3)/ADC1_IN2 *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port A4** | Timer 2 - break input / */[Timer 2 - trigger]* / LCD COM 0 / ADC1 input 2/ *[Comparator 1 positive input]* |
| 10 | 6 | 6 | D4 | PA5/TIM3_BKIN/ *[TIM3_ETR](2)/* LCD_COM1(3)/ADC1_IN1/ *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port A5** | Timer 3 - break input / *[Timer 3 - trigger]* / LCD_COM 1 / ADC1 input 1/ *[Comparator 1 positive input]* |

**Table 5. High-density and medium+ density STM8L15x pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | UFQFPN48 and LQFP48 | WLCSP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 11 | 7 | 7 | -(4) | PA6/ADC1_TRIG/ LCD_COM2(3)/ADC1_IN0/ *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port A6** | ADC1 - trigger / LCD_COM2 / ADC1 input 0/ *[Comparator 1 positive input]* |
| 12 | 8 | 8 | -(4) | PA7/LCD_SEG0(3)/ TIM5_CH1 | I/O | FT(6) | **X** | X | X | HS | X | X | **Port A7** | LCD segment 0 / TIM5 channel 1 |
| 39 | 31 | 24 | E3 | PB0(5)/TIM2_CH1/ LCD_SEG10(3)/ADC1_IN18 / *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port B0** | Timer 2 - channel 1 /LCD segment 10/ ADC1_IN18/ *[Comparator 1 positive input]* |
| 40 | 32 | 25 | G1 | PB1/TIM3_CH1/ LCD_SEG11(3)/ADC1_IN17 / *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port B1** | Timer 3 - channel 1 / LCD segment 11 / ADC1_IN17/ *[Comparator 1 positive input]* |
| 41 | 33 | 26 | F2 | PB2/ TIM2_CH2/LCD_SEG12(3)/ ADC1_IN16/*[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port B2** | Timer 2 - channel 2 / LCD segment 12 / ADC1_IN16/ *[Comparator 1 positive input]* |
| 42 | 34 | 27 | E2 | PB3/TIM2_ETR/ LCD_SEG13(3)/ADC1_IN15 /*[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port B3** | Timer 2 - trigger / LCD segment 13 /ADC1_IN15/ *[Comparator 1 positive input]* |
| 43 | 35 | - | - | PB4(5)/SPI1_NSS/ LCD_SEG14(3)/ADC1_IN14 /*[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port B4** | SPI1 master/slave select / LCD segment 14 / ADC1_IN14/ *[Comparator 1 positive input]* |
| - | - | 28 | D2 | PB4(5)/SPI1_NSS/ LCD_SEG14(3)/ADC1_IN14 /DAC_OUT2/ *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port B4** | SPI1 master/slave select / LCD segment 14 / ADC1_IN14 / DAC channel 2 output/ *[Comparator 1 positive input]* |

**Table 5. High-density and medium+ density STM8L15x pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | UFQFPN48 and LQFP48 | WLCSP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 44 | 36 | - | - | PB5/SPI1_SCK/ LCD_SEG15(3)/ADC1_IN13 / *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port B5** | SPI1 clock / LCD segment 15 / ADC1_IN13/ *[Comparator 1 positive input]* |
| - | - | 29 | D1 | PB5/SPI1_SCK/ LCD_SEG15(3)/ADC1_IN13 /DAC_OUT2/ *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port B5** | [SPI1 clock] / LCD segment 15 / ADC1_IN13 / DAC channel 2 output/ *[Comparator 1 positive input]* |
| 45 | 37 | - | - | PB6/SPI1_MOSI/ LCD_SEG16(3)/ADC1_IN12 /*[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port B6** | SPI1 master out/slave in/ LCD segment 16 / ADC1_IN12/ *[Comparator 1 positive input]* |
| - | - | 30 | F1 | PB6/SPI1_MOSI/ LCD_SEG16(3)/ADC1_IN12 /DAC_OUT2/*[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port B6** | SPI1 master out/ slave in / LCD segment 16 / ADC1_IN12 / DAC channel 2 output/*[Comparator 1 positive input]* |
| 46 | 38 | 31 | E1 | PB7/SPI1_MISO/ LCD_SEG17(3)/ ADC1_IN11/*[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port B7** | SPI1 master in- slave out/ LCD segment 17 / ADC1_IN11/*[Comparator 1 positive input]* |
| 65 | 53 | 37 | B1 | PC0/I2C1_SDA | I/O | FT(6) | **X** | - | X | | T(7) | | **Port C0** | I2C1 data |
| 66 | 54 | 38 | A1 | PC1/I2C1_SCL | I/O | FT(6) | **X** | - | X | | T(7) | | **Port C1** | I2C1 clock |
| 69 | 57 | 41 | B2 | PC2/USART1_RX/ LCD_SEG22/ADC1_IN6/ *[COMP1_INP]* /VREFINT | I/O | FT(6) | **X** | X | X | HS | X | X | **Port C2** | USART1 receive / LCD segment 22 / ADC1_IN6/ *[Comparator 1 positive input]* /Internal reference voltage output |
| - | - | 42 | A2 | PC3/USART1_TX/ LCD_SEG23(3)/ ADC1_IN5 | I/O | FT(6) | **X** | X | X | HS | X | X | **Port C3** | USART1 transmit / LCD segment 23 / ADC1_IN5 |

**Table 5. High-density and medium+ density STM8L15x pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | UFQFPN48 and LQFP48 | WLCSP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 70 | 58 | - | - | PC3/USART1_TX/ LCD_SEG23(3)/ ADC1_IN5/ *[COMP2_INM]* / *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port C3** | USART1 transmit / LCD segment 23 / ADC1_IN5 / *[Comparator 2 negative input]* /*[Comparator 1 input positive]* |
| 71 | 59 | - | - | PC4/USART1_CK/ I2C1_SMB/ *[CCO]*(2)/ LCD_SEG24(3)/ ADC1_IN4/*[COMP2_INM]* /*[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port C4** | USART1 synchronous clock / I2C1_SMB / *[Configurable clock output]* / LCD segment 24 / ADC1_IN4 / *[Comparator 2 negative input]* / *[Comparator 1 positive input]* |
| - | - | 43 | C2 | PC4/USART1_CK/ I2C1_SMB/*[CCO]*(2)/ LCD_SEG24(3)/ADC1_IN4/ *[COMP2_INM]* / *[COMP1_INP]* / *[LCD_COM4]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port C4** | USART1 synchronous clock / I2C1_SMB / *[Configurable clock output]* / LCD segment 24 / ADC1_IN4 / *[Comparator 2 negative input]* / *[Comparator 1 positive input]* / *[LCD_COM4]*(3) |
| 72 | 60 | 44 | A3 | PC5/OSC32_IN /*[SPI1_NSS]*(2)/ *[USART1_TX]*(2) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port C5** | LSE oscillator input / *[SPI1 master/slave select]* / *[USART1 transmit]* |
| 73 | 61 | 45 | B3 | PC6/OSC32_OUT/ *[SPI1_SCK]*(2)/ *[USART1_RX]*(2) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port C6** | LSE oscillator output / *[SPI1 clock]* / *[USART1 receive]* |
| 74 | 62 | - | - | PC7/LCD_SEG25(3)/ ADC1_IN3/*[COMP2_INM]* / *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port C7** | LCD segment 25 /ADC1_IN3/ *[Comparator 2 negative input]* / *[Comparator 1 positive input]* |

**Table 5. High-density and medium+ density STM8L15x pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | UFQFPN48 and LQFP48 | WLCSP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| - | - | 46 | -(4) | PC7/LCD_SEG25(3)/ ADC1_IN3/USART3_CK/ *[COMP2_INM]* / *[COMP1_INP]* / *[LCD_COM5]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port C7** | LCD segment 25 /ADC1_IN3/ USART3 synchronous clock/ *[Comparator 2 negative input]* / *[Comparator 1 positive input]*/ *[LCD_COM5]*(3) |
| 29 | 25 | 20 | G3 | PD0/TIM3_CH2/ *[ADC1_TRIG]*(2)/ LCD_SEG7(3)/ADC1_IN22/ *[COMP2_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D0** | Timer 3 - channel 2 / *[ADC1_Trigger]* / LCD segment 7 / ADC1_IN22 / *[Comparator 2 positive input]* |
| 30 | 26 | 21 | G2 | PD1/TIM3_ETR/ LCD_COM3(3)/ADC1_IN21/ *[COMP1_INP]*// *[COMP2_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D1** | Timer 3 - trigger / LCD_COM3 / ADC1_IN21 / *[Comparator 1 positive input]* /*[Comparator 2 positive input]* |
| 31 | 27 | 22 | E4 | PD2/TIM1_CH1 /LCD_SEG8(3)/ADC1_IN20/ *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D2** | Timer 1 - channel 1 / LCD segment 8 / ADC1_IN20/ *[Comparator 1 positive input]* |
| 32 | 28 | 23 | F3 | PD3/ TIM1_ETR/ LCD_SEG9(3)/ ADC1_IN19/ *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D3** | Timer 1 - trigger / LCD segment 9 / ADC1_IN19/ *[Comparator 1 positive input]* |
| 57 | 45 | - | - | PD4/TIM1_CH2 /LCD_SEG18(3)/ ADC1_IN10/ *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D4** | Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/ *[Comparator 1 positive input]* |
| - | - | 33 | C1 | PD4/TIM1_CH2 /LCD_SEG18(3)/ ADC1_IN10/SPI2_MISO/ *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D4** | Timer 1 - channel 2 / LCD segment 18 / ADC1_IN10/SPI2 master in/slave out/ *[Comparator 1 positive input]* |

**Table 5. High-density and medium+ density STM8L15x pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | UFQFPN48 and LQFP48 | WLCSP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 58 | 46 | - | - | PD5/TIM1_CH3 /LCD_SEG19(3)/ ADC1_IN9/ *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D5** | Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ *[Comparator 1 positive input]* |
| - | - | 34 | -(4) | PD5/TIM1_CH3 /LCD_SEG19(3)/ ADC1_IN9/SPI2_MOSI/ *[COMP1_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D5** | Timer 1 - channel 3 / LCD segment 19 / ADC1_IN9/ SPI2 master out/slave in/ *[Comparator 1 positive input]* |
| 59 | 47 | - | - | PD6/TIM1_BKIN /LCD_SEG20(3)/ ADC1_IN8/RTC_CALIB/ *[COMP1_INP]*/VREFINT | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D6** | Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration/*[Comparator 1 positive input]*/Internal reference voltage output |
| - | - | 35 | -(4) | PD6/TIM1_BKIN /LCD_SEG20(3)/ ADC1_IN8/RTC_CALIB/ SPI2_SCK/*[COMP1_INP]*/ VREFINT | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D6** | Timer 1 - break input / LCD segment 20 / ADC1_IN8 / RTC calibration/SPI2 clock/ *[Comparator 1 positive input]*/Internal reference voltage output |
| 60 | 48 | - | - | PD7/TIM1_CH1N /LCD_SEG21(3)/ ADC1_IN7/RTC_ALARM/ *[COMP1_INP]*/VREFINT | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D7** | Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm/*[Comparator 1 positive input]*/Internal reference voltage output |
| - | - | 36 | -(4) | PD7/TIM1_CH1N /LCD_SEG21(3)/ ADC1_IN7/RTC_ALARM /SPI2_NSS/*[COMP1_INP]*/ VREFINT | I/O | FT(6) | **X** | X | X | HS | X | X | **Port D7** | Timer 1 - inverted channel 1/ LCD segment 21 / ADC1_IN7 / RTC alarm /SPI2 master/slave select/*[Comparator 1 positive input]*/Internal reference voltage output |
| 61 | 49 | - | - | PG4/LCD_SEG32/ SPI2_NSS | I/O | FT(6) | **X** | X | X | HS | X | X | **Port G4** | LCD segment 32 / SPI2 master/slave select |

**Table 5. High-density and medium+ density STM8L15x pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | UFQFPN48 and LQFP48 | WLCSP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 62 | 50 | - | - | PG5/LCD_SEG33/ SPI2_SCK | I/O | FT(6) | **X** | X | X | HS | X | X | **Port G5** | LCD segment 33 / SPI2 clock |
| 63 | 51 | - | - | PG6/LCD_SEG34/ SPI2_MOSI | I/O | FT(6) | **X** | X | X | HS | X | X | **Port G6** | LCD segment 34 / SPI2 master out- slave in |
| 64 | 52 | - | - | PG7/LCD_SEG35/ SPI2_MISO | I/O | FT(6) | **X** | X | X | HS | X | X | **Port G7** | LCD segment 35 / SPI2 master in- slave out |
| 23 | 19 | 14 | -(4) | PE0/LCD_SEG1(3)/ TIM5_CH2 | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E0** | LCD segment 1/ Timer 5 channel 2 |
| 24 | 20 | 15 | -(4) | PE1/TIM1_CH2N /LCD_SEG2(3) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E1** | Timer 1 - inverted channel 2 / LCD segment 2 |
| 25 | 21 | 16 | -(4) | PE2/TIM1_CH3N /LCD_SEG3(3)/ *[CCO]*(2) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E2** | Timer 1 - inverted channel 3 / LCD segment 3 / *[Configurable clock output]* |
| 26 | - | - | - | PE3/LCD_SEG4(3) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E3** | LCD segment 4 |
| - | 22 | 17 | H2 | PE3/LCD_SEG4(3)/ USART2_RX | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E3** | LCD segment 4/ USART2 receive |
| 27 | - | - | - | PE4/LCD_SEG5(3)/ DAC_TRIG1 | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E4** | LCD segment 5/ DAC 1 trigger |
| - | 23 | 18 | H3 | PE4/LCD_SEG5(3)/ DAC_TRIG2/USART2_TX | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E4** | LCD segment 5/ DAC 2 trigger/ USART2 transmit |
| 28 | - | - | - | PE5/LCD_SEG6(3)/ ADC1_IN23/*[COMP1_INP]*/ *[COMP2_INP]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E5** | LCD segment 6 / ADC1_IN23/ *[Comparator 1 positive input]* /*[Comparator 2 positive input]* |
| - | 24 | 19 | -(4) | PE5/LCD_SEG6(3)/ ADC1_IN23/*[COMP1_INP]*/ *[COMP2_INP]* / USART2_CK | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E5** | LCD segment 6 / ADC1_IN23/ *[Comparator 1 positive input]* / *[Comparator 2 positive input]* /USART2 synchronous clock |

**Table 5. High-density and medium+ density STM8L15x pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | UFQFPN48 and LQFP48 | WLCSP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| - | - | 47 | -(4) | PE6/LCD_SEG26(3)/ PVD_IN/TIM5_BKIN/ USART3_TX/ *[LCD_COM6]*(3) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E6** | LCD segment 26 /PVD_IN /TIM5 break input / USART3 transmit/*[LCD_COM6]*(3) |
| 75 | 63 | - | - | PE6/LCD_SEG26(3)/ PVD_IN/TIM5_BKIN | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E6** | LCD segment 26 /PVD_IN /TIM5 break input |
| 76 | 64 | - | - | PE7/LED_SEG27/ TIM5_ETR | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E7** | LCD segment 27/ TIM5 trigger |
| - | - | 48 | -(4) | PE7/LED_SEG27/ TIM5_ETR/USART3_RX/ *[LCD_COM7]*(3) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port E7** | LCD segment 27/ TIM5 trigger/ USART3 receive/ *[LCD_COM7]*(3) |
| 77 | - | - | - | PI0/RTC_TAMP1/ *[SPI2_NSS]/[TIM3_CH1]* | I/O | FT(6) | **X** | X | - | HS | X | X | **Port I0** | RTC tamper 1 input *[SPI2 master/slave select]* *[TIM3 channel 1* |
| 78 | - | - | - | PI1/RTC_TAMP2/ *[SPI2_SCK]* | I/O | FT(6) | **X** | X | - | HS | X | X | **Port I1** | RTC tamper 2 input *[SPI2 clock]* |
| 79 | - | - | - | PI2/RTC_TAMP3/ *[SPI2_MOSI]* | I/O | FT(6) | **X** | X | - | HS | X | X | **Port I2** | RTC tamper 3 input *[SPI2 master out- slave in]* |
| 80 | - | - | - | PI3/ *[SPI2_MISO]/[TIM3_CH2]* | I/O | FT(6) | **X** | X | - | HS | X | X | **Port I3** | *[SPI2 master in- slave out]* *[TIM3 channel 2]* |
| - | - | 32 | -(4) | PF0/ADC1_IN24/ DAC_OUT1 | I/O | - | **X** | X | X | HS | X | X | **Port F0** | ADC1_IN24 / DAC 1 output |
| - | 39 | - | - | PF0/ADC1_IN24/ DAC_OUT1/*[USART3_TX]* | I/O | - | **X** | X | X | HS | X | X | **Port F0** | ADC1_IN24 / DAC 1 output/ *[USART3 transmit]* |
| 49 | - | - | - | PF0/ADC1_IN24/ DAC_OUT1/ *[USART3_TX]/[SPI1_MISO]* | I/O | - | **X** | X | X | HS | X | X | **Port F0** | ADC1_IN24 / DAC 1 output/ *[USART3 transmit]* *[SPI1* master in- slave out*]* |

**Table 5. High-density and medium+ density STM8L15x pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | UFQFPN48 and LQFP48 | WLCSP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 50 | - | - | - | PF1/ADC1_IN25/ DAC_OUT2/ *[USART3_RX]/ [SPI1_MOSI]* | I/O | - | **X** | X | X | HS | X | X | **Port F1** | ADC1_IN25/ DAC channel 2 output/ *[USART3 receive] [SPI1* master out- slave in*]* |
| - | 40 | - | - | PF1/ADC1_IN25/ DAC_OUT2/ *[USART3_RX]* | I/O | - | **X** | X | X | HS | X | X | **Port F1** | ADC1_IN25/ DAC channel 2 output/ *[USART3 receive]* |
| 51 | - | - | - | PF2/ADC1_IN26/ *[SPI1_SCK]/ [USART3_SCK]* | I/O | - | **X** | X | X | HS | X | X | **Port F2** | ADC1_IN26 *[SPI1 clock] [USART3 clock]* |
| 52 | - | - | - | PF3/ADC1_IN27/ *[SPI1_NSS]* | I/O | - | **X** | X | X | HS | X | X | **Port F3** | ADC1_IN27 *[SPI1 master/slave select]* |
| - | 41 | - | - | PF4/LCD_SEG36/ *[LCD _COM4]*(10) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port F4** | LCD segment 36/ *[LCD_COM4]*(10) |
| 53 | - | - | - | PF4/LCD_SEG40/ *[LCD_COM4]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port F4** | LCD segment 40/ *[LCD_COM4]*(10) |
| - | 42 | - | - | PF5/LCD_SEG37/ *[LCD_COM5]*(10) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port F5** | LCD segment 37/ *[LCD COM5]*(10) |
| 54 | - | - | - | PF5/LCD_SEG41/ *[LCD_COM5]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port F5** | LCD segment 41/ *[LCD COM5]*(10) |
| - | 43 | - | - | PF6/LCD_SEG38 /*[LCD_COM6]*(10) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port F6** | LCD segment 38/ *[LCD COM6]*(10) |
| 55 | - | - | - | PF6/LCD_SEG42/ *[LCD_COM6]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port F6** | LCD segment 42/ *[LCD COM6]*(10) |
| - | 44 | - | - | PF7/LCD_SEG39/ *[LCD_COM7]*(10) | I/O | FT(6) | **X** | X | X | HS | X | X | **Port F7** | LCD segment 39/ *[LCD COM7]*(10) |
| 56 | - | - | - | PF7/LCD_SEG43/ *[LCD_COM7]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port F7** | LCD segment 43/ *[LCD COM7]*(10) |
| 22 | 18 | 13 | H4 | VLCD(8) | S | - | - | - | - | - | - | - | LCD booster external capacitor | |
| 15 | 11 | 10 | - | $V_{DD1}$ | S | - | - | - | - | - | - | - | Digital power supply | |
| 14 | 10 | - | - | $V_{SS1}$ | S | - | - | - | - | - | - | - | I/O ground | |
| 16 | 12 | 11 | - | $V_{DDA}$ | S | - | - | - | - | - | - | - | Analog supply voltage | |

**Table 5. High-density and medium+ density STM8L15x pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | UFQFPN48 and LQFP48 | WLCSP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| - | - | - | G4 | $V_{DD1}/V_{DDA}/V_{REF+}$ | S | - | - | - | - | - | - | - | Digital power supply / Analog power supply / ADC1 positive voltage reference | |
| 17 | 13 | 12 | - | $V_{REF+}/V_{REF+_DAC}$ | S | - | - | - | - | - | - | - | ADC1 and DAC1/2 positive voltage reference | |
| 18 | 14 | - | - | PG0/LCD SEG28(3) /USART3_RX/ *[TIM2_BKIN]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port G0** | LCD segment 28/ USART3 receive / *[Timer 2 - break input]* |
| 19 | 15 | - | - | PG1/LCD SEG29(3) /USART3_TX/ *[TIM3_BKIN]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port G1** | LCD segment 29/ USART3 transmit / *[Timer 3 -break input]* |
| 20 | 16 | - | - | PG2/LCD_SEG30(3)/ USART3_CK | I/O | FT(6) | **X** | X | X | HS | X | X | **Port G2** | LCD segment 30/ USART 3 synchronous clock |
| 21 | 17 | - | - | PG3/LCD SEG 31 (3)/ *[TIM3_ETR]* | I/O | FT(6) | **X** | X | X | HS | X | X | **Port G3** | LCD segment 31/ *[Timer 3 - trigger]* |
| 33 | - | - | - | PH4/USART2_RX | I/O | FT(6) | **X** | X | X | HS | X | X | **Port H4** | USART2 receive |
| 34 | - | - | - | PH5/USART2_TX | I/O | FT(6) | **X** | X | X | HS | X | X | **Port H5** | USART2 transmit |
| 35 | - | - | - | PH6/USART2_CK/ TIM5_CH1 | I/O | FT(6) | **X** | X | X | HS | X | X | **Port H6** | USART2 synchronous clock/ Timer 5 - channel 1 |
| 36 | - | - | - | PH7/TIM5_CH2 | I/O | FT(6) | **X** | X | X | HS | X | X | **Port H7** | Timer 5 - channel 2 |
| - | - | 9 | F4 | $V_{SS}/V_{SSA}/V_{REF-}$ | S | - | - | - | - | - | - | - | I/O ground / Analog ground voltage / ADC1 negative voltage reference | |
| 13 | 9 | - | - | $V_{SSA}/V_{REF-}$ | S | - | - | - | - | - | - | - | Analog ground voltage / ADC1 negative voltage reference | |
| 37 | 29 | - | - | $V_{DD3}$ | S | - | - | - | - | - | - | - | IOs supply voltage | |
| 38 | 30 | - | H1 | $V_{SS3}$ | S | - | - | - | - | - | - | - | IOs ground voltage | |
| 5 | 1 | 1 | A4 | PA0(9)/*[USART1_CK]*(2)/ SWIM/BEEP/IR_TIM (10) | I/O | | X | **X** | X | HS | X | X | **Port A0** | *[USART1 synchronous clock]*(2)/ SWIM input and output / Beep output / Infrared Timer output |
| 68 | 56 | 40 | - | $V_{SS2}$ | S | - | - | - | - | - | - | - | IOs ground voltage | |
| 67 | 55 | 39 | - | $V_{DD2}$ | S | - | - | - | - | - | - | - | IOs supply voltage | |

**Table 5. High-density and medium+ density STM8L15x pin description (continued)**

| Pin number | | | | Pin name | Type | I/O level | Input | | | Output | | | Main function (after reset) | Default alternate function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LQFP80 | LQFP64 | UFQFPN48 and LQFP48 | WLCSP32 | | | | floating | wpu | Ext. interrupt | High sink/source | OD | PP | | |
| 48 | - | - | - | $V_{SS4}$ | S | - | - | - | - | - | - | - | IOs ground voltage | |
| 47 | - | - | - | $V_{DD4}$ | S | - | - | - | - | - | - | - | IOs supply voltage | |

1. At power-up, the PA1/NRST pin is a reset input pin with pull-up. To be used as a general purpose pin (PA1), it can be configured only as output push-pull, not as output open-drain nor as a general purpose input. Refer to Section *Configuring NRST/PA1 pin as general purpose output* in the STM8L15xxx and STM8L16xxx reference manual (RM0031).
2. [ ] Alternate function remapping option (if the same alternate function is shown twice, it indicates an exclusive choice not a duplication of the function).
3. Available on STM8L152x6/8 devices only.
4. Even if this I/O is not available on the device pin, it is considered as active and must be configured to input pull up or output mode by software to avoid spurious behavior and increased consumption.
5. A pull-up is applied to PB0 and PB4 during the reset phase. These two pins are input floating after reset release.
6. In the 5 V tolerant I/Os, the protection diode to $V_{DD}$ is not implemented.
7. In the open-drain output column, 'T' defines a true open-drain I/O (P-buffer, weak pull-up and protection diode to $V_{DD}$ are not implemented).
8. Available on STM8L152xx devices only. On STM8L151xx devices it is reserved and must be tied to $V_{DD}$.
9. The PA0 pin is in input pull-up during the reset phase and after reset release.
10. High Sink LED driver capability available on PA0.

*Note: Slope control of all GPIO pins can be programmed except true open drain pins and by default is limited to 2 MHz.*

### System configuration options

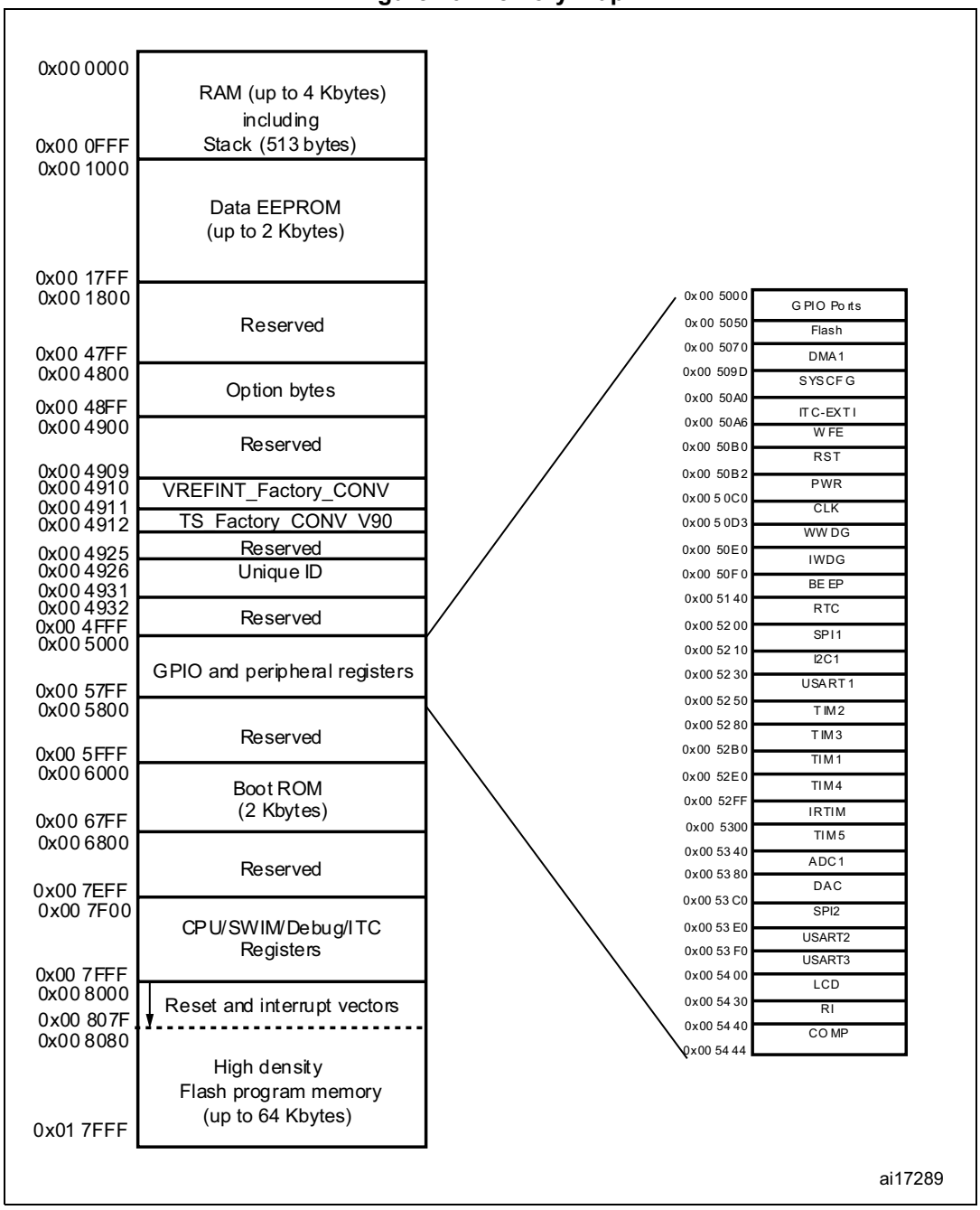
As shown in *Table 5: High-density and medium+ density STM8L15x pin description*, some alternate functions can be remapped on different I/O ports by programming one of the two remapping registers described in the "Routing interface (RI) and system configuration controller" section in the STM8L05xxx, STM8L15xxx and STM8L16xxx reference manual (RM0031).

# 5 Memory and register map

## 5.1 Memory mapping

The memory map is shown in *Figure 10*.

**Figure 10. Memory map**




1. Refer to *Table 9* for an overview of hardware register mapping, to *Table 8* for details on I/O port hardware registers, and to *Table 10* for information on CPU/SWIM/debug module controller registers.

**Table 6. Flash and RAM boundary addresses**

| Memory area | Size | Start address | End address |
|---|---|---|---|
| RAM | 2 Kbyte | 0x00 0000 | 0x00 07FF |
| | 4 Kbyte | 0x00 0000 | 0x00 0FFF |
| Flash program memory | 32 Kbyte | 0x00 8000 | 0x00 FFFF |
| | 64 Kbyte | | 0x01 7FFF |

## 5.2 Register map

**Table 7. Factory conversion registers**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 4910 | - | VREFINT_Factory_CONV(1) | Internal reference voltage factory conversion | 0xXX |
| 0x00 4911 | - | TS_Factory_CONV_V90(2) | Temperature sensor output voltage | 0xXX |

1. The VREFINT_Factory_CONV byte represents the 8 LSB of the result of the VREFINT 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x6.
2. The TS_Factory_CONV_V90 byte represents the 8 LSB of the result of the V90 12-bit ADC conversion performed in factory. The 2 MSB have a fixed value: 0x3.

**Table 8. I/O port hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5000 | Port A | PA_ODR | Port A data output latch register | 0x00 |
| 0x00 5001 | | PA_IDR | Port A input pin value register | 0xXX |
| 0x00 5002 | | PA_DDR | Port A data direction register | 0x00 |
| 0x00 5003 | | PA_CR1 | Port A control register 1 | 0x01 |
| 0x00 5004 | | PA_CR2 | Port A control register 2 | 0x00 |
| 0x00 5005 | Port B | PB_ODR | Port B data output latch register | 0x00 |
| 0x00 5006 | | PB_IDR | Port B input pin value register | 0xXX |
| 0x00 5007 | | PB_DDR | Port B data direction register | 0x00 |
| 0x00 5008 | | PB_CR1 | Port B control register 1 | 0x00 |
| 0x00 5009 | | PB_CR2 | Port B control register 2 | 0x00 |
| 0x00 500A | Port C | PC_ODR | Port C data output latch register | 0x00 |
| 0x00 500B | | PB_IDR | Port C input pin value register | 0xXX |
| 0x00 500C | | PC_DDR | Port C data direction register | 0x00 |
| 0x00 500D | | PC_CR1 | Port C control register 1 | 0x00 |
| 0x00 500E | | PC_CR2 | Port C control register 2 | 0x00 |

**Table 8. I/O port hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 500F | Port D | PD_ODR | Port D data output latch register | 0x00 |
| 0x00 5010 | | PD_IDR | Port D input pin value register | 0xXX |
| 0x00 5011 | | PD_DDR | Port D data direction register | 0x00 |
| 0x00 5012 | | PD_CR1 | Port D control register 1 | 0x00 |
| 0x00 5013 | | PD_CR2 | Port D control register 2 | 0x00 |
| 0x00 5014 | Port E | PE_ODR | Port E data output latch register | 0x00 |
| 0x00 5015 | | PE_IDR | Port E input pin value register | 0xXX |
| 0x00 5016 | | PE_DDR | Port E data direction register | 0x00 |
| 0x00 5017 | | PE_CR1 | Port E control register 1 | 0x00 |
| 0x00 5018 | | PE_CR2 | Port E control register 2 | 0x00 |
| 0x00 5019 | Port F | PF_ODR | Port F data output latch register | 0x00 |
| 0x00 501A | | PF_IDR | Port F input pin value register | 0xXX |
| 0x00 501B | | PF_DDR | Port F data direction register | 0x00 |
| 0x00 501C | | PF_CR1 | Port F control register 1 | 0x00 |
| 0x00 501D | | PF_CR2 | Port F control register 2 | 0x00 |
| 0x00 501E | Port G | PG_ODR | Port F data output latch register | 0x00 |
| 0x00 501F | | PG_IDR | Port G input pin value register | 0xXX |
| 0x00 5020 | | PG_DDR | Port G data direction register | 0x00 |
| 0x00 5021 | | PG_CR1 | Port G control register 1 | 0x00 |
| 0x00 5022 | | PG_CR2 | Port G control register 2 | 0x00 |
| 0x00 5023 | Port H | PH_ODR | Port H data output latch register | 0x00 |
| 0x00 5024 | | PH_IDR | Port H input pin value register | 0xXX |
| 0x00 5025 | | PH_DDR | Port H data direction register | 0x00 |
| 0x00 5026 | | PH_CR1 | Port H control register 1 | 0x00 |
| 0x00 5027 | | PH_CR2 | Port H control register 2 | 0x00 |
| 0x00 5028 | Port I | PI_ODR | Port I data output latch register | 0x00 |
| 0x00 5029 | | PI_IDR | Port I input pin value register | 0xXX |
| 0x00 502A | | PI_DDR | Port I data direction register | 0x00 |
| 0x00 502B | | PI_CR1 | Port I control register 1 | 0x00 |
| 0x00 502C | | PI_CR2 | Port I control register 2 | 0x00 |

**Table 9. General hardware register map**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 502E to 0x00 5049 | Reserved area (28 byte) | | | |
| 0x00 5050 | Flash | FLASH_CR1 | Flash control register 1 | 0x00 |
| 0x00 5051 | | FLASH_CR2 | Flash control register 2 | 0x00 |
| 0x00 5052 | | FLASH _PUKR | Flash program memory unprotection key register | 0x00 |
| 0x00 5053 | | FLASH _DUKR | Data EEPROM unprotection key register | 0x00 |
| 0x00 5054 | | FLASH _IAPSR | Flash in-application programming status register | 0x00 |
| 0x00 5055 to 0x00 506F | Reserved area (27 byte) | | | |
| 0x00 5070 | DMA1 | DMA1_GCSR | DMA1 global configuration & status register | 0xFC |
| 0x00 5071 | | DMA1_GIR1 | DMA1 global interrupt register 1 | 0x00 |
| 0x00 5072 to 0x00 5074 | | Reserved area (3 byte) | | |
| 0x00 5075 | | DMA1_C0CR | DMA1 channel 0 configuration register | 0x00 |
| 0x00 5076 | | DMA1_C0SPR | DMA1 channel 0 status & priority register | 0x00 |
| 0x00 5077 | | DMA1_C0NDTR | DMA1 number of data to transfer register (channel 0) | 0x00 |
| 0x00 5078 | | DMA1_C0PARH | DMA1 peripheral address high register (channel 0) | 0x52 |
| 0x00 5079 | | DMA1_C0PARL | DMA1 peripheral address low register (channel 0) | 0x00 |
| 0x00 507A | | Reserved area (1 byte) | | |
| 0x00 507B | | DMA1_C0M0ARH | DMA1 memory 0 address high register (channel 0) | 0x00 |
| 0x00 507C | | DMA1_C0M0ARL | DMA1 memory 0 address low register (channel 0) | 0x00 |
| 0x00 507D to 0x00 507E | | Reserved area (2 byte) | | |
| 0x00 507F | | DMA1_C1CR | DMA1 channel 1 configuration register | 0x00 |
| 0x00 5080 | | DMA1_C1SPR | DMA1 channel 1 status & priority register | 0x00 |
| 0x00 5081 | | DMA1_C1NDTR | DMA1 number of data to transfer register (channel 1) | 0x00 |
| 0x00 5082 | | DMA1_C1PARH | DMA1 peripheral address high register (channel 1) | 0x52 |
| 0x00 5083 | DMA1 | DMA1_C1PARL | DMA1 peripheral address low register (channel 1) | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5084 | Reserved area (1 byte) | | | |
| 0x00 5085 | DMA1 | DMA1_C1M0ARH | DMA1 memory 0 address high register (channel 1) | 0x00 |
| 0x00 5086 | | DMA1_C1M0ARL | DMA1 memory 0 address low register (channel 1) | 0x00 |
| 0x00 5087<br>0x00 5088 | Reserved area (2 byte) | | | |
| 0x00 5089 | DMA1 | DMA1_C2CR | DMA1 channel 2 configuration register | 0x00 |
| 0x00 508A | | DMA1_C2SPR | DMA1 channel 2 status & priority register | 0x00 |
| 0x00 508B | | DMA1_C2NDTR | DMA1 number of data to transfer register (channel 2) | 0x00 |
| 0x00 508C | | DMA1_C2PARH | DMA1 peripheral address high register (channel 2) | 0x52 |
| 0x00 508D | | DMA1_C2PARL | DMA1 peripheral address low register (channel 2) | 0x00 |
| 0x00 508E | | Reserved area (1 byte) | | |
| 0x00 508F | | DMA1_C2M0ARH | DMA1 memory 0 address high register (channel 2) | 0x00 |
| 0x00 5090 | | DMA1_C2M0ARL | DMA1 memory 0 address low register (channel 2) | 0x00 |
| 0x00 5091<br>0x00 5092 | Reserved area (2 byte) | | | |
| 0x00 5093 | DMA1 | DMA1_C3CR | DMA1 channel 3 configuration register | 0x00 |
| 0x00 5094 | | DMA1_C3SPR | DMA1 channel 3 status & priority register | 0x00 |
| 0x00 5095 | | DMA1_C3NDTR | DMA1 number of data to transfer register (channel 3) | 0x00 |
| 0x00 5096 | | DMA1_C3PARH_ C3M1ARH | DMA1 peripheral address high register (channel 3) | 0x40 |
| 0x00 5097 | | DMA1_C3PARL_ C3M1ARL | DMA1 peripheral address low register (channel 3) | 0x00 |
| 0x00 5098 | | DMA_C3M0EAR | DMA channel 3 memory 0 extended address register | 0x00 |
| 0x00 5099 | | DMA1_C3M0ARH | DMA1 memory 0 address high register (channel 3) | 0x00 |
| 0x00 509A | | DMA1_C3M0ARL | DMA1 memory 0 address low register (channel 3) | 0x00 |
| 0x00 509B to 0x00 509C | Reserved area (3 byte) | | | |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 509D | SYSCFG | SYSCFG_RMPCR3 | Remapping register 3 | 0x00 |
| 0x00 509E | | SYSCFG_RMPCR1 | Remapping register 1 | 0x00 |
| 0x00 509F | | SYSCFG_RMPCR2 | Remapping register 2 | 0x00 |
| 0x00 50A0 | ITC - EXTI | EXTI_CR1 | External interrupt control register 1 | 0x00 |
| 0x00 50A1 | | EXTI_CR2 | External interrupt control register 2 | 0x00 |
| 0x00 50A2 | | EXTI_CR3 | External interrupt control register 3 | 0x00 |
| 0x00 50A3 | | EXTI_SR1 | External interrupt status register 1 | 0x00 |
| 0x00 50A4 | | EXTI_SR2 | External interrupt status register 2 | 0x00 |
| 0x00 50A5 | | EXTI_CONF1 | External interrupt port select register 1 | 0x00 |
| 0x00 50A6 | WFE | WFE_CR1 | WFE control register 1 | 0x00 |
| 0x00 50A7 | | WFE_CR2 | WFE control register 2 | 0x00 |
| 0x00 50A8 | | WFE_CR3 | WFE control register 3 | 0x00 |
| 0x00 50A9 | | WFE_CR4 | WFE control register 4 | 0x00 |
| 0x00 50AA | ITC - EXTI | EXTI_CR4 | External interrupt control register 4 | 0x00 |
| 0x00 50AB | | EXTI_CONF2 | External interrupt port select register 2 | 0x00 |
| 0x00 50A9 to 0x00 50AF | Reserved area (7 byte) | | | |
| 0x00 50B0 | RST | RST_CR | Reset control register | 0x00 |
| 0x00 50B1 | | RST_SR | Reset status register | 0x01 |
| 0x00 50B2 | PWR | PWR_CSR1 | Power control and status register 1 | 0x00 |
| 0x00 50B3 | | PWR_CSR2 | Power control and status register 2 | 0x00 |
| 0x00 50B4 to 0x00 50BF | Reserved area (12 byte) | | | |
| 0x00 50C0 | CLK | CLK_CKDIVR | Clock master divider register | 0x03 |
| 0x00 50C1 | | CLK_CRTCR | Clock RTC register | 0x00(1) |
| 0x00 50C2 | | CLK_ICKCR | Internal clock control register | 0x11 |
| 0x00 50C3 | | CLK_PCKENR1 | Peripheral clock gating register 1 | 0x00 |
| 0x00 50C4 | | CLK_PCKENR2 | Peripheral clock gating register 2 | 0x00 |
| 0x00 50C5 | | CLK_CCOR | Configurable clock control register | 0x00 |
| 0x00 50C6 | | CLK_ECKCR | External clock control register | 0x00 |
| 0x00 50C7 | | CLK_SCSR | System clock status register | 0x01 |
| 0x00 50C8 | | CLK_SWR | System clock switch register | 0x01 |
| 0x00 50C9 | | CLK_SWCR | Clock switch control register | 0xX0 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 50CA | CLK | CLK_CSSR | Clock security system register | 0x00 |
| 0x00 50CB | | CLK_CBEEPR | Clock BEEP register | 0x00 |
| 0x00 50CC | | CLK_HSICALR | HSI calibration register | 0xXX |
| 0x00 50CD | | CLK_HSITRIMR | HSI clock calibration trimming register | 0x00 |
| 0x00 50CE | | CLK_HSIUNLCKR | HSI unlock register | 0x00 |
| 0x00 50CF | | CLK_REGCSR | Main regulator control status register | 0bxx11 100X |
| 0x00 50D0 | | CLK_PCKENR3 | Peripheral clock gating register 3 | 0x00 |
| 0x00 50D1 to 0x00 50D2 | Reserved area (2 byte) | | | |
| 0x00 50D3 | WWDG | WWDG_CR | WWDG control register | 0x7F |
| 0x00 50D4 | | WWDG_WR | WWDR window register | 0x7F |
| 0x00 50D5 to 00 50DF | Reserved area (11 byte) | | | |
| 0x00 50E0 | IWDG | IWDG_KR | IWDG key register | 0xXX |
| 0x00 50E1 | | IWDG_PR | IWDG prescaler register | 0x00 |
| 0x00 50E2 | | IWDG_RLR | IWDG reload register | 0xFF |
| 0x00 50E3 to 0x00 50EF | Reserved area (13 byte) | | | |
| 0x00 50F0 | BEEP | BEEP_CSR1 | BEEP control/status register 1 | 0x00 |
| 0x00 50F1 0x00 50F2 | | Reserved area (2 byte) | | |
| 0x00 50F3 | | BEEP_CSR2 | BEEP control/status register 2 | 0x1F |
| 0x00 50F4 to0x00 513F | Reserved area (76 byte) | | | |
| 0x00 5140 | RTC | RTC_TR1 | Time register 1 | 0x00 |
| 0x00 5141 | | RTC_TR2 | Time register 2 | 0x00 |
| 0x00 5142 | | RTC_TR3 | Time register 3 | 0x00 |
| 0x00 5143 | Reserved area (1 byte) | | | |
| 0x00 5144 | RTC | RTC_DR1 | Date register 1 | 0x01 |
| 0x00 5145 | | RTC_DR2 | Date register 2 | 0x21 |
| 0x00 5146 | | RTC_DR3 | Date register 3 | 0x00 |
| 0x00 5147 | Reserved area (1 byte) | | | |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5148 | RTC | RTC_CR1 | Control register 1 | 0x00(1) |
| 0x00 5149 | | RTC_CR2 | Control register 2 | 0x00(1) |
| 0x00 514A | | RTC_CR3 | Control register 3 | 0x00(1) |
| 0x00 514B | | Reserved area (1 byte) | | |
| 0x00 514C | | RTC_ISR1 | Initialization and status register 1 | 0x01 |
| 0x00 514D | | RTC_ISR2 | Initialization and Status register 2 | 0x00 |
| 0x00 514E<br>0x00 514F | Reserved area (2 byte) | | | |
| 0x00 5150 | RTC | RTC_SPRERH | Synchronous prescaler register high | 0x00(1) |
| 0x00 5151 | | RTC_SPRERL | Synchronous prescaler register low | 0xFF(1) |
| 0x00 5152 | | RTC_APRER | Asynchronous prescaler register | 0x7F(1) |
| 0x00 5153 | Reserved area (1 byte) | | | |
| 0x00 5154 | RTC | RTC_WUTRH | Wakeup timer register high | 0xFF(1) |
| 0x00 5155 | | RTC_WUTRL | Wakeup timer register low | 0xFF(1) |
| 0x00 5156 | Reserved area (1 byte) | | | |
| 0x00 5157 | RTC | RTC_SSRL | Subsecond register low | 0x00 |
| 0x00 5158 | | RTC_SSRH | Subsecond register high | 0x00 |
| 0x00 5159 | | RTC_WPR | Write protection register | 0x00 |
| 0x00 5158 | | RTC_SSRH | Subsecond register high | 0x00 |
| 0x00 5159 | | RTC_WPR | Write protection register | 0x00 |
| 0x00 515A | | RTC_SHIFTRH | Shift register high | 0x00 |
| 0x00 515B | | RTC_SHIFTRL | Shift register low | 0x00 |
| 0x00 515C | | RTC_ALRMAR1 | Alarm A register 1 | 0x00(1) |
| 0x00 515D | | RTC_ALRMAR2 | Alarm A register 2 | 0x00(1) |
| 0x00 515E | | RTC_ALRMAR3 | Alarm A register 3 | 0x00(1) |
| 0x00 515F | | RTC_ALRMAR4 | Alarm A register 4 | 0x00(1) |
| 0x00 5160 to<br>0x00 5163 | Reserved area (4 byte) | | | |
| 0x00 5164 | RTC | RTC_ALRMASSRH | Alarm A subsecond register high | 0x00(1) |
| 0x00 5165 | | RTC_ALRMASSRL | Alarm A subsecond register low | 0x00(1) |
| 0x00 5166 | | RTC_ALRMASSMSKR | Alarm A masking register | 0x00(1) |
| 0x00 5167 to<br>0x00 5169 | Reserved area (3 byte) | | | |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 516A | RTC | RTC_CALRH | Calibration register high | 0x00(1) |
| 0x00 516B | | RTC_CALRL | Calibration register low | 0x00(1) |
| 0x00 516C | | RTC_TCR1 | Tamper control register 1 | 0x00(1) |
| 0x00 516D | | RTC_TCR2 | Tamper control register 2 | 0x00(1) |
| 0x00 516E to 0x00 518A | Reserved area | | | |
| 0x00 5190 | CSSLSE | CSSLSE_CSR | CSS on LSE control and status register | 0x00(1) |
| 0x00 519A to 0x00 51FF | Reserved area | | | |
| 0x00 5200 | SPI1 | SPI1_CR1 | SPI1 control register 1 | 0x00 |
| 0x00 5201 | | SPI1_CR2 | SPI1 control register 2 | 0x00 |
| 0x00 5202 | | SPI1_ICR | SPI1 interrupt control register | 0x00 |
| 0x00 5203 | | SPI1_SR | SPI1 status register | 0x02 |
| 0x00 5204 | | SPI1_DR | SPI1 data register | 0x00 |
| 0x00 5205 | | SPI1_CRCPR | SPI1 CRC polynomial register | 0x07 |
| 0x00 5206 | | SPI1_RXCRCR | SPI1 Rx CRC register | 0x00 |
| 0x00 5207 | | SPI1_TXCRCR | SPI1 Tx CRC register | 0x00 |
| 0x00 5208 to 0x00 520F | Reserved area (8 byte) | | | |
| 0x00 5210 | I2C1 | I2C1_CR1 | I2C1 control register 1 | 0x00 |
| 0x00 5211 | | I2C1_CR2 | I2C1 control register 2 | 0x00 |
| 0x00 5212 | | I2C1_FREQR | I2C1 frequency register | 0x00 |
| 0x00 5213 | | I2C1_OARL | I2C1 own address register low | 0x00 |
| 0x00 5214 | | I2C1_OARH | I2C1 own address register high | 0x00 |
| 0x00 5215 | | I2C1_OARH | I2C1 own address register for dual mode | 0x00 |
| 0x00 5216 | | I2C1_DR | I2C1 data register | 0x00 |
| 0x00 5217 | | I2C1_SR1 | I2C1 status register 1 | 0x00 |
| 0x00 5218 | | I2C1_SR2 | I2C1 status register 2 | 0x00 |
| 0x00 5219 | | I2C1_SR3 | I2C1 status register 3 | 0x0X |
| 0x00 521A | | I2C1_ITR | I2C1 interrupt control register | 0x00 |
| 0x00 521B | | I2C1_CCRL | I2C1 clock control register low | 0x00 |
| 0x00 521C | | I2C1_CCRH | I2C1 clock control register high | 0x00 |
| 0x00 521D | | I2C1_TRISER | I2C1 TRISE register | 0x02 |
| 0x00 521E | | I2C1_PECR | I2C1 packet error checking register | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 521F to 0x00 522F | Reserved area (17 byte) | | | |
| 0x00 5230 | USART1 | USART1_SR | USART1 status register | 0xC0 |
| 0x00 5231 | | USART1_DR | USART1 data register | 0xXX |
| 0x00 5232 | | USART1_BRR1 | USART1 baud rate register 1 | 0x00 |
| 0x00 5233 | | USART1_BRR2 | USART1 baud rate register 2 | 0x00 |
| 0x00 5234 | | USART1_CR1 | USART1 control register 1 | 0x00 |
| 0x00 5235 | | USART1_CR2 | USART1 control register 2 | 0x00 |
| 0x00 5236 | | USART1_CR3 | USART1 control register 3 | 0x00 |
| 0x00 5237 | | USART1_CR4 | USART1 control register 4 | 0x00 |
| 0x00 5238 | | USART1_CR5 | USART1 control register 5 | 0x00 |
| 0x00 5239 | | USART1_GTR | USART1 guard time register | 0x00 |
| 0x00 523A | | USART1_PSCR | USART1 prescaler register | 0x00 |
| 0x00 523B to 0x00 524F | Reserved area (21 byte) | | | |
| 0x00 5250 | TIM2 | TIM2_CR1 | TIM2 control register 1 | 0x00 |
| 0x00 5251 | | TIM2_CR2 | TIM2 control register 2 | 0x00 |
| 0x00 5252 | | TIM2_SMCR | TIM2 Slave mode control register | 0x00 |
| 0x00 5253 | | TIM2_ETR | TIM2 external trigger register | 0x00 |
| 0x00 5254 | | TIM2_DER | TIM2 DMA1 request enable register | 0x00 |
| 0x00 5255 | | TIM2_IER | TIM2 interrupt enable register | 0x00 |
| 0x00 5256 | | TIM2_SR1 | TIM2 status register 1 | 0x00 |
| 0x00 5257 | | TIM2_SR2 | TIM2 status register 2 | 0x00 |
| 0x00 5258 | | TIM2_EGR | TIM2 event generation register | 0x00 |
| 0x00 5259 | | TIM2_CCMR1 | TIM2 capture/compare mode register 1 | 0x00 |
| 0x00 525A | | TIM2_CCMR2 | TIM2 capture/compare mode register 2 | 0x00 |
| 0x00 525B | | TIM2_CCER1 | TIM2 capture/compare enable register 1 | 0x00 |
| 0x00 525C | | TIM2_CNTRH | TIM2 counter high | 0x00 |
| 0x00 525D | | TIM2_CNTRL | TIM2 counter low | 0x00 |
| 0x00 525E | | TIM2_PSCR | TIM2 prescaler register | 0x00 |
| 0x00 525F | | TIM2_ARRH | TIM2 auto-reload register high | 0xFF |
| 0x00 5260 | | TIM2_ARRL | TIM2 auto-reload register low | 0xFF |
| 0x00 5261 | | TIM2_CCR1H | TIM2 capture/compare register 1 high | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5262 | TIM2 | TIM2_CCR1L | TIM2 capture/compare register 1 low | 0x00 |
| 0x00 5263 | | TIM2_CCR2H | TIM2 capture/compare register 2 high | 0x00 |
| 0x00 5264 | | TIM2_CCR2L | TIM2 capture/compare register 2 low | 0x00 |
| 0x00 5265 | | TIM2_BKR | TIM2 break register | 0x00 |
| 0x00 5266 | | TIM2_OISR | TIM2 output idle state register | 0x00 |
| 0x00 5267 to 0x00 527F | Reserved area (25 byte) | | | |
| 0x00 5280 | TIM3 | TIM3_CR1 | TIM3 control register 1 | 0x00 |
| 0x00 5281 | | TIM3_CR2 | TIM3 control register 2 | 0x00 |
| 0x00 5282 | | TIM3_SMCR | TIM3 Slave mode control register | 0x00 |
| 0x00 5283 | | TIM3_ETR | TIM3 external trigger register | 0x00 |
| 0x00 5284 | | TIM3_DER | TIM3 DMA1 request enable register | 0x00 |
| 0x00 5285 | | TIM3_IER | TIM3 interrupt enable register | 0x00 |
| 0x00 5286 | | TIM3_SR1 | TIM3 status register 1 | 0x00 |
| 0x00 5287 | | TIM3_SR2 | TIM3 status register 2 | 0x00 |
| 0x00 5288 | | TIM3_EGR | TIM3 event generation register | 0x00 |
| 0x00 5289 | | TIM3_CCMR1 | TIM3 Capture/Compare mode register 1 | 0x00 |
| 0x00 528A | | TIM3_CCMR2 | TIM3 Capture/Compare mode register 2 | 0x00 |
| 0x00 528B | | TIM3_CCER1 | TIM3 Capture/Compare enable register 1 | 0x00 |
| 0x00 528C | | TIM3_CNTRH | TIM3 counter high | 0x00 |
| 0x00 528D | | TIM3_CNTRL | TIM3 counter low | 0x00 |
| 0x00 528E | | TIM3_PSCR | TIM3 prescaler register | 0x00 |
| 0x00 528F | | TIM3_ARRH | TIM3 Auto-reload register high | 0xFF |
| 0x00 5290 | | TIM3_ARRL | TIM3 Auto-reload register low | 0xFF |
| 0x00 5291 | | TIM3_CCR1H | TIM3 Capture/Compare register 1 high | 0x00 |
| 0x00 5292 | | TIM3_CCR1L | TIM3 Capture/Compare register 1 low | 0x00 |
| 0x00 5293 | | TIM3_CCR2H | TIM3 Capture/Compare register 2 high | 0x00 |
| 0x00 5294 | | TIM3_CCR2L | TIM3 Capture/Compare register 2 low | 0x00 |
| 0x00 5295 | | TIM3_BKR | TIM3 break register | 0x00 |
| 0x00 5296 | | TIM3_OISR | TIM3 output idle state register | 0x00 |
| 0x00 5297 to 0x00 52AF | Reserved area (25 byte) | | | |

Table 9. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 52B0 | TIM1 | TIM1_CR1 | TIM1 control register 1 | 0x00 |
| 0x00 52B1 | | TIM1_CR2 | TIM1 control register 2 | 0x00 |
| 0x00 52B2 | | TIM1_SMCR | TIM1 Slave mode control register | 0x00 |
| 0x00 52B3 | | TIM1_ETR | TIM1 external trigger register | 0x00 |
| 0x00 52B4 | | TIM1_DER | TIM1 DMA1 request enable register | 0x00 |
| 0x00 52B5 | | TIM1_IER | TIM1 Interrupt enable register | 0x00 |
| 0x00 52B6 | | TIM1_SR1 | TIM1 status register 1 | 0x00 |
| 0x00 52B7 | | TIM1_SR2 | TIM1 status register 2 | 0x00 |
| 0x00 52B8 | | TIM1_EGR | TIM1 event generation register | 0x00 |
| 0x00 52B9 | | TIM1_CCMR1 | TIM1 Capture/Compare mode register 1 | 0x00 |
| 0x00 52BA | | TIM1_CCMR2 | TIM1 Capture/Compare mode register 2 | 0x00 |
| 0x00 52BB | | TIM1_CCMR3 | TIM1 Capture/Compare mode register 3 | 0x00 |
| 0x00 52BC | | TIM1_CCMR4 | TIM1 Capture/Compare mode register 4 | 0x00 |
| 0x00 52BD | | TIM1_CCER1 | TIM1 Capture/Compare enable register 1 | 0x00 |
| 0x00 52BE | | TIM1_CCER2 | TIM1 Capture/Compare enable register 2 | 0x00 |
| 0x00 52BF | | TIM1_CNTRH | TIM1 counter high | 0x00 |
| 0x00 52C0 | | TIM1_CNTRL | TIM1 counter low | 0x00 |
| 0x00 52C1 | | TIM1_PSCRH | TIM1 prescaler register high | 0x00 |
| 0x00 52C2 | | TIM1_PSCRL | TIM1 prescaler register low | 0x00 |
| 0x00 52C3 | | TIM1_ARRH | TIM1 Auto-reload register high | 0xFF |
| 0x00 52C4 | | TIM1_ARRL | TIM1 Auto-reload register low | 0xFF |
| 0x00 52C5 | | TIM1_RCR | TIM1 Repetition counter register | 0x00 |
| 0x00 52C6 | | TIM1_CCR1H | TIM1 Capture/Compare register 1 high | 0x00 |
| 0x00 52C7 | | TIM1_CCR1L | TIM1 Capture/Compare register 1 low | 0x00 |
| 0x00 52C8 | | TIM1_CCR2H | TIM1 Capture/Compare register 2 high | 0x00 |
| 0x00 52C9 | | TIM1_CCR2L | TIM1 Capture/Compare register 2 low | 0x00 |
| 0x00 52CA | | TIM1_CCR3H | TIM1 Capture/Compare register 3 high | 0x00 |
| 0x00 52CB | | TIM1_CCR3L | TIM1 Capture/Compare register 3 low | 0x00 |
| 0x00 52CC | | TIM1_CCR4H | TIM1 Capture/Compare register 4 high | 0x00 |
| 0x00 52CD | | TIM1_CCR4L | TIM1 Capture/Compare register 4 low | 0x00 |
| 0x00 52CE | | TIM1_BKR | TIM1 break register | 0x00 |
| 0x00 52CF | | TIM1_DTR | TIM1 dead-time register | 0x00 |
| 0x00 52D0 | | TIM1_OISR | TIM1 output idle state register | 0x00 |
| 0x00 52D1 | | TIM1_DCR1 | DMA1 control register 1 | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 52D2 | TIM1 | TIM1_DCR2 | TIM1 DMA1 control register 2 | 0x00 |
| 0x00 52D3 | | TIM1_DMA1R | TIM1 DMA1 address for burst mode | 0x00 |
| 0x00 52D4 to 0x00 52DF | Reserved area (12 byte) | | | |
| 0x00 52E0 | TIM4 | TIM4_CR1 | TIM4 control register 1 | 0x00 |
| 0x00 52E1 | | TIM4_CR2 | TIM4 control register 2 | 0x00 |
| 0x00 52E2 | | TIM4_SMCR | TIM4 Slave mode control register | 0x00 |
| 0x00 52E3 | | TIM4_DER | TIM4 DMA1 request enable register | 0x00 |
| 0x00 52E4 | | TIM4_IER | TIM4 Interrupt enable register | 0x00 |
| 0x00 52E5 | | TIM4_SR1 | TIM4 status register 1 | 0x00 |
| 0x00 52E6 | | TIM4_EGR | TIM4 Event generation register | 0x00 |
| 0x00 52E7 | | TIM4_CNTR | TIM4 counter | 0x00 |
| 0x00 52E8 | | TIM4_PSCR | TIM4 prescaler register | 0x00 |
| 0x00 52E9 | | TIM4_ARR | TIM4 Auto-reload register | 0x00 |
| 0x00 52EA to 0x00 52FE | Reserved area (21 byte) | | | |
| 0x00 52FF | IRTIM | IR_CR | Infrared control register | 0x00 |
| 0x00 5300 | TIM5 | TIM5_CR1 | TIM5 control register 1 | 0x00 |
| 0x00 5301 | | TIM5_CR2 | TIM5 control register 2 | 0x00 |
| 0x00 5302 | | TIM5_SMCR | TIM5 Slave mode control register | 0x00 |
| 0x00 5303 | | TIM5_ETR | TIM5 external trigger register | 0x00 |
| 0x00 5304 | | TIM5_DER | TIM5 DMA1 request enable register | 0x00 |
| 0x00 5305 | | TIM5_IER | TIM5 interrupt enable register | 0x00 |
| 0x00 5306 | | TIM5_SR1 | TIM5 status register 1 | 0x00 |
| 0x00 5307 | | TIM5_SR2 | TIM5 status register 2 | 0x00 |
| 0x00 5308 | | TIM5_EGR | TIM5 event generation register | 0x00 |
| 0x00 5309 | | TIM5_CCMR1 | TIM5 Capture/Compare mode register 1 | 0x00 |
| 0x00 530A | | TIM5_CCMR2 | TIM5 Capture/Compare mode register 2 | 0x00 |
| 0x00 530B | | TIM5_CCER1 | TIM5 Capture/Compare enable register 1 | 0x00 |
| 0x00 530C | | TIM5_CNTRH | TIM5 counter high | 0x00 |
| 0x00 530D | | TIM5_CNTRL | TIM5 counter low | 0x00 |
| 0x00 530E | | TIM5_PSCR | TIM5 prescaler register | 0x00 |
| 0x00 530F | | TIM5_ARRH | TIM5 Auto-reload register high | 0xFF |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5310 | TIM5 | TIM5_ARRL | TIM5 Auto-reload register low | 0xFF |
| 0x00 5311 | | TIM5_CCR1H | TIM5 Capture/Compare register 1 high | 0x00 |
| 0x00 5312 | | TIM5_CCR1L | TIM5 Capture/Compare register 1 low | 0x00 |
| 0x00 5313 | | TIM5_CCR2H | TIM5 Capture/Compare register 2 high | 0x00 |
| 0x00 5314 | | TIM5_CCR2L | TIM5 Capture/Compare register 2 low | 0x00 |
| 0x00 5315 | | TIM5_BKR | TIM5 break register | 0x00 |
| 0x00 5316 | | TIM5_OISR | TIM5 output idle state register | 0x00 |
| 0x00 5317 to 0x00 533F | Reserved area | | | |
| 0x00 5340 | ADC1 | ADC1_CR1 | ADC1 configuration register 1 | 0x00 |
| 0x00 5341 | | ADC1_CR2 | ADC1 configuration register 2 | 0x00 |
| 0x00 5342 | | ADC1_CR3 | ADC1 configuration register 3 | 0x1F |
| 0x00 5343 | | ADC1_SR | ADC1 status register | 0x00 |
| 0x00 5344 | | ADC1_DRH | ADC1 data register high | 0x00 |
| 0x00 5345 | | ADC1_DRL | ADC1 data register low | 0x00 |
| 0x00 5346 | | ADC1_HTRH | ADC1 high threshold register high | 0x0F |
| 0x00 5347 | | ADC1_HTRL | ADC1 high threshold register low | 0xFF |
| 0x00 5348 | | ADC1_LTRH | ADC1 low threshold register high | 0x00 |
| 0x00 5349 | | ADC1_LTRL | ADC1 low threshold register low | 0x00 |
| 0x00 534A | | ADC1_SQR1 | ADC1 channel sequence 1 register | 0x00 |
| 0x00 534B | | ADC1_SQR2 | ADC1 channel sequence 2 register | 0x00 |
| 0x00 534C | | ADC1_SQR3 | ADC1 channel sequence 3 register | 0x00 |
| 0x00 534D | | ADC1_SQR4 | ADC1 channel sequence 4 register | 0x00 |
| 0x00 534E | | ADC1_TRIGR1 | ADC1 trigger disable 1 | 0x00 |
| 0x00 534F | | ADC1_TRIGR2 | ADC1 trigger disable 2 | 0x00 |
| 0x00 5350 | | ADC1_TRIGR3 | ADC1 trigger disable 3 | 0x00 |
| 0x00 5351 | | ADC1_TRIGR4 | ADC1 trigger disable 4 | 0x00 |
| 0x00 5352 to 0x00 537F | Reserved area (46 byte) | | | |
| 0x00 5380 | DAC | DAC_CH1CR1 | DAC channel 1 control register 1 | 0x00 |
| 0x00 5381 | | DAC_CH1CR2 | DAC channel 1 control register 2 | 0x00 |
| 0x00 5382 | | DAC_CH2CR1 | DAC channel 2 control register 1 | 0x00 |
| 0x00 5383 | | DAC_CH2CR2 | DAC channel 2 control register 2 | 0x00 |
| 0x00 5384 | | DAC_SWTRIG | DAC software trigger register | 0x00 |
| 0x00 5385 | | DAC_SR | DAC status register | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5386 to 0x00 5387 | Reserved area (2 byte) | | | |
| 0x00 5388 | DAC | DAC_CH1RDHRH | DAC channel 1 right aligned data holding register high | 0x00 |
| 0x00 5389 | | DAC_CH1RDHRL | DAC channel 1 right aligned data holding register low | 0x00 |
| 0x00 538A to 0x00 538B | Reserved area (2 byte) | | | |
| 0x00 538C | DAC | DAC_CH1LDHRH | DAC channel 1 left aligned data holding register high | 0x00 |
| 0x00 538D | DAC | DAC_CH1LDHRL | DAC channel 1 left aligned data holding register low | 0x00 |
| 0x00 538E to 0x00 538F | Reserved area (2 byte) | | | |
| 0x00 5390 | DAC | DAC_CH1DHR8 | DAC channel 1 8-bit data holding register | 0x00 |
| 0x00 5391 to 0x00 5393 | Reserved area (3 byte) | | | |
| 0x00 5394 | DAC | DAC_CH2RDHRH | DAC channel 2 right aligned data holding register high | 0x00 |
| 0x00 5395 | | DAC_CH2RDHRL | DAC channel 2 right aligned data holding register low | 0x00 |
| 0x00 5396 to 0x00 5397 | Reserved area (2 byte) | | | |
| 0x00 5398 | DAC | DAC_CH2LDHRH | DAC channel 2 left aligned data holding register high | 0x00 |
| 0x00 5399 | | DAC_CH2LDHRL | DAC channel 2 left aligned data holding register low | 0x00 |
| 0x00 539A to 0x00 539B | Reserved area (2 byte) | | | |
| 0x00 539C | DAC | DAC_CH2DHR8 | DAC channel 2 8-bit data holding register | 0x00 |
| 0x00 539D to 0x00 539F | Reserved area (3 byte) | | | |
| 0x00 53A0 | DAC | DAC_DCH1RDHRH | DAC channel 1 right aligned data holding register high | 0x00 |
| 0x00 53A1 | | DAC_DCH1RDHRL | DAC channel 1 right aligned data holding register low | 0x00 |
| 0x00 53A2 to 0x00 53AB | Reserved area (3 byte) | | | |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 53AC | DAC | DAC_DORH | DAC data output register high | 0x00 |
| 0x00 53AD | | DAC_DORL | DAC data output register low | 0x00 |
| 0x00 53A2 | | DAC_DCH2RDHRH | DAC channel 2 right aligned data holding register high | 0x00 |
| 0x00 53A3 | | DAC_DCH2RDHRL | DAC channel 2 right aligned data holding register low | 0x00 |
| 0x00 53A4 | | DAC_DCH1LDHRH | DAC channel 1left aligned data holding register high | 0x00 |
| 0x00 53A5 | | DAC_DCH1LDHRL | DAC channel 1left aligned data holding register low | 0x00 |
| 0x00 53A6 | | DAC_DCH2LDHRH | DAC channel 2 left aligned data holding register high | 0x00 |
| 0x00 53A7 | | DAC_DCH2LDHRL | DAC channel 2 left aligned data holding register low | 0x00 |
| 0x00 53A8 | | DAC_DCH1DHR8 | DAC channel 1 8-bit mode data holding register | 0x00 |
| 0x00 53A9 | | DAC_DCH2DHR8 | DAC channel 2 8-bit mode data holding register | 0x00 |
| 0x00 53AA to 0x00 53AB | Reserved area (2 byte) | | | |
| 0x00 53AC | DAC | DAC_CH1DORH Reset value | DAC channel 1 data output register high | 0x00 |
| 0x00 53AD | | DAC_CH1DORL Reset value | DAC channel 1 data output register low | 0x00 |
| 0x00 53AE to 0x00 53AF | Reserved area (2 byte) | | | |
| 0x00 53B0 | DAC | DAC_CH2DORH Reset value | DAC channel 2 data output register high | 0x00 |
| 0x00 53B1 | | DAC_CH2DORL Reset value | DAC channel 2 data output register low | 0x00 |
| 0x00 53B2 to 0x00 53BF | Reserved area | | | |
| 0x00 53C0 | SPI2 | SPI2_CR1 | SPI2 control register 1 | 0x00 |
| 0x00 53C1 | | SPI2_CR2 | SPI2 control register 2 | 0x00 |
| 0x00 53C2 | | SPI2_ICR | SPI2 interrupt control register | 0x00 |
| 0x00 53C3 | | SPI2_SR | SPI2 status register | 0x02 |
| 0x00 53C4 | | SPI2_DR | SPI2 data register | 0x00 |
| 0x00 53C5 | | SPI2_CRCPR | SPI2 CRC polynomial register | 0x07 |
| 0x00 53C6 | | SPI2_RXCRCR | SPI2 Rx CRC register | 0x00 |
| 0x00 53C7 | | SPI2_TXCRCR | SPI2 Tx CRC register | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 53C8 to 0x00 53DF | Reserved area | | | |
| 0x00 53E0 | USART2 | USART2_SR | USART2 status register | 0xC0 |
| 0x00 53E1 | | USART2_DR | USART2 data register | 0xXX |
| 0x00 53E2 | | USART2_BRR1 | USART2 baud rate register 1 | 0x00 |
| 0x00 53E3 | | USART2_BRR2 | USART2 baud rate register 2 | 0x00 |
| 0x00 53E4 | | USART2_CR1 | USART2 control register 1 | 0x00 |
| 0x00 53E5 | | USART2_CR2 | USART2 control register 2 | 0x00 |
| 0x00 53E6 | | USART2_CR3 | USART2 control register 3 | 0x00 |
| 0x00 53E7 | | USART2_CR4 | USART2 control register 4 | 0x00 |
| 0x00 53E8 | | USART2_CR5 | USART2 control register 5 | 0x00 |
| 0x00 53E9 | | USART2_GTR | USART2 guard time register | 0x00 |
| 0x00 53EA | | USART2_PSCR | USART2 prescaler register | 0x00 |
| 0x00 53EB to 0x00 53EF | Reserved area | | | |
| 0x00 53F0 | USART3 | USART3_SR | USART3 status register | 0xC0 |
| 0x00 53F1 | | USART3_DR | USART3 data register | 0xXX |
| 0x00 53F2 | | USART3_BRR1 | USART3 baud rate register 1 | 0x00 |
| 0x00 53F3 | | USART3_BRR2 | USART3 baud rate register 2 | 0x00 |
| 0x00 53F4 | | USART3_CR1 | USART3 control register 1 | 0x00 |
| 0x00 53F5 | | USART3_CR2 | USART3 control register 2 | 0x00 |
| 0x00 53F6 | | USART3_CR3 | USART3 control register 3 | 0x00 |
| 0x00 53F7 | | USART3_CR4 | USART3 control register 4 | 0x00 |
| 0x00 53F8 | | USART3_CR5 | USART3 control register 5 | 0x00 |
| 0x00 53F9 | | USART3_GTR | USART3 guard time register | 0x00 |
| 0x00 53FA | | USART3_PSCR | USART3 prescaler register | 0x00 |
| 0x00 53FB to 0x00 53FF | Reserved area | | | |

Table 9. General hardware register map (continued)

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5400 | LCD | LCD_CR1 | LCD control register 1 | 0x00 |
| 0x00 5401 | | LCD_CR2 | LCD control register 2 | 0x00 |
| 0x00 5402 | | LCD_CR3 | LCD control register 3 | 0x00 |
| 0x00 5403 | | LCD_FRQ | LCD frequency selection register | 0x00 |
| 0x00 5404 | | LCD_PM0 | LCD Port mask register 0 | 0x00 |
| 0x00 5405 | | LCD_PM1 | LCD Port mask register 1 | 0x00 |
| 0x00 5406 | | LCD_PM2 | LCD Port mask register 2 | 0x00 |
| 0x00 5407 | | LCD_PM3 | LCD Port mask register 3 | 0x00 |
| 0x00 5408 | | LCD_PM4 | LCD Port mask register 4 | 0x00 |
| 0x00 5409 | | LCD_PM5 | LCD Port mask register 5 | 0x00 |
| 0x00 540A to 0x00 540B | Reserved area (2 byte) | | | |
| 0x00 540C | LCD | LCD_RAM0 | LCD display memory 0 | 0x00 |
| 0x00 540D | | LCD_RAM1 | LCD display memory 1 | 0x00 |
| 0x00 540E | | LCD_RAM2 | LCD display memory 2 | 0x00 |
| 0x00 540F | | LCD_RAM3 | LCD display memory 3 | 0x00 |
| 0x00 5410 | | LCD_RAM4 | LCD display memory 4 | 0x00 |
| 0x00 5411 | | LCD_RAM5 | LCD display memory 5 | 0x00 |
| 0x00 5412 | | LCD_RAM6 | LCD display memory 6 | 0x00 |
| 0x00 5413 | | LCD_RAM7 | LCD display memory 7 | 0x00 |
| 0x00 5414 | | LCD_RAM8 | LCD display memory 8 | 0x00 |
| 0x00 5415 | | LCD_RAM9 | LCD display memory 9 | 0x00 |
| 0x00 5416 | | LCD_RAM10 | LCD display memory 10 | 0x00 |
| 0x00 5417 | | LCD_RAM11 | LCD display memory 11 | 0x00 |
| 0x00 5418 | | LCD_RAM12 | LCD display memory 12 | 0x00 |
| 0x00 5419 | | LCD_RAM13 | LCD display memory 13 | 0x00 |
| 0x00 541A | | LCD_RAM14 | LCD display memory 14 | 0x00 |
| 0x00 541B | | LCD_RAM15 | LCD display memory 15 | 0x00 |
| 0x00 541C | | LCD_RAM16 | LCD display memory 16 | 0x00 |
| 0x00 541D | | LCD_RAM17 | LCD display memory 17 | 0x00 |
| 0x00 541E | | LCD_RAM18 | LCD display memory 18 | 0x00 |
| 0x00 541F | | LCD_RAM19 | LCD display memory 19 | 0x00 |
| 0x00 5420 | | LCD_RAM20 | LCD display memory 20 | 0x00 |
| 0x00 5421 | LCD | LCD_RAM21 | LCD display memory 21 | 0x00 |

**Table 9. General hardware register map (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 5422 to 0x00 542E | Reserved area | | | |
| 0x00 542F | LCD | LCD_CR4 | LCD control register 4 | 0x00 |
| 0x00 5430 | RI | Reserved area (1 byte) | | 0x00 |
| 0x00 5431 | | RI_ICR1 | Timer input capture routing register 1 | 0x00 |
| 0x00 5432 | | RI_ICR2 | Timer input capture routing register 2 | 0x00 |
| 0x00 5433 | | RI_IOIR1 | I/O input register 1 | 0xXX |
| 0x00 5434 | | RI_IOIR2 | I/O input register 2 | 0xXX |
| 0x00 5435 | | RI_IOIR3 | I/O input register 3 | 0xXX |
| 0x00 5436 | | RI_IOCMR1 | I/O control mode register 1 | 0x00 |
| 0x00 5437 | | RI_IOCMR2 | I/O control mode register 2 | 0x00 |
| 0x00 5438 | | RI_IOCMR3 | I/O control mode register 3 | 0x00 |
| 0x00 5439 | | RI_IOSR1 | I/O switch register 1 | 0x00 |
| 0x00 543A | | RI_IOSR2 | I/O switch register 2 | 0x00 |
| 0x00 543B | | RI_IOSR3 | I/O switch register 3 | 0x00 |
| 0x00 543C | | RI_IOGCR | I/O group control register | 0x3F |
| 0x00 543D | | RI_ASCR1 | Analog switch register 1 | 0x00 |
| 0x00 543E | | RI_ASCR2 | Analog switch register 2 | 0x00 |
| 0x00 543F | | RI_RCR | Resistor control register 1 | 0x00 |
| 0x00 5440 | COMP1/ COMP2 | COMP_CSR1 | Comparator control and status register 1 | 0x00 |
| 0x00 5441 | | COMP_CSR2 | Comparator control and status register 2 | 0x00 |
| 0x00 5442 | | COMP_CSR3 | Comparator control and status register 3 | 0x00 |
| 0x00 5443 | | COMP_CSR4 | Comparator control and status register 4 | 0x00 |
| 0x00 5444 | | COMP_CSR5 | Comparator control and status register 5 | 0x00 |

1. These registers are not impacted by a system reset. They are reset at power-on.

**Table 10. CPU/SWIM/debug module/interrupt controller registers**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 7F00 | CPU(1) | A | Accumulator | 0x00 |
| 0x00 7F01 | | PCE | Program counter extended | 0x00 |
| 0x00 7F02 | | PCH | Program counter high | 0x00 |
| 0x00 7F03 | | PCL | Program counter low | 0x00 |
| 0x00 7F04 | | XH | X index register high | 0x00 |
| 0x00 7F05 | | XL | X index register low | 0x00 |
| 0x00 7F06 | | YH | Y index register high | 0x00 |
| 0x00 7F07 | | YL | Y index register low | 0x00 |
| 0x00 7F08 | | SPH | Stack pointer high | 0x03 |
| 0x00 7F09 | | SPL | Stack pointer low | 0xFF |
| 0x00 7F0A | | CCR | Condition code register | 0x28 |
| 0x00 7F0B to 0x00 7F5F | | Reserved area (85 byte) | | |
| 0x00 7F60 | CPU | CFG_GCR | Global configuration register | 0x00 |
| 0x00 7F70 | ITC-SPR | ITC_SPR1 | Interrupt Software priority register 1 | 0xFF |
| 0x00 7F71 | | ITC_SPR2 | Interrupt Software priority register 2 | 0xFF |
| 0x00 7F72 | | ITC_SPR3 | Interrupt Software priority register 3 | 0xFF |
| 0x00 7F73 | | ITC_SPR4 | Interrupt Software priority register 4 | 0xFF |
| 0x00 7F74 | | ITC_SPR5 | Interrupt Software priority register 5 | 0xFF |
| 0x00 7F75 | | ITC_SPR6 | Interrupt Software priority register 6 | 0xFF |
| 0x00 7F76 | | ITC_SPR7 | Interrupt Software priority register 7 | 0xFF |
| 0x00 7F77 | | ITC_SPR8 | Interrupt Software priority register 8 | 0xFF |
| 0x00 7F78 to 0x00 7F79 | Reserved area (2 byte) | | | |
| 0x00 7F80 | SWIM | SWIM_CSR | SWIM control status register | 0x00 |
| 0x00 7F81 to 0x00 7F8F | Reserved area (15 byte) | | | |

**Table 10. CPU/SWIM/debug module/interrupt controller registers (continued)**

| Address | Block | Register label | Register name | Reset status |
|---|---|---|---|---|
| 0x00 7F90 | DM | DM_BK1RE | DM breakpoint 1 register extended byte | 0xFF |
| 0x00 7F91 | | DM_BK1RH | DM breakpoint 1 register high byte | 0xFF |
| 0x00 7F92 | | DM_BK1RL | DM breakpoint 1 register low byte | 0xFF |
| 0x00 7F93 | | DM_BK2RE | DM breakpoint 2 register extended byte | 0xFF |
| 0x00 7F94 | | DM_BK2RH | DM breakpoint 2 register high byte | 0xFF |
| 0x00 7F95 | | DM_BK2RL | DM breakpoint 2 register low byte | 0xFF |
| 0x00 7F96 | | DM_CR1 | DM Debug module control register 1 | 0x00 |
| 0x00 7F97 | | DM_CR2 | DM Debug module control register 2 | 0x00 |
| 0x00 7F98 | | DM_CSR1 | DM Debug module control/status register 1 | 0x10 |
| 0x00 7F99 | | DM_CSR2 | DM Debug module control/status register 2 | 0x00 |
| 0x00 7F9A | | DM_ENFCTR | DM enable function register | 0xFF |
| 0x00 7F9B to 0x00 7F9F | Reserved area (5 byte) | | | |

1. Accessible by debug module only

# 6 Interrupt vector mapping

**Table 11. Interrupt mapping**

| IRQ No. | Source block | Description | Wakeup from Halt mode | Wakeup from Active-halt mode | Wakeup from Wait (WFI mode) | Wakeup from Wait (WFE mode)(1) | Vector address |
|---|---|---|---|---|---|---|---|
| - | RESET | Reset | Yes | Yes | Yes | Yes | 0x00 8000 |
| - | TRAP | Software interrupt | - | - | - | - | 0x00 8004 |
| 0 | TLI(2) | External Top level Interrupt | - | - | - | - | 0x00 8008 |
| 1 | FLASH | EOP/WR_PG_DIS | - | - | Yes | Yes(3) | 0x00 800C |
| 2 | DMA1 0/1 | DMA1 channels 0/1 | - | - | Yes | Yes(3) | 0x00 8010 |
| 3 | DMA1 2/3 | DMA1 channels 2/3 | - | - | Yes | Yes(3) | 0x00 8014 |
| 4 | RTC/LSE_ CSS | RTC alarm interrupt/LSE CSS interrupt | Yes | Yes | Yes | Yes | 0x00 8018 |
| 5 | EXTI E/F/PVD(4) | PortE/F interrupt/PVD interrupt | Yes | Yes | Yes | Yes(3) | 0x00 801C |
| 6 | EXTIB/G | External interrupt port B/G | Yes | Yes | Yes | Yes(3) | 0x00 8020 |
| 7 | EXTID/H | External interrupt port D/H | Yes | Yes | Yes | Yes(3) | 0x00 8024 |
| 8 | EXTI0 | External interrupt 0 | Yes | Yes | Yes | Yes(3) | 0x00 8028 |
| 9 | EXTI1 | External interrupt 1 | Yes | Yes | Yes | Yes(3) | 0x00 802C |
| 10 | EXTI2 | External interrupt 2 | Yes | Yes | Yes | Yes(3) | 0x00 8030 |
| 11 | EXTI3 | External interrupt 3 | Yes | Yes | Yes | Yes(3) | 0x00 8034 |
| 12 | EXTI4 | External interrupt 4 | Yes | Yes | Yes | Yes(3) | 0x00 8038 |
| 13 | EXTI5 | External interrupt 5 | Yes | Yes | Yes | Yes(3) | 0x00 803C |
| 14 | EXTI6 | External interrupt 6 | Yes | Yes | Yes | Yes(3) | 0x00 8040 |
| 15 | EXTI7 | External interrupt 7 | Yes | Yes | Yes | Yes(3) | 0x00 8044 |
| 16 | LCD | LCD interrupt | - | - | Yes | Yes | 0x00 8048 |
| 17 | CLK/ TIM1/ DAC | System clock switch/CSS interrupt/TIM1 break/DAC | - | - | Yes | Yes | 0x00 804C |
| 18 | COMP1/ COMP2 ADC1 | Comparator 1 and 2 interrupt/ADC1 | Yes | Yes | Yes | Yes(3) | 0x00 8050 |
| 19 | TIM2/ USART2 | TIM2 update /overflow/trigger/break/ USART2 transmission complete/transmit data register empty interrupt | - | - | Yes | Yes(3) | 0x00 8054 |

**Table 11. Interrupt mapping (continued)**

| IRQ No. | Source block | Description | Wakeup from Halt mode | Wakeup from Active-halt mode | Wakeup from Wait (WFI mode) | Wakeup from Wait (WFE mode)(1) | Vector address |
|---|---|---|---|---|---|---|---|
| 20 | TIM2/ USART2 | Capture/Compare/USART 2 interrupt | - | - | Yes | Yes(3) | 0x00 8058 |
| 21 | TIM3/ USART3 | TIM3 Update /Overflow/Trigger/Break/ USART3 transmission complete/transmit data register empty interrupt | - | - | Yes | Yes(3) | 0x00 805C |
| 22 | TIM3/ USART3 | TIM3 Capture/Compare/ USART3 Receive register data full/overrun/idle line detected/parity error/ interrupt | - | - | Yes | Yes(3) | 0x00 8060 |
| 23 | TIM1 | Update /overflow/trigger/ COM | - | - | - | Yes(3) | 0x00 8064 |
| 24 | TIM1 | Capture/Compare | - | - | - | Yes(3) | 0x00 8068 |
| 25 | TIM4 | Update/overflow/trigger | - | - | Yes | Yes(3) | 0x00 806C |
| 26 | SPI1 | End of Transfer | Yes | Yes | Yes | Yes(3) | 0x00 8070 |
| 27 | USART 1/ TIM5 | USART1 transmission complete/transmit data register empty/ TIM5 update/overflow/ trigger/break | - | - | Yes | Yes(3) | 0x00 8074 |
| 28 | USART 1/ TIM5 | USART1 Receive register data full/overrun/idle line detected/parity error/ TIM5 capture/compare | - | - | Yes | Yes(3) | 0x00 8078 |
| 29 | $I^2C1$/SPI2 | $I^2C1$ interrupt(5)/ SPI2 | Yes | Yes | Yes | Yes(3) | 0x00 807C |

1. The Low-power wait mode is entered when executing a WFE instruction in Low-power run mode.
2. The TLI interrupt is the logic OR between TIM2 overflow interrupt, and TIM4 overflow interrupts.
3. In WFE mode, this interrupt is served if it has been previously enabled. After processing the interrupt, the processor goes back to WFE mode. When this interrupt is configured as a wakeup event, the CPU wakes up and resumes processing.
4. The interrupt from PVD is logically OR-ed with Port E and F interrupts. Register EXTI_CONF allows to select between Port E and Port F interrupt (see *External interrupt port select register (EXTI_CONF)* in the RM0031).
5. The device is woken up from Halt or Active-halt mode only when the address received matches the interface address.

# 7 Option bytes

Option bytes contain configurations for device hardware features as well as the memory protection of the device. They are stored in a dedicated memory block.

All option bytes can be modified in ICP mode (with SWIM) by accessing the EEPROM address. See *Table 12* for details on option byte addresses.

The option bytes can also be modified 'on the fly' by the application in IAP mode, except for the ROP, UBC and PCODESIZE values which can only be taken into account when they are modified in ICP mode (with the SWIM).

Refer to the STM8L15x/STM8L16x Flash programming manual (PM0054) and STM8 SWIM and debug manual (UM0470) for information on SWIM programming procedures.

**Table 12. Option byte addresses**

| Address | Option name | Option byte No. | Option bits | | | | | | | | Factory default setting |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| 00 4800 | Read-out protection (ROP) | OPT0 | ROP[7:0] | | | | | | | | 0xAA |
| 00 4802 | UBC (User Boot code size) | OPT1 | UBC[7:0] | | | | | | | | 0x00 |
| 00 4807 | PCODESIZE | OPT2 | PCODE[7:0] | | | | | | | | 0x00 |
| 00 4808 | Independent watchdog option | OPT3 [3:0] | Reserved | | | | WWDG_HALT | WWDG_HW | IWDG_HALT | IWDG_HW | 0x00 |
| 00 4809 | Number of stabilization clock cycles for HSE and LSE oscillators | OPT4 | Reserved | | | | LSECNT[1:0] | | HSECNT[1:0] | | 0x00 |
| 00 480A | Brownout reset (BOR) | OPT5 [3:0] | Reserved | | | | BOR_TH | | | BOR_ON | 0x00 |
| 00 480B | Bootloader option bytes (OPTBL) | OPTBL [15:0] | OPTBL[15:0] | | | | | | | | 0x00 |
| 00 480C | | | | | | | | | | | 0x00 |

**Table 13. Option byte description**

| Option byte no. | Option description |
|---|---|
| OPT0 | **ROP[7:0]** Memory readout protection (ROP)<br>0xAA: Disable readout protection (write access via SWIM protocol)<br>Refer to Readout protection section in the STM8L reference manual (RM0031). |
| OPT1 | **UBC[7:0]** Size of the user boot code area<br>UBC[7:0] Size of the user boot code area<br>0x00: No UBC<br>0x01: Page 0 reserved for the UBC and write protected.<br>...<br>0xFF: Page 0 to 254 reserved for the UBC and write-protected.<br>Refer to User boot code section in the STM8L reference manual (RM0031). |
| OPT2 | **PCODESIZE[7:0]** Size of the proprietary code area<br>0x00: No proprietary code area<br>0x01: Page 0 reserved for the proprietary code and read/write protected.<br>...<br>0xFF: Page 0 to 254 reserved for the proprietary code and read/write protected.<br>Refer to Proprietary code area (PCODE) section in the STM8L reference manual (RM0031) for more details. |
| OPT3 | **IWDG_HW:** Independent watchdog<br>0: Independent watchdog activated by software<br>1: Independent watchdog activated by hardware |
| | **IWDG_HALT:** Independent watchdog off in Halt/Active-halt<br>0: Independent watchdog continues running in Halt/Active-halt mode<br>1: Independent watchdog stopped in Halt/Active-halt mode |
| | **WWDG_HW:** Window watchdog<br>0: Window watchdog activated by software<br>1: Window watchdog activated by hardware |
| | **WWDG_HALT:** Window window watchdog reset on Halt/Active-halt<br>0: Window watchdog stopped in Halt mode<br>1: Window watchdog generates a reset when MCU enters Halt mode |
| OPT4 | **HSECNT**: Number of HSE oscillator stabilization clock cycles<br>0x00 - 1 clock cycle<br>0x01 - 16 clock cycles<br>0x10 - 512 clock cycles<br>0x11 - 4096 clock cycles |
| | **LSECNT**: Number of LSE oscillator stabilization clock cycles<br>0x00 - 1 clock cycle<br>0x01 - 16 clock cycles<br>0x10 - 512 clock cycles<br>0x11 - 4096 clock cycles |

**Table 13. Option byte description (continued)**

| Option byte no. | Option description |
|---|---|
| OPT5 | **BOR_ON**:<br>0: Brownout reset off<br>1: Brownout reset on |
| | **BOR_TH[3:1]**: Brownout reset thresholds. Refer to *Table 19* for details on the thresholds according to the value of BOR_TH bits. |
| OPTBL | **OPTBL[15:0]**:<br>This option is checked by the boot ROM code after reset. Depending on the content of addresses 00 480B, 00 480C and 0x8000 (reset vector) the CPU jumps to the bootloader or to the reset vector.<br>Refer to the UM0560 bootloader user manual for more details. |

# 8 Unique ID

STM8 devices feature a 96-bit unique device identifier which provides a reference number that is unique for any device and in any context. The 96 bits of the identifier can never be altered by the user.

The unique device identifier can be read in single bytes and may then be concatenated using a custom algorithm.

The unique device identifier is ideally suited:

- For use as serial numbers
- For use as security keys to increase the code security in the program memory while using and combining this unique ID with software cryptographic primitives and protocols before programming the internal memory.
- To activate secure boot processes

**Table 14. Unique ID registers (96 bits)**

| Address | Content description | Unique ID bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x4926 | X co-ordinate on the wafer | U_ID[7:0] | | | | | | | |
| 0x4927 | | U_ID[15:8] | | | | | | | |
| 0x4928 | Y co-ordinate on the wafer | U_ID[23:16] | | | | | | | |
| 0x4929 | | U_ID[31:24] | | | | | | | |
| 0x492A | Wafer number | U_ID[39:32] | | | | | | | |
| 0x492B | Lot number | U_ID[47:40] | | | | | | | |
| 0x492C | | U_ID[55:48] | | | | | | | |
| 0x492D | | U_ID[63:56] | | | | | | | |
| 0x492E | | U_ID[71:64] | | | | | | | |
| 0x492F | | U_ID[79:72] | | | | | | | |
| 0x4930 | | U_ID[87:80] | | | | | | | |
| 0x4931 | | U_ID[95:88] | | | | | | | |

# 9 Electrical parameters

## 9.1 Parameter conditions

Unless otherwise specified, all voltages are referred to $V_{SS}$.

### 9.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A$= 25 °C and $T_A$ = $T_A$ max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

### 9.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A$ = 25 °C, $V_{DD}$ = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

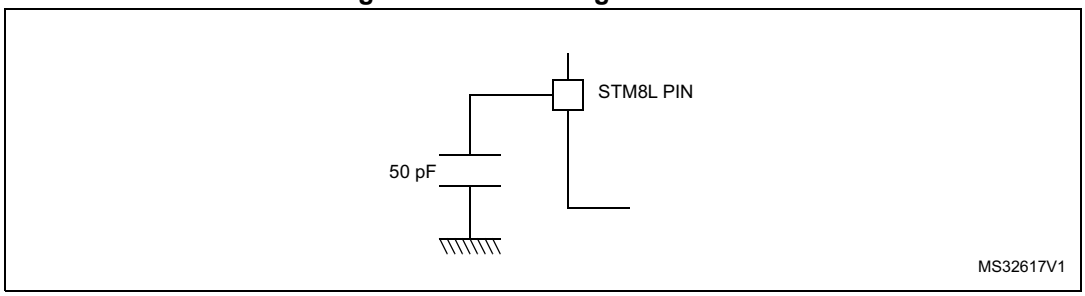
### 9.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 9.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

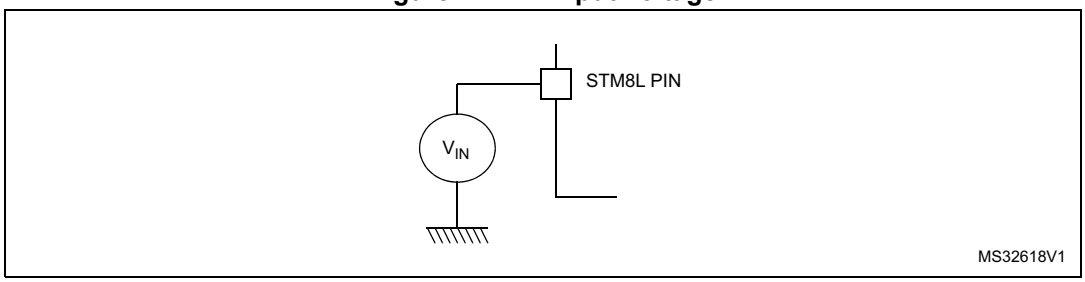
**Figure 11. Pin loading conditions**



### 9.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

**Figure 12. Pin input voltage**




## 9.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 15: Voltage characteristics*, *Table 16: Current characteristics*, and *Table 17: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect the device's reliability.

The device's mission profile (application conditions) is compliant with the JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

**Table 15. Voltage characteristics**

| Symbol | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$- $V_{SS}$ | External supply voltage (including $V_{DDA}$)(1) | - 0.3 | 4.0 | V |
| $V_{IN}$(2) | Input voltage on true open-drain pins (PC0 and PC1) | $V_{SS}$ - 0.3 | $V_{DD}$ + 4.0 | |
| | Input voltage on five-volt tolerant (FT) pins | $V_{SS}$ - 0.3 | $V_{DD}$ + 4.0 | |
| | Input voltage on any other pin | $V_{SS}$ - 0.3 | 4.0 | |
| $V_{ESD}$ | Electrostatic discharge voltage | see *Absolute maximum ratings (electrical sensitivity) on page 123* | | |

1. All power ($V_{DD1}$, $V_{DD2}$, $V_{DD3}$, $V_{DD4}$, $V_{DDA}$) and ground ($V_{SS1}$, $V_{SS2}$, $V_{SS3}$, $V_{SS4}$, $V_{SSA}$) pins must always be connected to the external power supply.
2. $V_{IN}$ maximum must always be respected. Refer to *Table 16.* for maximum allowed injected current values.

**Table 16. Current characteristics**

| Symbol | Ratings | Max. | Unit |
|---|---|---|---|
| $I_{VDD}$ | Total current into $V_{DD}$ power line (source) | 80 | mA |
| $I_{VSS}$ | Total current out of $V_{SS}$ ground line (sink) | 80 | |
| $I_{IO}$ | Output current sunk by IR_TIM pin (with high sink LED driver capability) | 80 | |
| | Output current sunk by any other I/O and control pin | 25 | |
| | Output current sourced by any I/Os and control pin | - 25 | |
| $I_{INJ(PIN)}$ | Injected current on true open-drain pins (PC0 and PC1)(1) | - 5 / +0 | |
| | Injected current on five-volt tolerant (FT) pins(1) | - 5 / +0 | |
| | Injected current on any other pin (2) | - 5 / +5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins) (3) | ± 25 | |

1. Positive injection is not possible on these I/Os. A negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15.* for maximum allowed input voltage values.
2. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to *Table 15.* for maximum allowed input voltage values.
3. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 17. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -65 to +150 | ° C |
| $T_J$ | Maximum junction temperature | 150 | |

## 9.3 Operating conditions

Subject to general operating conditions for $V_{DD}$ and $T_A$.

### 9.3.1 General operating conditions

**Table 18. General operating conditions**

| Symbol | Parameter | Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{SYSCLK}$(1) | System clock frequency | 1.65 V ≤$V_{DD}$ < 3.6 V | | 0 | 16 | MHz |
| $V_{DD}$ | Standard operating voltage | BOR detector disabled (D suffix version) | | 1.65 | 3.6 | V |
| | | BOR detector enabled | | 1.8(2) | | |
| $V_{DDA}$ | Analog operating voltage | ADC and DAC not used | Must be at the same potential as $V_{DD}$ | 1.65 | 3.6 | V |
| | | ADC or DAC used | | 1.8 | 3.6 | V |
| $P_D$(3) | Power dissipation at $T_A$= 85 °C for suffix 6 devices | LQFP80 | | - | 526 | mW |
| | | LQFP64 | | - | 416 | |
| | | UFQFPN48 | | - | 625 | |
| | | LQFP48 | | - | 307 | |
| | | WLCSP32 | | - | 317 | |
| | Power dissipation at $T_A$= 125 °C for suffix 3 devices and at $T_A$= 105 °C for suffix 7 devices | LQFP80 | | - | 131 | |
| | | LQFP64 | | - | 104 | |
| | | UFQFPN48 | | - | 156 | |
| | | LQFP48 | | - | 77 | |
| $T_A$ | Temperature range | 1.65 V ≤$V_{DD}$ < 3.6 V (6 suffix version) | | -40 | 85 | °C |
| | | 1.65 V ≤$V_{DD}$ < 3.6 V (7 suffix version) | | -40 | 105 | |
| | | 1.65 V ≤$V_{DD}$ < 3.6 V (3 suffix version) | | -40 | 125 | |
| $T_J$ | Junction temperature range | -40 °C ≤$T_A$ < 85 °C (6 suffix version) | | -40 | 105 | |
| | | -40 °C ≤ $T_A$ < 105 °C (7 suffix version) | | -40 | 110(4) | |
| | | -40 °C≤ $T_A$ < 125 °C (3 suffix version) | | -40 | 130(4) | |

1. $f_{SYSCLK} = f_{CPU}$
2. 1.8 V at power-up, 1.65 V at power-down if BOR is disabled by option byte
3. To calculate $P_{Dmax}(T_A)$, use the formula $P_{Dmax}=(T_{Jmax} - T_A)/\Theta_{JA}$ with $T_{Jmax}$ in this table and $\Theta_{JA}$ in “Thermal characteristics” table.
4. $T_{Jmax}$ is given by the test limit. Above this value the product behavior is not guaranteed.

### 9.3.2 Embedded reset and power control block characteristics

**Table 19. Embedded reset and power control block characteristics**

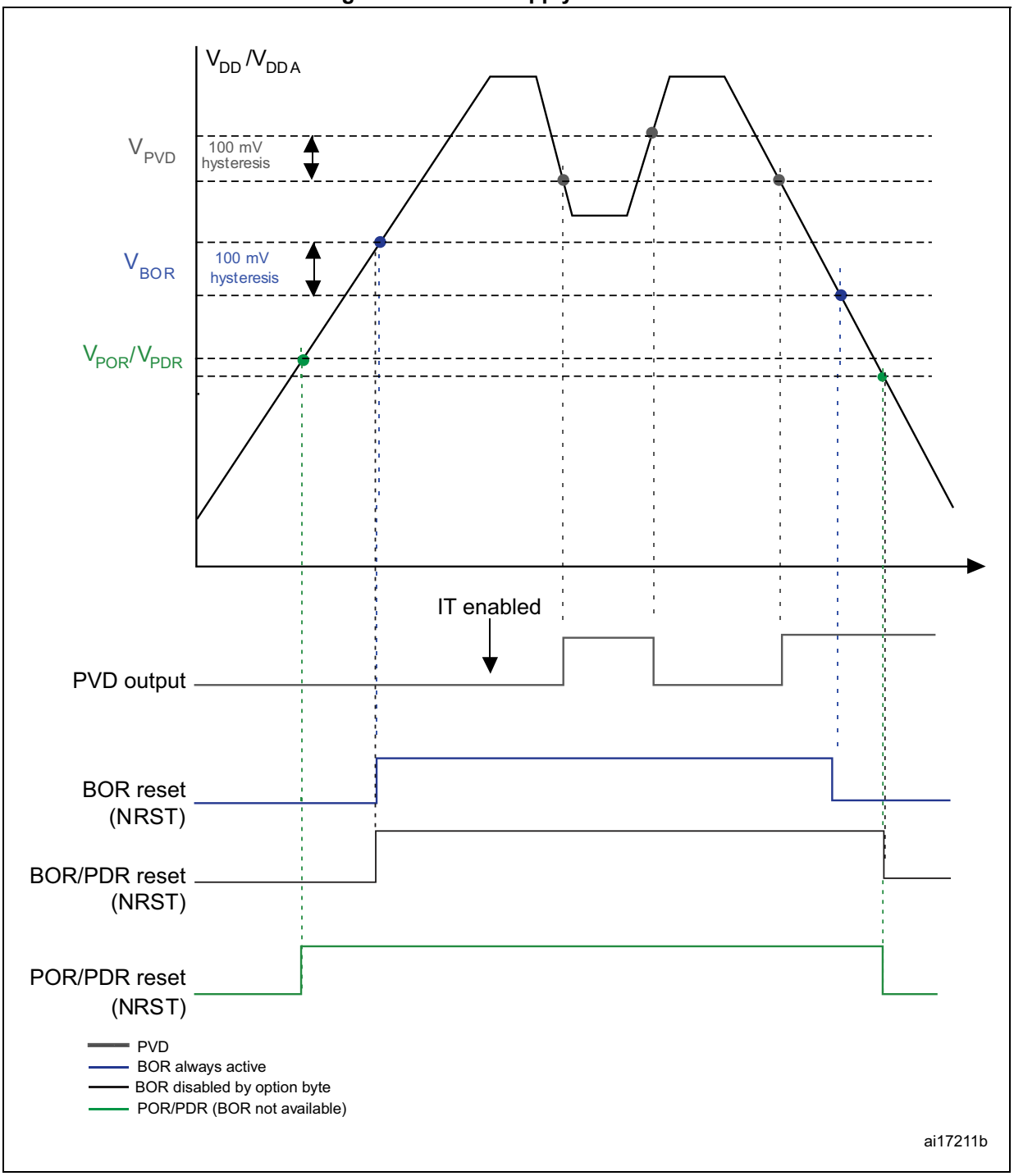
| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | BOR detector enabled | 0(1) | - | ∞(1) | µs/V |
| | | BOR detector disabled | 0(1) | - | 1(1) | ms/V |
| | $V_{DD}$ fall time rate | BOR detector enabled | 20(1) | - | ∞(1) | µs/V |
| | | BOR detector disabled | Reset below voltage functional range | | | |
| $t_{TEMP}$ | Reset release delay | $V_{DD}$ rising BOR detector enabled | - | 3 | - | ms |
| | | $V_{DD}$ rising BOR detector disabled | - | 1 | - | |
| $V_{POR}$ | Power-on reset threshold | Rising edge | 1.3(2) | 1.5 | 1.65 | V |
| $V_{PDR}$ | Power-down reset threshold | Falling edge | 1.3(2) | 1.5 | 1.65 | |
| $V_{BOR0}$ | Brown-out reset threshold 0 (BOR_TH[2:0]=000) | Falling edge | 1.67 | 1.7 | 1.74 | |
| | | Rising edge | 1.69 | 1.75 | 1.80 | |
| $V_{BOR1}$ | Brown-out reset threshold 1 (BOR_TH[2:0]=001) | Falling edge | 1.87 | 1.93 | 1.97 | |
| | | Rising edge | 1.96 | 2.04 | 2.07 | |
| $V_{BOR2}$ | Brown-out reset threshold 2 (BOR_TH[2:0]=010) | Falling edge | 2.22 | 2.3 | 2.35 | |
| | | Rising edge | 2.31 | 2.41 | 2.44 | |
| $V_{BOR3}$ | Brown-out reset threshold 3 (BOR_TH[2:0]=011) | Falling edge | 2.45 | 2.55 | 2.60 | |
| | | Rising edge | 2.54 | 2.66 | 2.7 | |
| $V_{BOR4}$ | Brown-out reset threshold 4 (BOR_TH[2:0]=100) | Falling edge | 2.68 | 2.80 | 2.85 | |
| | | Rising edge | 2.78 | 2.90 | 2.95 | |

**Table 19. Embedded reset and power control block characteristics (continued)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD0}$ | PVD threshold 0 | Falling edge | 1.80 | 1.84 | 1.88 | V |
| | | Rising edge | 1.88 | 1.94 | 1.99 | |
| $V_{PVD1}$ | PVD threshold 1 | Falling edge | 1.98 | 2.04 | 2.09 | |
| | | Rising edge | 2.08 | 2.14 | 2.18 | |
| $V_{PVD2}$ | PVD threshold 2 | Falling edge | 2.2 | 2.24 | 2.28 | |
| | | Rising edge | 2.28 | 2.34 | 2.38 | |
| $V_{PVD3}$ | PVD threshold 3 | Falling edge | 2.39 | 2.44 | 2.48 | |
| | | Rising edge | 2.47 | 2.54 | 2.58 | |
| $V_{PVD4}$ | PVD threshold 4 | Falling edge | 2.57 | 2.64 | 2.69 | |
| | | Rising edge | 2.68 | 2.74 | 2.79 | |
| $V_{PVD5}$ | PVD threshold 5 | Falling edge | 2.77 | 2.83 | 2.88 | |
| | | Rising edge | 2.87 | 2.94 | 2.99 | |
| $V_{PVD6}$ | PVD threshold 6 | Falling edge | 2.97 | 3.05 | 3.09 | |
| | | Rising edge | 3.08 | 3.15 | 3.20 | |
| Vhyst | Hysteresis voltage | BOR0 threshold | - | 40 | - | mV |
| | | All BOR and PVD thresholds excepting BOR0 | - | 100 | - | |

1. Data guaranteed by design.
2. Data based on characterization results.

**Figure 13. Power supply thresholds**



### 9.3.3 Supply current characteristics

#### Total current consumption

The MCU is placed under the following conditions:

- All I/O pins in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except if explicitly mentioned.

In the following table, data are based on characterization results, unless otherwise specified.

Subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 20. Total current consumption in Run mode**

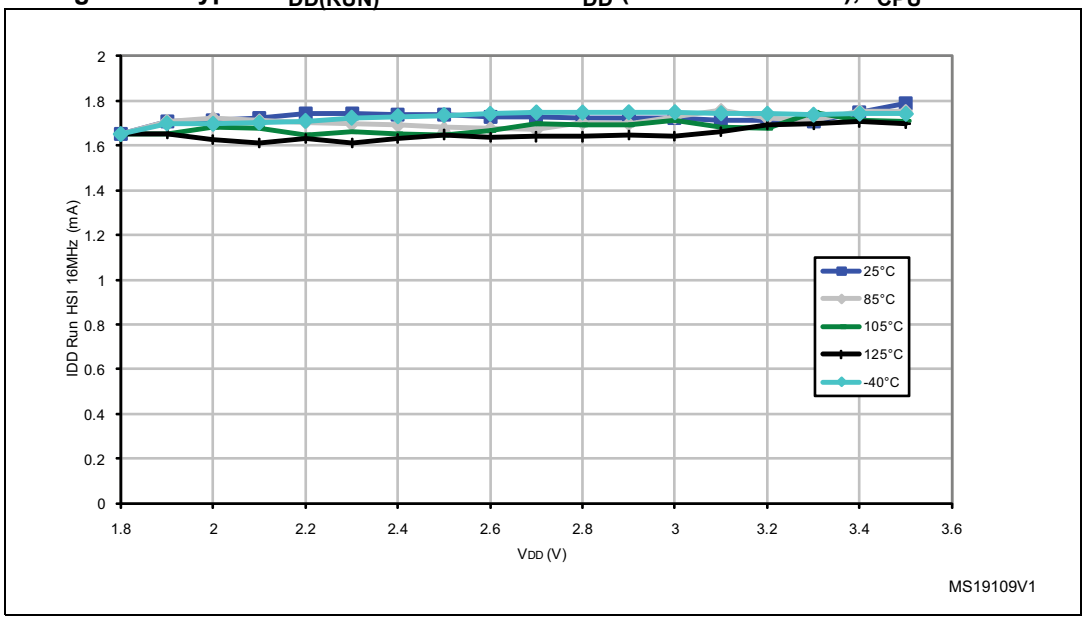
| Symbol | Para meter | Conditions(1) | | | Typ. | Max. | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 55°C | 85 °C (2) | 105 °C (3) | 125 °C (4) | |
| $I_{DD(RUN)}$ | Supply current in run mode (5) | All peripherals OFF, code executed from RAM, $V_{DD}$ from 1.65 V to 3.6 V | HSI RC osc. (16 MHz)(6) | $f_{CPU}$ = 125 kHz | 0.22 | 0.28 | 0.39 | 0.47 | 0.51 | mA |
| | | | | $f_{CPU}$ = 1 MHz | 0.32 | 0.38 | 0.49 | 0.57 | 0.61 | |
| | | | | $f_{CPU}$ = 4 MHz | 0.59 | 0.65 | 0.76 | 0.84 | 0.88 | |
| | | | | $f_{CPU}$ = 8 MHz | 0.93 | 0.99 | 1.1 | 1.18 | 1.22 | |
| | | | | $f_{CPU}$ = 16 MHz | 1.62 | 1.68 | 1.79(7) | 1.87(7) | 1.91(7) | |
| | | | HSE external clock ($f_{CPU}$=$f_{HSE}$) (8) | $f_{CPU}$ = 125 kHz | 0.21 | 0.25 | 0.35 | 0.44 | 0.49 | |
| | | | | $f_{CPU}$ = 1 MHz | 0.3 | 0.34 | 0.44 | 0.53 | 0.58 | |
| | | | | $f_{CPU}$ = 4 MHz | 0.57 | 0.61 | 0.71 | 0.8 | 0.85 | |
| | | | | $f_{CPU}$ = 8 MHz | 0.95 | 0.99 | 1.09 | 1.18 | 1.23 | |
| | | | | $f_{CPU}$ = 16 MHz | 1.73 | 1.77 | 1.87(7) | 1.96(7) | 2.01(7) | |
| | | | LSI RC osc. (typ. 38 kHz) | $f_{CPU}$ = $f_{LSI}$ | 0.029 | 0.035 | 0.039 | 0.044 | 0.055 | |
| | | | LSE external clock (32.768 kHz) | $f_{CPU}$ = $f_{LSE}$ | 0.028 | 0.034 | 0.038 | 0.042 | 0.054 | |

**Table 20. Total current consumption in Run mode (continued)**

| Symbol | Para meter | Conditions(1) | | | Typ. | Max. | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 55°C | 85 °C (2) | 105 °C (3) | 125 °C (4) | |
| $I_{DD(RUN)}$ | Supply current in Run mode | All peripherals OFF, code executed from Flash, $V_{DD}$ from 1.65 V to 3.6 V | HSI RC osc.(9) | $f_{CPU}$ = 125 kHz | 0.35 | 0.46 | 0.48 | 0.51 | 0.59 | mA |
| | | | | $f_{CPU}$ = 1 MHz | 0.54 | 0.65 | 0.67 | 0.7 | 0.78 | |
| | | | | $f_{CPU}$ = 4 MHz | 1.16 | 1.27 | 1.29 | 1.32 | 1.4 | |
| | | | | $f_{CPU}$ = 8 MHz | 1.97 | 2.08 | 2.1 | 2.13 | 2.21 | |
| | | | | $f_{CPU}$ = 16 MHz | 3.54 | 3.65 | 3.67 | 3.7 | 3.78 | |
| | | | HSE external clock ($f_{CPU}$=$f_{HSE}$) (8) | $f_{CPU}$ = 125 kHz | 0.35 | 0.44 | 0.46 | 0.49 | 0.58 | |
| | | | | $f_{CPU}$ = 1 MHz | 0.53 | 0.62 | 0.64 | 0.67 | 0.76 | |
| | | | | $f_{CPU}$ = 4 MHz | 1.13 | 1.22 | 1.24 | 1.27 | 1.36 | |
| | | | | $f_{CPU}$ = 8 MHz | 2 | 2.09 | 2.11 | 2.14 | 2.23 | |
| | | | | $f_{CPU}$ = 16 MHz | 3.69 | 3.78 | 3.8 | 3.83 | 3.92 | |
| | | | LSI RC osc. | $f_{CPU}$ = $f_{LSI}$ | 0.110 | 0.123 | 0.130 | 0.138 | 0.180 | |
| | | | LSE external clock (32.768 kHz)(10) | $f_{CPU}$ = $f_{LSE}$ | 0.100 | 0.101 | 0.104 | 0.119 | 0.163 | |

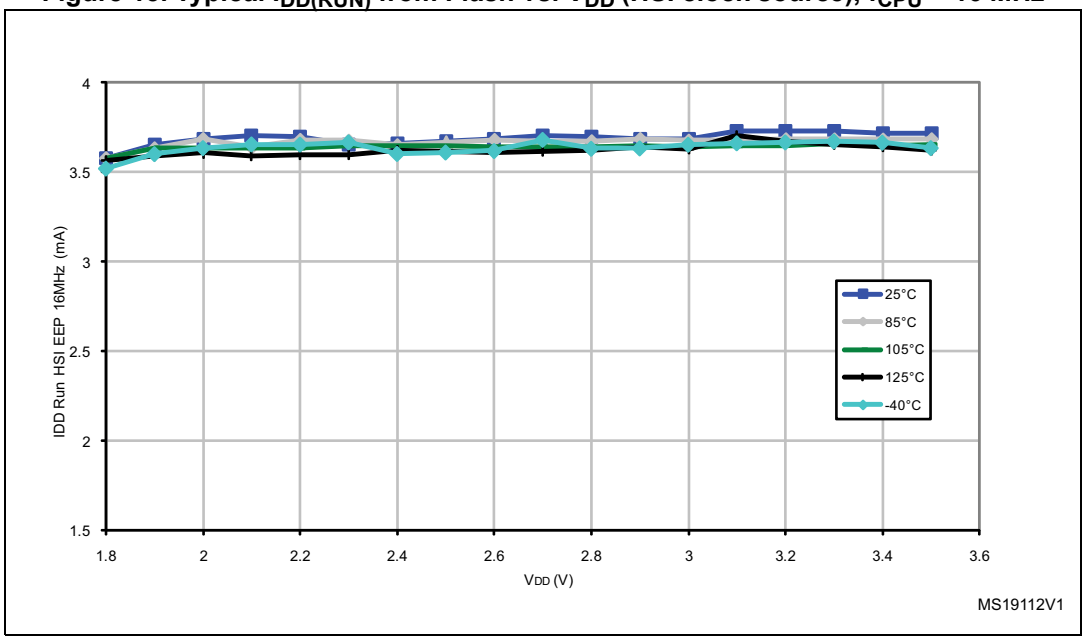
1. All peripherals OFF, $V_{DD}$ from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU}$=$f_{SYSCLK}$
2. For devices with suffix 6
3. For devices with suffix 7
4. For devices with suffix 3
5. CPU executing typical data processing
6. The run from RAM consumption can be approximated with the linear formula: $I_{DD}$(run_from_RAM) = Freq. * 95 µA/MHz + 250 µA
7. Tested in production.
8. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 31*.
9. The run from Flash consumption can be approximated with the linear formula: $I_{DD}$(run_from_Flash) = Freq. * 200 µA/MHz + 330 µA
10. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*

**Figure 14. Typical $I_{DD(RUN)}$ from RAM vs. $V_{DD}$ (HSI clock source), $f_{CPU}$ =16 MHz**




1. Typical current consumption measured with code executed from RAM.

**Figure 15. Typical $I_{DD(RUN)}$ from Flash vs. $V_{DD}$ (HSI clock source), $f_{CPU}$ = 16 MHz**




1. Typical current consumption measured with code executed from Flash.

In the following table, data are based on characterization results, unless otherwise specified.

**Table 21. Total current consumption in Wait mode**

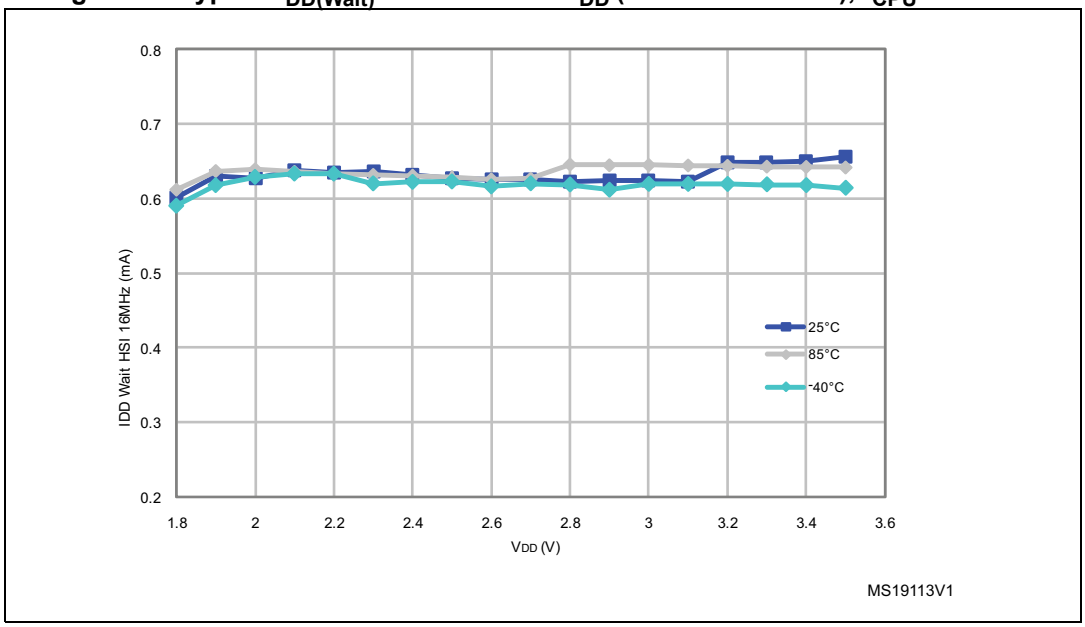
| Symbol | Parameter | Conditions[1] | | | Typ | Max | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 55°C | 85 °C (2) | 105 °C (3) | 125 °C (4) | |
| $I_{DD(Wait)}$ | Supply current in Wait mode | CPU not clocked, all peripherals OFF, code executed from RAM with Flash in $I_{DDQ}$ mode,(5) $V_{DD}$ from 1.65 V to 3.6 V | HSI | $f_{CPU}$ = 125 kHz | 0.21 | 0.29 | 0.33 | 0.36 | 0.43 | mA |
| | | | | $f_{CPU}$ = 1 MHz | 0.25 | 0.33 | 0.37 | 0.4 | 0.47 | |
| | | | | $f_{CPU}$ = 4 MHz | 0.32 | 0.4 | 0.44 | 0.47 | 0.54 | |
| | | | | $f_{CPU}$ = 8 MHz | 0.42 | 0.496 | 0.54 | 0.56 | 0.64 | |
| | | | | $f_{CPU}$ = 16 MHz | 0.66 | 0.736 | 0.78(6) | 0.8(6) | 0.88(6) | |
| | | | HSE external clock ($f_{CPU}$=$f_{HSE}$) (7) | $f_{CPU}$ = 125 kHz | 0.19 | 0.21 | 0.3 | 0.35 | 0.41 | |
| | | | | $f_{CPU}$ = 1 MHz | 0.2 | 0.23 | 0.32 | 0.36 | 0.43 | |
| | | | | $f_{CPU}$ = 4 MHz | 0.27 | 0.3 | 0.39 | 0.43 | 0.5 | |
| | | | | $f_{CPU}$ = 8 MHz | 0.37 | 0.4 | 0.49 | 0.53 | 0.6 | |
| | | | | $f_{CPU}$ = 16 MHz | 0.63 | 0.66 | 0.75(6) | 0.79(6) | 0.86(6) | |
| | | | LSI | $f_{CPU}$ = $f_{LSI}$ | 0.028 | 0.037 | 0.039 | 0.044 | 0.054 | |
| | | | LSE(8) external clock (32.768 kHz) | $f_{CPU}$ = $f_{LSE}$ | 0.027 | 0.035 | 0.038 | 0.042 | 0.051 | |

**Table 21. Total current consumption in Wait mode (continued)**

| Symbol | Parameter | Conditions[1] | | | Typ | Max | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | 55°C | 85 °C (2) | 105 °C (3) | 125 °C (4) | |
| $I_{DD(Wait)}$ | Supply current in Wait mode | CPU not clocked, all peripherals OFF, code executed from Flash, $V_{DD}$ from 1.65 V to 3.6 V | HSI | $f_{CPU}$ = 125 kHz | 0.27 | 0.36 | 0.42 | 0.46 | 0.51 | mA |
| | | | | $f_{CPU}$ = 1 MHz | 0.29 | 0.38 | 0.44 | 0.48 | 0.53 | |
| | | | | $f_{CPU}$ = 4 MHz | 0.37 | 0.46 | 0.52 | 0.56 | 0.61 | |
| | | | | $f_{CPU}$ = 8 MHz | 0.45 | 0.55 | 0.61 | 0.65 | 0.7 | |
| | | | | $f_{CPU}$ = 16 MHz | 0.69 | 0.79 | 0.85 | 0.89 | 0.94 | |
| | | | HSE[7] external clock ($f_{CPU}$= HSE) | $f_{CPU}$ = 125 kHz | 0.23 | 0.29 | 0.32 | 0.4 | 0.47 | |
| | | | | $f_{CPU}$ = 1 MHz | 0.24 | 0.31 | 0.34 | 0.41 | 0.48 | |
| | | | | $f_{CPU}$ = 4 MHz | 0.32 | 0.39 | 0.42 | 0.49 | 0.56 | |
| | | | | $f_{CPU}$ = 8 MHz | 0.42 | 0.49 | 0.51 | 0.59 | 0.66 | |
| | | | | $f_{CPU}$ = 16 MHz | 0.7 | 0.77 | 0.79 | 0.87 | 0.94 | |
| | | | LSI | $f_{CPU} = f_{LSI}$ | 0.037 | 0.085 | 0.105 | 0.123 | 0.153 | |
| | | | LSE[8] external clock (32.768 kHz) | $f_{CPU} = f_{LSE}$ | 0.036 | 0.082 | 0.095 | 0.119 | 0.133 | |

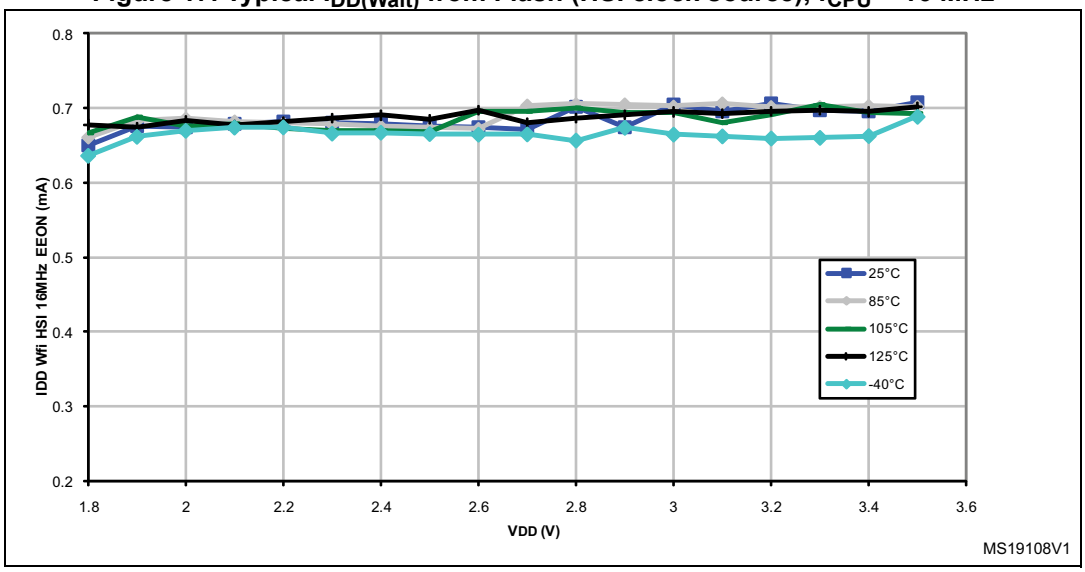
1. All peripherals OFF, $V_{DD}$ from 1.65 V to 3.6 V, HSI internal RC osc., $f_{CPU} = f_{SYSCLK}$
2. For devices with suffix 6.
3. For devices with suffix 7.
4. For devices with suffix 3.
5. Flash is configured in $I_{DDQ}$ mode in Wait mode by setting the EPM or WAITM bit in the Flash_CR1 register.
6. Tested in production.
7. Oscillator bypassed (HSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the HSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 31*.
8. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ HSE}$) must be added. Refer to *Table 32*

**Figure 16. Typical $I_{DD(Wait)}$ from RAM vs. $V_{DD}$ (HSI clock source), $f_{CPU}$ = 16 MHz**




1. Typical current consumption measured with code executed from RAM.

**Figure 17. Typical $I_{DD(Wait)}$ from Flash (HSI clock source), $f_{CPU}$ = 16 MHz**




1. Typical current consumption measured with code executed from Flash.

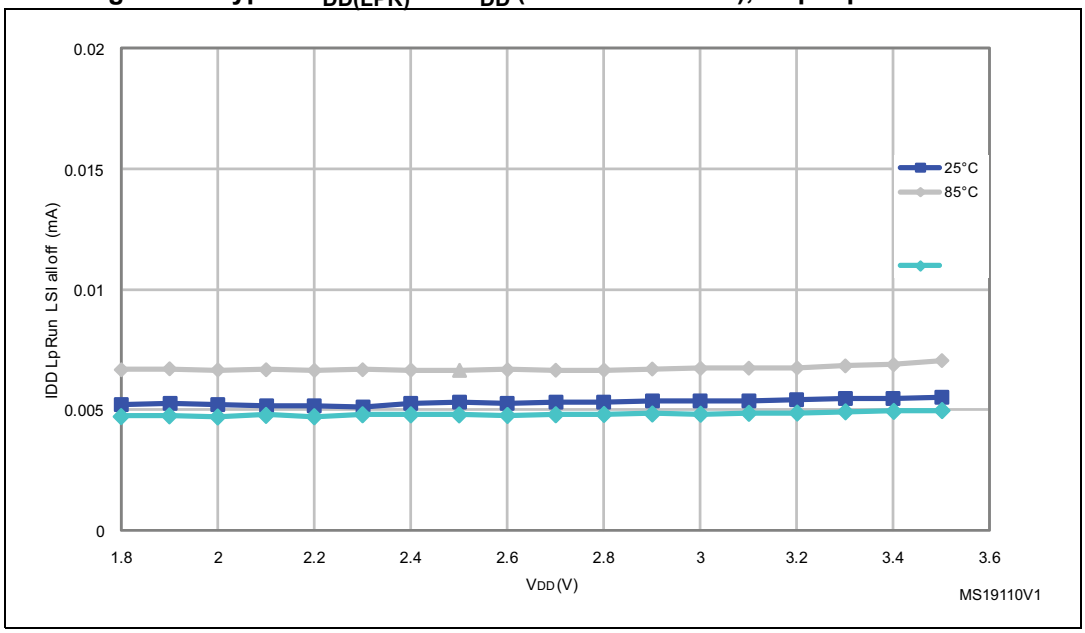
In the following table, data are based on characterization results, unless otherwise specified.

**Table 22. Total current consumption and timing in Low-power run mode at $V_{DD}$ = 1.65 V to 3.6 V**

| Symbol | Parameter | Conditions[1] | | | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(LPR)}$ | Supply current in Low-power run mode | LSI RC osc. (at 38 kHz) | all peripherals OFF | $T_A$ = -40 °C to 25 °C | 5.86 | 6.38 | µA |
| | | | | $T_A$ = 55 °C | 6.52 | 7.06 | |
| | | | | $T_A$ = 85 °C | 7.68 | 8.7 | |
| | | | | $T_A$ = 105 °C | 10.14 | 11.77 | |
| | | | | $T_A$ = 125 °C | 14.4 | 18.27 | |
| | | | with TIM2 active[2] | $T_A$ = -40 °C to 25 °C | 6.2 | 6.73 | |
| | | | | $T_A$ = 55 °C | 6.86 | 7.41 | |
| | | | | $T_A$ = 85 °C | 9.71 | 10.81 | |
| | | | | $T_A$ = 105 °C | 13.17 | 15.39 | |
| | | | | $T_A$ = 125 °C | 16.72 | 21.1 | |
| | | LSE [3] external clock (32.768 kHz) | all peripherals OFF | $T_A$ = -40 °C to 25 °C | 5.42 | 5.94 | |
| | | | | $T_A$ = 55 °C | 5.9 | 6.52 | |
| | | | | $T_A$ = 85 °C | 6.14 | 6.8 | |
| | | | | $T_A$ = 105 °C | 7.46 | 8.2 | |
| | | | | $T_A$ = 125 °C | 10.25 | 12.81 | |
| | | | with TIM2 active [2] | $T_A$ = -40 °C to 25 °C | 5.87 | 6.48 | |
| | | | | $T_A$ = 55 °C | 6.44 | 6.95 | |
| | | | | $T_A$ = 85 °C | 6.7 | 7.65 | |
| | | | | $T_A$ = 105 °C | 8.01 | 9.15 | |
| | | | | $T_A$ = 125 °C | 10.62 | 16.09 | |

1. No floating I/Os
2. Timer 2 clock enabled and counter running
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*

**Figure 18. Typical $I_{DD(LPR)}$ vs. $V_{DD}$ (LSI clock source), all peripherals OFF**



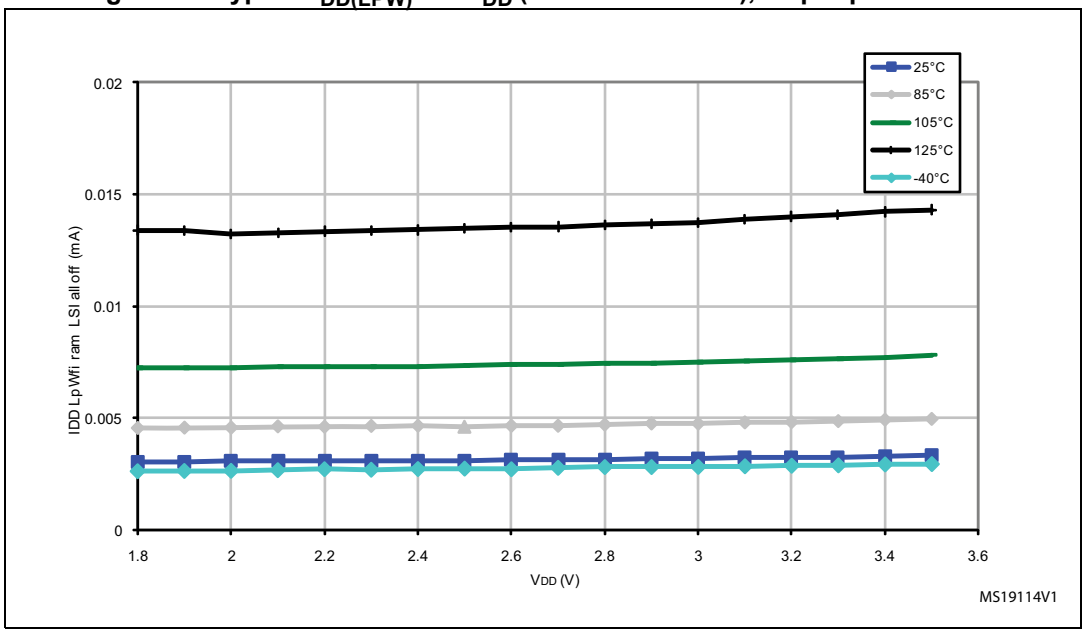
In the following table, data are based on characterization results, unless otherwise specified.

**Table 23. Total current consumption in Low-power wait mode at $V_{DD}$ = 1.65 V to 3.6 V**

| Symbol | Parameter | Conditions[1] | | | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(LPW)}$ | Supply current in Low-power wait mode | LSI RC osc. (at 38 kHz) | all peripherals OFF | $T_A$ = -40 °C to 25 °C | 3.03 | 3.41 | µA |
| | | | | $T_A$ = 55 °C | 3.38 | 3.78 | |
| | | | | $T_A$ = 85 °C | 4.6 | 5.34 | |
| | | | | $T_A$ = 105 °C | 7.25 | 8.84 | |
| | | | | $T_A$ = 125 °C | 11.89 | 16.18 | |
| | | | with TIM2 active[2] | $T_A$ = -40 °C to 25 °C | 3.78 | 4.21 | |
| | | | | $T_A$ = 55 °C | 4.13 | 4.57 | |
| | | | | $T_A$ = 85 °C | 5.29 | 6.08 | |
| | | | | $T_A$ = 105 °C | 7.54 | 9.13 | |
| | | | | $T_A$ = 125 °C | 12.47 | 15.56 | |
| | | LSE external clock[3] (32.768 kHz) | all peripherals OFF | $T_A$ = -40 °C to 25 °C | 2.46 | 2.89 | |
| | | | | $T_A$ = 55 °C | 2.58 | 3.07 | |
| | | | | $T_A$ = 85 °C | 3.32 | 4.05 | |
| | | | | $T_A$ = 105 °C | 4.63 | 6.17 | |
| | | | | $T_A$ = 125 °C | 7.52 | 11.68 | |
| | | | with TIM2 active [2] | $T_A$ = -40 °C to 25 °C | 2.88 | 3.29 | |
| | | | | $T_A$ = 55 °C | 2.97 | 3.42 | |
| | | | | $T_A$ = 85 °C | 3.69 | 4.55 | |
| | | | | $T_A$ = 105 °C | 5.09 | 6.78 | |
| | | | | $T_A$ = 125 °C | 7.91 | 12.15 | |

1. No floating I/Os.
2. Timer 2 clock enabled and counter is running.
3. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*.

**Figure 19. Typical $I_{DD(LPW)}$ vs. $V_{DD}$ (LSI clock source), all peripherals OFF**




1. Typical current consumption measured with code executed from RAM.

In the following table, data are based on characterization results, unless otherwise specified.

**Table 24. Total current consumption and timing in Active-halt mode at $V_{DD}$ = 1.65 V to 3.6 V**

| Symbol | Parameter | Conditions[1] | | | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(AH)}$ | Supply current in Active-halt mode | LSI RC (at 38 kHz) | LCD OFF[2] | $T_A$ = -40 °C to 25 °C | 0.92 | 2.25 | µA |
| | | | | $T_A$ = 55 °C | 1.32 | 3.44 | |
| | | | | $T_A$ = 85 °C | 1.63 | 3.87 | |
| | | | | $T_A$ = 105 °C | 3 | 7.94 | |
| | | | | $T_A$ = 125 °C | 5.6 | 13.8 | |
| | | | LCD ON (static duty/ external $V_{LCD}$) [3] | $T_A$ = -40 °C to 25 °C | 1.56 | 3.6 | |
| | | | | $T_A$ = 55 °C | 1.64 | 3.8 | |
| | | | | $T_A$ = 85 °C | 2.12 | 5.03 | |
| | | | | $T_A$ = 105 °C | 3.34 | 8.2 | |
| | | | | $T_A$ = 125 °C | 5.83 | 14.4 | |
| | | | LCD ON (1/4 duty/ external $V_{LCD}$) [4] | $T_A$ = -40 °C to 25 °C | 1.92 | 4.56 | |
| | | | | $T_A$ = 55 °C | 2.1 | 4.97 | |
| | | | | $T_A$ = 85 °C | 2.6 | 6.14 | |
| | | | | $T_A$ = 105 °C | 3.62 | 8.49 | |
| | | | | $T_A$ = 125 °C | 6.1 | 15.92 | |
| | | | LCD ON (1/4 duty/ internal $V_{LCD}$) [5] | $T_A$ = -40 °C to 25 °C | 4.2 | 9.88 | |
| | | | | $T_A$ = 55 °C | 4.39 | 10.32 | |
| | | | | $T_A$ = 85 °C | 4.84 | 11.5 | |
| | | | | $T_A$ = 105 °C | 5.98 | 15 | |
| | | | | $T_A$ = 125 °C | 7.21 | 18.07 | |

**Table 24. Total current consumption and timing in Active-halt mode at $V_{DD}$ = 1.65 V to 3.6 V (continued)**

| Symbol | Parameter | Conditions[1] | | | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{DD(AH)}$ | Supply current in Active-halt mode | LSE external clock (32.768 kHz) (6) | LCD OFF(7) | $T_A$ = -40 °C to 25 °C | 0.54 | 1.35 | µA |
| | | | | $T_A$ = 55 °C | 0.61 | 1.44 | |
| | | | | $T_A$ = 85 °C | 0.91 | 2.27 | |
| | | | | $T_A$ = 105 °C | 2.24 | 5.42 | |
| | | | | $T_A$ = 125 °C | 5.03 | 12 | |
| | | | LCD ON (static duty/ external $V_{LCD}$) (3) | $T_A$ = -40 °C to 25 °C | 0.91 | 2.13 | |
| | | | | $T_A$ = 55 °C | 1.05 | 2.55 | |
| | | | | $T_A$ = 85 °C | 1.42 | 3.65 | |
| | | | | $T_A$ = 105 °C | 2.63 | 6.35 | |
| | | | | $T_A$ = 125 °C | 5.24 | 13.15 | |
| | | | LCD ON (1/4 duty/ external $V_{LCD}$) (4) | $T_A$ = -40 °C to 25 °C | 1.6 | 2.84 | |
| | | | | $T_A$ = 55 °C | 1.76 | 4.37 | |
| | | | | $T_A$ = 85 °C | 2.14 | 5.23 | |
| | | | | $T_A$ = 105 °C | 3.37 | 8.5 | |
| | | | | $T_A$ = 125 °C | 5.92 | 15.19 | |
| | | | LCD ON (1/4 duty/ internal $V_{LCD}$) (5) | $T_A$ = -40 °C to 25 °C | 3.89 | 9.15 | |
| | | | | $T_A$ = 55 °C | 3.89 | 9.15 | |
| | | | | $T_A$ = 85 °C | 4.25 | 10.49 | |
| | | | | $T_A$ = 105 °C | 5.42 | 16.31 | |
| | | | | $T_A$ = 125 °C | 6.58 | 16.6 | |
| $I_{DD(WUFAH)}$ | Supply current during wakeup time from Active-halt mode (using HSI) | - | - | - | 2.4 | - | mA |
| $t_{WU_HSI(AH)}$ (8)(9) | Wakeup time from Active-halt mode to Run mode (using HSI) | - | - | - | 4.7 | 7 | µs |
| $t_{WU_LSI(AH)}$ (8)(9) | Wakeup time from Active-halt mode to Run mode (using LSI) | - | - | - | 150 | - | µs |

1. No floating I/O, unless otherwise specified.
2. RTC enabled. Clock source = LSI
3. RTC enabled, LCD enabled with external $V_{LCD}$ = 3 V, static duty, division ratio = 256, all pixels active, no LCD connected.
4. RTC enabled, LCD enabled with external $V_{LCD}$, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
5. LCD enabled with internal LCD booster $V_{LCD}$ = 3 V, 1/4 duty, 1/3 bias, division ratio = 64, all pixels active, no LCD connected.
6. Oscillator bypassed (LSEBYP = 1 in CLK_ECKCR). When configured for external crystal, the LSE consumption ($I_{DD\ LSE}$) must be added. Refer to *Table 32*

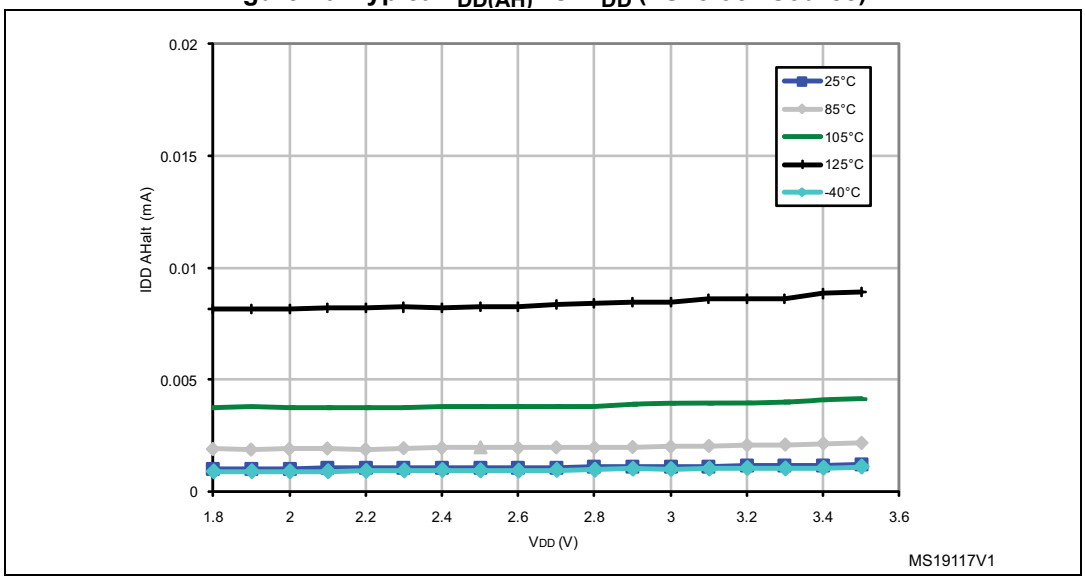
7. RTC enabled. Clock source = LSE
8. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after $t_{WU}$.
9. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register.

**Table 25. Typical current consumption in Active-halt mode, RTC clocked by LSE external crystal**

| Symbol | Parameter | Condition[1] | | Typ. | Unit |
|---|---|---|---|---|---|
| $I_{DD(AH)}$ [2] | Supply current in Active-halt mode | $V_{DD}$ = 1.8 V | LSE | 1.2 | µA |
| | | | LSE/32[3] | 0.9 | |
| | | $V_{DD}$ = 3 V | LSE | 1.4 | |
| | | | LSE/32[3] | 1.1 | |
| | | $V_{DD}$ = 3.6 V | LSE | 1.6 | |
| | | | LSE/32[3] | 1.3 | |

1. No floating I/O, unless otherwise specified.
2. Based on measurements on bench with 32.768 kHz external crystal oscillator.
3. RTC clock is LSE divided by 32.

**Figure 20. Typical $I_{DD(AH)}$ vs. $V_{DD}$ (LSI clock source)**



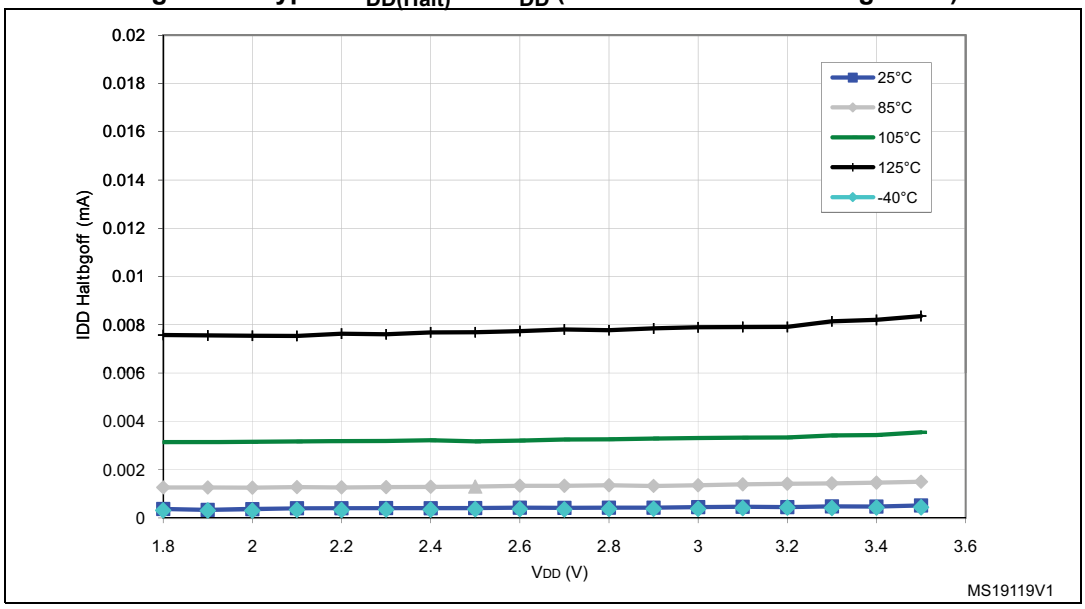
In the following table, data are based on characterization results, unless otherwise specified.

**Table 26. Total current consumption and timing in Halt mode at $V_{DD}$ = 1.65 to 3.6 V**

| Symbol | Parameter | Condition(1) | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $I_{DD(Halt)}$ | Supply current in Halt mode (Ultra-low-power ULP bit =1 in the PWR_CSR2 register) | $T_A$ = -40 °C to 25 °C | 400 | 1600(2) | nA |
| | | $T_A$ = 55 °C | 810 | 2400 | |
| | | $T_A$ = 85 °C | 1600 | 4500(2) | |
| | | $T_A$ = 105 °C | 2900 | 7700(2) | |
| | | $T_A$ = 125 °C | 5.6 | 18(2) | µA |
| $I_{DD(WUHalt)}$ | Supply current during wakeup time from Halt mode (using HSI) | | 2.4 | | mA |
| $t_{WU_HSI(Halt)}$(3)(4) | Wakeup time from Halt to Run mode (using HSI) | | 4.7 | 7 | µs |
| $t_{WU_LSI(Halt)}$(3)(4) | Wakeup time from Halt mode to Run mode (using LSI) | | 150 | | µs |

1. $T_A$ = -40 to 125 °C, no floating I/O, unless otherwise specified
2. Tested in production
3. ULP=0 or ULP=1 and FWU=1 in the PWR_CSR2 register
4. Wakeup time until start of interrupt vector fetch.
   The first word of interrupt routine is fetched 4 CPU cycles after $t_{WU}$

**Figure 21. Typical $I_{DD(Halt)}$ vs. $V_{DD}$ (internal reference voltage OFF)**



### Current consumption of on-chip peripherals

**Table 27. Peripheral current consumption**

| Symbol | Parameter | | Typ. $V_{DD}$ = 3.0 V | Unit |
|---|---|---|---|---|
| $I_{DD(TIM1)}$ | TIM1 supply current(1) | | 10 | µA/MHz |
| $I_{DD(TIM2)}$ | TIM2 supply current (1) | | 7 | |
| $I_{DD(TIM3)}$ | TIM3 supply current (1) | | 7 | |
| $I_{DD(TIM5)}$ | TIM5 supply current (1) | | 7 | |
| $I_{DD(TIM4)}$ | TIM4 timer supply current (1) | | 3 | |
| $I_{DD(USART1)}$ | USART1 supply current (2) | | 5 | |
| $I_{DD(USART2)}$ | USART2 supply current (2) | | 5 | |
| $I_{DD(USART3)}$ | USART3 supply current (2) | | 5 | |
| $I_{DD(SPI1)}$ | SPI1 supply current (2) | | 3 | |
| $I_{DD(SPI2)}$ | SPI2 supply current (2) | | 3 | |
| $I_{DD(I2C1)}$ | $I^2C1$ supply current (2) | | 4 | |
| $I_{DD(DMA1)}$ | DMA1 supply current(2) | | 3 | |
| $I_{DD(WWDG)}$ | WWDG supply current(2) | | 1 | |
| $I_{DD(ALL)}$ | Peripherals ON(3) | | 63 | |
| $I_{DD(ADC1)}$ | ADC1 supply current(4) | | 1500 | µA |
| $I_{DD(DAC)}$ | DAC supply current(5) | | 370 | |
| $I_{DD(COMP1)}$ | Comparator 1 supply current(6) | | 0.160 | |
| $I_{DD(COMP2)}$ | Comparator 2 supply current(6) | Slow mode | 2 | |
| | | Fast mode | 5 | |
| $I_{DD(PVD/BOR)}$ | Power voltage detector and brownout Reset unit supply current (7) | | 2.6 | |
| $I_{DD(BOR)}$ | Brownout Reset unit supply current (7) | | 2.4 | |
| $I_{DD(IDWDG)}$ | Independent watchdog supply current | including LSI supply current | 0.45 | |
| | | excluding LSI supply current | 0.05 | |

1. Data based on a differential $I_{DD}$ measurement between all peripherals OFF and a timer counter running at 16 MHz. The CPU is in Wait mode in both cases. No IC/OC programmed, no I/O pins toggling. Not tested in production.
2. Data based on a differential $I_{DD}$ measurement between the on-chip peripheral in reset configuration and not clocked and the on-chip peripheral when clocked and not kept under reset. The CPU is in Wait mode in both cases. No I/O pins toggling. Not tested in production.
3. Peripherals listed above the $I_{DD(ALL)}$ parameter ON: TIM1, TIM2, TIM3, TIM4, TIM5, USART1, USART2, USART3, SPI1, SPI2, I2C1, DMA1, WWDG.
4. Data based on a differential $I_{DD}$ measurement between ADC in reset configuration and continuous ADC conversion.

5. Data based on a differential $I_{DD}$ measurement between DAC in reset configuration and continuous DAC conversion of $V_{DD}$ /2. Floating DAC output.
6. Data based on a differential $I_{DD}$ measurement between COMP1 or COMP2 in reset configuration and COMP1 or COMP2 enabled with static inputs. Supply current of internal reference voltage excluded.
7. Including supply current of internal reference voltage.

**Table 28. Current consumption under external reset**

| Symbol | Parameter | Conditions | | Typ. | Unit |
|---|---|---|---|---|---|
| $I_{DD(RST)}$ | Supply current under external reset (1) | PB1/PB3/PA5 pins are externally tied to $V_{DD}$ | $V_{DD}$ = 1.8 V | 48 | µA |
| | | | $V_{DD}$ = 3 V | 80 | |
| | | | $V_{DD}$ = 3.6 V | 95 | |

1. All pins except PA0, PB0 and PB4 are floating under reset. PA0, PB0 and PB4 are configured with pull-up under reset. PB1, PB3 and PA5 must be tied externally under reset to avoid the consumption due to their schmitt trigger.

## 9.3.4 Clock and timing characteristics

### HSE external clock (HSEBYP = 1 in CLK_ECKCR)

Subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 29. HSE external clock characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE_ext}$ (1) | External clock source frequency | | 1 | | 16 | MHz |
| $V_{HSEH}$ | OSC_IN input pin high level voltage | | 0.7 x $V_{DD}$ | | $V_{DD}$ | V |
| $V_{HSEL}$ | OSC_IN input pin low level voltage | | $V_{SS}$ | | 0.3 x $V_{DD}$ | |
| $C_{in(HSE)}$ (1) | OSC_IN input capacitance | | | 2.6 | | pF |
| $I_{LEAK_HSE}$ | OSC_IN input leakage current | $V_{SS} < V_{IN} < V_{DD}$ | | | ±1 | µA |

1. Guaranteed by design.

### LSE external clock (LSEBYP=1 in CLK_ECKCR)

The LSE is available on STM8L151xx and STM8L152xx devices only.

Subject to general operating conditions for $V_{DD}$ and $T_A$.

**Table 30. LSE external clock characteristics**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{LSE_ext}$(1) | External clock source frequency | | 32.768 | | kHz |
| $V_{LSEH}$(2) | OSC32_IN input pin high level voltage | 0.7 x $V_{DD}$ | | $V_{DD}$ | V |
| $V_{LSEL}$(2) | OSC32_IN input pin low level voltage | $V_{SS}$ | | 0.3 x $V_{DD}$ | |
| $C_{in(LSE)}$(1) | OSC32_IN input capacitance | | 0.6 | | pF |
| $I_{LEAK_LSE}$ | OSC32_IN input leakage current | | | ±1 | µA |

1. Guaranteed by design.
2. Data based on characterization results.

### HSE crystal/ceramic resonator oscillator

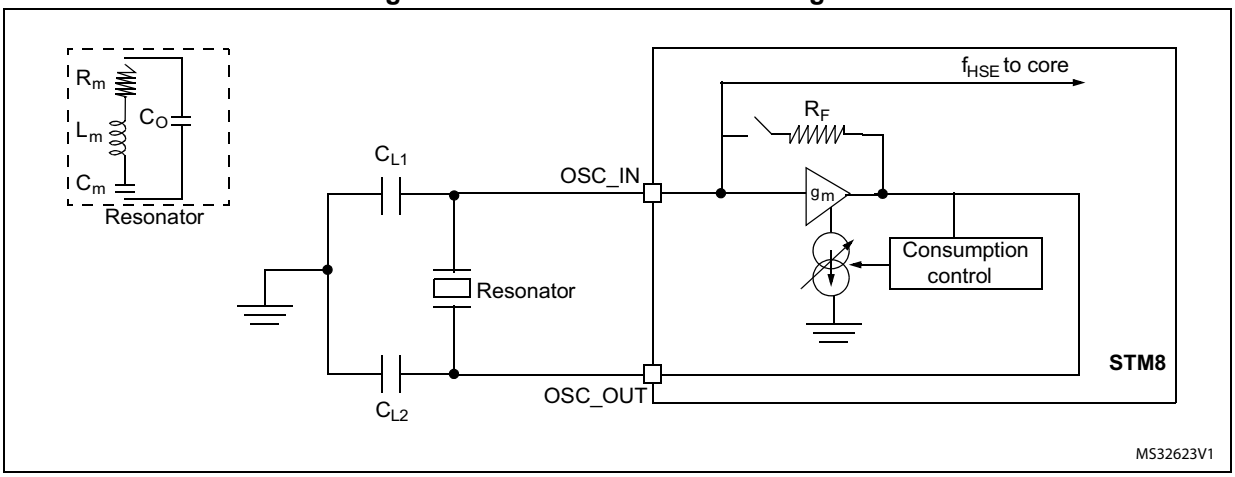
The HSE clock can be supplied with a 1 to 16 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

**Table 31. HSE oscillator characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{HSE}$ | High speed external oscillator frequency | | 1 | | 16 | MHz |
| $R_F$ | Feedback resistor | | | 200 | | kΩ |
| C(1)(2) | Recommended load capacitance | | | 20 | | pF |
| $I_{DD(HSE)}$ | HSE oscillator power consumption | C = 20 pF, $f_{OSC}$ = 16 MHz | | | 2.5 (startup) 0.7 (stabilized)(3) | mA |
| | | C = 10 pF, $f_{OSC}$ =16 MHz | | | 2.5 (startup) 0.46 (stabilized)(3) | |
| $g_m$ | Oscillator transconductance | | 3.5(3) | | | mA/V |
| $t_{SU(HSE)}$(4) | Startup time | $V_{DD}$ is stabilized | | 1 | | ms |

1. C=$C_{L1}$=$C_{L2}$ is approximately equivalent to 2 x crystal $C_{LOAD}$.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with small $R_m$ value. Refer to crystal manufacturer for more details
3. Guaranteed by design.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

**Figure 22. HSE oscillator circuit diagram**




### HSE oscillator critical $g_m$ formula

$$g_{mcrit} = (2 \times \Pi \times f_{HSE})^2 \times R_m(2Co + C)^2$$

$R_m$: Motional resistance (see crystal specification), $L_m$: Motional inductance (see crystal specification), $C_m$: Motional capacitance (see crystal specification), Co: Shunt capacitance (see crystal specification), $C_{L1}$=$C_{L2}$=C: Grounded external capacitance
$g_m >> g_{mcrit}$

## LSE crystal/ceramic resonator oscillator

The LSE is available on STM8L151x6/8 and STM8L152x6/8 devices.

The LSE clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph is based on characterization results with specified typical external components. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details (frequency, package, accuracy...).

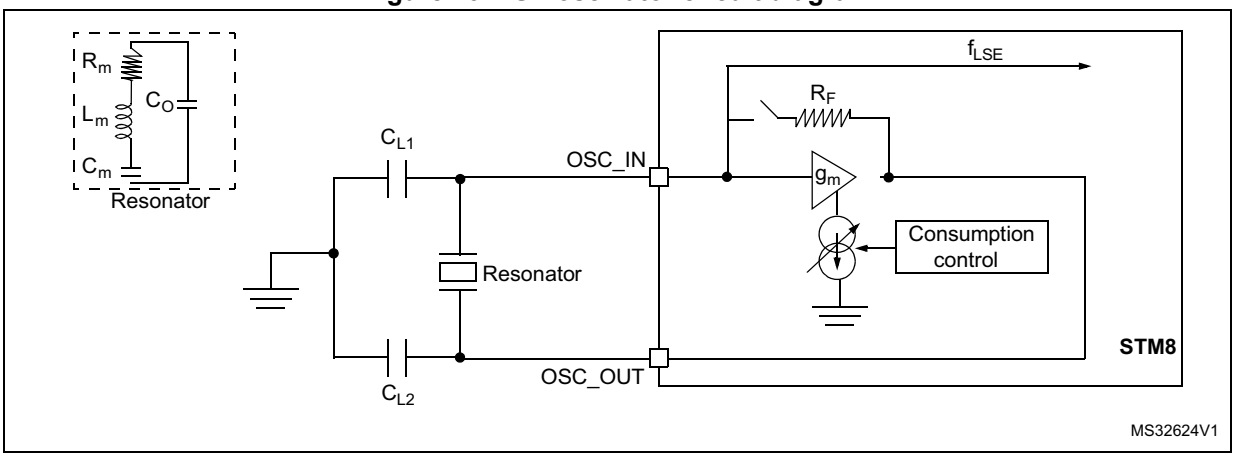
**Table 32. LSE oscillator characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE}$ | Low speed external oscillator frequency | | | 32.768 | | kHz |
| $R_F$ | Feedback resistor | $\Delta V$ = 200 mV | | 1.2 | | MΩ |
| $C^{(1)(2)}$ | Recommended load capacitance | | | 8 | | pF |
| $I_{DD(LSE)}$ | LSE oscillator power consumption | $V_{DD}$ = 1.8 V | | 450 | | nA |
| | | $V_{DD}$ = 3 V | | 600 | | |
| | | $V_{DD}$ = 3.6 V | | 750 | | |
| $g_m$ | Oscillator transconductance | | 3(3) | | | µA/V |
| $t_{SU(LSE)}^{(4)}$ | Startup time | $V_{DD}$ is stabilized | | 1 | | s |

1. C=$C_{L1}$=$C_{L2}$ is approximately equivalent to 2 x crystal $C_{LOAD}$.
2. The oscillator selection can be optimized in terms of supply current using a high quality resonator with a small $R_m$ value. Refer to crystal manufacturer for more details.
3. Guaranteed by design.

4. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

**Figure 23. LSE oscillator circuit diagram**




## Internal clock sources

Subject to general operating conditions for $V_{DD}$, and $T_A$.

## High speed internal RC oscillator (HSI)

In the following table, data are based on characterization results unless otherwise specified.

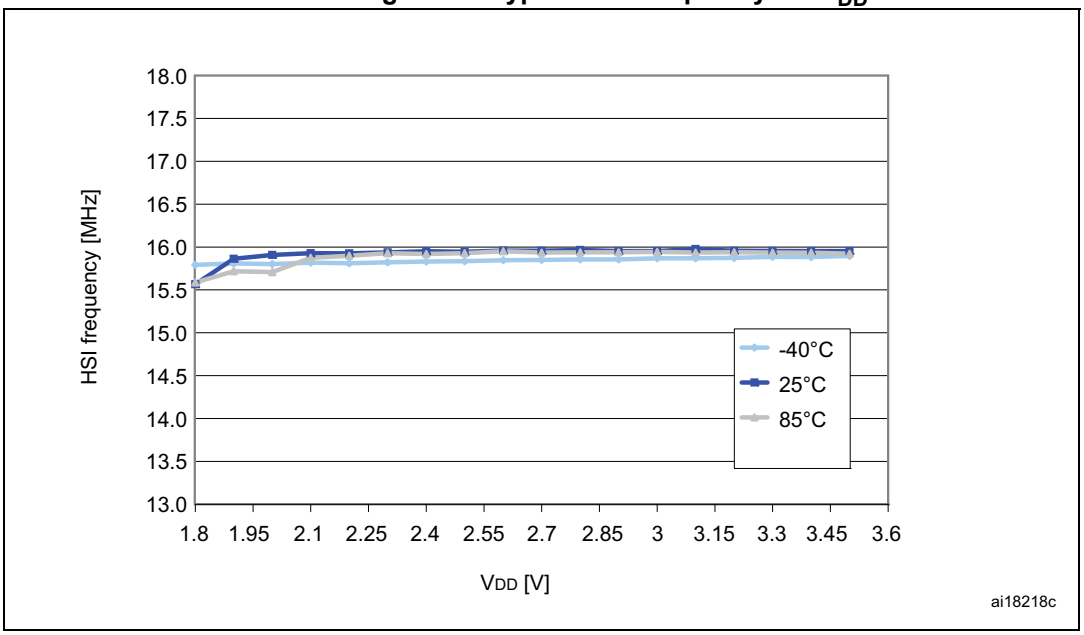
**Table 33. HSI oscillator characteristics**

| Symbol | Parameter | Conditions(1) | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | Frequency | $V_{DD}$ = 3.0 V | | 16 | | MHz |
| $ACC_{HSI}$ | Accuracy of HSI oscillator (factory calibrated) | $V_{DD}$ = 3.0 V, $T_A$ = 25 °C | -1 (2) | | 1 (2) | % |
| | | $V_{DD}$ = 3.0 V, 0 °C ≤$T_A$ ≤ 55 °C | -1.5 | | 1.5 | % |
| | | $V_{DD}$ = 3.0 V, -10 °C ≤$T_A$ ≤ 70 °C | -2 | | 2 | % |
| | | $V_{DD}$ = 3.0 V, -10 °C ≤$T_A$ ≤ 85 °C | -2.5 | | 2 | % |
| | | $V_{DD}$ = 3.0 V, -10 °C ≤$T_A$ ≤ 125 °C | -4.5 | | 2 | % |
| | | 1.65 V ≤$V_{DD}$ ≤ 3.6 V, -40 °C ≤$T_A$ ≤ 125 °C | -4.5 | | 3 | % |
| TRIM | HSI user trimming step(3) | Trimming code ≠ multiple of 16 | | 0.4 | 0.7 | % |
| | | Trimming code = multiple of 16 | | | ± 1.5 | % |
| $t_{su(HSI)}$ | HSI oscillator setup time (wakeup time) | | | 3.7 | 6 (4) | µs |
| $I_{DD(HSI)}$ | HSI oscillator power consumption | | | 100 | 140(4) | µA |

1. $V_{DD}$ = 3.0 V, $T_A$ = -40 to 125 °C unless otherwise specified.
2. Tested in production.
3. The trimming step differs depending on the trimming code. It is usually negative on the codes which are multiples of 16 (0x00, 0x10, 0x20, 0x30...0xE0). Refer to the AN3101 “STM8L15x internal RC oscillator calibration” application note for more details.

4. Guaranteed by design.

**Figure 24. Typical HSI frequency vs. $V_{DD}$**




## Low speed internal RC oscillator (LSI)

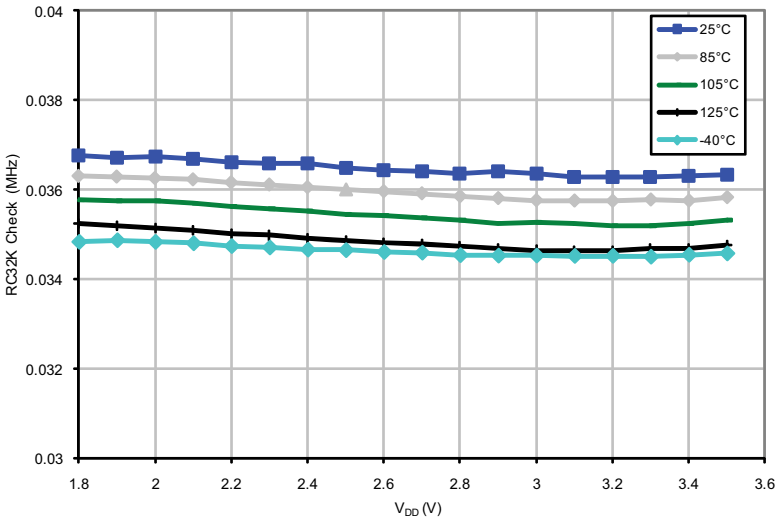
In the following table, data are based on characterization results.

**Table 34. LSI oscillator characteristics**

| Symbol | Parameter | Conditions(1) | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{LSI}$ | Frequency | | 26 | 38 | 56 | kHz |
| $t_{su(LSI)}$ | LSI oscillator wakeup time | | | | 200(2) | µs |
| $D_{(LSI)}$ | LSI oscillator frequency drift(3) | 0 °C ≤$T_A$≤85 °C | -12 | | 11 | % |

1. $V_{DD}$ = 1.65 V to 3.6 V, $T_A$ = -40 to 125 °C unless otherwise specified.
2. Guaranteed by design.
3. This is a deviation for an individual part, once the initial frequency has been measured.

Figure 25. Typical LSI clock source frequency vs. $V_{DD}$




## 9.3.5 Memory characteristics

$T_A$ = -40 to 125 °C unless otherwise specified.

Table 35. RAM and hardware registers

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{RM}$ | Data retention mode (1) | Halt mode (or Reset) | 1.65 | - | - | V |

1. Minimum supply voltage without losing data stored in RAM (in Halt mode or under Reset) or in hardware registers (only in Halt mode). Guaranteed by characterization.

## Flash memory

**Table 36. Flash program and data EEPROM memory**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. (1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage (all modes, read/write/erase) | $f_{SYSCLK}$ = 16 MHz | 1.65 | | 3.6 | V |
| $t_{prog}$ | Programming time for 1 or 128 bytes (block) erase/write cycles (on programmed byte) | - | - | 6 | - | ms |
| | Programming time for 1 to 128 bytes (block) write cycles (on erased byte) | - | - | 3 | - | |
| $I_{prog}$ | Programming/ erasing consumption | $T_A$=+25 °C, $V_{DD}$ = 3.0 V | - | 0.7 | - | mA |
| | | $T_A$=+25 °C, $V_{DD}$ = 1.8 V | - | | - | |
| $t_{RET}$ (2) | Data retention (program memory) after 10000 erase/write cycles at $T_A$=-40 to +85 °C (6 suffix) | $T_{RET}$=+85 °C | 30 (1) | - | - | years |
| | Data retention (program memory) after 10000 erase/write cycles at $T_A$=-40 to +125 °C (3 suffix) | $T_{RET}$=+125 °C | 5 (1) | - | - | |
| | Data retention (data memory) after 300000 erase/write cycles at $T_A$=-40 to +85 °C (6 suffix) | $T_{RET}$=+85 °C | 30 (1) | - | - | |
| | Data retention (data memory) after 300000 erase/write cycles at $T_A$=-40 to +125 °C (3 suffix) | $T_{RET}$=+125 °C | 5 (1) | - | - | |
| $N_{RW}$ (3) | Erase/write cycles (program memory) | $T_A$=-40 to +85 °C (6 suffix), $T_A$=-40 to +105 °C (7 suffix) or $T_A$=-40 to +125 °C (3 suffix) | 10 (1) | - | - | kcycles |
| | Erase/write cycles (data memory) | | 300 (1) (4) | - | - | |

1. Data based on characterization results.
2. Conforming to JEDEC JESD22a117
3. The physical granularity of the memory is 4 bytes, so cycling is performed on 4 bytes even when a write/erase operation addresses a single byte.
4. Data based on characterization performed on the whole data memory.

### 9.3.6 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

#### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error, out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation, LCD levels, etc.).

The test results are given in the following table.

**Table 37. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on true open-drain pins | -5 | +0 | mA |
| | Injected current on all 5 V tolerant (FT) pins | -5 | +0 | |
| | Injected current on any other pin | -5 | +5 | |

### 9.3.7 I/O port pin characteristics

#### General characteristics

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified. All unused pins must be kept at a fixed voltage: using the output mode of the I/O for example or an external pull-up or pull-down resistor.

**Table 38. I/O static characteristics**

| Symbol | Parameter | Conditions(1) | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low level voltage(2) | Input voltage on true open-drain pins (PC0 and PC1) | $V_{SS}$-0.3 | - | 0.3 x $V_{DD}$ | V |
| | | Input voltage on five-volt tolerant (FT) pins | $V_{SS}$-0.3 | - | 0.3 x $V_{DD}$ | |
| | | Input voltage on any other pin | $V_{SS}$-0.3 | - | 0.3 x $V_{DD}$ | |
| $V_{IH}$ | Input high level voltage (2) | Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD}$ < 2 V | 0.70 x $V_{DD}$ | - | 5.2 | V |
| | | Input voltage on true open-drain pins (PC0 and PC1) with $V_{DD} \geq 2$ V | | - | 5.5 | |
| | | Input voltage on five-volt tolerant (FT) pins with $V_{DD}$ < 2 V | 0.70 x $V_{DD}$ | - | 5.2 | |
| | | Input voltage on five-volt tolerant (FT) pins with $V_{DD} \geq 2$ V | | - | 5.5 | |
| | | Input voltage on any other pin | 0.70 x $V_{DD}$ | - | $V_{DD}$+0.3 | |
| $V_{hys}$ | Schmitt trigger voltage hysteresis (3) | Standard I/Os | - | 200 | - | mV |
| | | True open drain I/Os | - | 200 | - | |
| $I_{lkg}$ | Input leakage current (4) | $V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os | - | - | 50 (5) | nA |
| | | $V_{SS} \leq V_{IN} \leq V_{DD}$ True open drain I/Os | - | - | 200(5) | |
| | | $V_{SS} \leq V_{IN} \leq V_{DD}$ PA0 with high sink LED driver capability | - | - | 200(5) | |
| $R_{PU}$ | Weak pull-up equivalent resistor(2)(6) | $V_{IN}=V_{SS}$ | 30 | 45 | 60 | kΩ |
| $C_{IO}$ | I/O pin capacitance | - | - | 5 | - | pF |

1. $V_{DD}$ = 3.0 V, $T_A$ = -40 to 125 °C unless otherwise specified.
2. Data based on characterization results.
3. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
4. The max. value may be exceeded if negative current is injected on adjacent pins.
5. Not tested in production.
6. $R_{PU}$ pull-up equivalent resistor based on a resistive transistor (corresponding $I_{PU}$ current characteristics described in *Figure 29*).

Figure 26. Typical $V_{IL}$ and $V_{IH}$ vs. $V_{DD}$ (standard I/Os)

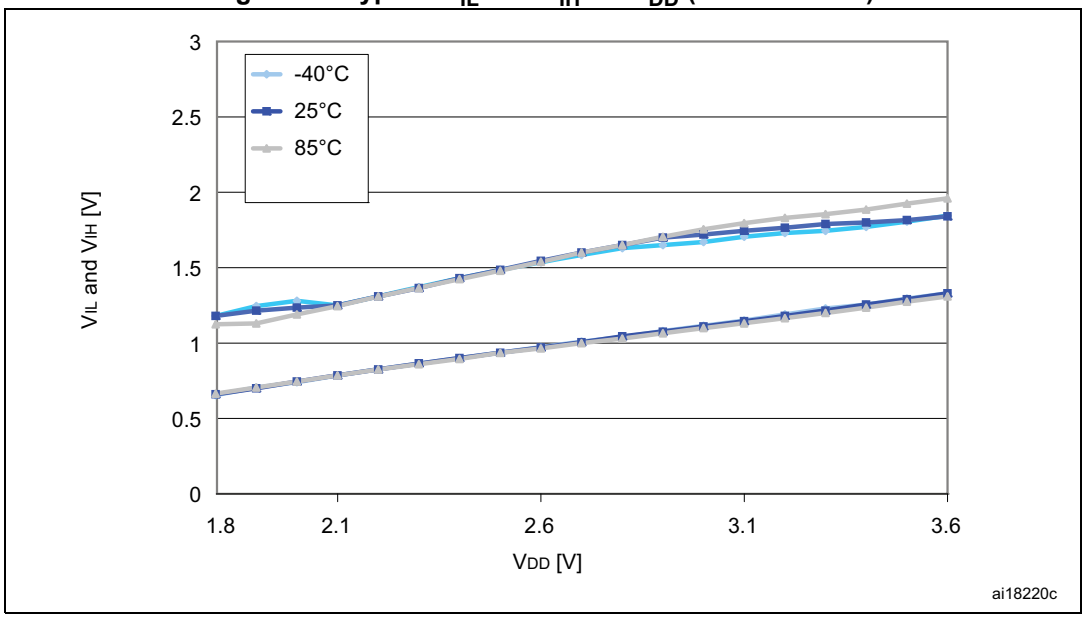



Figure 27. Typical $V_{IL}$ and $V_{IH}$ vs. $V_{DD}$ (true open drain I/Os)

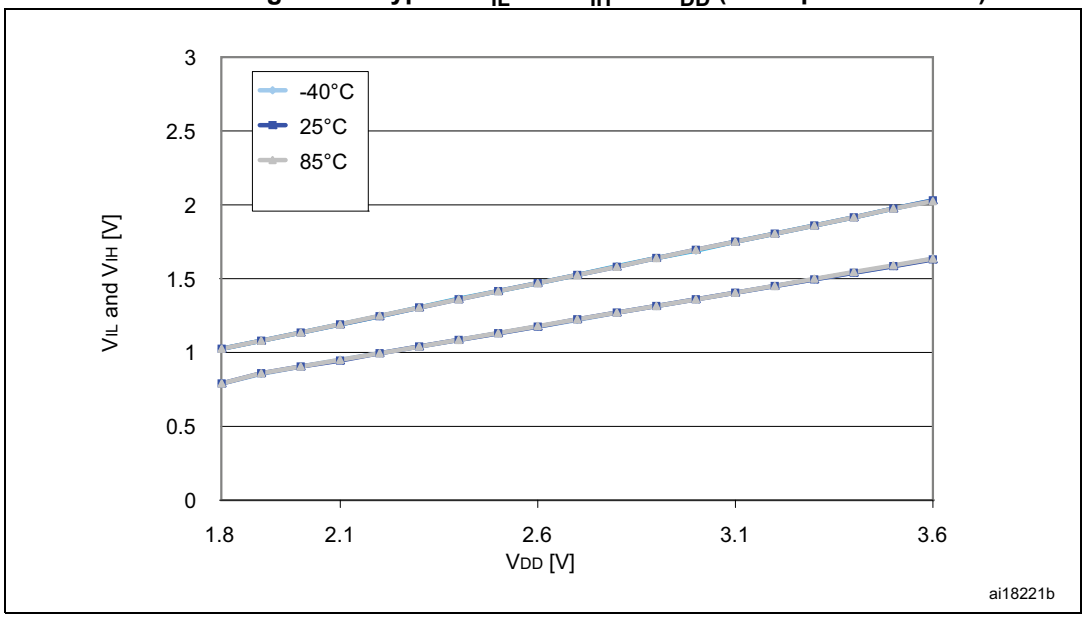


Figure 28. Typical pull-up resistance $R_{PU}$ vs. $V_{DD}$ with $V_{IN}=V_{SS}$

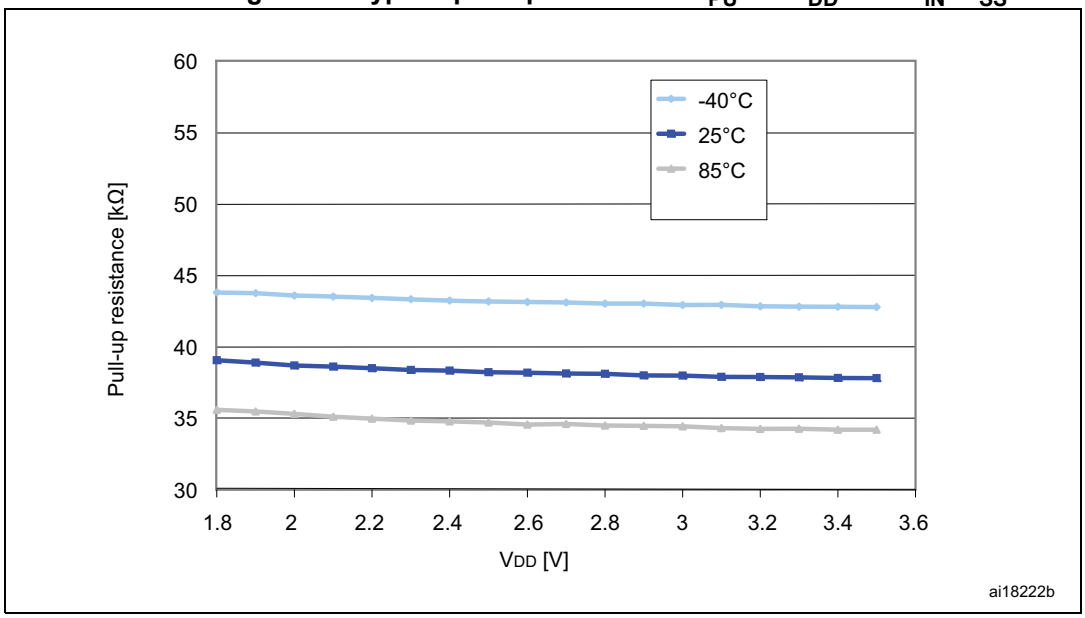
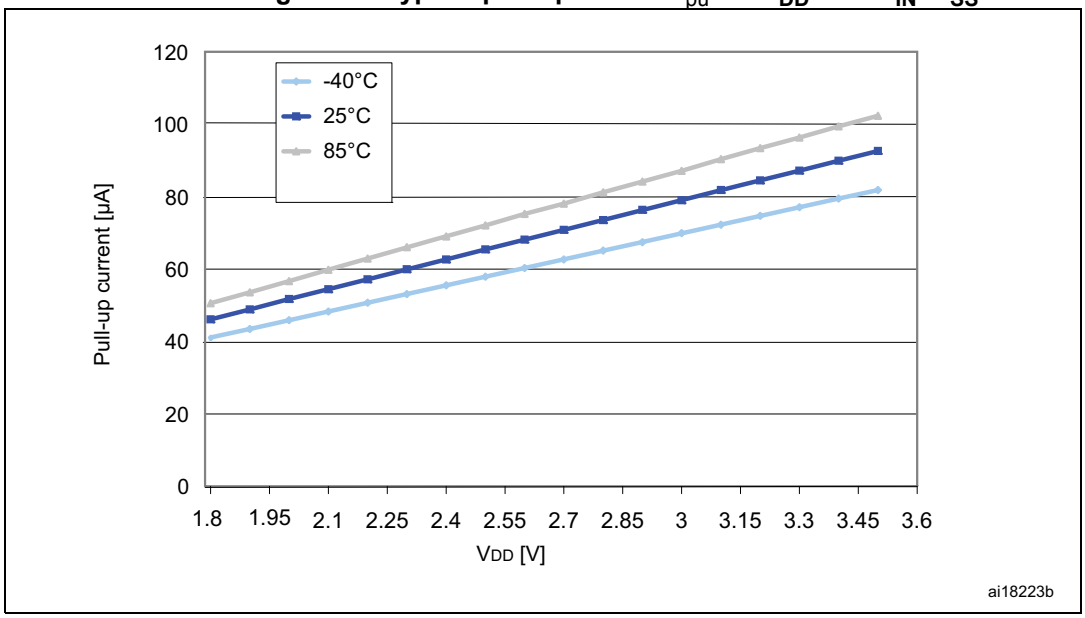



Figure 29. Typical pull-up current $I_{pu}$ vs. $V_{DD}$ with $V_{IN}=V_{SS}$




### Output driving current

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 39. Output driving current (high sink ports)**

| I/O Type | Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Standard | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +2 mA, $V_{DD}$ = 3.0 V | - | 0.45 | V |
| | | | $I_{IO}$ = +2 mA, $V_{DD}$ = 1.8 V | - | 0.45 | |
| | | | $I_{IO}$ = +10 mA, $V_{DD}$ = 3.0 V | - | 0.7 | |
| | $V_{OH}$ (2) | Output high level voltage for an I/O pin | $I_{IO}$ = -2 mA, $V_{DD}$ = 3.0 V | $V_{DD}$-0.45 | - | |
| | | | $I_{IO}$ = -1 mA, $V_{DD}$ = 1.8 V | $V_{DD}$-0.45 | - | |
| | | | $I_{IO}$ = -10 mA, $V_{DD}$ = 3.0 V | $V_{DD}$-0.7 | - | |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.
2. The $I_{IO}$ current sourced must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VDD}$.

**Table 40. Output driving current (true open drain ports)**

| I/O Type | Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| Open drain | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +3 mA, $V_{DD}$ = 3.0 V | - | 0.45 | V |
| | | | $I_{IO}$ = +1 mA, $V_{DD}$ = 1.8 V | - | 0.45 | |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

**Table 41. Output driving current (PA0 with high sink LED driver capability)**

| I/O Type | Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| IR | $V_{OL}$ (1) | Output low level voltage for an I/O pin | $I_{IO}$ = +20 mA, $V_{DD}$ = 2.0 V | - | 0.45 | V |

1. The $I_{IO}$ current sunk must always respect the absolute maximum rating specified in *Table 16* and the sum of $I_{IO}$ (I/O ports and control pins) must not exceed $I_{VSS}$.

**Figure 30. Typical $V_{OL}$ @ $V_{DD}$ = 3.0 V (high sink ports)**

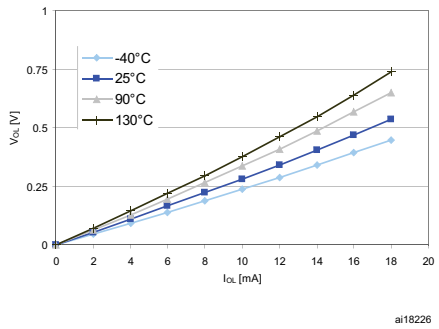



**Figure 31. Typical $V_{OL}$ @ $V_{DD}$ = 1.8 V (high sink ports)**

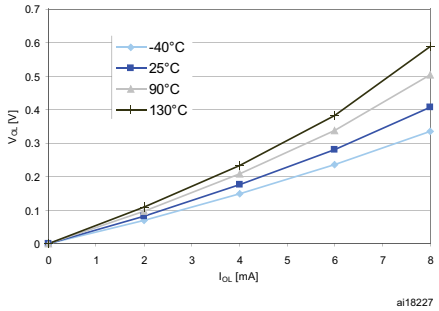



**Figure 32. Typical $V_{OL}$ @ $V_{DD}$ = 3.0 V (true open drain ports)**

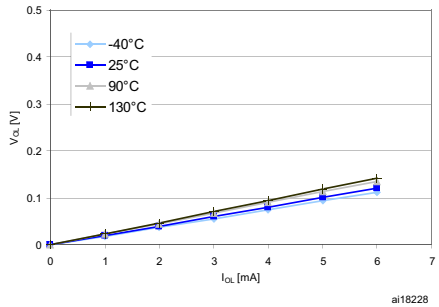



**Figure 33. Typical $V_{OL}$ @ $V_{DD}$ = 1.8 V (true open drain ports)**

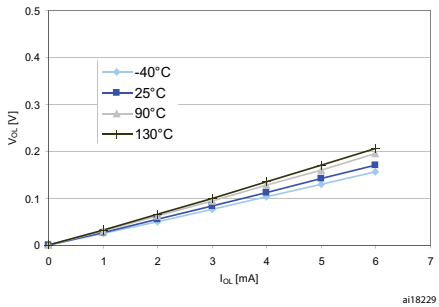



**Figure 34. Typical $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 3.0 V (high sink ports)**

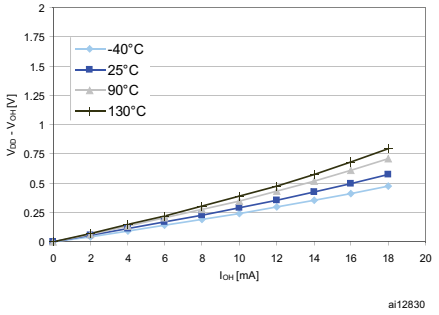
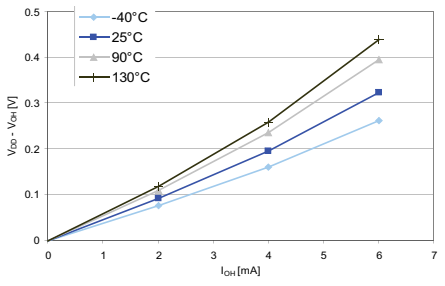



**Figure 35. Typical $V_{DD}$ - $V_{OH}$ @ $V_{DD}$ = 1.8 V (high sink ports)**




### NRST pin

Subject to general operating conditions for $V_{DD}$ and $T_A$ unless otherwise specified.

**Table 42. $\overline{\text{NRST}}$ pin characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low level voltage (1) | - | $V_{SS}$ | - | 0.8 | V |
| $V_{IH(NRST)}$ | NRST input high level voltage (1) | - | 1.4 | - | $V_{DD}$ | |
| $V_{OL(NRST)}$ | NRST output low level voltage (1) | $I_{OL}$ = 2 mA<br>2.7 V ≤$V_{DD}$ ≤3.6 V | - | - | 0.4 | |
| | | $I_{OL}$ = 1.5 mA<br>$V_{DD}$ < 2.7 V | - | - | | |
| $V_{HYST}$ | NRST input hysteresis(3) | - | 10%$V_{DD}$(2) | - | - | mV |
| $R_{PU(NRST)}$ | NRST pull-up equivalent resistor(1) | - | 30 | 45 | 60 | kΩ |
| $V_{F(NRST)}$ | NRST input filtered pulse (3) | - | | - | 50 | ns |
| $V_{NF(NRST)}$ | NRST input not filtered pulse (3) | - | 300 | - | - | |

1. Data based on characterization results.
2. 200 mV min.
3. Data guaranteed by design.

**Figure 36. Typical NRST pull-up resistance $R_{PU}$ vs. $V_{DD}$**

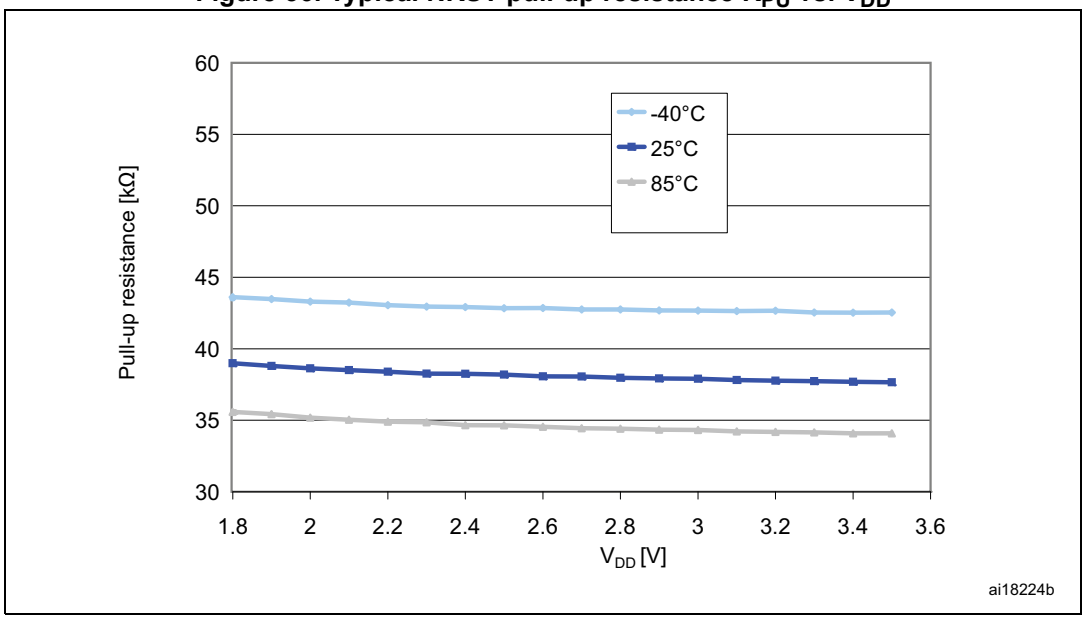
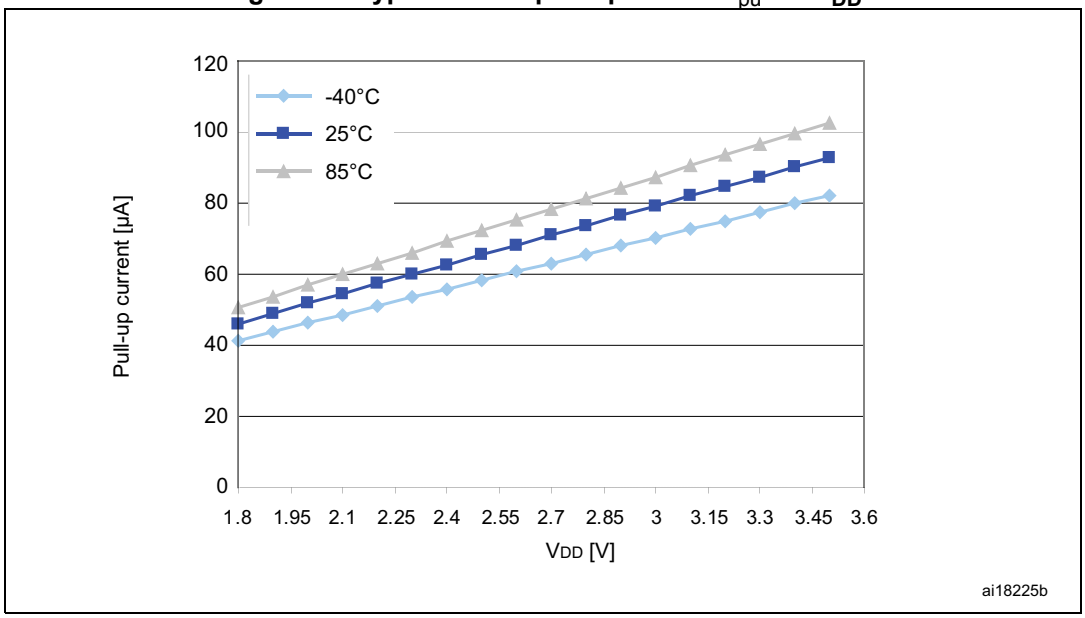
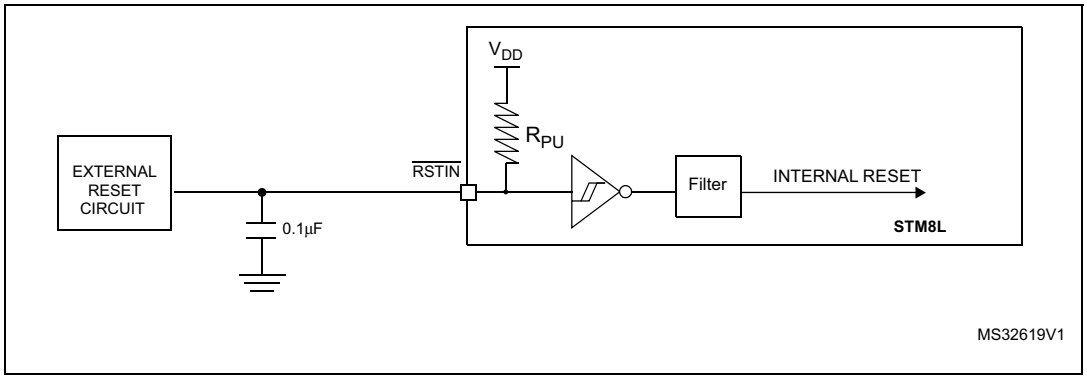


**Figure 37. Typical NRST pull-up current $I_{pu}$ vs. $V_{DD}$**




The reset network shown in *Figure 38* protects the device against parasitic resets. The user must ensure that the level on the NRST pin can go below the $V_{IL}$ max. level specified in *Table 42*. Otherwise the reset is not taken into account internally. For power consumption-sensitive applications, the capacity of the external reset capacitor can be reduced to limit the charge/discharge current. If the NRST signal is used to reset the external circuitry, the user must pay attention to the charge/discharge time of the external capacitor to meet the reset timing conditions of the external devices. The minimum recommended capacity is 10 nF.

**Figure 38. Recommended NRST pin configuration**



## 9.3.8 Communication interfaces

### SPI1 - Serial peripheral interface

Unless otherwise specified, the parameters given in *Table 43* are derived from tests performed under ambient temperature, $f_{SYSCLK}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Section 9.3.1*. Refer to I/O port characteristics for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

**Table 43. SPI1 characteristics**

| Symbol | Parameter | Conditions(1) | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$<br>$1/t_{c(SCK)}$ | SPI1 clock frequency | Master mode | 0 | 8 | MHz |
| | | Slave mode | 0 | 8 | |
| $t_{r(SCK)}$<br>$t_{f(SCK)}$ | SPI1 clock rise and fall time | Capacitive load: C = 30 pF | - | 30 | ns |
| $t_{su(NSS)}$(2) | NSS setup time | Slave mode | 4 x $1/f_{SYSCLK}$ | - | |
| $t_{h(NSS)}$(2) | NSS hold time | Slave mode | 80 | - | |
| $t_{w(SCKH)}$(2)<br>$t_{w(SCKL)}$(2) | SCK high and low time | Master mode,<br>$f_{MASTER}$ = 8 MHz, $f_{SCK}$= 4 MHz | 105 | 145 | |
| $t_{su(MI)}$(2)<br>$t_{su(SI)}$(2) | Data input setup time | Master mode | 30 | - | |
| | | Slave mode | 3 | - | |
| $t_{h(MI)}$(2)<br>$t_{h(SI)}$(2) | Data input hold time | Master mode | 15 | - | |
| | | Slave mode | 0 | - | |
| $t_{a(SO)}$(2)(3) | Data output access time | Slave mode | - | 3x $1/f_{SYSCLK}$ | |
| $t_{dis(SO)}$(2)(4) | Data output disable time | Slave mode | 30 | - | |
| $t_{v(SO)}$(2) | Data output valid time | Slave mode (after enable edge) | - | 60 | |
| $t_{v(MO)}$(2) | Data output valid time | Master mode (after enable edge) | - | 20 | |
| $t_{h(SO)}$(2) | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| $t_{h(MO)}$(2) | | Master mode (after enable edge) | 1 | - | |

1. Parameters are given by selecting 10 MHz I/O output frequency.
2. Values based on design simulation and/or characterization results.
3. Min. time is for the minimum time to drive the output and max. time is for the maximum time to validate the data.
4. Min. time is for the minimum time to invalidate the output and max. time is for the maximum time to put the data in Hi-Z.

**Figure 39. SPI1 timing diagram - slave mode and CPHA=0**

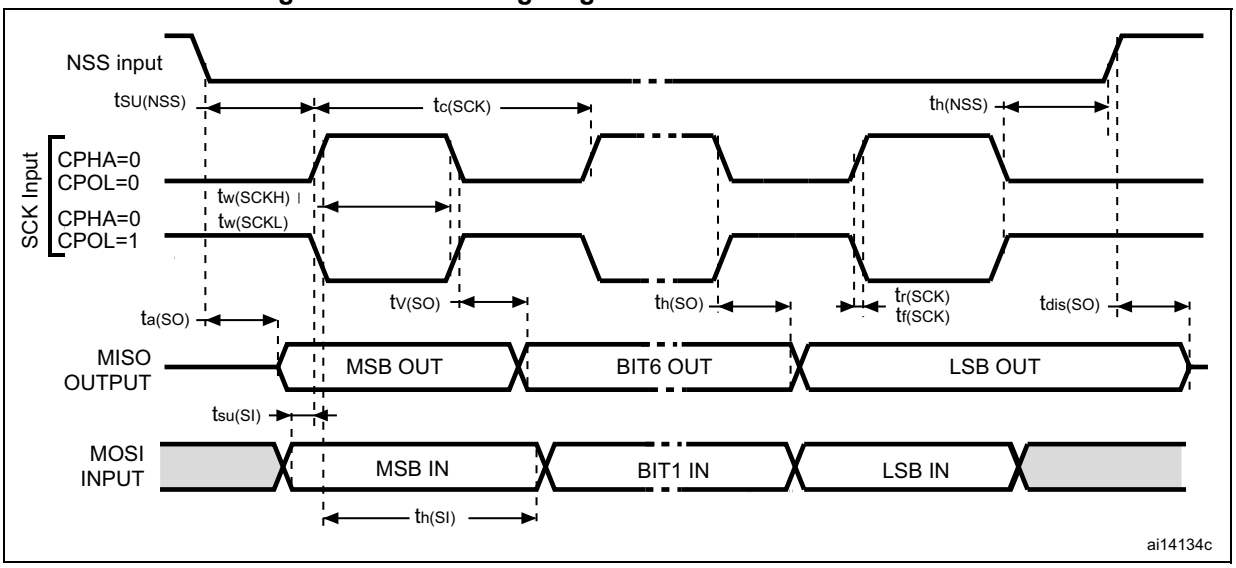
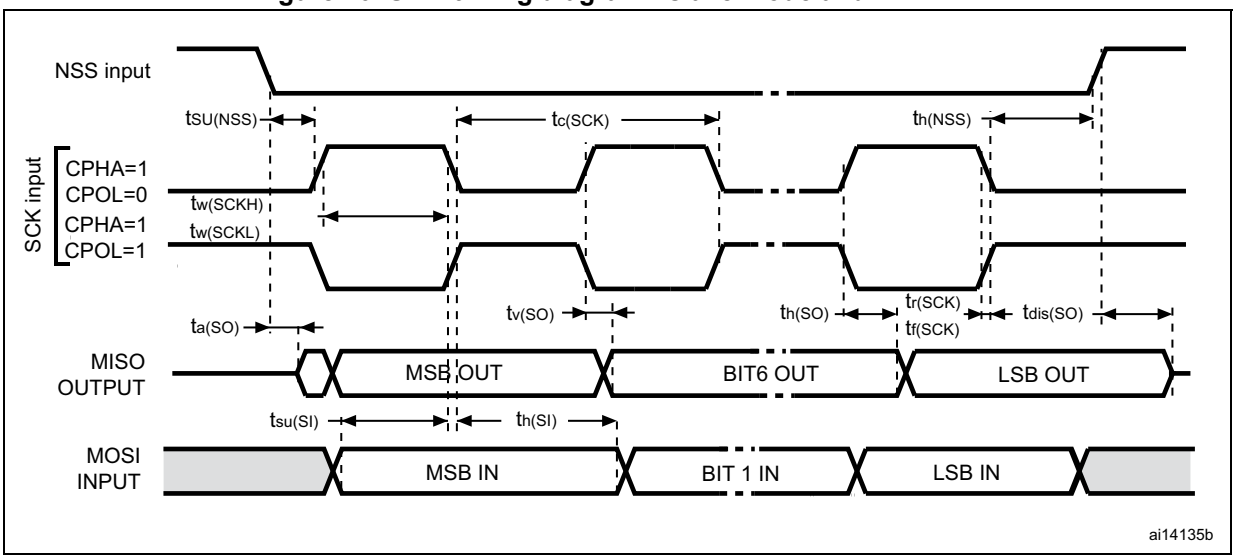
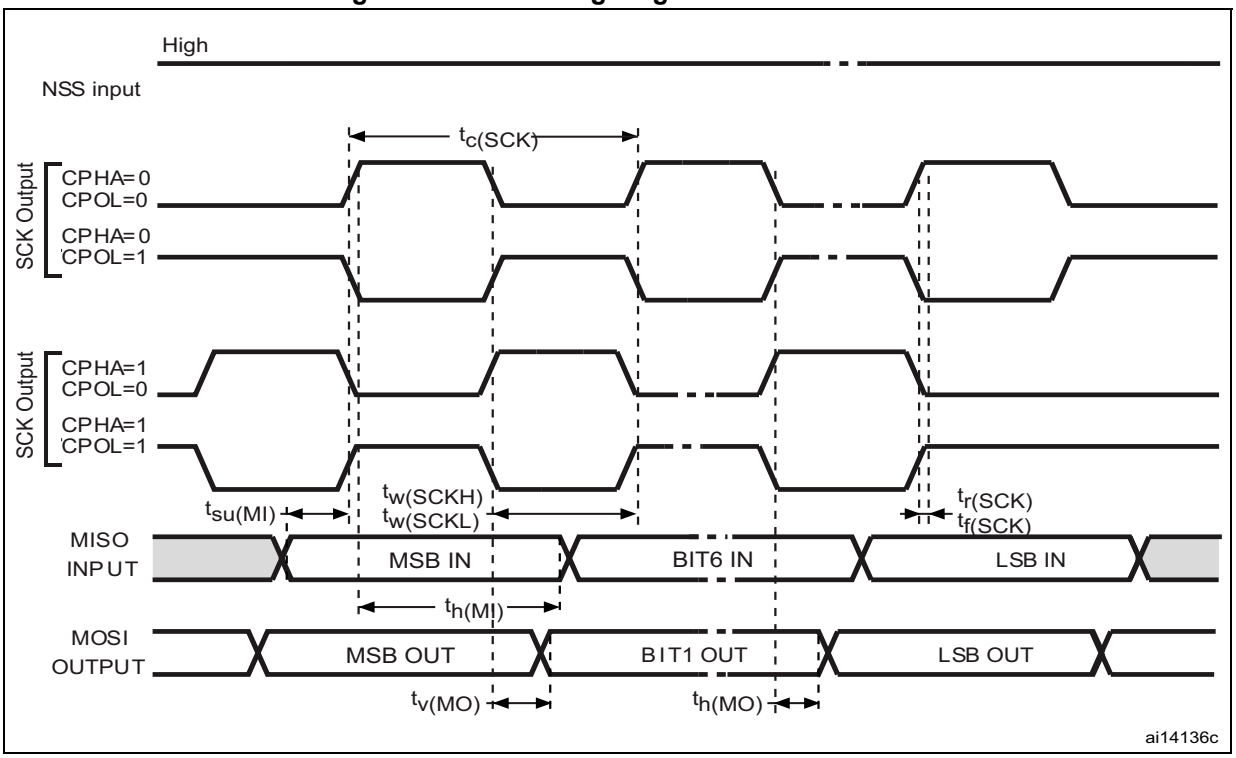



**Figure 40. SPI1 timing diagram - slave mode and CPHA=1**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

**Figure 41. SPI1 timing diagram - master mode**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

## I²C - Inter IC control interface

Subject to general operating conditions for $V_{DD}$, $f_{SYSCLK}$, and $T_A$ unless otherwise specified.

The STM8L I²C interface (I2C1) meets the requirements of the Standard I²C communication protocol described in the following table with the restriction mentioned below:

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (SDA and SCL).

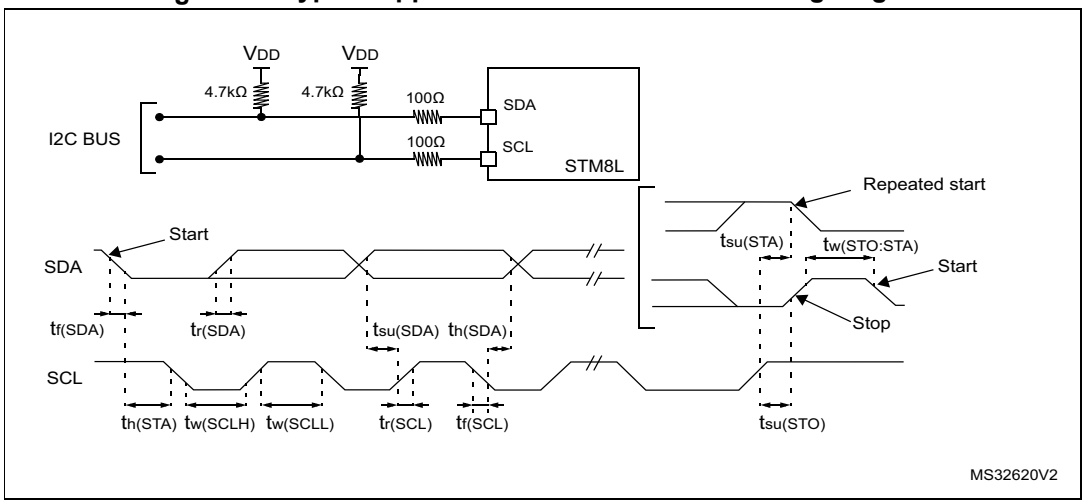
**Table 44. I2C characteristics**

| Symbol | Parameter | Standard mode I²C | | Fast mode I²C(1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min.(2) | Max. (2) | Min. (2) | Max. (2) | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | - | 0 | 900 | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 1000 | - | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 300 | - | 300 | |
| $t_{h(STA)}$ | START condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated START condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | STOP condition setup time | 4.0 | - | 0.6 | - | µs |
| $t_{w(STO:STA)}$ | STOP to START condition time (bus free) | 4.7 | - | 1.3 | - | µs |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

1. $f_{SYSCLK}$ must be at least equal to 8 MHz to achieve max fast I²C speed (400 kHz).
2. Data based on standard I²C protocol requirement, not tested in production.

*Note: For speeds around 200 kHz, the achieved speed can have a ±5% tolerance.*
*For other speed ranges, the achieved speed can have a ±2% tolerance.*
*The above variations depend on the accuracy of the external components used.*

**Figure 42. Typical application with I²C bus and timing diagram**




1. Measurement points are done at CMOS levels: 0.3 x $V_{DD}$ and 0.7 x $V_{DD}$

### 9.3.9 LCD controller (STM8L152x6/8 only)

In the following table, data are guaranteed by design.

**Table 45. LCD characteristics**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{LCD}$ | LCD external voltage | - | | 3.6 | V |
| $V_{LCD0}$ | LCD internal reference voltage 0 | - | 2.6 | - | |
| $V_{LCD1}$ | LCD internal reference voltage 1 | - | 2.7 | - | |
| $V_{LCD2}$ | LCD internal reference voltage 2 | - | 2.8 | - | |
| $V_{LCD3}$ | LCD internal reference voltage 3 | - | 3.0 | - | |
| $V_{LCD4}$ | LCD internal reference voltage 4 | - | 3.1 | - | |
| $V_{LCD5}$ | LCD internal reference voltage 5 | - | 3.2 | - | |
| $V_{LCD6}$ | LCD internal reference voltage 6 | - | 3.4 | - | |
| $V_{LCD7}$ | LCD internal reference voltage 7 | - | 3.5 | - | |
| $C_{EXT}$ | $V_{LCD}$ external capacitance | 0.1 | 1 | 2 | µF |
| $I_{DD}$ | Supply current(1) at $V_{DD}$ = 1.8 V | - | 3 | - | µA |
| | Supply current(1) at $V_{DD}$ = 3 V | - | 3 | - | |
| $R_{HN}$(2) | High value resistive network (low drive) | - | 6.6 | - | MΩ |
| $R_{LN}$(3) | Low value resistive network (high drive) | - | 240 | - | kΩ |
| $V_{33}$ | Segment/Common higher level voltage | - | | $V_{LCDx}$ | V |
| $V_{34}$ | Segment/Common 3/4 level voltage | - | $3/4V_{LCDx}$ | - | |
| $V_{23}$ | Segment/Common 2/3 level voltage | - | $2/3V_{LCDx}$ | - | |
| $V_{12}$ | Segment/Common 1/2 level voltage | - | $1/2V_{LCDx}$ | - | |
| $V_{13}$ | Segment/Common 1/3 level voltage | - | $1/3V_{LCDx}$ | - | |
| $V_{14}$ | Segment/Common 1/4 level voltage | - | $1/4V_{LCDx}$ | - | |
| $V_0$ | Segment/Common lowest level voltage | 0 | - | - | |

1. LCD enabled with 3 V internal booster (LCD_CR1 = 0x08), 1/4 duty, 1/3 bias, division ratio= 64, all pixels active, no LCD connected.
2. $R_{HN}$ is the total high value resistive network.
3. $R_{LN}$ is the total low value resistive network.

#### VLCD external capacitor (STM8L152x6/8 only)

The application can achieve a stabilized LCD reference voltage by connecting an external capacitor $C_{EXT}$ to the $V_{LCD}$ pin. $C_{EXT}$ is specified in *Table 45*.

### 9.3.10 Embedded reference voltage

In the following table, data are based on characterization results unless otherwise specified.

**Table 46. Reference voltage characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{REFINT}$ | Internal reference voltage consumption | - | - | 1.4 | | µA |
| $T_{S_VREFINT}$(1)(2) | ADC sampling time when reading the internal reference voltage | - | - | 5 | 10 | µs |
| $I_{BUF}$(1) | Internal reference voltage buffer consumption (used for ADC) | - | - | 13.5 | 25 | µA |
| $V_{REFINT\ out}$ | Reference voltage output | - | 1.202 (3) | 1.224 | 1.242 (3) | V |
| $I_{LPBUF}$(1) | Internal reference voltage low-power buffer consumption (used for comparators or output) | - | - | 730 | 1200 | nA |
| $I_{REFOUT}$(1)(4) | Buffer output current | - | - | | 1 | µA |
| $C_{REFOUT}$ | Reference voltage output load | - | - | | 50 | pF |
| $t_{VREFINT}$(1) | Internal reference voltage startup time | - | - | 2 | 3 | ms |
| $t_{BUFEN}$(1)(2) | Internal reference voltage buffer startup time once enabled | - | - | | 10 | µs |
| $ACC_{VREFINT}$(5) | Accuracy of $V_{REFINT}$ stored in the VREFINT_Factory_CONV byte | - | - | | ± 5 | mV |
| $STAB_{VREFINT}$ | Stability of $V_{REFINT}$ over temperature | -40 °C ≤$T_A$≤ 125 °C | - | 20 | 50 | ppm/°C |
| | Stability of $V_{REFINT}$ over temperature | 0 °C ≤$T_A$≤ 50 °C | - | - | 20 | ppm/°C |
| $STAB_{VREFINT}$ | Stability of $V_{REFINT}$ after 1000 hours | - | - | - | 1000 | ppm |

1. Guaranteed by design.
2. Defined when ADC output reaches its final value ±1/2LSB
3. Tested in production at $V_{DD}$ = 3 V ±10 mV.
4. To guarantee less than 1% $V_{REFOUT}$ deviation
5. Measured at $V_{DD}$ = 3 V ±10 mV. This value takes into account $V_{DD}$ accuracy and ADC conversion accuracy.

### 9.3.11 Temperature sensor

In the following table, data are based on characterization results unless otherwise specified.

**Table 47. TS characteristics**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{90}$ (1) | Sensor reference voltage at 90°C ±5 °C, | 0.580 | 0.597 | 0.614 | V |
| $T_L$ | $V_{SENSOR}$ linearity with temperature | - | ±1 | ±2 | °C |
| Avg_slope(2) | Average slope | 1.59 | 1.62 | 1.65 | mV/°C |
| $IDD_{(TEMP)}$(2) | Consumption | - | 3.4 | 6 | µA |
| $T_{START}$(2)(3) | Temperature sensor startup time | - | - | 10 | µs |
| $T_{S_TEMP}$(2) | ADC sampling time when reading the temperature sensor | - | 5 | 10 | µs |

1. Tested in production at $V_{DD}$ = 3 V ±10 mV. The 8 LSB of the $V_{90}$ ADC conversion result are stored in the TS_Factory_CONV_V90 byte.
2. Guaranteed by design.
3. Defined for ADC output reaching its final value ±1/2LSB.

### 9.3.12 Comparator characteristics

In the following tables, data are guaranteed by design.

**Table 48. Comparator 1 characteristics**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | | 1.65 | - | 3.6 | V |
| $R_{400K}$ | $R_{400K}$ value | - | - | 400 | - | kΩ |
| $R_{10K}$ | $R_{10K}$ value | - | - | 10 | - | |
| $V_{IN}$ | Comparator 1 input voltage range | - | 0.6 | - | $V_{DDA}$ | V |
| $t_{START}$ | Comparator startup time | - | - | 7 | 10 | µs |
| td | Propagation delay(2) | - | - | 3 | 10 | |
| Voffset | Comparator offset | - | - | ±3 | ±10 | mV |
| $d_{Voffset}/dt$ | Comparator offset variation in worst voltage stress conditions | $V_{DDA}$ = 3.6 V<br>$V_{IN+}$ = 0 V<br>$V_{IN-}$ = $V_{REFINT}$<br>$T_A$ = 25 °C | 0 | 1.5 | 10 | mV/1000 h |
| $I_{COMP1}$ | Current consumption(3) | - | - | 160 | 260 | nA |

1. Based on characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage not included.

**Table 49. Comparator 2 characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.65 | | 3.6 | V |
| $V_{IN}$ | Comparator 2 input voltage range | - | 0 | | $V_{DDA}$ | V |
| $t_{START}$ | Comparator startup time | Fast mode | - | 15 | 20 | µs |
| | | Slow mode | - | 20 | 25 | |
| $t_{d\ slow}$ | Propagation delay(2) in slow mode | 1.65 V ≤ $V_{DDA}$ ≤ 2.7 V | - | 1.8 | 3.5 | |
| | | 2.7 V ≤ $V_{DDA}$ ≤ 3.6 V | - | 2.5 | 6 | |
| $t_{d\ fast}$ | Propagation delay(2) in fast mode | 1.65 V ≤ $V_{DDA}$ ≤ 2.7 V | - | 0.8 | 2 | |
| | | 2.7 V ≤ $V_{DDA}$ ≤ 3.6 V | - | 1.2 | 4 | |
| $V_{offset}$ | Comparator offset error | - | - | ±4 | ±20 | mV |
| $d_{Threshold}/dt$ | Threshold voltage temperature coefficient | $V_{DDA}$ = 3.3V<br>$T_A$ = 0 to 50 °C<br>V- = $V_{REF+}$, 3/4 $V_{REF+}$,<br>1/2 $V_{REF+}$, 1/4 $V_{REF+}$. | - | 15 | 30 | ppm /°C |
| $I_{COMP2}$ | Current consumption(3) | Fast mode | - | 3.5 | 5 | µA |
| | | Slow mode | - | 0.5 | 2 | |

1. Based on characterization.
2. The delay is characterized for 100 mV input step with 10 mV overdrive on the inverting input, the non-inverting input set to the reference.
3. Comparator consumption only. Internal reference voltage (necessary for comparator operation) is not included.

### 9.3.13 12-bit DAC characteristics

In the following table, data are guaranteed by design.

**Table 50. DAC characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.8 | - | 3.6 | V |
| $V_{REF+}$ | Reference supply voltage | - | 1.8 | - | $V_{DDA}$ | |
| $I_{VREF}$ | Current consumption on $V_{REF+}$ supply | $V_{REF+}$ = 3.3 V, no load, middle code (0x800) | - | 130 | 220 | µA |
| | | $V_{REF+}$ = 3.3 V, no load, worst code (0x000) | - | 220 | 350 | |
| $I_{VDDA}$ | Current consumption on $V_{DDA}$ supply | $V_{DDA}$ = 3.3 V, no load, middle code (0x800) | - | 210 | 320 | |
| | | $V_{DDA}$ = 3.3 V, no load, worst code (0x000) | - | 320 | 520 | |
| $T_A$ | Temperature range | | -40 | - | 125 | °C |
| $R_L$ (1) (2) | Resistive load | DACOUT buffer ON | 5 | - | - | kΩ |
| $R_O$ | Output impedance | DACOUT buffer OFF | - | 8 | 10 | kΩ |
| $C_L$ (3) | Capacitive load | | - | - | 50 | pF |
| DAC_OUT (4) | DAC_OUT voltage | DACOUT buffer ON | 0.2 | - | $V_{DDA}$ - 0.2 | V |
| | | DACOUT buffer OFF | 0 | - | $V_{REF+}$ -1 LSB | V |
| $t_{settling}$ | Settling time (full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches the final value ±1LSB) | $R_L \geq$ 5 kΩ, $C_L \leq$ 50 pF | - | 7 | 12 | µs |
| Update rate | Max frequency for a correct DAC_OUT (@95%) change when small variation of the input code (from code i to i+1LSB). | $R_L \geq$ 5 kΩ, $C_L \leq$ 50 pF | - | - | 1 | Msps |
| $t_{WAKEUP}$ | Wakeup time from OFF state. Input code between lowest and highest possible codes. | $R_L \geq$ 5 kΩ, $C_L \leq$ 50 pF | - | 9 | 15 | µs |
| PSRR+ | Power supply rejection ratio (to $V_{DDA}$) (static DC measurement) | $R_L \geq$ 5 kΩ, $C_L \leq$ 50 pF | - | -60 | -35 | dB |

1. Resistive load between DACOUT and GNDA
2. Output on PF0 or PF1
3. Capacitive load at DACOUT pin
4. It gives the output excursion of the DAC

In the following table, data based on characterization results.

**Table 51. DAC accuracy**

| Symbol | Parameter | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| DNL | Differential non linearity(1) | $R_L$ ≥5 kΩ, $C_L$≤50 pF DACOUT buffer ON(2) | 1.5 | 3 | 12-bit LSB |
| | | No load DACOUT buffer OFF | 1.5 | 3 | |
| INL | Integral non linearity(3) | $R_L$ ≥5 kΩ, $C_L$≤ 50 pF DACOUT buffer ON(2) | 2 | 4 | |
| | | No load DACOUT buffer OFF | 2 | 4 | |
| Offset | Offset error(4) | $R_L$ ≥5 kΩ, $C_L$≤ 50 pF DACOUT buffer ON(2) | ±10 | ±25 | |
| | | No load DACOUT buffer OFF | ±5 | ±8 | |
| Offset1 | Offset error at Code 1 (5) | DACOUT buffer OFF | ±1.5 | ±5 | |
| Gain error | Gain error(6) | $R_L$ ≥5 kΩ, $C_L$≤ 50 pF DACOUT buffer ON(2) | +0.1/-0.2 | +0.2/-0.5 | % |
| | | No load DACOUT buffer OFF | +0/-0.2 | +0/-0.4 | |
| TUE | Total unadjusted error | $R_L$ ≥5 kΩ, $C_L$≤ 50 pF DACOUT buffer ON(2) | 12 | 30 | 12-bit LSB |
| | | No load -DACOUT buffer OFF | 8 | 12 | |

1. Difference between two consecutive codes - 1 LSB.
2. In 48-pin package devices the DAC2 output buffer must be kept off and no load must be applied on the DAC_OUT2 output.
3. Difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023.
4. Difference between the value measured at Code (0x800) and the ideal value = $V_{REF+}$/2.
5. Difference between the value measured at Code (0x001) and the ideal value.
6. Difference between the ideal slope of the transfer function and the measured slope computed from Code 0x000 and 0xFFF when buffer is ON, and from Code giving 0.2 V and ($V_{DDA}$ -0.2) V when buffer is OFF.

In the following table, data are guaranteed by design.

**Table 52. DAC output on PB4-PB5-PB6(1)**

| Symbol | Parameter | Conditions | Max | Unit |
|---|---|---|---|---|
| $R_{int}$ | Internal resistance between DAC output and PB4-PB5-PB6 output | 2.7 V < $V_{DD}$ < 3.6 V | 1.4 | kΩ |
| | | 2.4 V < $V_{DD}$ < 3.6 V | 1.6 | |
| | | 2.0 V < $V_{DD}$ < 3.6 V | 3.2 | |
| | | 1.8 V < $V_{DD}$ < 3.6 V | 8.2 | |

1. 32 or 28-pin packages only. The DAC channel can be routed either on PB4, PB5 or PB6 using the routing interface I/O switch registers.

### 9.3.14 12-bit ADC1 characteristics

In the following table, data are guaranteed by design.

**Table 53. ADC1 characteristics**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | 1.8 | | 3.6 | V |
| $V_{REF+}$ | Reference supply voltage | 2.4 V ≤$V_{DDA}$≤ 3.6 V | 2.4 | | $V_{DDA}$ | |
| | | 1.8 V≤$V_{DDA}$≤ 2.4 V | $V_{DDA}$ | | | |
| $V_{REF-}$ | Lower reference voltage | - | $V_{SSA}$ | | | |
| $I_{VDDA}$ | Current on the $V_{DDA}$ input pin | - | - | 1000 | 1450 | µA |
| $I_{VREF+}$ | Current on the $V_{REF+}$ input pin | - | - | 400 | 700 (peak)(1) | |
| | | - | - | | 450 (average)(1) | |
| $V_{AIN}$ | Conversion voltage range | - | 0(2) | - | $V_{REF+}$ | |
| $T_A$ | Temperature range | - | -40 | - | 125 | °C |
| $R_{AIN}$ | External resistance on $V_{AIN}$ | on PF0/1/2/3 fast channels | - | - | 50(3) | kΩ |
| | | on all other channels | - | - | | |
| $C_{ADC}$ | Internal sample and hold capacitor | on PF0/1/2/3 fast channels | - | 16 | - | pF |
| | | on all other channels | - | | - | |
| $f_{ADC}$ | ADC sampling clock frequency | 2.4 V≤$V_{DDA}$≤3.6 V without zooming | 0.320 | - | 16 | MHz |
| | | 1.8 V≤$V_{DDA}$≤2.4 V with zooming | 0.320 | - | 8 | |
| $f_{CONV}$ | 12-bit conversion rate | $V_{AIN}$ on PF0/1/2/3 fast channels | - | - | 1(3)(4) | |
| | | $V_{AIN}$ on all other channels | - | - | 760(3)(4) | kHz |
| $f_{TRIG}$ | External trigger frequency | - | - | - | $t_{conv}$ | $1/f_{ADC}$ |
| $t_{LAT}$ | External trigger latency | - | - | - | 3.5 | $1/f_{SYSCLK}$ |

**Table 53. ADC1 characteristics (continued)**

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_S$ | Sampling time | $V_{AIN}$ PF0/1/2/3 fast channels $V_{DDA}$ < 2.4 V | 0.43(3)(4) | - | - | µs |
| | | $V_{AIN}$ PF0/1/2/3 fast channels 2.4 V ≤$V_{DDA}$≤ 3.6 V | 0.22(3)(4) | - | - | |
| | | $V_{AIN}$ on slow channels $V_{DDA}$ < 2.4 V | 0.86(3)(4) | - | - | |
| | | $V_{AIN}$ on slow channels 2.4 V ≤$V_{DDA}$≤ 3.6 V | 0.41(3)(4) | - | - | |
| $t_{conv}$ | 12-bit conversion time | - | 12 + $t_S$ | | | $1/f_{ADC}$ |
| | | 16 MHz | 1(3) | | | µs |
| $t_{WKUP}$ | Wakeup time from OFF state | - | - | - | 3 | µs |
| $t_{IDLE}$(5) | Time before a new conversion | - | - | - | ∞ | s |
| $t_{VREFINT}$ | Internal reference voltage startup time | - | - | - | refer to *Table 46* | ms |

1. The current consumption through $V_{REF}$ is composed of two parameters:
   - one constant (max 300 µA)
   - one variable (max 400 µA), only during sampling time + 2 first conversion pulses.
   So, peak consumption is 300+400 = 700 µA and average consumption is 300 + [(4 sampling + 2) /16] x 400 = 450 µA at 1Msps
2. $V_{REF-}$ must be tied to ground.
3. Minimum sampling and conversion time is reached for maximum $R_{AIN}$= 0.5 kΩ.
4. Value obtained for continuous conversion on fast channel.
5. The time between 2 conversions, or between ADC ON and the first conversion must be lower than $t_{IDLE}$.

In the following three tables, data are guaranteed by characterization result.

**Table 54. ADC1 accuracy with $V_{DDA}$ = 3.3 V to 2.5 V**

| Symbol | Parameter | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| DNL | Differential non linearity | $f_{ADC}$ = 16 MHz | 1 | 1.6 | LSB |
| | | $f_{ADC}$ = 8 MHz | 1 | 1.6 | |
| | | $f_{ADC}$ = 4 MHz | 1 | 1.5 | |
| INL | Integral non linearity | $f_{ADC}$ = 16 MHz | 1.2 | 2 | |
| | | $f_{ADC}$ = 8 MHz | 1.2 | 1.8 | |
| | | $f_{ADC}$ = 4 MHz | 1.2 | 1.7 | |
| TUE | Total unadjusted error | $f_{ADC}$ = 16 MHz | 2.2 | 3.0 | |
| | | $f_{ADC}$ = 8 MHz | 1.8 | 2.5 | |
| | | $f_{ADC}$ = 4 MHz | 1.8 | 2.3 | |
| Offset | Offset error | $f_{ADC}$ = 16 MHz | 1.5 | 2 | |
| | | $f_{ADC}$ = 8 MHz | 1 | 1.5 | |
| | | $f_{ADC}$ = 4 MHz | 0.7 | 1.2 | |
| Gain | Gain error | $f_{ADC}$ = 16 MHz | 1 | 1.5 | |
| | | $f_{ADC}$ = 8 MHz | | | |
| | | $f_{ADC}$ = 4 MHz | | | |

**Table 55. ADC1 accuracy with $V_{DDA}$ = 2.4 V to 3.6 V**

| Symbol | Parameter | Typ. | Max. | Unit |
|---|---|---|---|---|
| DNL | Differential non linearity | 1 | 2 | LSB |
| INL | Integral non linearity | 1.7 | 3 | |
| TUE | Total unadjusted error | 2 | 4 | |
| Offset | Offset error | 1 | 2 | |
| Gain | Gain error | 1.5 | 3 | |

**Table 56. ADC1 accuracy with $V_{DDA}$ = $V_{REF}^+$ = 1.8 V to 2.4 V**

| Symbol | Parameter | Typ. | Max. | Unit |
|---|---|---|---|---|
| DNL | Differential non linearity | 1 | 2 | LSB |
| INL | Integral non linearity | 2 | 3 | |
| TUE | Total unadjusted error | 3 | 5 | |
| Offset | Offset error | 2 | 3 | |
| Gain | Gain error | 2 | 3 | |

**Figure 43. ADC1 accuracy characteristics**

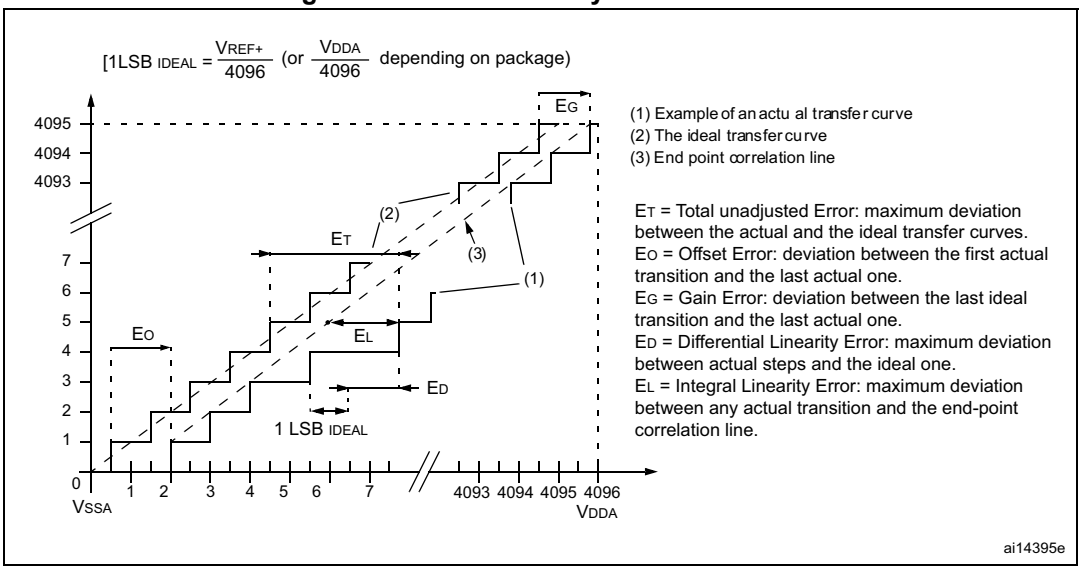
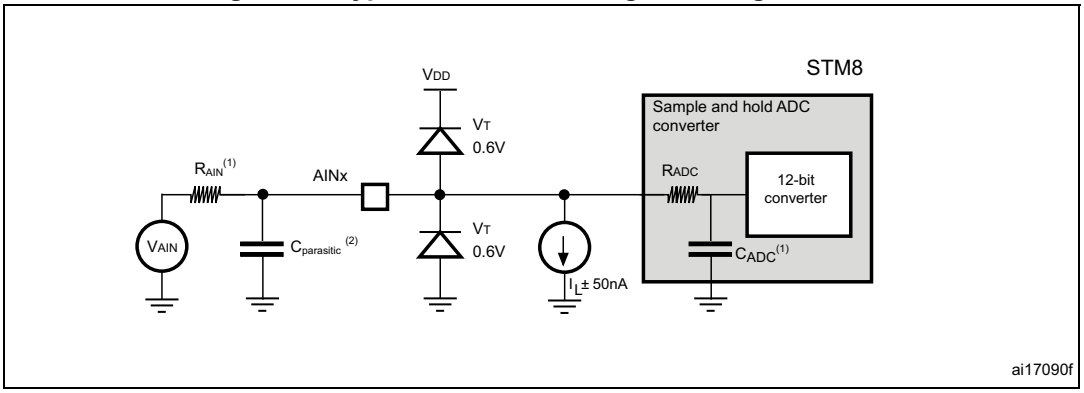



**Figure 44. Typical connection diagram using the ADC**




1. Refer to *Table 53* for the values of $R_{AIN}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

**Figure 45. Maximum dynamic current consumption on $V_{REF+}$ supply pin during ADC conversion**

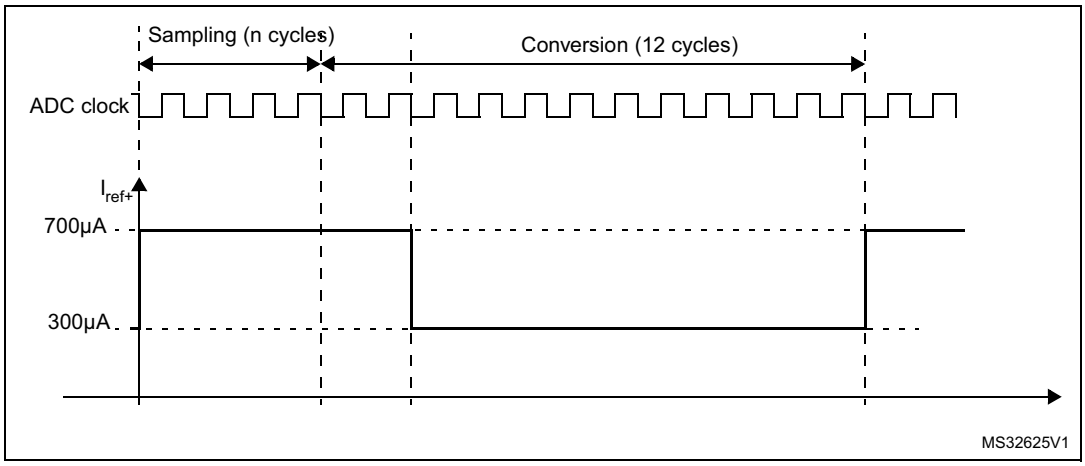



**Table 57. $R_{AIN}$ max for $f_{ADC}$ = 16 MHz(1)**

| Ts (cycles) | Ts (µs) | $R_{AIN}$ max (kohm) | | | |
|---|---|---|---|---|---|
| | | Slow channels | | Fast channels | |
| | | 2.4 V < $V_{DDA}$ < 3.6 V | 1.8 V < $V_{DDA}$ < 2.4 V | 2.4 V < $V_{DDA}$ < 3.3 V | 1.8 V < $V_{DDA}$ < 2.4 V |
| 4 | 0.25 | Not allowed | Not allowed | 0.7 | Not allowed |
| 9 | 0.5625 | 0.8 | Not allowed | 2.0 | 1.0 |
| 16 | 1 | 2.0 | 0.8 | 4.0 | 3.0 |
| 24 | 1.5 | 3.0 | 1.8 | 6.0 | 4.5 |
| 48 | 3 | 6.8 | 4.0 | 15.0 | 10.0 |
| 96 | 6 | 15.0 | 10.0 | 30.0 | 20.0 |
| 192 | 12 | 32.0 | 25.0 | 50.0 | 40.0 |
| 384 | 24 | 50.0 | 50.0 | 50.0 | 50.0 |

1. Guaranteed by design.

### General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 46* or *Figure 47*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. Good quality ceramic 10 nF capacitors should be used. They should be placed as close as possible to the chip.

**Figure 46. Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)**

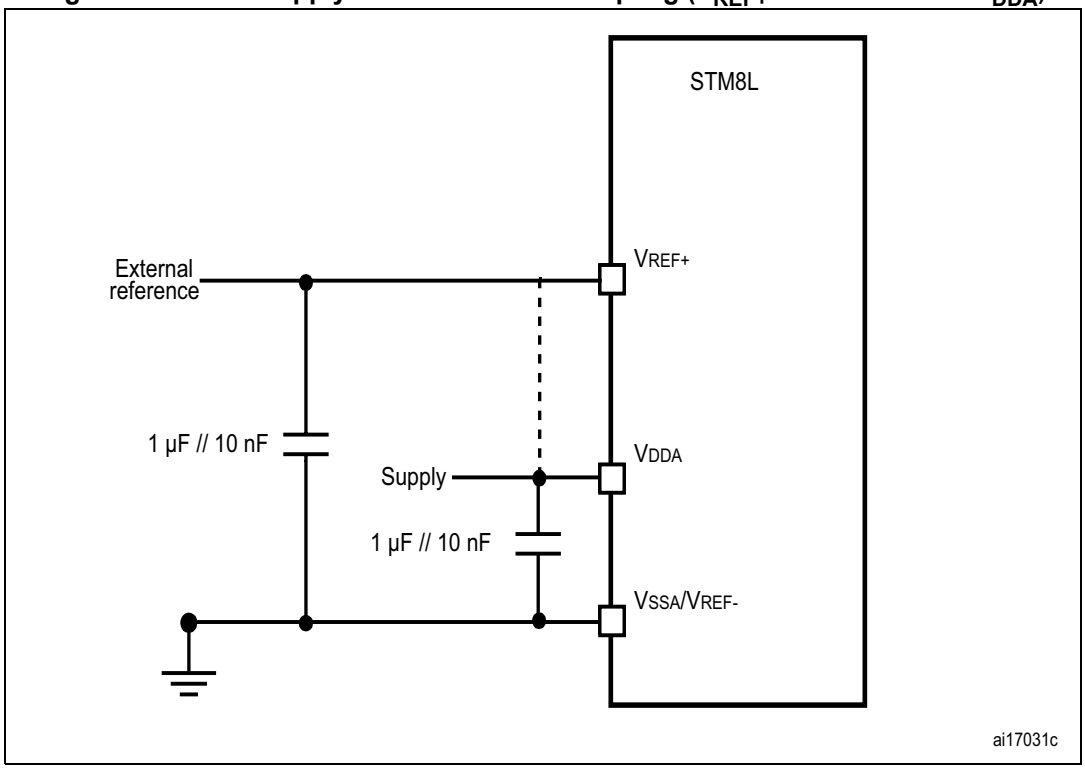
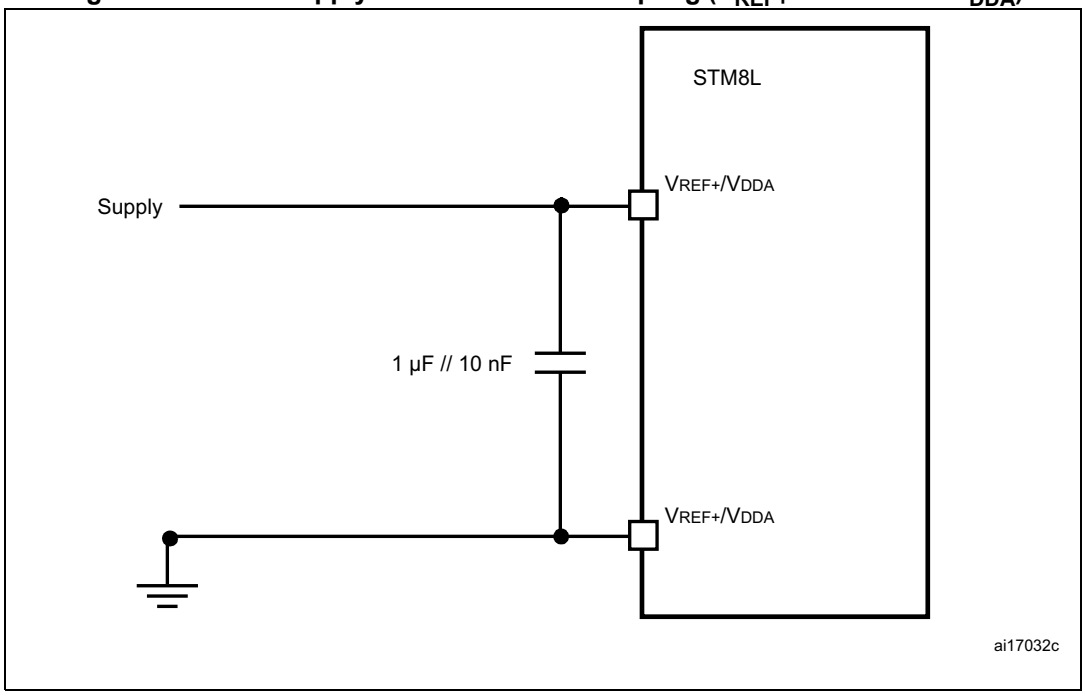



**Figure 47. Power supply and reference decoupling ($V_{REF+}$ connected to $V_{DDA}$)**



## 9.3.15 EMC characteristics

Susceptibility tests are performed on a sample basis during product characterization.

### Functional EMS (electromagnetic susceptibility)

Based on a simple running application on the product (toggling 2 LEDs through I/O ports), the product is stressed by two electromagnetic events until a failure occurs (indicated by the LEDs).

- **ESD**: Electrostatic discharge (positive and negative) is applied on all pins of the device until a functional disturbance occurs. This test conforms with the IEC 61000 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test conforms with the IEC 61000 standard.

A device reset allows normal operations to be resumed. The test results are given in the table below based on the EMS levels and classes defined in application note AN1709.

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

**Prequalification trials:**

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

**Table 58. EMS data**

| Symbol | Parameter | Conditions | | Level/ Class |
|---|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{CPU}$= 16 MHz, conforms to IEC 61000 | | 2B |
| $V_{EFTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, $f_{CPU}$ = 16 MHz, conforms to IEC 61000 | Using HSI | 4A |
| | | | Using HSE | 2B |

### Electromagnetic interference (EMI)

Based on a simple application running on the product (toggling 2 LEDs through the I/O ports), the product is monitored in terms of emission. This emission test is in line with the norm IEC61967-2 which specifies the board and the loading of each pin.

**Table 59. EMI data (1)**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. | Unit |
|---|---|---|---|---|---|
| | | | | 16 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = +25 °C, LQFP80 conforming to IEC61967-2 | 0.1 MHz to 30 MHz | 10 | dBµV |
| | | | 30 MHz to 130 MHz | 4 | |
| | | | 130 MHz to 1 GHz | 1 | |
| | | | SAE EMI Level | 1.5 | - |

1. Not tested in production.

### Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity. For more details, refer to the application note AN1181.

### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts*(n+1) supply pin). Two models can be simulated: human body model and charge device model. This test conforms to the JESD22-A114A/C101 or ANSI/ESD STM5.3.1 standards.

**Table 60. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Package | Class | Maximum value (1) | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C, conforming to JESD22-A414 | All | 2 | 2000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C, conforming to ANSI/ESD STM5.3.1 | WLCSP32 | TBD | TBD | |
| | | $T_A$ = +25 °C, conforming to JESD22-C101 | All other | II | 500 | |

1. Data based on characterization results.

### Static latch-up

- **LU**: 3 complementary static tests are required on 10 parts to assess the latch-up performance. A supply overvoltage (applied to each power supply pin) and a current injection (applied to each input, output and configurable I/O pin) are performed on each sample. This test conforms to the EIA/JESD 78 IC latch-up standard. For more details, refer to the application note AN1181.

**Table 61. Electrical sensitivities**

| Symbol | Parameter | Class |
|---|---|---|
| LU | Static latch-up class | II |

## 9.4 Thermal characteristics

The maximum chip junction temperature ($T_{Jmax}$) must never exceed the values given in *Table 18: General operating conditions on page 71*.

The maximum chip-junction temperature, $T_{Jmax}$, in degree Celsius, may be calculated using the following equation:

$$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \Theta_{JA})$$

Where:

- $T_{Amax}$ is the maximum ambient temperature in °C
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance in °C/W
- $P_{Dmax}$ is the sum of $P_{INTmax}$ and $P_{I/Omax}$ ($P_{Dmax} = P_{INTmax} + P_{I/Omax}$)
- $P_{INTmax}$ is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.
- $P_{I/Omax}$ represents the maximum power dissipation on output pins
  Where:
  $P_{I/Omax} = \Sigma (V_{OL}*I_{OL}) + \Sigma((V_{DD}-V_{OH})*I_{OH})$,
  taking into account the actual $V_{OL}/I_{OL}$ and $V_{OH}/I_{OH}$ of the I/Os at low and high level in the application.

**Table 62. Thermal characteristics(1)**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance junction-ambient LQFP 48 - 7 x 7 mm | 65 | °C/W |
| | Thermal resistance junction-ambient UFQFPN 48 - 7 x 7mm | 32 | |
| | Thermal resistance junction-ambient WLCSP32 | 63 | |
| | Thermal resistance junction-ambient LQFP 64 - 10 x 10 mm | 48 | |
| | Thermal resistance junction-ambient LQFP 80 - 14 x 14 mm | 38 | |

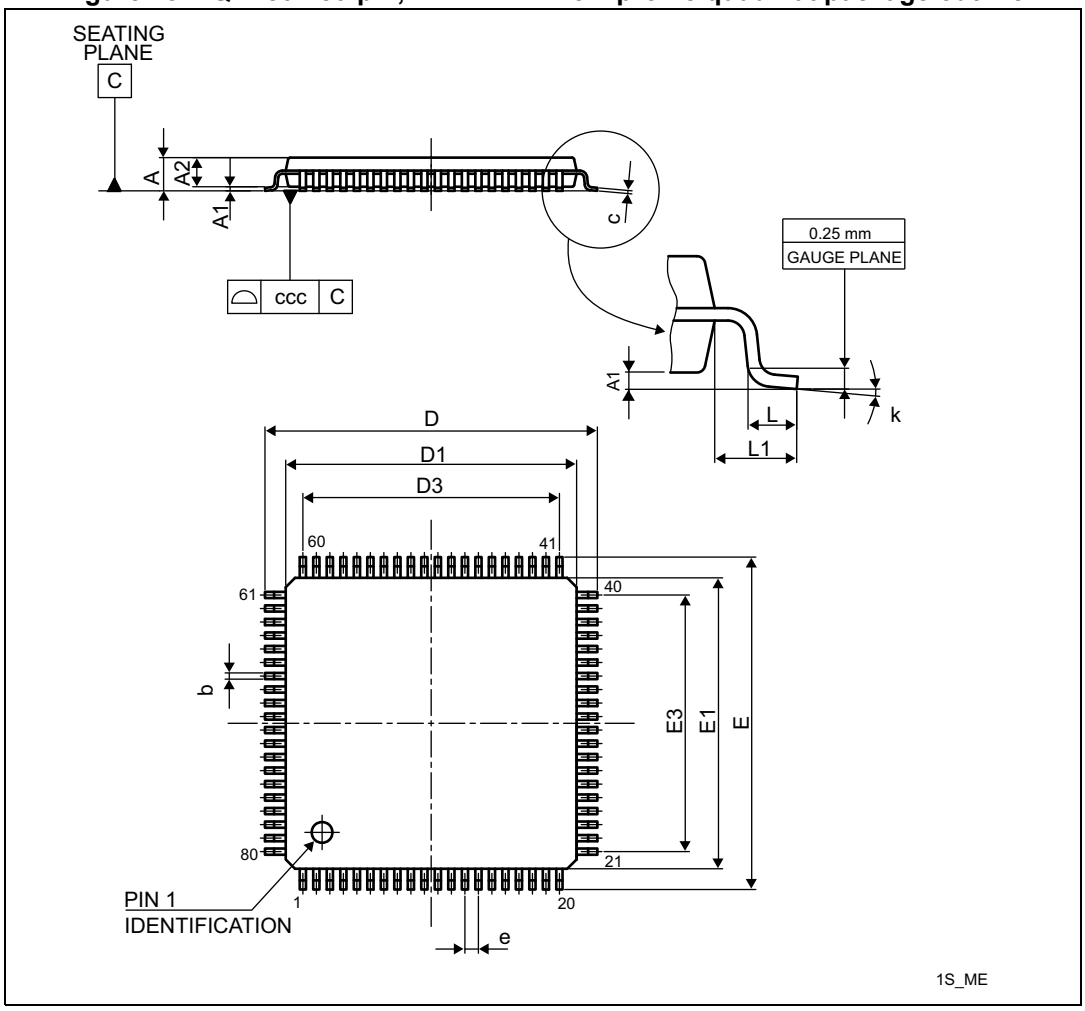
1. Thermal resistances are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment.

# 10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

## 10.1 LQFP80 package information

**Figure 48. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline**



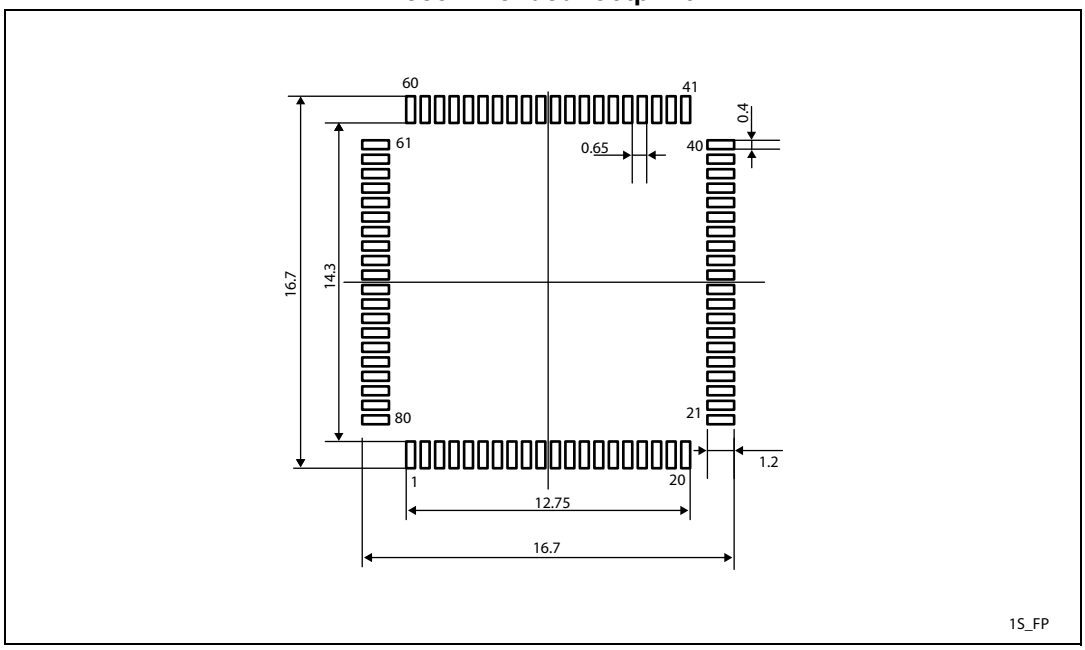

1. Drawing is not to scale.

**Table 63. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data(1)**

| Symbol | millimeters | | | inches | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.220 | 0.320 | 0.380 | 0.0087 | 0.0126 | 0.0150 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| D1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| D3 | - | 12.350 | - | - | 0.4862 | - |
| E | 15.800 | 16.000 | 16.200 | 0.6220 | 0.6299 | 0.6378 |
| E1 | 13.800 | 14.000 | 14.200 | 0.5433 | 0.5512 | 0.5591 |
| E3 | - | 12.350 | - | - | 0.4862 | - |
| e | - | 0.650 | - | - | 0.0256 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.100 | - | - | 0.0039 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 49. LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint**



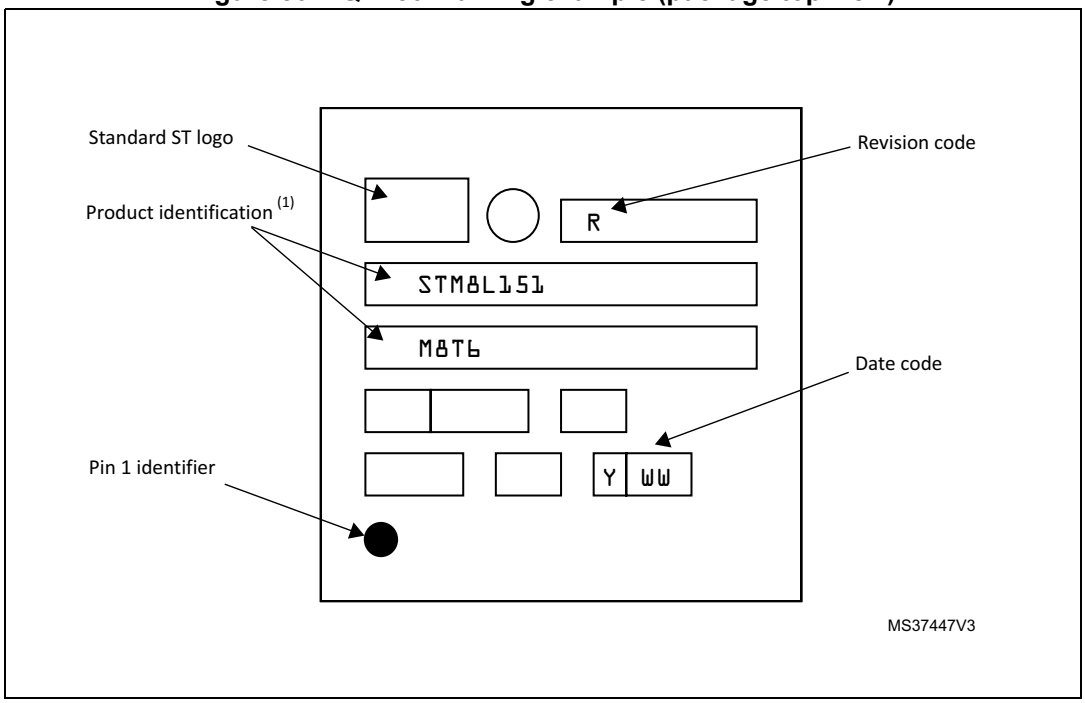

1. Dimensions are expressed in millimeters.

### Device marking for LQFP80

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

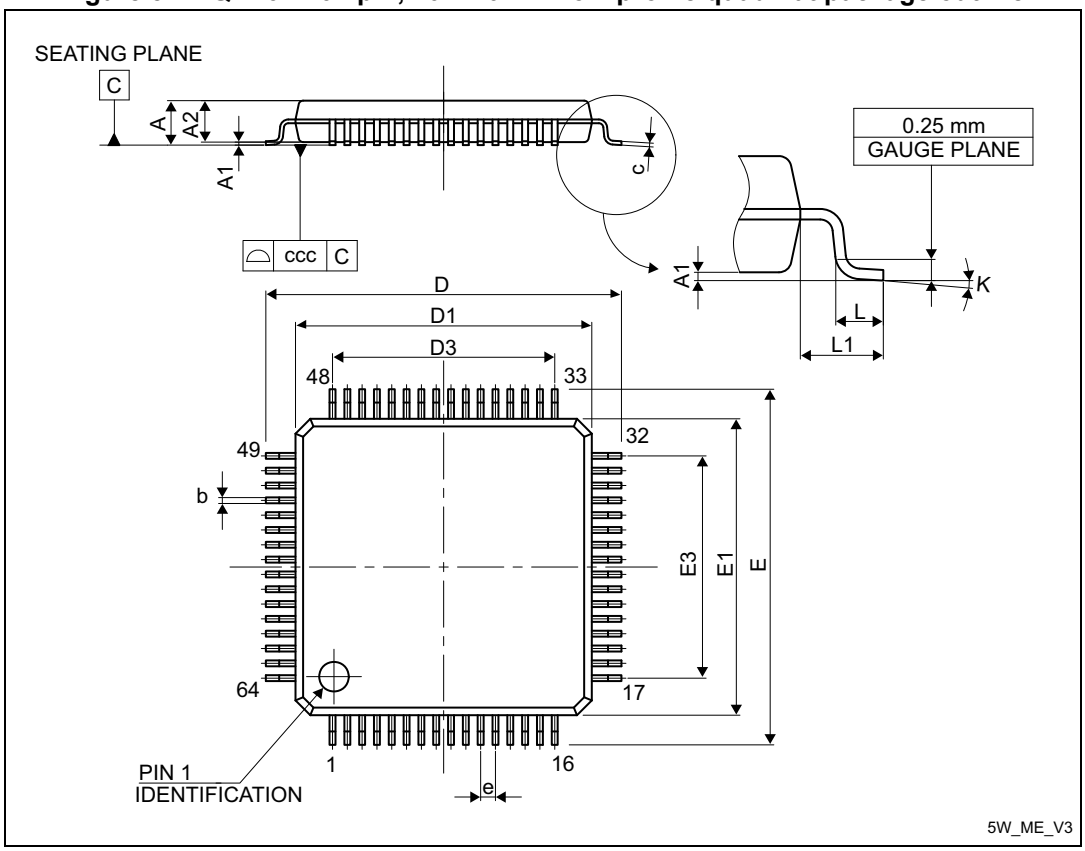
**Figure 50. LQFP80 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 10.2 LQFP64 package information

**Figure 51. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline**




1. Drawing is not to scale.

**Table 64. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data**

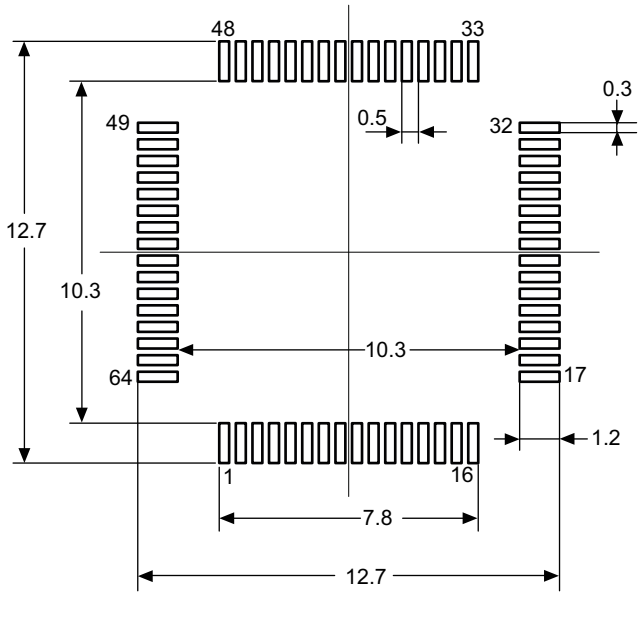
| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |

**Table 64. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 52. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint**



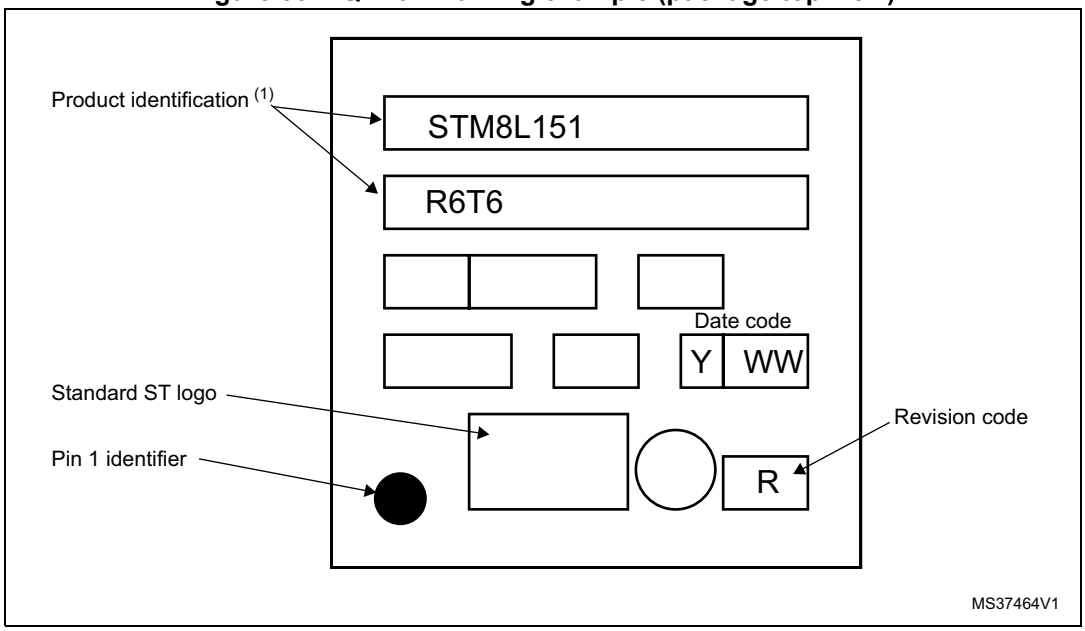

1. Dimensions are expressed in millimeters.

### Device marking for LQFP64

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

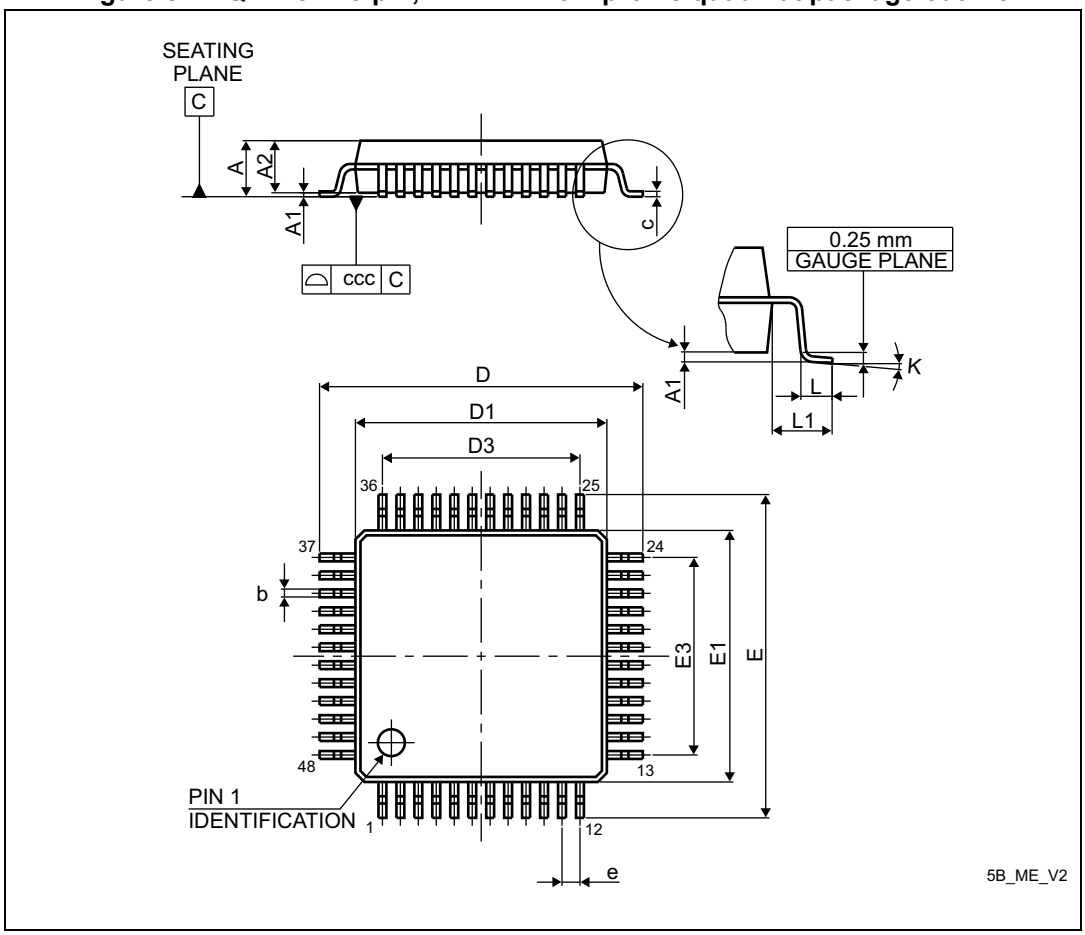
**Figure 53. LQFP64 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 10.3 LQFP48 package information

**Figure 54. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline**



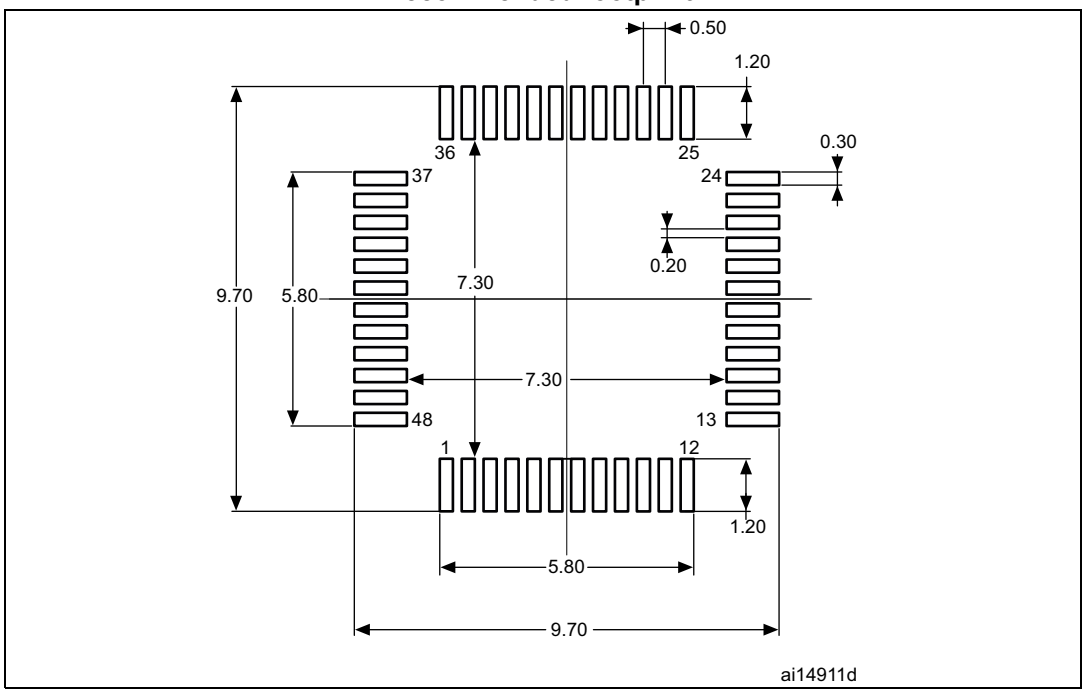

1. Drawing is not to scale.

**Table 65. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 55. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint**



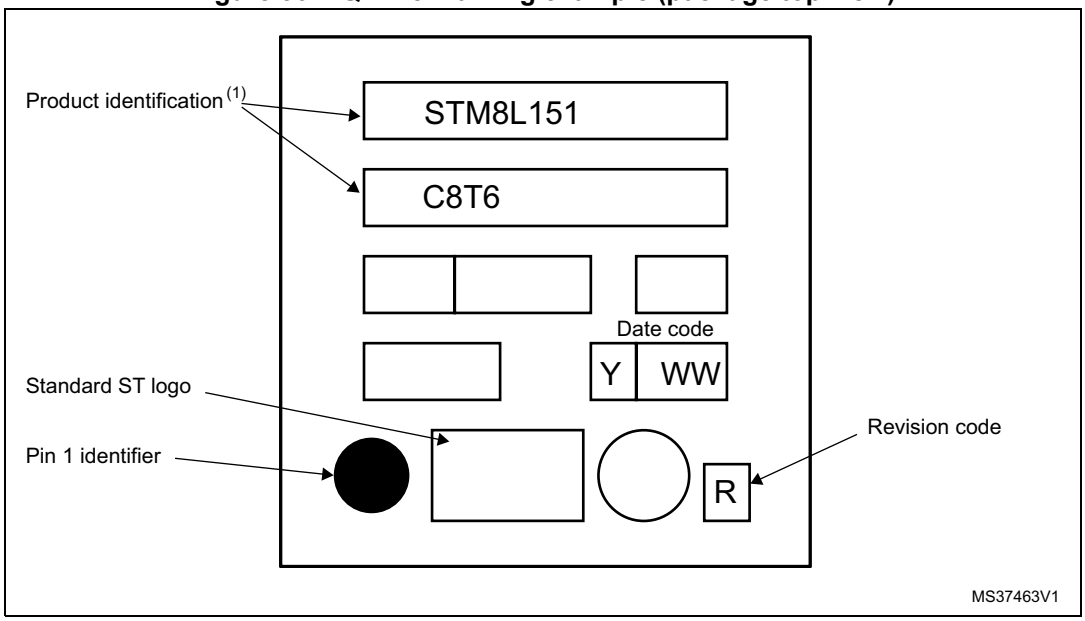

1. Dimensions are expressed in millimeters.

### Device marking for LQFP48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

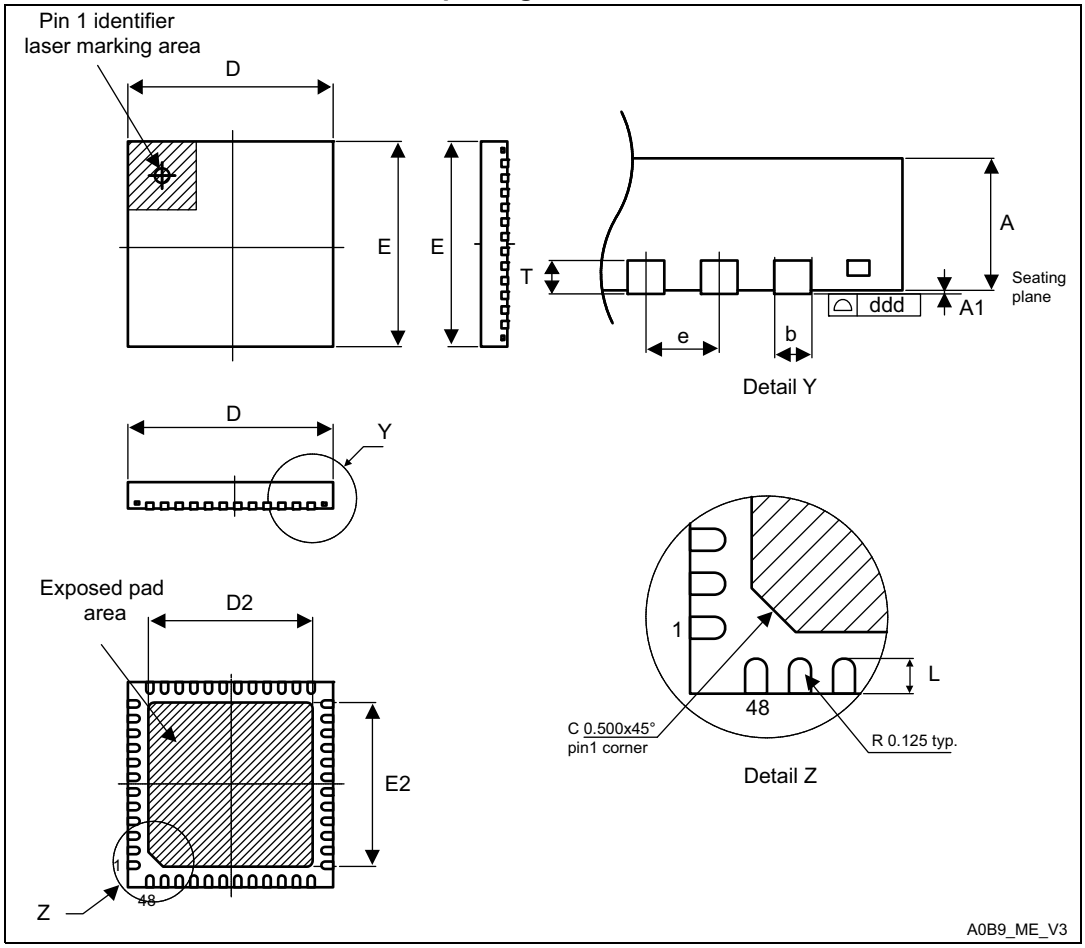
**Figure 56. LQFP48 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 10.4 UFQFPN48 package information

**Figure 57. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline**



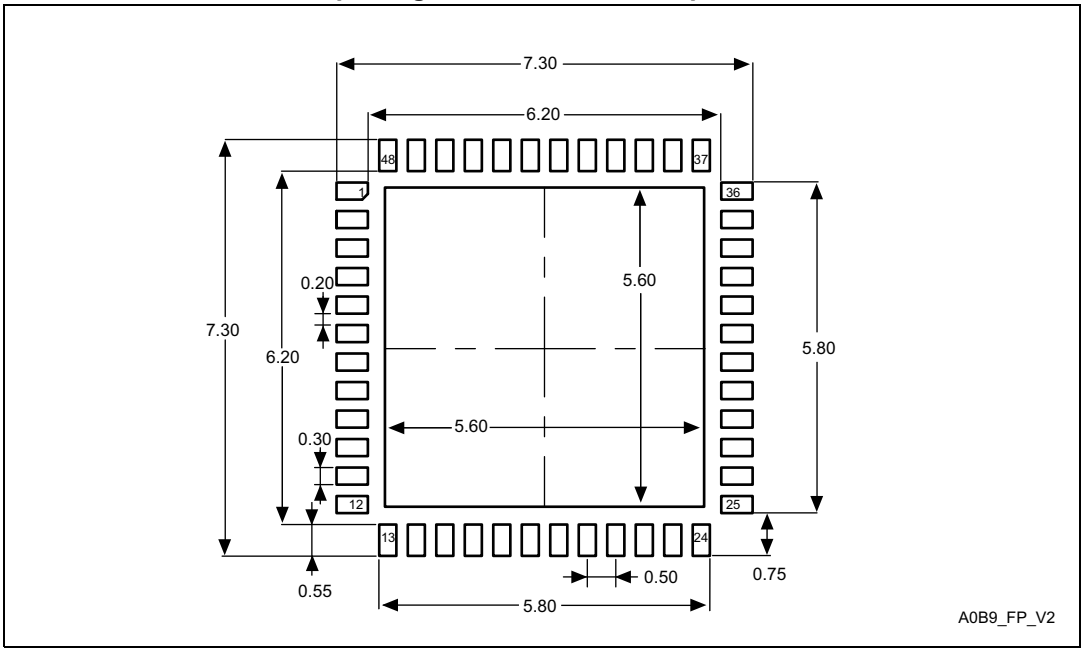

1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

**Table 66. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.500 | 0.550 | 0.600 | 0.0197 | 0.0217 | 0.0236 |
| A1 | 0.000 | 0.020 | 0.050 | 0.0000 | 0.0008 | 0.0020 |
| D | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| E | 6.900 | 7.000 | 7.100 | 0.2717 | 0.2756 | 0.2795 |
| D2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| E2 | 5.500 | 5.600 | 5.700 | 0.2165 | 0.2205 | 0.2244 |
| L | 0.300 | 0.400 | 0.500 | 0.0118 | 0.0157 | 0.0197 |
| T | - | 0.152 | - | - | 0.0060 | - |
| b | 0.200 | 0.250 | 0.300 | 0.0079 | 0.0098 | 0.0118 |
| e | - | 0.500 | - | - | 0.0197 | - |
| ddd | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 58. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint**



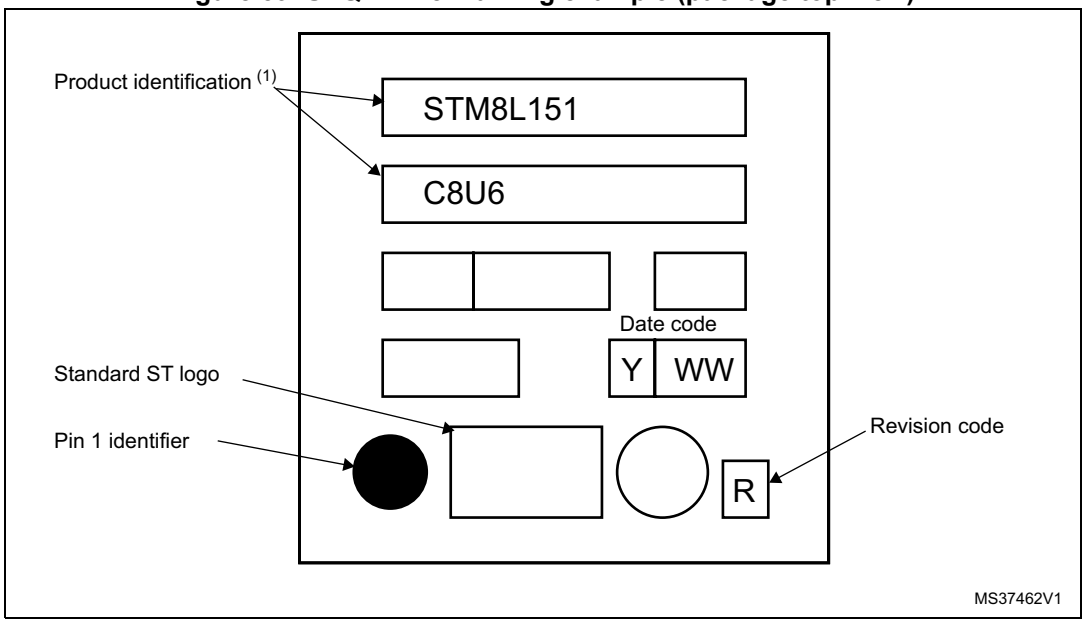

1. Dimensions are expressed in millimeters.

### Device marking for UFQFPN48

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

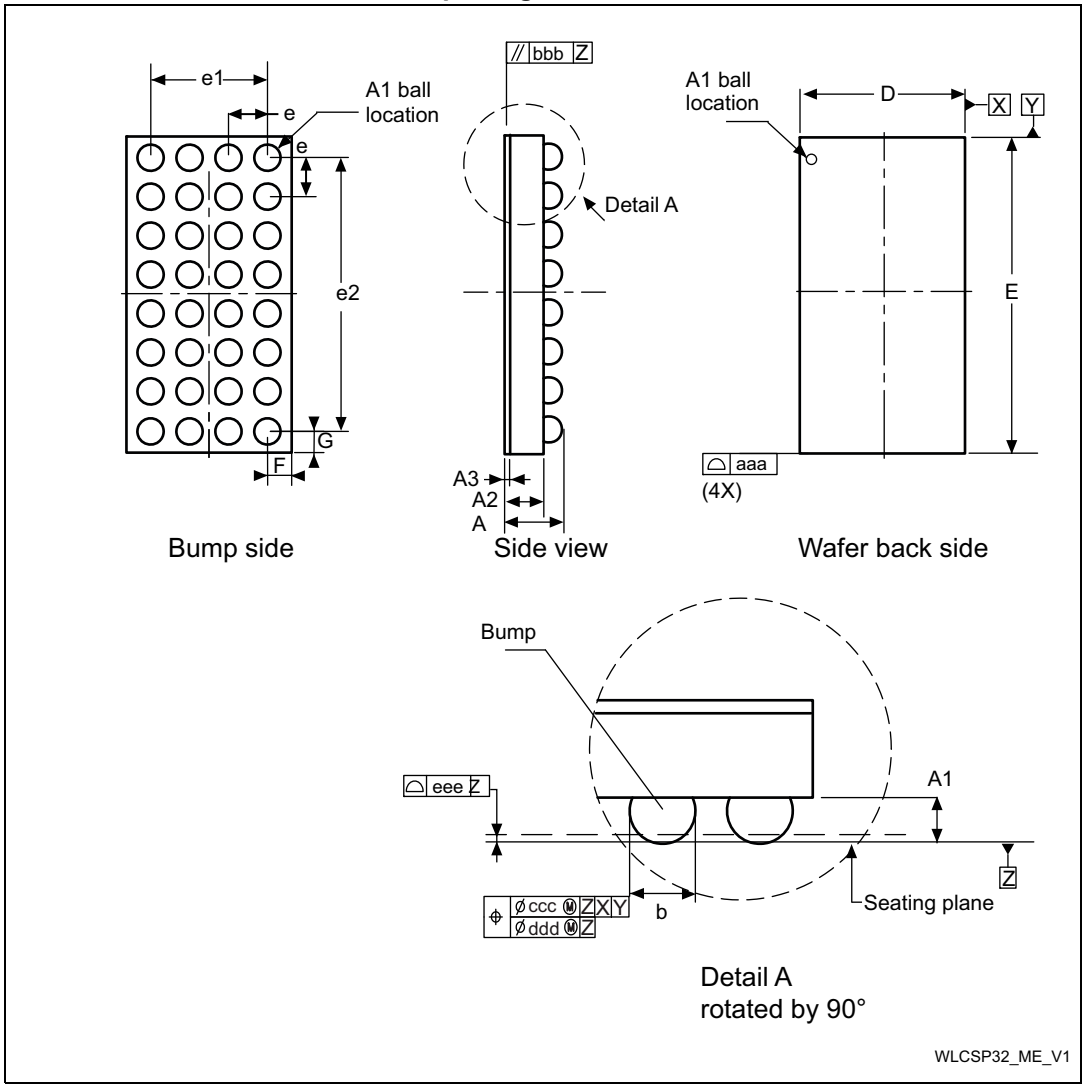
**Figure 59. UFQFPN48 marking example (package top view)**




1. Parts marked as “ES”,”E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

## 10.5 WLCSP32 package information

**Figure 60. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package outline**




1. Drawing is not to scale.
2. Preliminary drawing.

**Table 67. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package mechanical data(1)**

| Symbol | millimeters | | | inches(2) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.525 | 0.555 | 0.585 | 0.0207 | 0.0219 | 0.0230 |
| A1 | - | 0.175 | - | - | 0.0069 | - |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| A3(3) | - | 0.025 | - | - | 0.0010 | - |
| b(4) | 0.220 | 0.250 | 0.280 | 0.0087 | 0.0098 | 0.0110 |
| D | 1.878 | 1.913 | 1.948 | 0.0739 | 0.0753 | 0.0767 |
| E | 3.294 | 3.329 | 3.364 | 0.1297 | 0.1311 | 0.1324 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 1.200 | - | - | 0.0472 | - |
| e2 | - | 2.800 | - | - | 0.1102 | - |
| F | - | 0.3565 | - | - | 0.0140 | - |
| G | - | 0.2645 | - | - | 0.0104 | - |
| aaa | - | - | 0.100 | - | - | 0.0039 |
| bbb | - | - | 0.100 | - | - | 0.0039 |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| ddd | - | - | 0.050 | - | - | 0.0020 |
| eee | - | - | 0.050 | - | - | 0.0020 |

1. Preliminary data.
2. Values in inches are converted from mm and rounded to 4 decimal digits.
3. Back side coating.
4. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

**Figure 61. WLCSP32 - 32-ball, 1.913 x 3.329 mm, 0.4 mm pitch wafer level chip scale package recommended footprint**

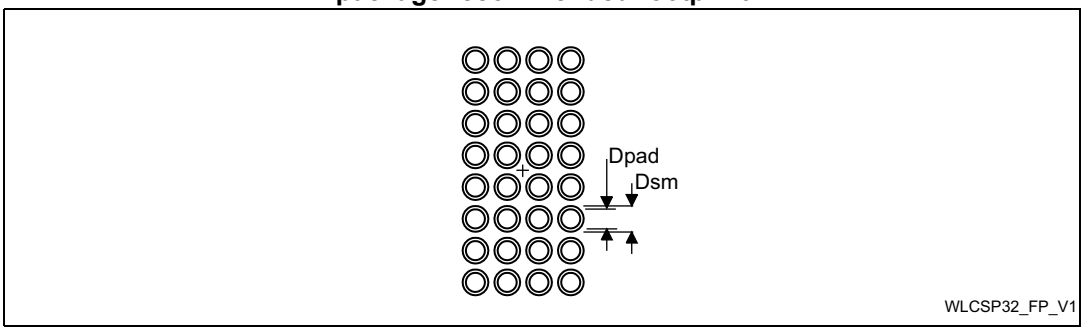


**Table 68. WLCSP32 recommended PCB design rules**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.4 mm |
| Dpad | 0.225 mm |
| Dsm | 0.290 mm typical (depending on the solder mask registration tolerance) |
| Stencil opening | 0.250 mm |
| Stencil thickness | 0.100 mm |

# 11 Ordering information

**Table 69. Ordering information scheme**

Example: STM8 L 152 C 8 T 6 D xx

**Device family**

STM8 microcontroller

**Product type**

L = Low-power

**Device subfamily**

151: Devices without LCD

152: Devices with LCD

**Pin count**

K = 32 balls

C = 48 pins

R = 64 pins

M = 80 pins

**Program memory size**

8 = 64 Kbyte of Flash memory

6 = 32 Kbyte of Flash memory

**Package**

T = LQFP

U = UFQFPN

Y = WLCSP32

**Temperature range**

3 = Industrial temperature range, – 40 to 125 °C

7 = Industrial temperature range, – 40 to 105 °C

6 = Industrial temperature range, – 40 to 85 °C

**Option**

Blank = $V_{DD}$ range from 1.8 to 3.6 V and BOR enabled

D = $V_{DD}$ range from 1.65 to 3.6 V and BOR disabled

**Packing**

TR = tape and reel

For a list of available options (e.g. memory size, package) and order-able part numbers or for further information on any aspect of this device, please go to *www.st.com* or contact the ST Sales Office nearest to you.

# 12 Revision history

Table 70. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 13-Sep-2010 | 1 | Initial release. |
| 20-Dec-2010 | 2 | Updated *Section 9.3.3: Supply current characteristics*<br>Updated *Section 9.3.2: Embedded reset and power control block characteristics*.<br>Updated *Section 9.3.3: Supply current characteristics*<br>Updated *Section 9.3.13: 12-bit DAC characteristics*<br>Updated *Section 9.3.14: 12-bit ADC1 characteristics*<br>Updated *Section 9.3.15: EMC characteristics* |
| 17-Jan-2011 | 3 | Removed references to STM8L150M8 devices. |
| 11-Mar-2011 | 4 | Updated *Table 1: Device summary*.<br>*Table 5: High-density and medium+ density STM8L15x pin description*: updated PB4/43&35, PB4/28, PC1, PI3, and pins 33 to 36 of LQFP80; updated footnotes.<br>TIMx_TRIG changed to TIMx_ETR and “Standard port” changed to “high sink port”.<br>*Table 15: Voltage characteristics*: updated<br>*Table 16: Current characteristics*: updated<br>*Table 35: RAM and hardware registers*: updated VRM data min. retention.<br>Added *Table 9.3.6: I/O current injection characteristics*.<br>*Table 38: I/O static characteristics*: updated<br>*Table 45: LCD characteristics*: updated |

**Table 70. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 03-Apr-2013 | 5 | Updated capacitive sensing channels and “Dynamic consumption” in *Features*<br>Updated LCD feature in *Table 2: High-density and medium+ density STM8L15xx6/8 low power device features and peripheral counts*<br>Updated Halt mode definition in *Section 3.1: Low-power modes*<br>Added *Bootloader*<br>Updated *Section 3.12: System configuration controller and routing interface*<br>Added *Section 3.13: Touch sensing*<br>*Table 5: High-density and medium+ density STM8L15x pin description*: updated NRST/PA1, PI0, PI1, PI2, PE0, PE1, PE2, PF4, PF5, PF6, PF7, footnote *1.* and added *Note:*<br>Updated ‘0x00 502E to 0x00 5049’ reserved area in *Table 9: General hardware register map*<br>Updated reference to SWIM/DEBUG manual in *Section 7: Option bytes*<br>Updated BOR factory default settings to 0x00 in *Table 12: Option byte addresses*<br>Corrected ROP option byte value in *Table 12: Option byte addresses*<br>Added *Figure 45: Maximum dynamic current consumption on $V_{REF+}$ supply pin during ADC conversion*<br>Updated STABVREFINT max value in *Table 46: Reference voltage characteristics*<br>Updated *Figure 41: SPI1 timing diagram - master mode*<br>Added *Table 57: $R_{AIN}$ max for $f_{ADC}$ = 16 MHz*<br>Updated Max DAC_OUT in *Table 50: DAC characteristics*<br>Updated *Section 9.3.12: Comparator characteristics* |
| 31-Jul-2013 | 6 | Added ‘Top view’ footnotes under the pinout figures in *Section 4: Pin description*<br>Updated the PF4-PF7 pins for the LQFP80 in *Table 5: High-density and medium+ density STM8L15x pin description*<br>Updated all packages:<br>Updated *Figure 57: UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline* and *Table 65: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*<br>Added *Figure 49: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint*<br>Added ‘tape and reel’ in *Table 69: Ordering information scheme* |

Table 70. Document revision history (continued)

| Date | Revision | Changes |
|---|---|---|
| 19-Feb-2015 | 7 | Updated<br>– *Table 63: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package mechanical data*,<br>– *Figure 48: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package outline*,<br>– *Figure 49: LQFP80 - 80-pin, 14 x 14 mm low-profile quad flat package recommended footprint*,<br>– *Table 64: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data*,<br>– *Figure 51: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline*,<br>– *Figure 52: LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint*,<br>– *Table 65: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package mechanical data*,<br>– *Figure 54: LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline*,<br>– *Table 66: UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data*,<br>– *Figure 57: UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline*,<br>– *Figure 58: UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint*.<br>Added:<br>– *Figure 50: LQFP80 marking example (package top view)*<br>– *Figure 53: LQFP64 marking example (package top view)*<br>– *Figure 56: LQFP48 marking example (package top view)*<br>– *Figure 59: UFQFPN48 marking example (package top view)* |
| 07-Sep-2015 | 8 | Added<br>– *Figure 9: STM8L152K8 32-ball ballout* and the related warning,<br>– *Section 10.5: WLCSP32 package information*.<br>Updated:<br>– *Table 1: Device summary*,<br>– *Table 2: High-density and medium+ density STM8L15xx6/8 low power device features and peripheral counts*,<br>– *Table 5: High-density and medium+ density STM8L15x pin description*,<br>– *Table 18: General operating conditions*,<br>– *Table 60: ESD absolute maximum ratings*,<br>– *Table 62: Thermal characteristics*,<br>– *Table 69: Ordering information scheme*. |
| 08-Dec-2016 | 9 | Updated TIM3 channel 3 to TIM3 channel 1 (LQFP80 pin 77) and SPI2 clock to SPI1 clock (LQFP80 pin 51) in *Table 5: High-density and medium+ density STM8L15x pin description*.<br>Updated BOR_TH reference (OPT5) in *Table 13: Option byte description*. |

**Table 70. Document revision history (continued)**

| Date | Revision | Changes |
|---|---|---|
| 15-Feb-2017 | 10 | Updated value of feature 12-bit synchronized ADC (number of channels) for STM8L15xK8 on *Table 2: High-density and medium+ density STM8L15xx6/8 low power device features and peripheral counts*. |
| 04-May-2018 | 11 | Updated:<br>– Pin PI3/ [SPI2_MISO]/[TIM3_CH2] row on I*Table 5: High-density and medium+ density STM8L15x pin description*<br>– *Section 9.2: Absolute maximum ratings*<br>– *Section 10: Package information*: all “Device marking” titles were updated to add the package name to the title. |

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