

## 74ABT3284

### 18-Bit Synchronous Datapath Multiplexer

#### General Description

The 74ABT3284 is a synchronous datapath buffer designed to transmit four 9-bit bytes of data onto one or two 9-bit bytes in 2:1 or 4:1 multiplexed configurations. In addition, the non-inverting transceiver supports bidirectional data transfer in transparent or registered modes. A data byte from any one of the six ports can be stored during transparent operation for later recall. Data input to any port may also be read back to itself for byte manipulation or system self-diagnostic purposes.

The 74ABT3284 is useful for interleaving data in memory applications or for use in bus-to-bus communications where variations in data word length or construction are required.

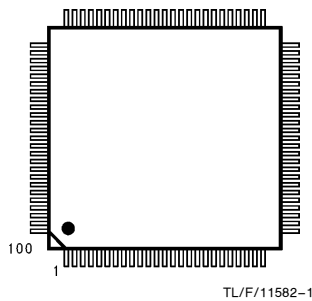
- 18-bit 2:1 or 9-bit 4:1 multiplexed modes
- Registered or transparent datapath operation
- Output enables and select lines have the option of being synchronized for pipelined operation
- Independent input, output register and control synchronizing clocks insure maximum timing flexibility
- Independent control signals insure functional flexibility
- Guaranteed simultaneous switching noise level and dynamic threshold performance
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

#### Features

- Advanced BiCMOS technology provides high speed at low power consumption

| Commercial   | Package Number | Package Description                                       |
|--------------|----------------|-----------------------------------------------------------|
| 74ABT3284VJG | VJG100A        | 100-Lead (14mm x 14mm) Molded Plastic Quad Flatpak, JEDEC |

#### Connection Diagram



#### Pin Assignment

| Pin |                                | Pin |                 | Pin |                 | Pin |                 |
|-----|--------------------------------|-----|-----------------|-----|-----------------|-----|-----------------|
| 1   | Mode__SO                       | 26  | V <sub>CC</sub> | 51  | CP__IN          | 76  | V <sub>CC</sub> |
| 2   | CP__AX                         | 27  | A <sub>8</sub>  | 52  | OE <sub>B</sub> | 77  | D <sub>8</sub>  |
| 3   | OE <sub>C</sub>                | 28  | A <sub>7</sub>  | 53  | LDBI            | 78  | D <sub>7</sub>  |
| 4   | LDCI                           | 29  | A <sub>6</sub>  | 54  | LDBO            | 79  | D <sub>6</sub>  |
| 5   | LDCO                           | 30  | GND             | 55  | Mode__W         | 80  | GND             |
| 6   | SA <sub>2</sub> X <sub>1</sub> | 31  | A <sub>5</sub>  | 56  | YSEL            | 81  | D <sub>5</sub>  |
| 7   | SA <sub>2</sub> X <sub>0</sub> | 32  | A <sub>4</sub>  | 57  | OE <sub>Y</sub> | 82  | D <sub>4</sub>  |
| 8   | X <sub>0</sub>                 | 33  | A <sub>3</sub>  | 58  | Y <sub>8</sub>  | 83  | D <sub>3</sub>  |
| 9   | X <sub>1</sub>                 | 34  | A <sub>2</sub>  | 59  | Y <sub>7</sub>  | 84  | D <sub>2</sub>  |
| 10  | GND                            | 35  | GND             | 60  | GND             | 85  | GND             |
| 11  | X <sub>2</sub>                 | 36  | A <sub>1</sub>  | 61  | Y <sub>6</sub>  | 86  | D <sub>1</sub>  |
| 12  | X <sub>3</sub>                 | 37  | A <sub>0</sub>  | 62  | Y <sub>5</sub>  | 87  | D <sub>0</sub>  |
| 13  | X <sub>4</sub>                 | 38  | V <sub>CC</sub> | 63  | Y <sub>4</sub>  | 88  | V <sub>CC</sub> |
| 14  | X <sub>5</sub>                 | 39  | B <sub>0</sub>  | 64  | Y <sub>3</sub>  | 89  | C <sub>0</sub>  |
| 15  | X <sub>6</sub>                 | 40  | B <sub>1</sub>  | 65  | Y <sub>2</sub>  | 90  | C <sub>1</sub>  |
| 16  | GND                            | 41  | GND             | 66  | GND             | 91  | GND             |
| 17  | X <sub>7</sub>                 | 42  | B <sub>2</sub>  | 67  | Y <sub>1</sub>  | 92  | C <sub>2</sub>  |
| 18  | X <sub>8</sub>                 | 43  | B <sub>3</sub>  | 68  | Y <sub>0</sub>  | 93  | C <sub>3</sub>  |
| 19  | OE <sub>X</sub>                | 44  | B <sub>4</sub>  | 69  | LDDO            | 94  | C <sub>4</sub>  |
| 20  | XSEL <sub>0</sub>              | 45  | B <sub>5</sub>  | 70  | LDDI            | 95  | C <sub>5</sub>  |
| 21  | XSEL <sub>1</sub>              | 46  | GND             | 71  | ASEL1           | 96  | GND             |
| 22  | LDAO                           | 47  | B <sub>6</sub>  | 72  | ASEL0           | 97  | C <sub>6</sub>  |
| 23  | LDAI                           | 48  | B <sub>7</sub>  | 73  | OE <sub>D</sub> | 98  | C <sub>7</sub>  |
| 24  | OE <sub>A</sub>                | 49  | B <sub>8</sub>  | 74  | CP__XA          | 99  | C <sub>8</sub>  |
| 25  | V <sub>CC</sub>                | 50  | V <sub>CC</sub> | 75  | Mode__SC        | 100 | V <sub>CC</sub> |

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## Functional Description

The 74ABT3284 is a bi-directional registered data-path routing device which can multiplex/de-multiplex four 9-bit “A-side” data ports (Ports A, B, C, D) onto/from one 9-bit “X-side” port (Port X). Alternatively, it can be configured for mux/demux of two 18-bit data paths (Ports A and C, B and D) onto/from one 18-bit data path (Ports X and Y).

Each of the six 9-bit I/O ports have independent active low TRI-STATE® output enable control logic which can be configured to operate asynchronously or synchronously. With `MODE__SO` low, direct asynchronous output control is provided. With `MODE__SO` high, output enable control is asserted synchronously on the positive edge of the `CP__IN` clock. All I/O port inputs are continuously active allowing output state feedback.

The four A-side ports (A, B, C, D) contain independently enabled input and output data registers for storage of data passing in either direction. The input register (AIR, BIR, CIR, DIR) is loaded/held on the positive edge of `CP__AX` when the respective Load Control pin (LDAI, LDBI, LDCI, LDDI) is asserted high/low. The Input Registers can be loaded with data from the corresponding A-side port. The output register (AOR, BOR, COR, DOR) is loaded/held on the positive edge of `CP__XA` when the respective Load Control pin (LDAO, LDBO, LDCO, LDDO) is asserted high/low. The Output Registers can be loaded with data from Port X when `MODE__WS` is asserted low. When `MODE__WS` is asserted high, the Output Registers A and C can be loaded with Port X data and the B and D Output Registers can be loaded with data from Port Y.

When routing data from A-side to X-side, Data Path Control is provided for the following options via the `SA2X` inputs; Transparent mode where Input Register is bypassed but can simultaneously monitor A-side data; Registered Mode where X-side receives data from the selected Input Registers; Readback Mode where X-side receives data from the selected Output Registers. A-side data from Ports A, B, C, or D can be selected to Port X via the `XSEL` data path select inputs. Ports B or D can be selected to Port Y via the `YSEL` data path select input.

When routing data from X-side to A-side, Data Path Control is provided for the following options via the `ASEL` inputs; Transparent mode where Output Register is bypassed but can simultaneously monitor X-side data; Registered Mode where the A-side Port receives data from the corresponding Output Register; Readback Mode where the A-side Port receives data from the corresponding Input Registers. `MODE__WS` asserted low selects Port X data to be passed to Ports A, B, C, and D. With `MODE__WS` asserted high, Port X data is passed to Ports A and C with Port Y data passed to Ports B and D.

All Data Path Control Inputs and Input/Output Register Load Enable Inputs are active high and can be asserted asynchronously or synchronously. When `MODE__SC` is low, these inputs operate asynchronously. When `MODE__SC` is high, the inputs are asserted synchronously on the positive edge of the `CP__IN` clock.

When operating the Data Path Control and/or the Output Enable Input groups with `MODE__SC` and/or `MODE__SO` “hard wired” high for synchronous mode, a single pre-clock of `CP__IN` will be required following power-up to insure that all internal synchronous control registers are in the appropriate known state. if the application requires “on the fly” changes from asynchronous to synchronous operation, then the respective control/enable pin data must be pre-clocked via `CP__IN` and held steady prior to and during any low to high transition of the `MODE__SO` or `MODE__SC` to properly initiate the sync control registers for synchronous control mode.

## Pin Descriptions

| Pin Name               | Description                                                 | Operation   |
|------------------------|-------------------------------------------------------------|-------------|
| <code>OEa</code>       | Output Enable Inputs (Active Low)                           | Sync/ Async |
| <code>LDaI</code>      | Load Enable Inputs for the Input Registers                  | Sync/ Async |
| <code>LDaO</code>      | Load Enable Inputs for the Output Registers                 | Sync/ Async |
| <code>ASEL(0,1)</code> | A-Side Data Path Select Inputs                              | Sync/ Async |
| <code>SA2X(0,1)</code> | X-Side Data Path Select Inputs                              | Sync/ Async |
| <code>XSEL(0,1)</code> | X-Port Data Path Select Inputs                              | Sync/ Async |
| <code>YSEL</code>      | Y-Port Data Path Select Input                               | Sync/ Async |
| <code>MODE__W</code>   | Word Mode Select Input for the X/Y to A-Side Direction      | Sync/ Async |
| <code>MODE__SO</code>  | Enable Input for Synchronous Output Enable Control          | Async       |
| <code>MODE__SC</code>  | Enable Input for Synchronous Data Path Control              | Async       |
| <code>CP__IN</code>    | Clock Input for Synchronous Control (Positive Edge Trigger) |             |
| <code>CP__AX</code>    | Clock Input for Input Registers (Positive Edge Trigger)     |             |
| <code>CP__XA</code>    | Clock Input for Output Registers (Positive Edge Trigger)    |             |

## Function Tables

Output Enable Control Table

| Inputs                             |            |                                                                                   | Outputs               | Control Mode | Function                                 |
|------------------------------------|------------|-----------------------------------------------------------------------------------|-----------------------|--------------|------------------------------------------|
| $\overline{OE}$ (A, B, C, D, X, Y) | MODE__SO   | CP__IN                                                                            | Port A, B, C, D, X, Y |              |                                          |
| L                                  | L          | X                                                                                 | ENABLE                | ASYNC        | ENABLED OUTPUT, I/O input always active  |
| H                                  | L          | X                                                                                 | DISABLE               | ASYNC        | DISABLED OUTPUT, I/O input always active |
| (Notes 2, 3)                       | H (Note 1) |  | (Note 3)              | SYNC         | (Note 3)                                 |

**Note 1:** Low to High transitions of MODE\_\_SO must be immediately preceded by a low to high transition (clock edge) on CP\_\_IN while holding Synchronous Control Inputs  $\overline{OE}$  (A, B, C, D, X, Y) steady to preset internal registers and assure predictable operation during the control mode change from asynchronous to synchronous.

**Note 2:**  $\overline{OE}$  (A, B, C, D, X, Y) levels are synchronously asserted by the positive transition of CP\_\_IN when MODE\_\_SO is high.

**Note 3:** Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP\_\_IN.

A Side Data Path Select Function Table

| Inputs       |              |            |                                                                                     | Data Path        |                | Control Mode | Function                                                                         |
|--------------|--------------|------------|-------------------------------------------------------------------------------------|------------------|----------------|--------------|----------------------------------------------------------------------------------|
| ASEL(1)      | ASEL(0)      | MODE__SC   | CP__IN                                                                              | From Reg/Port    | To Port        |              |                                                                                  |
| L            | L            | L          | X                                                                                   | (A, B, C, D) IR  | A, B, C, D     | ASYNC        | Readback; Contents of Input Register (A, B, C, D) IR to Port (A, B, C, D)        |
| L            | H            | L          | X                                                                                   | (A, B, C, D) OR  | A, B, C, D     | ASYNC        | Clocked Path; Contents of Output Register (A, B, C, D) OR to Port (A, B, C, D)   |
| H            | L            | L          | X                                                                                   | Port X           | A, B, C, & D   | ASYNC        | Transparent Path; Port X to Port A, B, C, & D                                    |
| H            | H            | L          | X                                                                                   | Port X<br>Port Y | A & C<br>B & D | ASYNC        | Transparent Path; Port X to Port A & C<br>Transparent Path; Port Y to Port B & D |
| (Notes 2, 3) | (Notes 2, 3) | H (Note 1) |  | (Note 3)         | (Note 3)       | SYNC         | (Note 3)                                                                         |

**Note 1:** Low to High transitions of MODE\_\_SC must be immediately preceded by a low to high transition (clock edge) on CP\_\_IN while holding Synchronous Control Inputs ASEL(0) and ASEL(1) steady to preset internal registers and assure predictable operation during the control mode change from asynchronous to synchronous.

**Note 2:** ASEL(0) and ASEL(1) levels are synchronously asserted by the positive transition of CP\_\_IN when MODE\_\_SC is high.

**Note 3:** Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP\_\_IN.

Input Register Control Table

| Inputs            |                  |            |                                                                                     |                                                                                     | Register        | Control Mode | Function                                                                                 |
|-------------------|------------------|------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----------------|--------------|------------------------------------------------------------------------------------------|
| Port (A, B, C, D) | LD(A, B, C, D) I | MODE__SC   | CP__IN                                                                              | CP__XA                                                                              | (A, B, C, D) IR |              |                                                                                          |
| X                 | L                | L          | X                                                                                   |  | HOLD            | ASYNC        | HOLD; Input Register holds previous state.                                               |
| L (H)             | H                | L          | X                                                                                   |  | L (H)           | ASYNC        | LOAD; Port A, B, C, D clocked to Input Register (A, B, C, D) IR via CP__AX positive edge |
| (Note 3)          | (Notes 2, 3)     | H (Note 1) |  | (Note 3)                                                                            | (Note 3)        | SYNC         | (Note 3)                                                                                 |

**Note 1:** Low to High transitions of MODE\_\_SO must be immediately preceded by a low to high transition (clock edge) on CP\_\_IN while holding Synchronous Control Inputs LDAI, LDBI, LDCI, and LDDI steady to preset internal registers and assure predictable operation during the control mode change from asynchronous to synchronous.

**Note 2:** LDAI, LDBI, LDCI and LDDI levels are synchronously asserted by the positive transition of CP\_\_IN when MODE\_\_SC is high.

**Note 3:** Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP\_\_IN.

## Function Tables (Continued)

Output Register Control Table

| Inputs   |          |                  |              |            |                                                                                   |                                                                                   | Output Register |           | Control Mode | Function                                              |
|----------|----------|------------------|--------------|------------|-----------------------------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------------|-----------|--------------|-------------------------------------------------------|
| Port X   | Port Y   | LD(A, B, C, D) O | MODE__W      | MODE__SC   | CP__IN                                                                            | CP__XA                                                                            | (A, C) OR       | (B, D) OR |              |                                                       |
| X        | X        | L                | X            | L          | X                                                                                 |  | HOLD            | HOLD      | ASYNC        | HOLD OR                                               |
| L (H)    | X        | H                | L            | L          | X                                                                                 |  | L (H)           | L (H)     | ASYNC        | LOAD OR<br>Port X to OR (A, B, C, D)                  |
| L (H)    | L (H)    | H                | H            | L          | X                                                                                 |  | L (H)           | L (H)     | ASYNC        | LOAD OR<br>Port X to OR (A, C)<br>Port Y to OR (B, D) |
| (Note 3) | (Note 3) | (Notes 2, 3)     | (Notes 2, 3) | H (Note 1) |  | (Note 3)                                                                          | (Note 3)        | (Note 3)  | SYNC         | (Note 3)                                              |

**Note 1:** Low to High transitions of MODE\_\_SC must be immediately preceded by a low to high transition (clock edge) on CP\_\_IN while holding Synchronous Control Inputs LDAO, LDBO, LDCO, LDDO and MODE\_\_W steady to preset internal registers and assure predictable operation during the control mode change from asynchronous to synchronous.

**Note 2:** LDAO, LDBO, LDCO, LDDO and MODE\_\_W levels are synchronously asserted by the positive transition of CP\_\_IN when MODE\_\_SC is high.

**Note 3:** Synchronous Control Mode Functions are same as Asynchronous at time  $T + 1$  of CP\_\_IN.

## Function Tables (Continued)

1st Level X Side Data Path Select Function Table

| Inputs       |              |            |                                                                                   | Data Path       |                  | Control Mode | Function                                                                                 |
|--------------|--------------|------------|-----------------------------------------------------------------------------------|-----------------|------------------|--------------|------------------------------------------------------------------------------------------|
| SA2X(1)      | SA2X(0)      | MODE__SC   | CP__IN                                                                            | From Reg/Port   | To Internal Node |              |                                                                                          |
| L            | L            | L          | X                                                                                 | A, B, C, D      | (A, B, C, D) X   | ASYN         | Transparent datapath from Port (A, B, C, D) to internal node (A, B, C, D) X              |
| L            | H            | L          | X                                                                                 | (A, B, C, D) IR | (A, B, C, D) X   | ASYN         | Clocked Path; Contents of Input Register (A, B, C, D) IR to internal node (A, B, C, D) X |
| H            | L            | L          | X                                                                                 | (A, B, C, D) OR | (A, B, C, D) X   | ASYN         | Readback; contents of Output register (A, B, C, D) OR to internal node (A, B, C, D) X    |
| H            | H            | L          | X                                                                                 | GND             | (A, B, C, D) X   | ASYN         | D diagnostic; Select all 36 bits as low and pass to the internal node (A, B, C, D) X     |
| (Notes 2, 3) | (Notes 2, 3) | H (Note 1) |  | (Note 3)        | (Note 3)         | SYNC         | (Note 3)                                                                                 |

**Note 1:** Low to High transitions of MODE\_\_SC must be immediately preceded by a low to high transition (clock edge) on CP\_\_IN while holding Synchronous Control Inputs SA2X(0) and SA2X(1) steady to preset internal sync registers and assure predictable operation during the control mode change from asynchronous to synchronous.

**Note 2:** SA2X(0) and SA2X(1) levels are synchronously asserted by the positive transition of CP\_\_IN when MODE\_\_SC is high.

**Note 3:** Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP\_\_IN.

2nd Level X Side Data Path Select Function Table for Port X

| Inputs       |              |            |                                                                                     | Data Path          |          | Control Mode | Function                   |
|--------------|--------------|------------|-------------------------------------------------------------------------------------|--------------------|----------|--------------|----------------------------|
| XSEL(1)      | XSEL(0)      | MODE__SC   | CP__IN                                                                              | From Internal Node | To Port  |              |                            |
| L            | L            | L          | X                                                                                   | AX                 | X        | ASYN         | Internal Node AX to Port X |
| L            | H            | L          | X                                                                                   | BX                 | X        | ASYN         | Internal Node BX to Port X |
| H            | L            | L          | X                                                                                   | CX                 | X        | ASYN         | Internal Node CX to Port X |
| H            | H            | L          | X                                                                                   | DX                 | X        | ASYN         | Internal Node DX to Port X |
| (Notes 2, 3) | (Notes 2, 3) | H (Note 1) |  | (Note 3)           | (Note 3) | SYNC         | (Note 3)                   |

**Note 1:** Low to High transitions of MODE\_\_SC must be immediately preceded by a low to high transition (clock edge) on CP\_\_IN while holding Synchronous Control Inputs XSEL(0) and XSEL(1) steady to preset internal sync registers and assure predictable operation during the control mode change from asynchronous to synchronous.

**Note 2:** XSEL(0) and XSEL(1) levels are synchronously asserted by the positive transition of CP\_\_IN when MODE\_\_SC is high.

**Note 3:** Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP\_\_IN.

2nd Level X Side Data Path Select Function Table for Port Y

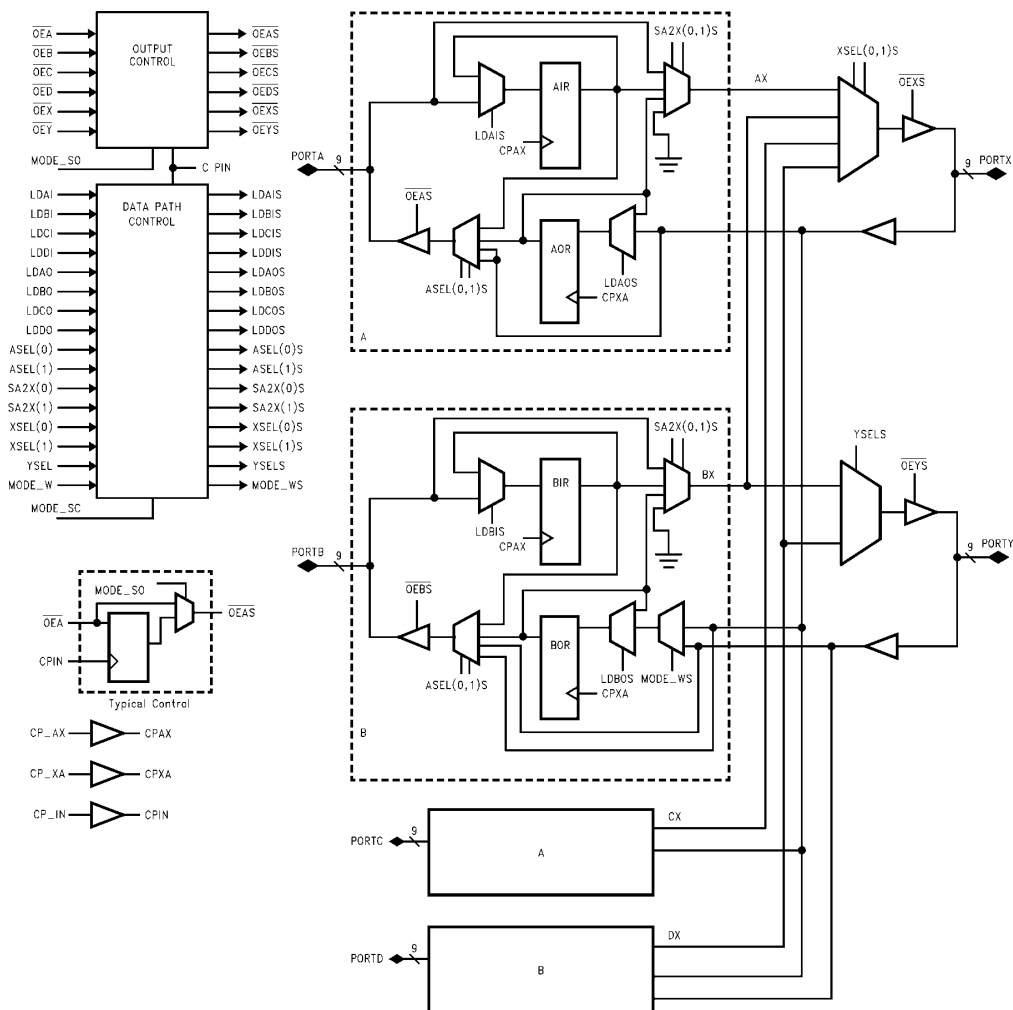
| Inputs       |            |                                                                                     | Data Path          |          | Control Mode | Function                   |
|--------------|------------|-------------------------------------------------------------------------------------|--------------------|----------|--------------|----------------------------|
| YSEL         | MODE__SC   | CP__IN                                                                              | From Internal Node | To Port  |              |                            |
| L            | L          | X                                                                                   | BX                 | Y        | ASYN         | Internal Node BX to Port Y |
| H            | L          | X                                                                                   | DX                 | Y        | ASYN         | Internal Node DX to Port Y |
| (Notes 2, 3) | H (Note 1) |  | (Note 3)           | (Note 3) | SYNC         | (Note 3)                   |

**Note 1:** Low to High transitions of MODE\_\_SC must be immediately preceded by a low to high transition (clock edge) on CP\_\_IN while holding Synchronous Control Inputs YSEL steady to preset internal registers and assure predictable operation during the control mode change from asynchronous to synchronous.

**Note 2:** YSEL levels are synchronously asserted by the positive transition of CP\_\_IN when MODE\_\_SC is high.

**Note 3:** Synchronous Control Mode Functions are same as Asynchronous at time T + 1 of CP\_\_IN.

## Logic Diagrams

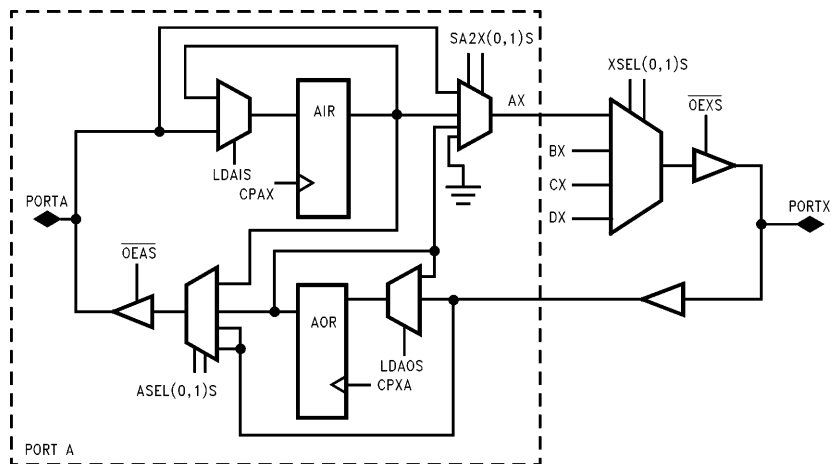


TL/F/11582-2

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### FIGURE 1. 18-Bit Synchronous Datapath Multiplexer

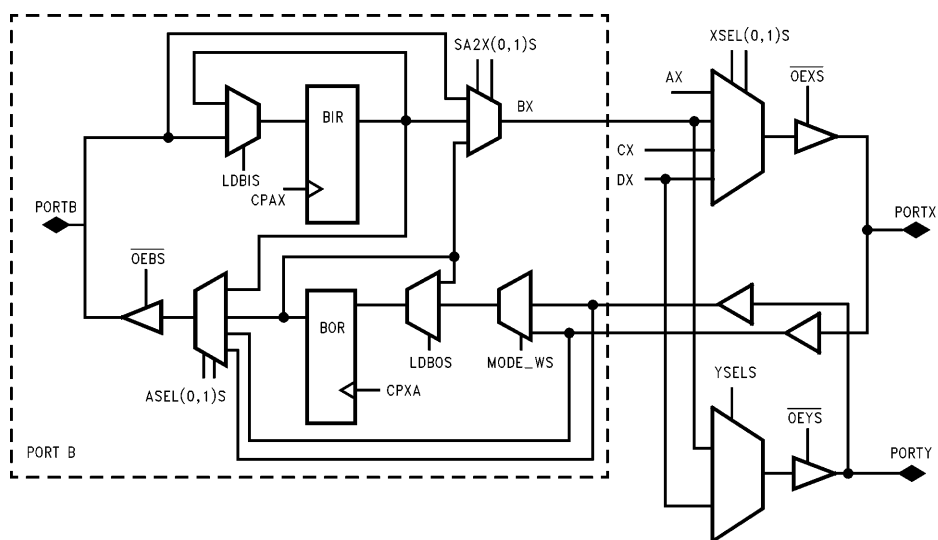
### Logic Diagrams (Continued)



**Note:** Port C configured identical to Port A.

**FIGURE 2. Synchronous Bus Multiplexer  
A-X Datapath**

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**Note:** Port D configured identical to Port B.

**FIGURE 3. Synchronous Bus Multiplexer  
B PORT Datapath**

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## Absolute Maximum Ratings (Note 1)

|                                             |                                      |
|---------------------------------------------|--------------------------------------|
| Storage Temperature                         | −65°C to +150°C                      |
| Ambient Temperature under Bias              | −55°C to +125°C                      |
| Junction Temperature under Bias             |                                      |
| Ceramic                                     | −55°C to +175°C                      |
| Plastic                                     | −55°C to +150°C                      |
| V <sub>CC</sub> Pin Potential to Ground Pin | −0.5V to +7.0V                       |
| Input Voltage (Note 2)                      | −0.5V to +7.0V                       |
| Input Current (Note 2)                      | −30 mA to +5.0 mA                    |
| Voltage Applied to Any Output               |                                      |
| in the Disabled or Power-off State          | −0.5V to +5.5V                       |
| in the HIGH STATE                           | −0.5V to V <sub>CC</sub>             |
| Current Applied to Output                   |                                      |
| in LOW State (Max)                          | twice the rated I <sub>OL</sub> (mA) |

|                            |         |
|----------------------------|---------|
| DC Latchup Source Current  | −300 mA |
| Over Voltage Latchup (I/O) | 10V     |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

|                              |                |
|------------------------------|----------------|
| Free Air Ambient Temperature |                |
| Commercial                   | −40°C to +85°C |
| Supply Voltage               |                |
| Commercial                   | +4.5V to +5.5V |
| Minimum Input Edge Rate      | (ΔV/Δt)        |
| Data Input                   | 50 mV/ns       |
| Enable Input                 | 20 mV/ns       |
| Clock Input                  | 100 mV/ns      |

## DC Electrical Characteristics

| Symbol                             | Parameter                               | ABT3284    |      |      | Units      | V <sub>CC</sub> | Conditions                                                                                                                                                  |
|------------------------------------|-----------------------------------------|------------|------|------|------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                                    |                                         | Min        | Typ  | Max  |            |                 |                                                                                                                                                             |
| V <sub>IH</sub>                    | Input HIGH Voltage                      | 2.0        |      |      | V          |                 | Recognized HIGH Signal                                                                                                                                      |
| V <sub>IL</sub>                    | Input LOW Voltage                       |            | 0.8  |      | V          |                 | Recognized LOW Signal                                                                                                                                       |
| V <sub>CD</sub>                    | Input Clamp Voltage                     |            |      | −1.2 | V          | Min             | I <sub>IN</sub> = −18 mA                                                                                                                                    |
| V <sub>OH</sub>                    | Output HIGH Voltage                     | 2.5<br>2.0 |      |      | V          | Min             | I <sub>OH</sub> = −3 mA<br>I <sub>OH</sub> = −32 mA (Note 3)                                                                                                |
| V <sub>OL</sub>                    | Output LOW Voltage                      |            | 0.55 |      | V          | Min             | I <sub>OL</sub> = 64 mA (Note 4)                                                                                                                            |
| I <sub>IH</sub>                    | Input HIGH Current                      |            | 5    |      | μA         | Max             | V <sub>IN</sub> = V <sub>CC</sub>                                                                                                                           |
| I <sub>BVI</sub>                   | Input HIGH Current Breakdown Test       |            | 7    |      | μA         | Max             | V <sub>IN</sub> = 7.0V Control Inputs                                                                                                                       |
| I <sub>BVIT</sub>                  | Input HIGH Current Breakdown Test (I/O) |            | 100  |      | μA         | Max             | V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> , D <sub>n</sub> , X <sub>n</sub> , Y <sub>n</sub> )                               |
| I <sub>IL</sub>                    | Input LOW Current                       |            | −5   |      | μA         | Max             | V <sub>IN</sub> = 0.5V Control Inputs                                                                                                                       |
| V <sub>ID</sub>                    | Input Leakage Test                      | 4.75       |      |      | V          | 0.0             | I <sub>ID</sub> = 1.9 μA Control Inputs<br>All Data Pins Grounded                                                                                           |
| I <sub>IH</sub> + I <sub>OZH</sub> | Output Leakage Current                  |            | 50   |      | μA         | 0–5.5           | V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> , D <sub>n</sub> , X <sub>n</sub> , Y <sub>n</sub> )<br>All Output Enables = 2.0V |
| I <sub>IL</sub> + I <sub>OZL</sub> | Output Leakage Current                  |            | −50  |      | μA         | 0–5.5           | V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> , D <sub>n</sub> , X <sub>n</sub> , Y <sub>n</sub> )<br>All Output Enables = 2.0V |
| I <sub>OS</sub>                    | Output Short-Circuit Current            | −100       | −275 |      | mA         | Max             | V <sub>OUT</sub> = 0.0V (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> , D <sub>n</sub> , X <sub>n</sub> , Y <sub>n</sub> ) (Note 5)                     |
| I <sub>CEX</sub>                   | Output High Leakage Current             |            | 50   |      | μA         | Max             | V <sub>OUT</sub> = V <sub>CC</sub> (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> , D <sub>n</sub> , X <sub>n</sub> , Y <sub>n</sub> )                   |
| I <sub>ZZ</sub>                    | Bus Drainage Test                       |            | 100  |      | μA         | 0.0             | V <sub>OUT</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> , C <sub>n</sub> , D <sub>n</sub> , X <sub>n</sub> , Y <sub>n</sub> )                              |
| I <sub>CCH</sub>                   | Power Supply Current                    |            | 2.5  |      | mA         | Max             | All Outputs HIGH                                                                                                                                            |
| I <sub>CCL</sub>                   | Power Supply Current                    |            | 140  |      | mA         | Max             | 36 Outputs LOW                                                                                                                                              |
| I <sub>CCZ</sub>                   | Power Supply Current                    |            | 2.5  |      | mA         | Max             | Output Enables = V <sub>CC</sub> ;<br>All Others at GND                                                                                                     |
| I <sub>CCT</sub>                   | Additional I <sub>CC</sub> /Input       |            | 2.5  |      | mA         | Max             | V <sub>IN</sub> = V <sub>CC</sub> − 2.1V<br>All Others at V <sub>CC</sub> or GND                                                                            |
| I <sub>CCD</sub>                   | Dynamic I <sub>CC</sub> No Load         |            | 0.35 |      | mA/<br>MHz | Max             | Outputs Open, Transparent Mode<br>Output Enables = GND<br>One Bit Toggling, 50% Duty Cycle                                                                  |

**Note 3:** Up to 18 outputs can each source 32 mA continuously, or any combination of outputs can source up to a total of 324 mA. For example, 36 outputs can continuously each source 16 mA.

**Note 4:** Up to 18 outputs can each sink 64 mA continuously, or any combination of outputs can sink up to a total of 648 mA. For example, 36 outputs can continuously each sink 32 mA.

**Note 5:** One output at a time, duration 1 second maximum.



## DC Electrical Characteristics (Continued)

| Symbol           | Parameter                                    | Min  | Typ  | Max | Units | V <sub>CC</sub> | Conditions<br>C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω |
|------------------|----------------------------------------------|------|------|-----|-------|-----------------|-------------------------------------------------------------|
| V <sub>OLP</sub> | Quiet Output Maximum Dynamic V <sub>OL</sub> |      | 0.7  | 1.0 | V     | 5.0             | T <sub>A</sub> = 25°C (Note 1)                              |
| V <sub>OLV</sub> | Quiet Output Minimum Dynamic V <sub>OL</sub> | −0.8 | −0.5 |     | V     | 5.0             | T <sub>A</sub> = 25°C (Note 1)                              |
| V <sub>OHV</sub> | Minimum High Level Dynamic Output Voltage    | 2.5  | 3.0  |     | V     | 5.0             | T <sub>A</sub> = 25°C (Note 3)                              |
| V <sub>IHD</sub> | Minimum High Level Dynamic Input Voltage     | 2.0  | 1.7  |     | V     | 5.0             | T <sub>A</sub> = 25°C (Note 2)                              |
| V <sub>ILD</sub> | Maximum Low Level Dynamic Input Voltage      |      | 1.2  | 0.8 | V     | 5.0             | T <sub>A</sub> = 25°C (Note 2)                              |

**Note 1:** Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

**Note 2:** Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V<sub>ILD</sub>), 0V to threshold (V<sub>IHD</sub>). Guaranteed, but not tested.

**Note 3:** Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

## AC Electrical Characteristics Single Output Switching

| Symbol                               | Parameter                                                                                   | 74ABT                                                                     |     | 74ABT                                                                                      |     | Units |
|--------------------------------------|---------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|-----|--------------------------------------------------------------------------------------------|-----|-------|
|                                      |                                                                                             | T <sub>A</sub> = 25°C<br>V <sub>CC</sub> = 5.0V<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> = −40°C to +85°C<br>V <sub>CC</sub> = 4.5V to 5.5V<br>C <sub>L</sub> = 50pF |     |       |
|                                      |                                                                                             | Min                                                                       | Max | Min                                                                                        | Max |       |
| f <sub>MAX</sub>                     | Max Operating Frequency                                                                     | 150                                                                       |     |                                                                                            |     |       |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay A, B, C, D or X<br>Inputs to X or A, B, C, D Outputs.<br>Transparent Mode | 1.5                                                                       | 5.5 | 1.5                                                                                        | 5.5 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay B, D or Y Inputs<br>to Y or B, D Outputs. Transparent Mode                | 1.0                                                                       | 5.0 | 1.0                                                                                        | 5.0 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay CP__XA ↑ to<br>A, B, C, or D. Registered Mode                             | 1.5                                                                       | 6.0 | 1.5                                                                                        | 6.0 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay CP__AX ↑ to<br>X. Registered Mode                                         | 1.5                                                                       | 7.0 | 1.5                                                                                        | 7.0 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay CP__AX ↑ to<br>Y. Registered Mode                                         | 1.5                                                                       | 6.5 | 1.5                                                                                        | 6.5 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay ASELn to<br>A, B, C or D. Asynchronous Mode                               | 2.0                                                                       | 7.5 | 2.0                                                                                        | 7.5 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay CP__IN ↑ to<br>A, B, C or D. ASELn Synchronous Mode                       | 2.5                                                                       | 8.5 | 2.5                                                                                        | 8.5 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay SA2Xn to<br>X or Y. Asynchronous Mode                                     | 1.5                                                                       | 7.5 | 1.5                                                                                        | 7.5 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay CP__IN ↑ to<br>X or Y. SA2Xn Synchronous Mode                             | 2.0                                                                       | 8.5 | 2.0                                                                                        | 8.5 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay XSELn to<br>X. Asynchronous Mode                                          | 1.5                                                                       | 6.0 | 1.5                                                                                        | 6.0 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay CP__IN ↑ to<br>X. XSELn Synchronous Mode                                  | 2.0                                                                       | 7.5 | 2.0                                                                                        | 7.5 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay YSELn to<br>Y. Asynchronous Mode                                          | 1.0                                                                       | 5.5 | 1.0                                                                                        | 5.5 | ns    |
| t <sub>PHL</sub><br>t <sub>PLH</sub> | Propagation Delay CP__IN ↑ to<br>Y. YSELn Synchronous Mode                                  | 1.5                                                                       | 6.5 | 1.5                                                                                        | 6.5 | ns    |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Asynchronous Enable Time                                                                    | 1.0                                                                       | 6.0 | 1.0                                                                                        | 6.0 | ns    |
| t <sub>PZH</sub><br>t <sub>PZL</sub> | Synchronous Enable Time                                                                     | 1.5                                                                       | 7.0 | 1.5                                                                                        | 7.0 | ns    |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Asynchronous Disable Time                                                                   | 1.0                                                                       | 7.5 | 1.0                                                                                        | 7.5 | ns    |
| t <sub>PHZ</sub><br>t <sub>PLZ</sub> | Synchronous Disable Time                                                                    | 1.5                                                                       | 8.5 | 1.5                                                                                        | 8.5 | ns    |

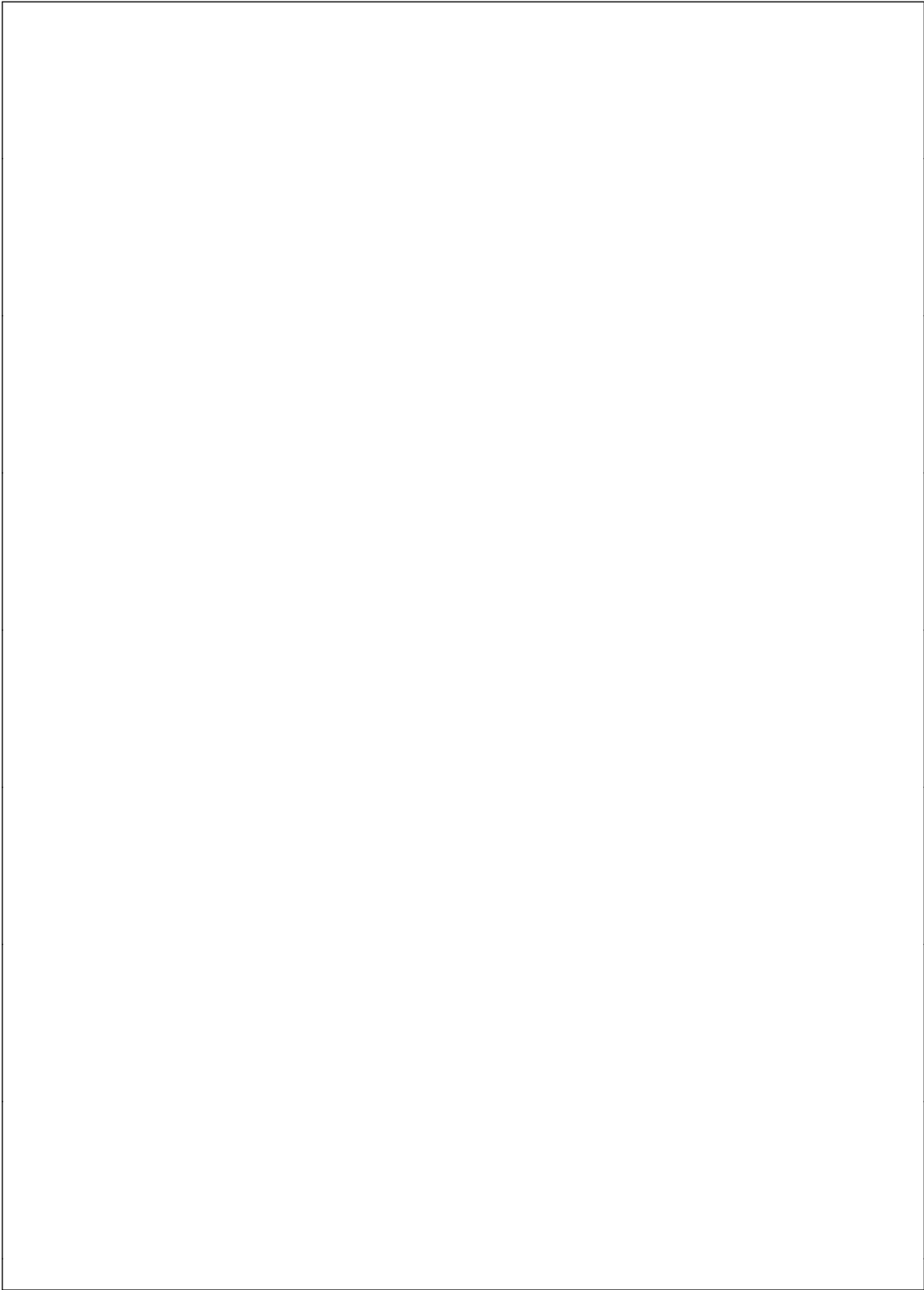
## AC Operating Requirements Single Output Switching

| Symbol                             | Parameter                                                                                                        | 74ABT                                                                        | 74ABT                                                                                                                 | Units |
|------------------------------------|------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------|-------|
|                                    |                                                                                                                  | $T_A = 25^{\circ}\text{C}$<br>$V_{CC} = 5.0\text{V}$<br>$C_L = 50\text{ pF}$ | $T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$<br>$V_{CC} = 4.5\text{V to } 5.5\text{V}$<br>$C_L = 50\text{ pF}$ |       |
|                                    |                                                                                                                  | Min                                                                          | Max                                                                                                                   |       |
| $t_s(\text{H})$<br>$t_s(\text{L})$ | Setup Time High or Low A, B, C, D<br>X or Y. Data to CP__AX $\uparrow$ or CP__XA $\uparrow$<br>(Registered Mode) | 4.0                                                                          | 4.0                                                                                                                   | ns    |
| $t_h(\text{H})$<br>$t_h(\text{L})$ | Hold Time High or Low A, B, C, D<br>X or Y. Data to CP__AX $\uparrow$ or CP__XA $\uparrow$<br>(Registered Mode)  | 0.0                                                                          | 0.0                                                                                                                   | ns    |
| $t_s(\text{H})$<br>$t_s(\text{L})$ | Setup Time High or Low Control<br>Inputs to CP__IN $\uparrow$ . (Synchronous Mode)                               | 3.0                                                                          | 3.0                                                                                                                   | ns    |
| $t_h(\text{H})$<br>$t_h(\text{L})$ | Hold Time High or Low Control<br>Inputs to CP__IN $\uparrow$ . (Synchronous Mode)                                | 0.0                                                                          | 0.0                                                                                                                   | ns    |
| $t_s(\text{H})$                    | Setup Time High, CP__IN $\uparrow$ to<br>CP__AX $\uparrow$ or CP__XA $\uparrow$ .                                | 5.0                                                                          | 5.0                                                                                                                   | ns    |
| $t_h(\text{L})$                    | Hold Time Low, CP__IN $\uparrow$ to<br>CP__AX $\uparrow$ or CP__XA $\uparrow$ .                                  | 0.0                                                                          | 0.0                                                                                                                   | ns    |
| $t_w(\text{H})$<br>$t_w(\text{L})$ | CLK Pulsewidth High<br>CLK Pulsewidth Low                                                                        | 3.0<br>4.0                                                                   | 3.0<br>4.0                                                                                                            | ns    |

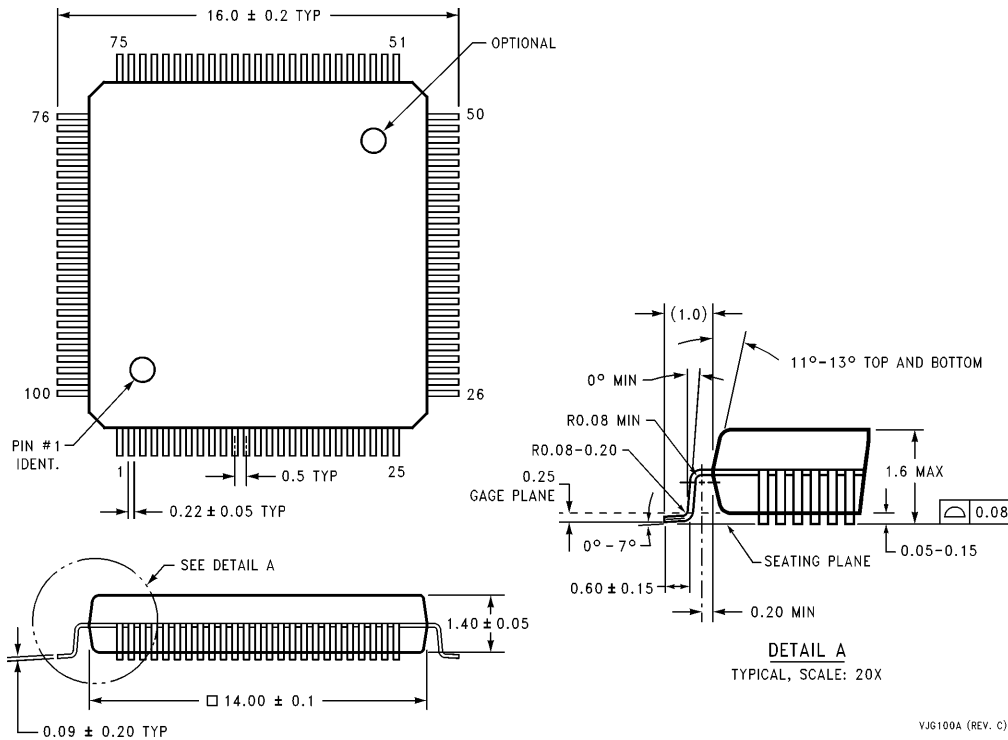
## Capacitance

| Symbol             | Parameter         | Typ | Units | Conditions<br>$T_A = 25^{\circ}\text{C}$                     |
|--------------------|-------------------|-----|-------|--------------------------------------------------------------|
| $C_{IN}$           | Input Capacitance | 5   | pF    | $V_{CC} = 0\text{V}$ Control Inputs                          |
| $C_{I/O}$ (Note 1) | I/O Capacitance   | 11  | pF    | $V_{CC} = 5.0\text{V}$<br>( $A_n, B_n, C_n, D_n, X_n, Y_n$ ) |

**Note 1:**  $C_{I/O}$  is measured at frequency  $f = 1\text{ MHz}$ , per MIL-STD-883B, Method 3012.



# Physical Dimensions inches (millimeters)



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