The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

For More Information

Please contact your local sales office for additional information about Cypress products and solutions.

About Cypress

Cypress is the leader in advanced embedded system solutions for the world's most innovative automotive, industrial, smart home appliances, consumer electronics and medical products. Cypress' microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first. Cypress is committed to providing customers with the best support and development resources on the planet enabling them to disrupt markets by creating new product categories in record time. To learn more, go to www.cypress.com.

MB39C502/503/504

High Efficiency Step Down DC/DC Controller Datasheet

Description

MB39C502 is a single output step down DC/DC controller using external FETs. It achieves the high efficiency with "Enhanced Low Power Mode (LPM) Operation" in light load. In Enhanced LPM, this controller operates that the quiescent current is reduced only 30µA and the switching frequency is fallen by extending on time. These operations enable to improve the efficiency in light load. Internal compensation circuit with current mode architecture and internal boost switch allow reducing the BOM parts and the component area.

Features

- High Efficiency with Enhanced LPM Operation
- Automatic Transition for PFM/PWM
- Enhanced LPM Operation Transferred by SLP_N Assertion
- Over Current Alerting
- Reference Voltage Accuracy: ±1%
- Output Voltage Range : 0.7V to 2.0V (MB39C502)
  : 2.4V to 3.5V (MB39C503)
  : fixed 5V (MB39C504)
- VIN Input Voltage Range : 4.0V to 25V (MB39C502/C503)
  : 5.4V to 25V (MB39C504)
- VDD Input Voltage Range: 4.5V to 5.5V (MB39C502/C503)
- Internal 5V LDO with Switchover (MB39C504)
- Fixed Frequency Emulated On-Time Control: 800kHz
- Current Mode Architecture with Internal Compensation Circuit
- Internal Boost Switch
- Fixed 700µs Soft Start Time without Load Dependence
- Internal Discharge FET
- Power Good Monitor
- Enhanced Protection Functions: OVP, UVP, ILIM
- Thermal Shutdown
- Small 3mm × 3mm × 0.75mm QFN16 Package

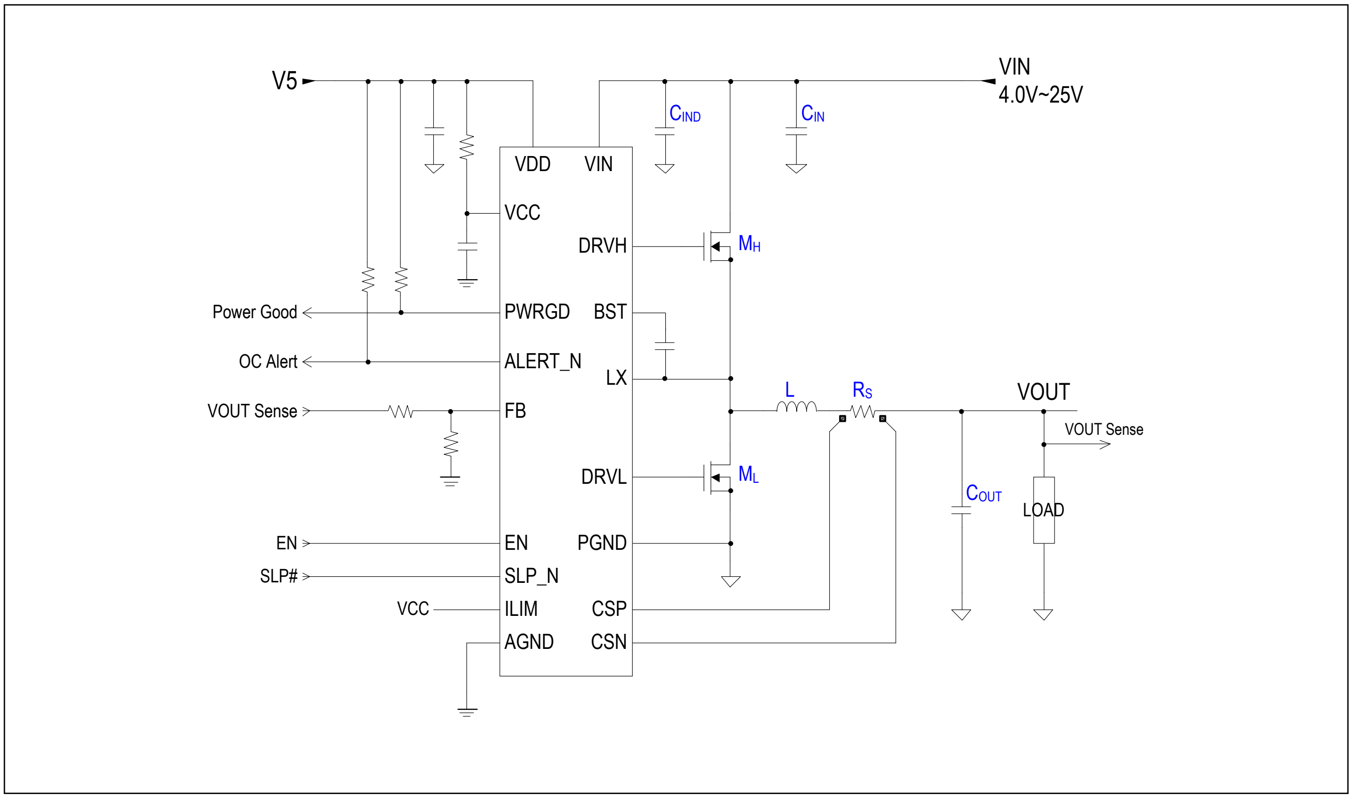
Applications

- Point of Load VR for Note PC
- General Purpose Step Down Regulator

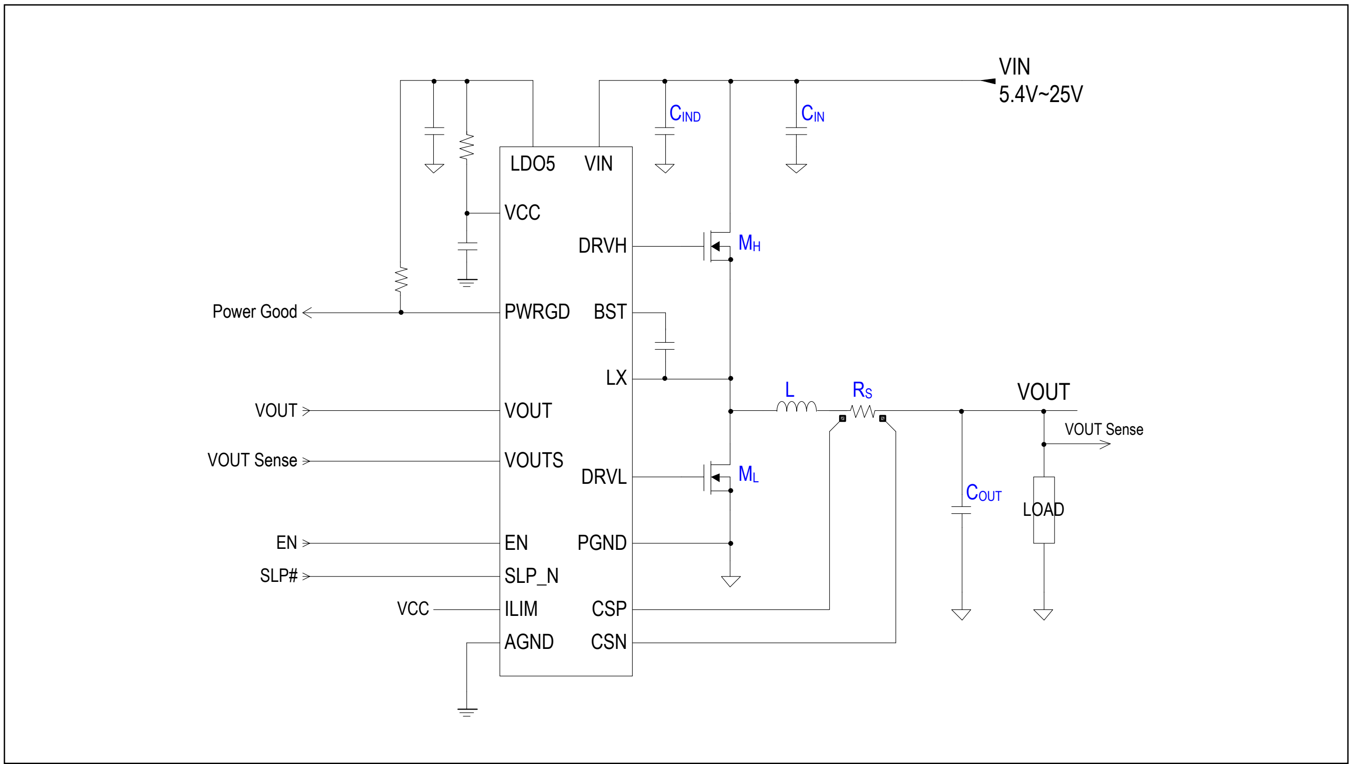
Contents

1. Typical Application

(MB39C502/C503)

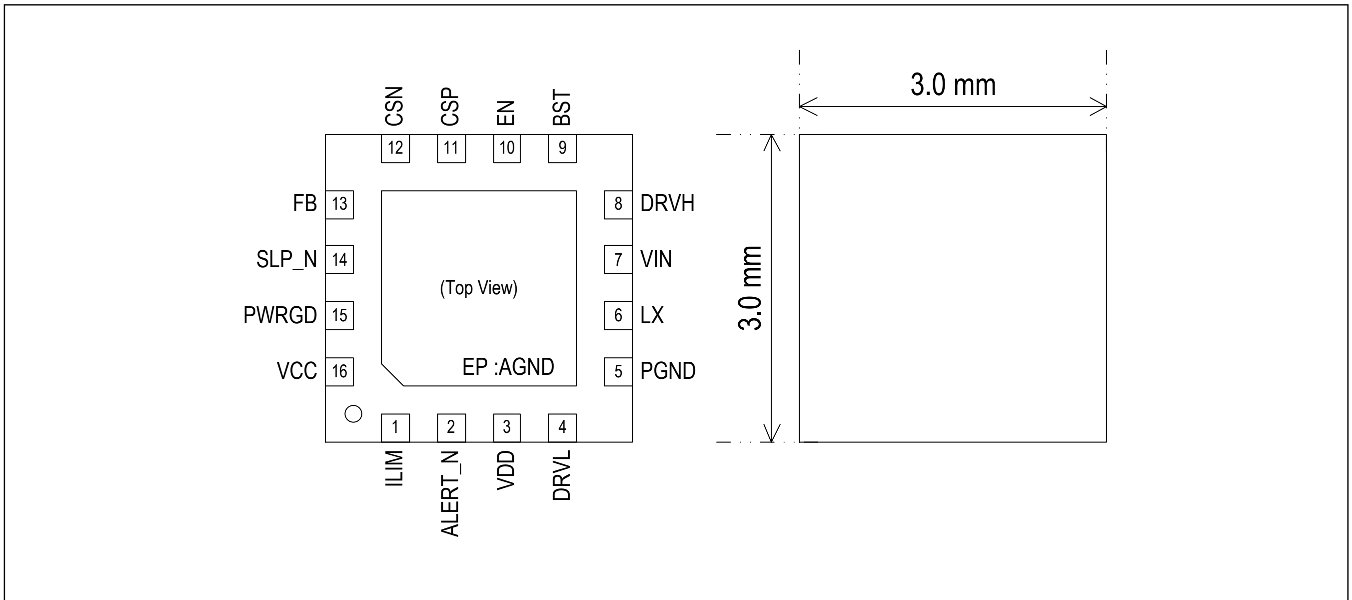


(MB39C504)

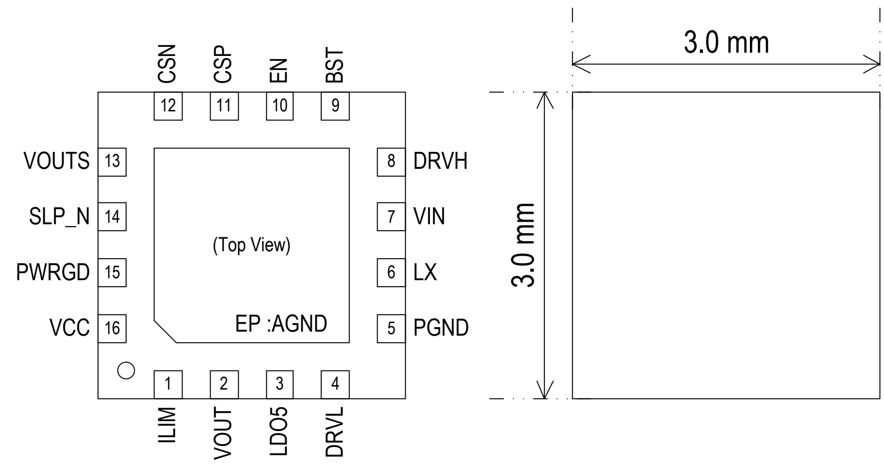


2. Pin Configuration

(MB39C502/C503)



(MB39C504)


CSN
CSP
EN
BST
12
11
10
9
VOUTS
13
SLP_N
14
PWRGD
15
VCC
16
8
DRVH
7
VIN
6
LX
5
PGND
(Top View)
EP :AGND
1
2
3
4
ILIM
VOUT
LDO5
DRVL
3.0 mm
3.0 mm

3. Pin Configuration

(MB39C502/C503)

Pin Number	Pin Name	I/O	Description
1	ILIM(*1)	I	Connect to VCC terminal.
2	ALERT_N	O	Open drain output terminal with over current alerting.
3	VDD	I	Power supply voltage input terminal of switching FET gate driver.
4	DRVL	O	Low side switching FET gate driver output terminal.
5	PGND	-	Power ground.
6	LX	-	Inductor and high side switching FET source connection terminal.
7	VIN	I	Power supply of switching regulator input terminal.
8	DRVH	O	High side switching FET gate driver output terminal.
9	BST	I	Boost capacitor connection terminal.
10	EN	I	Enable input of PWM controller. When turning on, apply greater than 0.65V and less than 5.5V. When turning off, apply less than 0.25V.
11	CSP	I	Current sensing positive input terminal.
12	CSN	I	Current sensing negative input terminal.
13	FB	I	Feedback voltage input of switching regulator.
14	SLP_N	I	Low power mode signal input terminal. Transferred to low power mode by connecting to “L” level
15	PWRGD	O	Open drain output terminal with power good.
16	VCC	I	Power supply voltage input terminal of PWM controller.
EP	AGND	-	Analog ground.

*1: ILIM terminal should be fixed to connect to VCC terminal.

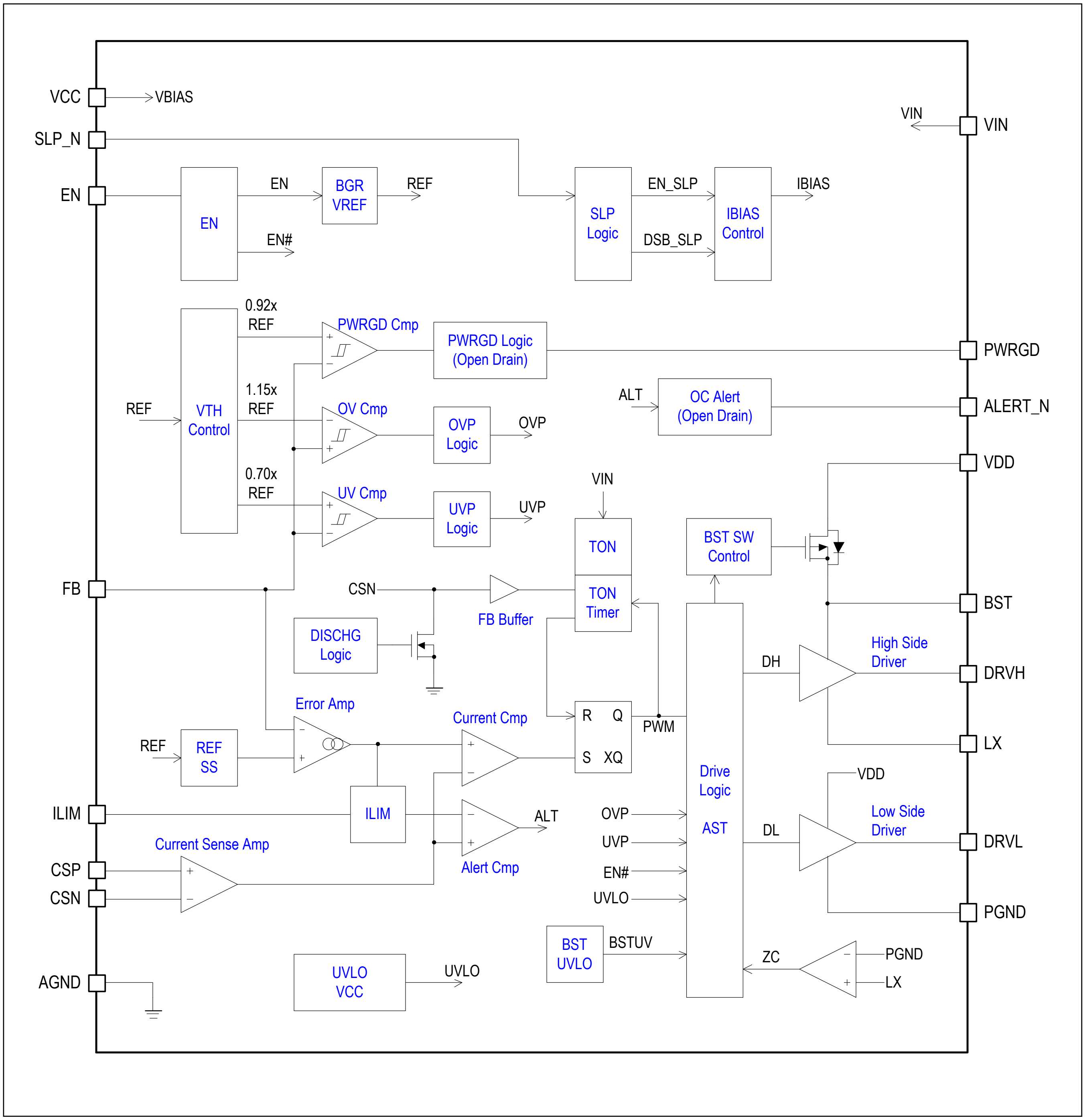
(MB39C504)

Pin Number	Pin Name	I/O	Description
1	ILIM(*1)	I	Connect to VCC terminal whenever.
2	VOUT	I	DCDC output voltage input for switchover.
3	LDO5	O	5V LDO output terminal.
4	DRVL	O	Low side switching FET gate driver output terminal.
5	PGND	-	Power ground.
6	LX	-	Inductor and high side switching FET source connection terminal.
7	VIN	I	Power supply of switching regulator input terminal.
8	DRVH	O	High side switching FET gate driver output terminal.
9	BST	I	Boost capacitor connection terminal.
10	EN	I	Enable input of PWM controller. When turning on, apply greater than 2.5V and less than 25V. When turning off, apply less than 0.6V.
11	CSP	I	Current sensing positive input terminal.
12	CSN	I	Current sensing negative input terminal.
13	VOUTS	I	DCDC output voltage input terminal.
14	SLP_N	I	Low power mode signal input terminal. Transferred to low power mode by connecting to “L” level
15	PWRGD	O	Open drain output terminal with power good.
16	VCC	I	Power supply voltage input terminal of PWM controller.
EP	AGND	-	Analog ground.

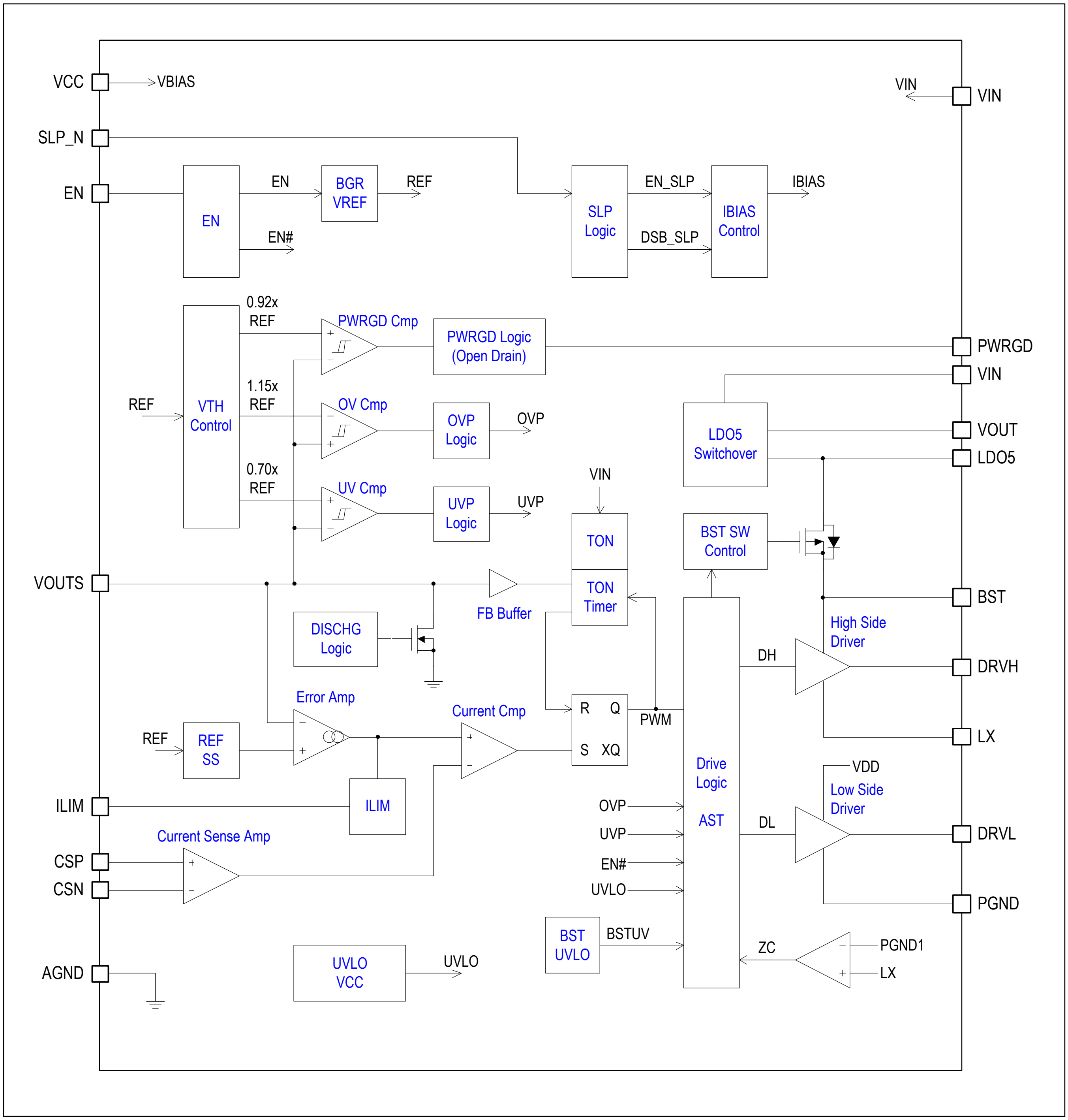
*1: ILIM terminal should be fixed to connect to VCC terminal.

4. Block Diagram

(MB39C502/C503)



(MB39C504)


VCC
VBIAS
SLP_N
EN
EN
EN
EN#
BGR VREF
REF
SLP Logic
EN_SLP
DSB_SLP
IBIAS Control
IBIAS
VIN
VIN
0.92x REF
PWRGD Cmp
PWRGD Logic (Open Drain)
PWRGD
VIN
REF
VTH Control
1.15x REF
OV Cmp
OVP Logic
OVP
LDO5 Switchover
VOUT
LDO5
0.70x REF
UV Cmp
UVP Logic
UVP
VIN
TON
BST SW Control
VOUTS
FB Buffer
TON Timer
BST
DISCHG Logic
High Side Driver
DH
DRVH
Error Amp
Current Cmp
R Q
S XQ
PWM
LX
REF
REF SS
Drive Logic
AST
VDD
Low Side Driver
ILIM
ILIM
OVP
UVP
EN#
UVLO
DL
DRVL
Current Sense Amp
CSP
CSN
PGND
BST UVLO
BSTUV
ZC
PGND1
LX
AGND
UVLO VCC
UVLO

5. Absolute Maximum Rating

(MB39C502/C503/C504)

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{VIN}	VIN input voltage	–0.3	+28	V
	V_{VCC}	VCC input voltage	–0.3	+6.5	V
	V_{VDD}	VDD input voltage (MB39C502/C503)	–0.3	+6.5	V
	V_{VOUT}	VOUT input voltage (MB39C504)	–0.3	+6.5	V
Terminal voltage	V_{BST}	BST bias voltage	–0.3	+34.5	V
	V_{LX}	LX switching voltage	–2	+28	V
	V_{FB}	FB input voltage (MB39C502/C503)	–0.3	V_{VCC} +0.3	V
	V_{VOUTS}	VOUTS input voltage	–0.3	+6.5	V
	V_{INPUT}	ILIM input voltage	–0.3	V_{VCC} +0.3	V
	V_{CS}	CSP, CSN input voltage	–0.3	+6.5	V
	V_{EN}	EN input voltage (MB39C502/C503)	–0.3	+6.5	V
		EN input voltage (MB39C504)	–0.3	+28	V
	V_{SLP}	SLP_N input voltage	–0.3	+6.5	V
	V_{NOD}	PWRGD, ALERT_N bias voltage	–0.3	+6.5	V
Difference voltage	V_{BST-LX}	BST–LX difference voltage	–0.3	+6.5	V
	$V_{BST-VDD}$	BST–VDD difference voltage (MB39C502/C503)	-	+28	V
	$V_{BST-LDO5}$	BST–VOUT, LDO5 difference voltage (MB39C504)	-	+28	V
	V_{GND}	AGND–PGND difference voltage	–0.3	+0.3	V
	$V_{CSP-CSN}$	CSP–CSN difference voltage	–0.3	+0.3	V
Output current	I_{DRV}	DRVH, DRVL DC current	–60	+60	mA
	I_{NOD}	PWRGD	-	+2	mA
	I_{ALERT}	ALERT_N sink current (MB39C502/C503)	-	+2	mA
Power dissipation	P_D	Ta ≤ ±25°C	-	2100(*1)	mW
Storage temperature	T_{STG}	-	–55	+125	°C

*1: When the IC is mounted on 10cm × 10cm four-layer square epoxy board. IC is mounted on a four-layer epoxy board, which terminal bias, and the IC’s thermal pad is connected to the epoxy board.

WARNING

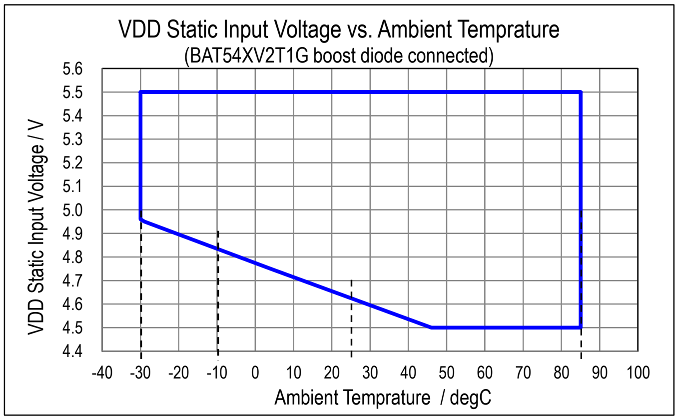
− *Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.*

6. Recommended Operating Conditions

(MB39C502/C503/C504)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{VIN}	VIN input voltage (MB39C502/C503)	4.0	-	25	V
	V_{VIN}	VIN input voltage (MB39C504)	5.4	-	25	V
	V_{VCC}	VCC input voltage	4.5	-	5.5	V
	V_{VDD}	VDD input voltage (MB39C502)	4.5(*1)	-	5.5	V
	V_{VDD}	VDD input voltage (MB39C503)	4.5	-	5.5	V
	V_{LDO5}	VOUT input voltage (MB39C504)	4.5	-	5.5	V
Terminal voltage	V_{BST}	BST bias voltage	0	-	30.5	V
	V_{LX}	LX switching voltage	–1	-	25	V
	V_{INPUT}	FB, ILIM input voltage (MB39C502/C503)	0	-	V_{VCC}	V
	V_{INPUT}	ILIM input voltage (MB39C504)	0	-	V_{VCC}	V
	V_{CS}	CSP, CSN input voltage (MB39C502)	0	-	2.0	V
	V_{CS}	CSP, CSN input voltage (MB39C503)	0	-	3.5	V
	V_{CS}	CSP, CSN, VOUTS input voltage (MB39C504)	0	-	5.5	V
	V_{EN}	EN, SLP_N input voltage (MB39C502/C503)	0	-	5.5	V
	V_{EN}	EN input voltage (MB39C504)	0	-	25	V
	V_{SLP}	SLP_N input voltage (MB39C504)	0	-	5.5	V
	V_{NOD}	PWRGD, ALERT_N bias voltage (MB39C502/C503)	0	-	5.5	V
	V_{NOD}	PWRGD bias voltage (MB39C504)	0	-	5.5	V
Difference voltage	$V_{BST\text{-}LX}$	BST–LX difference voltage	0	-	5.5	V
	$V_{BST\text{-}VDD}$	BST–VDD difference voltage (MB39C502/C503)	-	-	25	V
	$V_{BST\text{-}LDO5}$	BST–VOUT, LDO5 difference voltage (MB39C504)	-	-	25	V
	V_{GND}	AGND–PGND difference voltage	–0.05	-	0.05	V
	$V_{CSP\text{-}CSN}$	CSP–CSN difference voltage	0	-	35	mV
Output current	I_{DRV}	DRVH, DRVL DC current	–45	-	45	mA
	I_{NOD}	PWRGD, ALERT_N sink current	-	-	1	mA
BST capacitor	C_{BST}	Connect BST to LX capacitor	-	0.47	-	µF
VCC capacitor	C_{VCC}	Connect VCC to AGND capacitor	-	1.0	-	µF
VDD capacitor	C_{VDD}	Connect VDD to PGND capacitor (MB39C502/C503)	-	4.7	-	µF
LDO5 capacitor	C_{LDO5}	Connect LDO5 to PGND capacitor(MB39C504)	-	4.7	-	µF
Operating ambient temperature	T_A	Ambient temperature	–30	-	85	°C

*1: This VDD minimum input voltage indicates dynamic input range below 1ms. Refer to figure (next page) about the static VDD minimum input voltage.



WARNING

- *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
- *Always use semiconductor devices within their recommended operating condition ranges.*
- *Operation outside these ranges may adversely affect reliability and could result in device failure.*
- *No warranty is made with respect to use, conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

7. Electrical Characteristics

(MB39C502)

VIN = 7.4V, VDD, BST and EN connect to 5V power supply, PGND, LX = 0V. T_A = –30°C to +85°C, unless otherwise noted.

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
REFERENCE VOLTAGE						
Internal reference voltage	V_{REF}	This voltage is compared to feedback voltage. Ta = 25°C	0.693	0.700	0.707	V
		Ta = –10°C to 85°C	0.686	-	0.714	V
FB input current	I_{FB}	VFB = 1.0V	–0.1	-	0.1	μA
ENABLE, SLP_N						
Enable condition	V_{EN}	Enable voltage range	0.65	-	5.5	V
	V_{DSB}	Disable voltage range	0	-	0.25	V
EN input current	I_{EN}	V_{EN} = 5.0V	-	0	0.1	μA
SLP_N enable condition	V_{SLPDSB}	LPM disable voltage range	0.65	-	5.5	V
	V_{SLPEN}	LPM enable voltage range	0	-	0.35	V
SLP_N input current	I_{SLP_N}	V_{SLP_N} = 5.0V	-	0	0.1	μA
SUPPLY CURRENT						
VDD supply current	I_{VDDPWM}	VDD, VCC input current at PWM operating. T_A = 25°C	-	380	760	μA
	I_{VDDPFM}	VDD, VCC input current at idle state in PFM operation. Static 0A inductor current. T_A = 25°C	-	180	360	μA
	I_{VDDLPM}	VDD, VCC input current at idle state in LPM operation. Static 0A inductor current. T_A = 25°C	-	30	60	μA
VDD shutdown current	I_{VDDSDN}	VDD, VCC input current at V_{EN} = 0V	-	0.1	1.0	μA
VIN supply current	I_{VIN}	V_{VIN} = 25V	-	10	15	μA
VIN shutdown current	I_{VINSDN}	VIN input current at V_{EN} = 0V	-	0.1	1.0	μA
UNDER VOLTAGE LOCKOUT						
VCC UVLO threshold	V_{UVLO}	UVLO release voltage	3.99	4.14	4.29	V
	V_{HYS}	Hysteresis	0.005	0.070	0.200	V
SOFT START, DISCHARGE						
Period of power on reset	t_{POR}	From enable ON to the switching initiating.	200	-	1000	μs
Ramp up time	t_{SS}	From the switching initiating after enable ON to the output voltage reaches 95%.	598	665	732	μs
Discharge resistance	R_{DISCHG}	VOUT = 0.2V, discharge enable.	50	100	200	Ω
Discharge ends voltage	V_{DISCHG}	V_{CSN} voltage.	0.07	0.10	0.13	V

VIN = 7.4V, VDD, BST and EN connect to 5V power supply, PGND, LX = 0V. T_A = –30°C to +85°C, unless otherwise noted.

(MB39C502)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
ON TIMER						
On time	t_{ON}	V_{VIN} = 7.4V, V_{CSN} = 1.2V	193	210	227	ns
Minimum on time	t_{MINON}	V_{VIN} = 7.4V, V_{CSN} = 0.2V	80	120	-	ns
Minimum off time	t_{MINOFF}		-	200	400	ns
CURRENTLIMITATION						
Current limitation threshold	V_{ILIMIT}	CSP–CSN difference voltage at ILIM connects to VCC.	19.0	24.0	29.0	mV
ILIM input current	I_{ILIM}	V_{ILIM} = 5.0V	-	0	0.1	μA
CSP, CSN input current	I_{CS}	V_{CS} = 1.2V	–5.0	–2.0	-	μA
OVER AND UNDER VOLTAGE PROTECTION						
Over voltage threshold ratio	RT_{OV}	For target output voltage. At output voltage increasing.	110	115	125	%
Propagation delay of OV	t_{OV}	-	4	10	25	μs
Under voltage threshold ratio	RT_{UV}	For target output voltage. At output voltage decreasing.	65	70	75	%
Propagation delay of UV	t_{UV}	-	40	100	200	μs
POWER GOOD MONITOR						
Power good threshold ratio	RT_{PG}	For target output voltage. At output voltage increasing.	86	92	98	%
Hysteresis Ratio	RT_{HYS}	-	3	5	7	%
Propagation delay	t_{PG}	Power good	20	50	200	μs
	t_{PB}	Power bad	4	10	25	μs
PWRGD leak current	I_{LKPG}	V_{PWRGD} = 5.5V	-	0	1	μA
PWRGD output voltage “L” level	V_{OLPG}	I_{PWRGD} = 1mA sink	-	0.05	0.10	V
THERMAL SHUT DOWN						
Shut down temperature	T_{TSDH}	Shut down temperature.	-	150(*1)	-	°C
	T_{TSDL}	Exited temperature from thermal shut down state.	-	125(*1)	-	°C
OVER CURRENT ALERTING						
Over current alerting threshold ratio	RT_{ALT}	For target current limitation. At output current increasing.	78	85	92	%
Propagation delay	t_{ALTON}	On alerting assertion	20	50	200	μs
	t_{ALTOFF}	On alerting de-assertion	3	10	25	μs
ALERT_N leak current	I_{LKALT}	V_{ALERT_N} = 5.5V	-	0	1	μA
ALERT_N output voltage “L” level	V_{OLALT}	I_{ALERT_N} = 1mA sink	-	0.05	0.10	V

*1: No production tested, ensure by design.

VIN = 7.4V, VDD, BST and EN connect to 5V power supply, PGND, LX = 0V. T_A = –30°C to +85°C, unless otherwise noted.

(MB39C502)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
DRIVER						
High side on resistance	R_{HOH}	At 100mA current sourcing	-	3(*1)	-	Ω
	R_{HOL}	At 100mA current sinking	-	1(*1)	-	Ω
Low side on resistance	R_{LOH}	At 100mA current sourcing	-	4(*1)	-	Ω
	R_{LOL}	At 100mA current sinking	-	0.75(*1)	-	Ω
High side source current	I_{SRCH}	V_{DRVH} = 2.5V	-	0.7(*1)	-	A
High side sink current	I_{SINKH}	V_{DRVH} = 2.5V	-	1.1(*1)	-	A
Low side source current	I_{SRCL}	V_{DRVL} = 2.5V	-	0.5(*1)	-	A
Low side sink current	I_{SINKL}	V_{DRVL} = 2.5V	-	1.7(*1)	-	A
Dead time	t_{DEAD}	From DRVH turn off to DRVL turn on. And reverse it.	10	20	-	ns
BOOST SWITCH						
Boost switch on resistance	R_{BST}	I_{BST} = 10mA	-	30	50	Ω
BST leak current	I_{LKBST}	V_{BST} = 30V	-	0.1	1.0	μA

*1: No production tested, ensure by design.

VIN = 7.4V, VDD, BST and EN connect to 5V power supply, PGND, LX = 0V. T_A = –30°C to +85°C, unless otherwise noted.

(MB39C503)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
REFERENCE VOLTAGE						
Internal reference voltage	V_{REF}	This voltage is compared to feedback voltage. Ta = 25°C	0.99	1.00	1.01	V
		Ta = –10°C to 85°C	0.98	-	1.02	V
FB input current	I_{FB}	VFB = 1.0V	–0.1	-	0.1	µA
ENABLE, SLP_N						
Enable condition	V_{EN}	Enable voltage range	0.65	-	5.5	V
	V_{DSB}	Disable voltage range	0	-	0.25	V
EN input current	I_{EN}	V_{EN} = 5.0V	-	0	0.1	µA
SLP_N enable condition	V_{SLPDSB}	LPM disable voltage range	0.65	-	5.5	V
	V_{SLPEN}	LPM enable voltage range	0	-	0.35	V
SLP_N input current	I_{SLP_N}	V_{SLP_N} = 5.0V	-	0	0.1	µA
SUPPLY CURRENT						
VDD supply current	I_{VDDPWM}	VDD, VCC input current at PWM operating. T_A = 25°C	-	380	760	µA
	I_{VDDPFM}	VDD, VCC input current at idle state in PFM operation. Static 0A inductor current. T_A = 25°C	-	180	360	µA
	I_{VDDLPM}	VDD, VCC input current at idle state in LPM operation. Static 0A inductor current. T_A = 25°C	-	30	60	µA
VDD shutdown current	I_{VDDSDN}	VDD, VCC input current at V_{EN} = 0V	-	0.1	1.0	µA
VIN supply current	I_{VIN}	V_{VIN} = 25V	-	10	15	µA
VIN shutdown current	I_{VINSDN}	VIN input current at V_{EN} = 0V	-	0.1	1.0	µA
UNDER VOLTAGE LOCKOUT						
VCC UVLO threshold	V_{UVLO}	UVLO release voltage	3.99	4.14	4.29	V
	V_{HYS}	Hysteresis	0.005	0.070	0.200	V
SOFT START, DISCHARGE						
Period of power on reset	t_{POR}	From enable ON to the switching initiating.	200	-	1000	µs
Ramp up time	t_{SS}	From the switching initiating after enable ON to the output voltage reaches 95%.	598	665	732	µs
Discharge resistance	R_{DISCHG}	VOUT = 0.2V, discharge enable.	50	100	200	Ω
Discharge ends voltage	V_{DISCHG}	V_{CSN} voltage.	0.07	0.10	0.13	V

VIN = 7.4V, VDD, BST and EN connect to 5V power supply, PGND, LX = 0V. T_A = –30°C to +85°C, unless otherwise noted.

(MB39C503)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
ON TIMER						
On time	t_{ON}	V_{VIN} = 7.4V, V_{CSN} = 3.3V	529	575	621	ns
Minimum on time	t_{MINON}	V_{VIN} = 7.4V, V_{CSN} = 0.2V	100	200		ns
Minimum off time	t_{MINOFF}	-		90	180	ns
CURRENTLIMITATION						
Current limitation threshold	V_{ILIMIT}	CSP–CSN difference voltage at ILIM connects to VCC.	21.0	26.0	31.0	mV
ILIM input current	I_{ILIM}	V_{ILIM} = 5.0V	-	0	0.1	µA
CSP input current	I_{CSP}	V_{CSP} = 3.3V	-	2.0	5.0	µA
CSN input current	I_{CSN}	V_{CSP} = 3.3V	-	8.0	20.0	µA
OVER AND UNDER VOLTAGE PROTECTION						
Over voltage threshold ratio	RT_{OV}	For target output voltage. At output voltage increasing.	110	115	125	%
Propagation delay of OV	t_{OV}	-	4	10	25	µs
Under voltage threshold ratio	RT_{UV}	For target output voltage. At output voltage decreasing.	65	70	75	%
Propagation delay of UV	t_{UV}	-	40	100	200	µs
POWER GOOD MONITOR						
Power good threshold ratio	RT_{PG}	For target output voltage. At output voltage increasing.	86	92	98	%
Hysteresis Ratio	RT_{HYS}	-	3	5	7	%
Propagation delay	t_{PG}	Power good	20	50	200	µs
	t_{PB}	Power bad	4	10	25	µs
PWRGD leak current	I_{LKPG}	V_{PWRGD} = 5.5V	-	0	1	µA
PWRGD output voltage “L” level	V_{OLPG}	I_{PWRGD} = 1mA sink	-	0.05	0.10	V
THERMAL SHUT DOWN						
Shut down temperature	T_{TSDH}	Shut down temperature.	-	150(*1)	-	°C
	T_{TSDL}	Exited temperature from thermal shut down state.	-	125(*1)	-	°C
OVER CURRENT ALERTING						
Over current alerting threshold ratio	RT_{ALT}	For target current limitation. At output current increasing.	78	85	92	%
Propagation delay	t_{ALTON}	On alerting assertion	20	50	200	µs
	t_{ALTOFF}	On alerting de-assertion	3	10	25	µs
ALERT_N leak current	I_{LKALT}	V_{ALERT_N} = 5.5V	-	0	1	µA
ALERT_N output voltage “L” level	V_{OLALT}	I_{ALERT_N} = 1mA sink	-	0.05	0.10	V

*1: No production tested, ensure by design.

VIN = 7.4V, VDD, BST and EN connect to 5V power supply, PGND, LX = 0V. T_A = –30°C to +85°C, unless otherwise noted.

(MB39C503)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
DRIVER						
High side on resistance	R_{HOH}	At 100mA current sourcing	-	3(*1)	-	Ω
	R_{HOL}	At 100mA current sinking	-	1(*1)	-	Ω
Low side on resistance	R_{LOH}	At 100mA current sourcing	-	4(*1)	-	Ω
	R_{LOL}	At 100mA current sinking	-	0.75(*1)	-	Ω
High side source current	I_{SRCH}	V_{DRVH} = 2.5V	-	0.7(*1)	-	A
High side sink current	I_{SINKH}	V_{DRVH} = 2.5V	-	1.1(*1)	-	A
Low side source current	I_{SRCL}	V_{DRVL} = 2.5V	-	0.5(*1)	-	A
Low side sink current	I_{SINKL}	V_{DRVL} = 2.5V	-	1.7(*1)	-	A
Dead time	t_{DEAD}	From DRVH turn off to DRVL turn on. And reverse it.	10	20	-	ns
BOOST SWITCH						
Boost switch on resistance	R_{BST}	I_{BST} = 10mA	-	30	50	Ω
BST leak current	I_{LKBST}	V_{BST} = 30V	-	0.1	1.0	μA

*1: No production tested, ensure by design.

VIN = 7.4V, VOUT, BST and EN connect to 5V power supply, PGND, LX = 0V. T_A = –30°C to +85°C, unless otherwise noted.

(MB39C504)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
REFERENCE VOLTAGE						
Internal reference voltage	V_{REF}	This voltage is compared to feedback voltage. Ta = 25°C	4.95	5.00	5.05	V
		Ta = –10°C to 85°C	4.90	-	5.10	V
VOUTS input current	I_{VOUTS}	V_{VOUTS} = 5.0V	2.5	5.0	12.5	μA
ENABLE, SLP_N						
Enable condition	V_{EN}	Enable voltage range	2.5	-	25	V
	V_{DSB}	Disable voltage range	0	-	0.6	V
EN input current	I_{EN}	V_{EN} = 5.0V	-	0.5	1.2	μA
SLP_N enable condition	V_{SLPDSB}	LPM disable voltage range	0.65	-	5.5	V
	V_{SLPEN}	LPM enable voltage range	0	-	0.35	V
SLP_N input current	I_{SLP_N}	V_{SLP_N} = 5.0V	-	0	0.1	μA
SUPPLY CURRENT						
VOUT supply current	$I_{VOUTPWM}$	VOUT, VCC input current at PWM operating. T_A = 25°C	-	400	800	μA
	$I_{VOUTPFM}$	VOUT, VCC input current at idle state in PFM operation. Static 0A inductor current. T_A = 25°C	-	200	400	μA
	$I_{VOUTLPM}$	VOUT, VCC input current at idle state in LPM operation. Static 0A inductor current. T_A = 25°C	-	50	100	μA
VOUT shutdown current	$I_{VOUTSDN}$	VOUT, VCC input current at V_{EN} = 0V	-	0.1	1.0	μA
VIN supply current	I_{VIN}	V_{VIN} = 25V	-	20	30	μA
VIN shutdown current	I_{VINSDN}	VIN input current at V_{EN} = 0V	-	0.1	1.0	μA
UNDER VOLTAGE LOCKOUT						
VCC UVLO threshold	V_{UVLO}	UVLO release voltage	3.99	4.14	4.29	V
	V_{HYS}	Hysteresis	0.005	0.070	0.200	V
SOFT START, DISCHARGE						
Period of power on reset	t_{POR}	From enable ON to the switching initiating.	300	-	1400	μs
Ramp up time	t_{SS}	From the switching initiating after enable ON to the output voltage reaches 95%.	598	665	732	μs
Discharge resistance	R_{DISCHG}	VOUT = 0.2V, discharge enable.	50	100	200	Ω
Discharge ends voltage	V_{DISCHG}	V_{CSN} voltage.	0.07	0.10	0.13	V

VIN = 7.4V, VOUT, BST and EN connect to 5V power supply, PGND, LX = 0V. T_A = –30°C to +85°C, unless otherwise noted.

(MB39C504)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
ON TIMER						
On time	t_{ON}	V_{VIN} = 7.4V, V_{VOUT} = 5.0V	802	872	942	ns
Minimum on time	t_{MINON}	V_{VIN} = 7.4V, V_{VOUT} = 0.2V	100	200	-	ns
Minimum off time	t_{MINOFF}	-	-	120	240	ns
CURRENTLIMITATION						
Current limitation threshold	V_{ILIMIT}	CSP–CSN difference voltage at ILIM connects to VCC.	21.0	26.0	31.0	mV
ILIM input current	I_{ILIM}	V_{ILIM} = 5.0V	-	0	0.1	µA
CSP input current	I_{CSP}	V_{CSP} = 5.0V	-	2.0	5.0	µA
CSN input current	I_{CSN}	V_{CSN} = 5.0V	-	8.0	20.0	µA
OVER AND UNDER VOLTAGE PROTECTION						
Over voltage threshold ratio	RT_{OV}	For target output voltage. At output voltage increasing.	110	115	125	%
Propagation delay of OV	t_{OV}	-	4	10	25	µs
Under voltage threshold ratio	RT_{UV}	For target output voltage. At output voltage decreasing.	65	70	75	%
Propagation delay of UV	t_{UV}	-	40	100	200	µs
POWER GOOD MONITOR						
Power good threshold ratio	RT_{PG}	For target output voltage. At output voltage increasing.	86	92	98	%
Hysteresis Ratio	RT_{HYS}	-	3	5	7	%
Propagation delay	t_{PG}	Power good	20	50	200	µs
	t_{PB}	Power bad	4	10	25	µs
PWRGD leak current	I_{LKPG}	V_{PWRGD} = 5.5V	-	0	1	µA
PWRGD output voltage "L" level	V_{OLPG}	I_{PWRGD} = 1mA sink	-	0.05	0.10	V
THERMAL SHUT DOWN						
Shut down temperature	T_{TSDH}	Shut down temperature.	-	150(*1)	-	°C
	T_{TSDL}	Exited temperature from thermal shut down state.	-	125(*1)	-	°C

*1: No production tested, ensure by design.

VIN = 7.4V, VOUT, BST and EN connect to 5V power supply, PGND, LX = 0V. T_A = –30°C to +85°C, unless otherwise noted.

(MB39C504)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
5V LDO						
Output voltage	V_{LDO5}	No switchover. VOUT input voltage < 4.4V	4.75	5.00	5.25	V
Output current	I_{LDO5}	No switchover. V_{VIN} = 5.4V	25	-	-	mA
Output short current	I_{LDO5S}	No switchover. V_{LDO5} = 0V	-	80	125	mA
Switchover voltage	V_{SWOVR}	VOUT voltage rising.	4.35	4.50	4.60	V
	V_{HYS}	Hysteresis voltage.	0.08	0.10	0.12	V
Startup time	t_{SLDO5}	LDO5 voltage reaches to 4.2V. C_{LDO5}, C_{VCC} = 1.0µF	100	150	400	µs
DRIVER						
High side on resistance	R_{HOH}	At 100mA current sourcing	-	3(*1)	-	Ω
	R_{HOL}	At 100mA current sinking	-	1(*1)	-	Ω
Low side on resistance	R_{LOH}	At 100mA current sourcing	-	4(*1)	-	Ω
	R_{LOL}	At 100mA current sinking	-	0.75(*1)	-	Ω
High side source current	I_{SRCH}	V_{DRVH} = 2.5V	-	0.7(*1)	-	A
High side sink current	I_{SINKH}	V_{DRVH} = 2.5V	-	1.1(*1)	-	A
Low side source current	I_{SRCL}	V_{DRVL} = 2.5V	-	0.5(*1)	-	A
Low side sink current	I_{SINKL}	V_{DRVL} = 2.5V	-	1.7(*1)	-	A
Dead time	t_{DEAD}	From DRVH turn off to DRVL turn on. And reverse it.	10	20	-	ns
BOOST SWITCH						
Boost switch on resistance	R_{BST}	I_{BST} = 10mA	-	30	50	Ω
BST leak current	I_{LKBST}	V_{BST} = 30V	-	0.1	1.0	µA

*1: No production tested, ensure by design.

8. Protections and Power Good function

8.1 Description

(MB39C502/C503/C504)

This PWM Control IC has some protection functions UVLO, OVP, UVP, ILIM, and TSD for the assumed various power system failures. Details of these protections are written as follows.

Under Voltage Lockout (UVLO)

The under voltage lockout (UVLO) protects ICs from malfunction and protects the system from destruction/deterioration, according to the reasons mentioned below.

- Transitional state when the voltage inputs to VCC (5V power supply) terminal.
- Momentary decrease

To prevent such a malfunction, this function detects a voltage drop of the 5V power supply, and stops IC operations. When the voltage of 5V power supply exceeds the threshold voltage of the under voltage lockout protection circuit, the system is restored.

Over Voltage Protection (OVP)

This function stops the output voltage when the output voltage has increased, and protects devices connected to the output. When the over voltage is detected, the controller is fixed that the high side switching FET is turned off and the low side switching FET is turned on with 10μs propagation delay. When the enable is reentered, this fixed state is released and beginning soft start.

Under Voltage Protection (UVP)

This function stops the output voltage when the output voltage has lowered, and protects devices connected to the output. When the under voltage is detected, the controller is fixed that the high side switching FET is turned off and the low side switching FET is turned off with 100μs propagation delay. When the enable is reentered, this fixed state is released and beginning soft start.

Over Current Limitation (ILIM)

This function limits the output current when it has increased, and protects devices connected to the output. This function detects the inductor valley current with current sense resister RSENSE. The differential voltage of the CSP-CSN terminals is amplified to x20 by internal current sense amplifier, and compared to the limit voltage of 480mV fixed at internal preset condition. Until the amplified voltage fall the limit voltage, the high side switching FET is held in the off state. After the voltage has fallen below the limit voltage, the high side switching FET is placed into the ON state. This limits the lower bound of the inductor current and also restricts the over current. As a result, it becomes operation that the output voltage droops.

Thermal Shutdown (TSD)

This function prevents the PWM Control IC from a thermal destruction. If the junction temperature reaches +150°C, the high side and low side switching FET are turned off. Then the discharge operation is carried out to discharge the output capacitor (The discharge operation continues until the state of the thermal shutdown released). If the junction temperature drops to +125°C, the soft start is automatically reactivated.

Power Good (PWRGD)

Power good flag is hoisted at PWRGD terminal (Open Drain) to “Hi-Z” level with 50μs propagation delay, when the output voltage becomes larger than 92% of the output setting voltage. It is related by the OVP protection written above. When the output voltage becomes lower than power good threshold level, the PWRGD terminal is changed to “L” level with 10μs propagation delay.

State Table of Protection Function

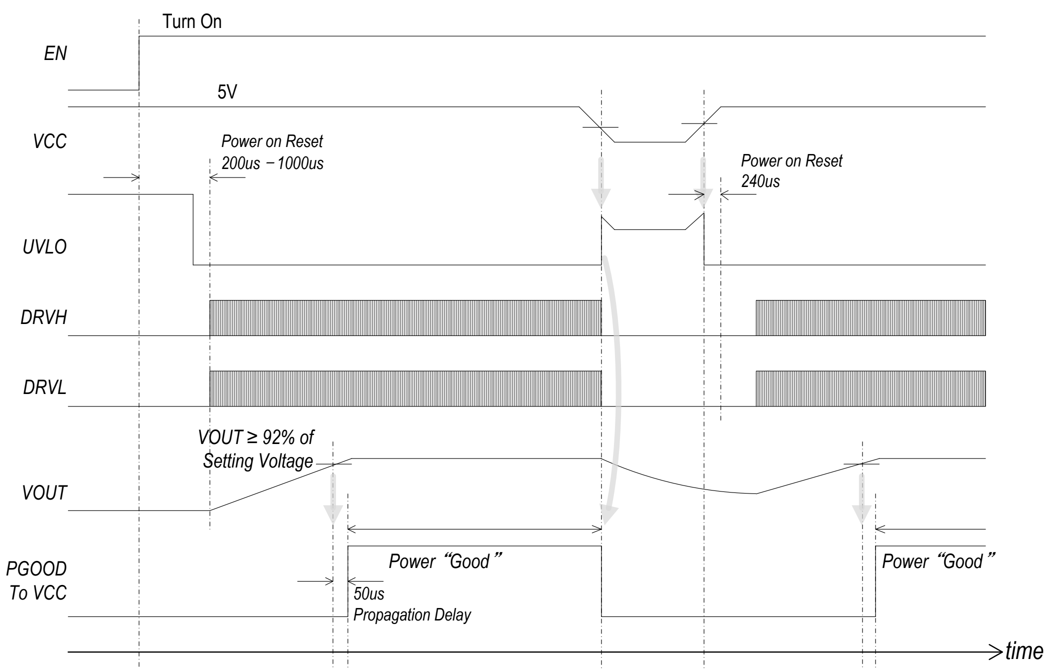
(MB39C502/C503/C504)

Protection Function	High Side FET	Low Side FET	Output state	Remarks
Under Voltage Lockout (UVLO)	OFF	OFF	OFF	After releasing UVLO, the System is an automatic restoration with soft start.
Over Voltage Protection (OVP)	OFF	ON	Latch OFF	Latch stall. It returns the System by enable reentry.
Under Voltage Protection (UVP)	OFF	OFF	Latch OFF	Latch stall. It returns the System by enable reentry.
Over Current Limitation (ILIM)	Switching	Switching	−	The output voltage is drooped with current limitation.
Thermal Shutdown (TSD)	OFF	OFF	OFF	After releasing TSD, the System is an automatic restoration with soft start.

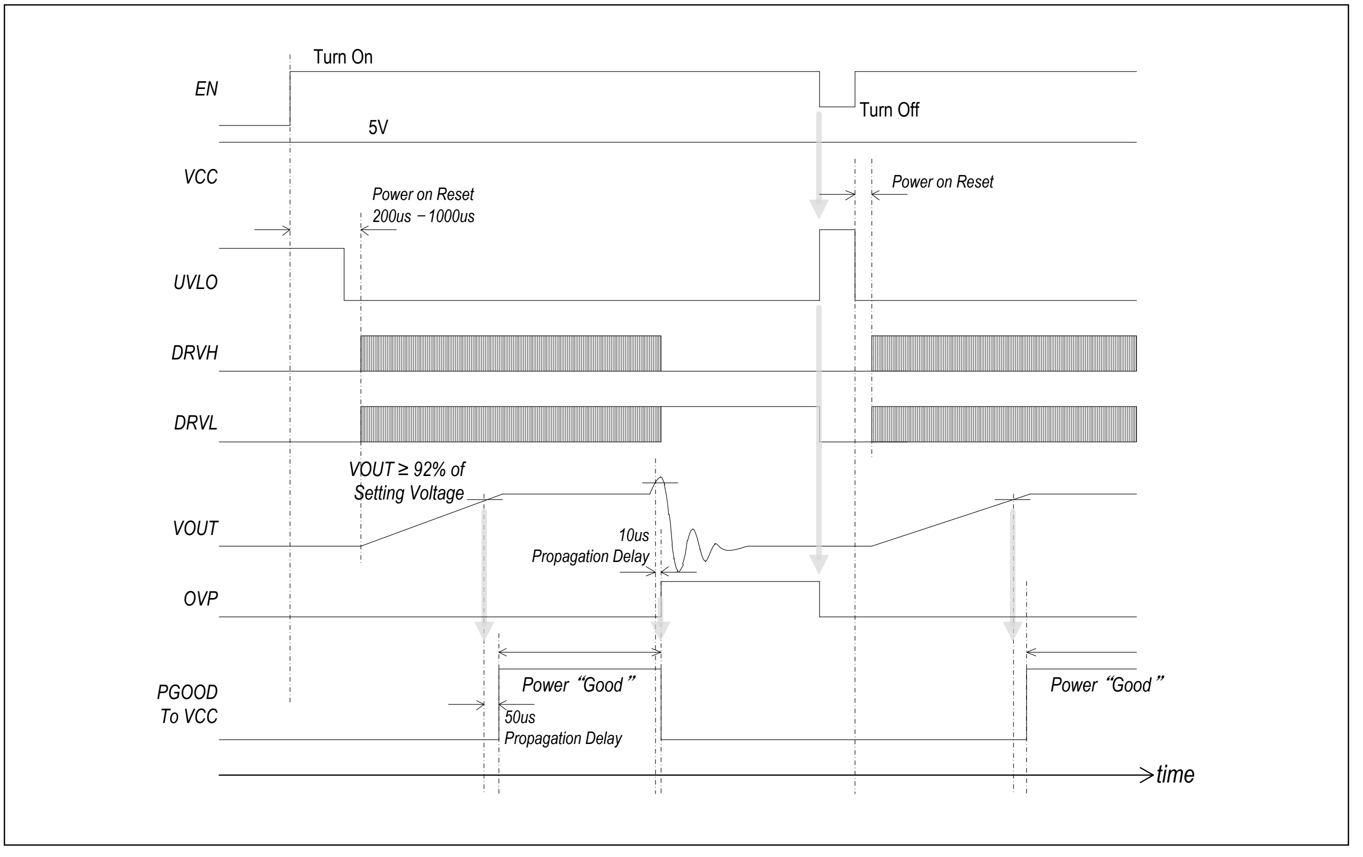
8.2 Timing Chart

(MB39C502/C503/C504)

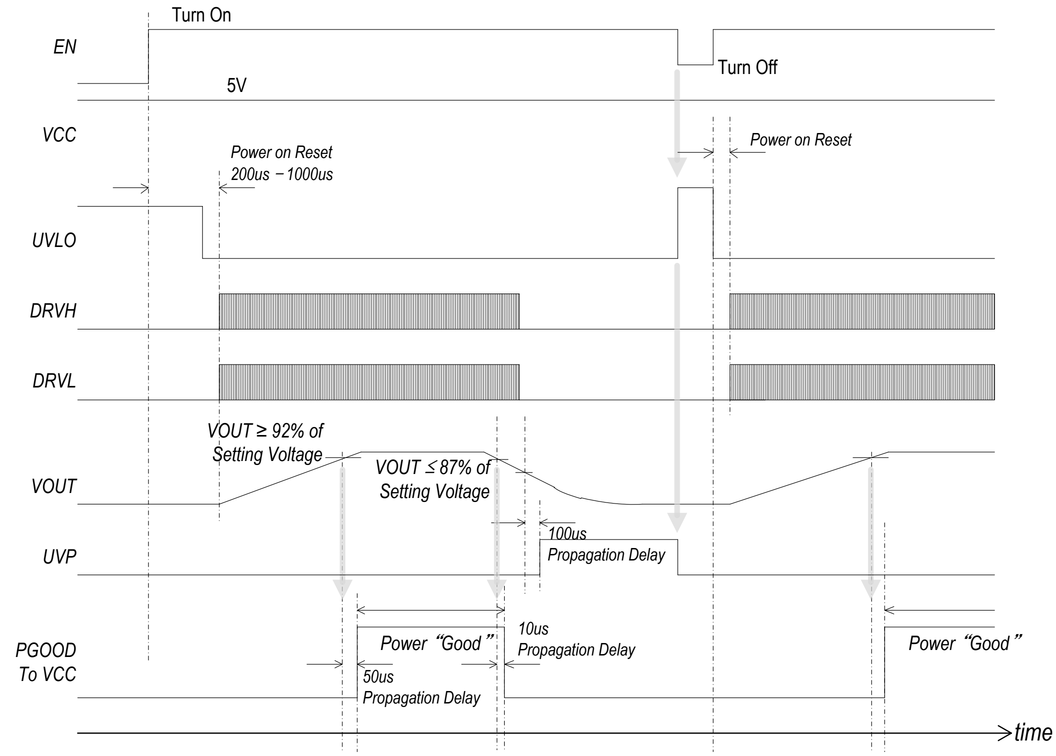
Under Voltage Lockout Protection (UVLO)



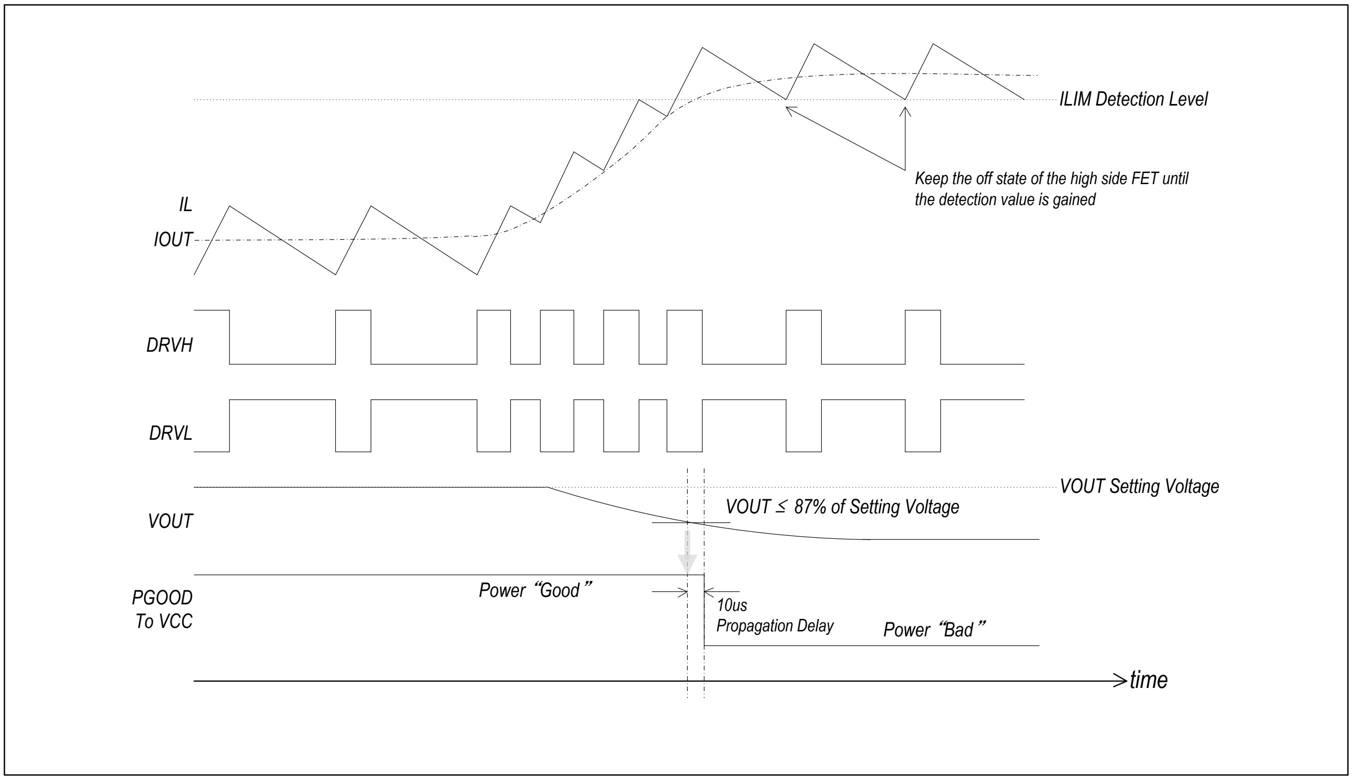
Over Voltage Protection (OVP)



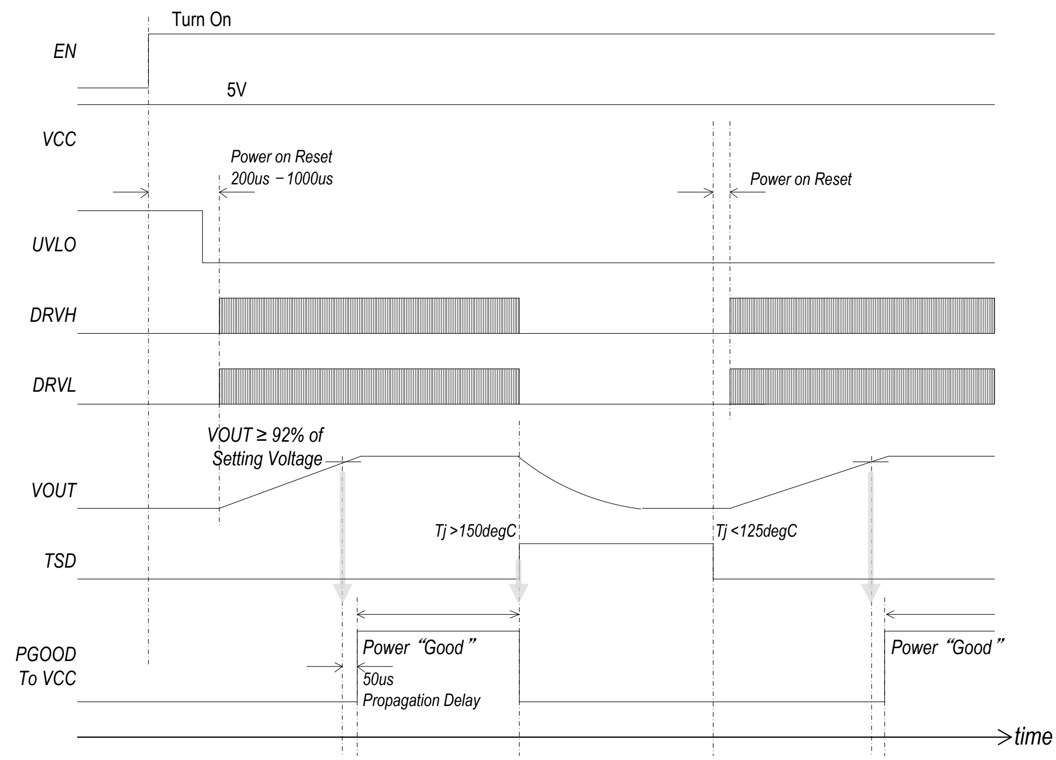
Under Voltage Protection (UVP)



Over Current Limitation (ILIM)



Thermal Shutdown (TSD)



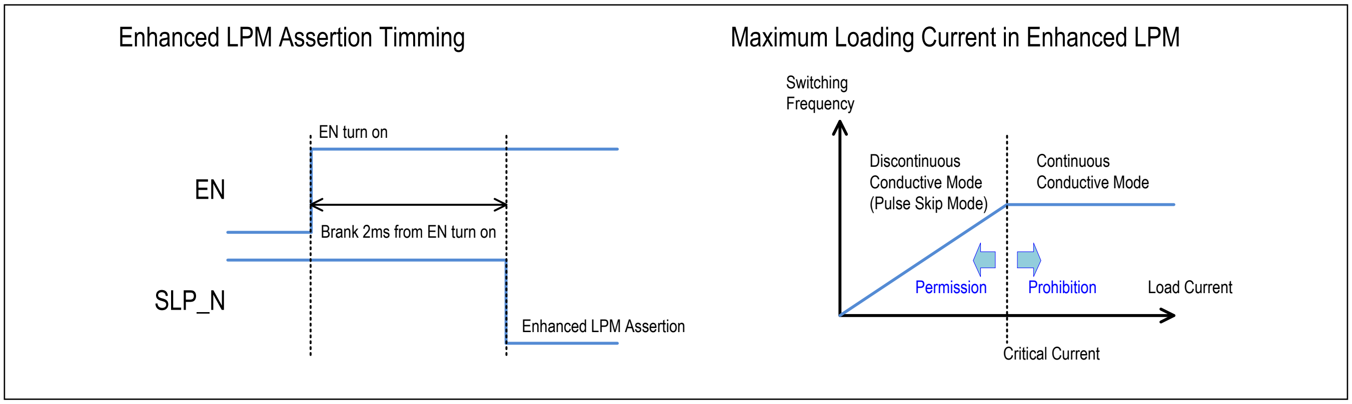
9. Enhanced LPM Description

(MB39C502/C503/C504)

This PWM controller has some features for high efficiency technology with "Ultra low quiescent current" and "Extended on time" on asserting SLP_L signal from the system.

Notes

- *Perform transferring to Enhanced LPM in the static switching state after 2ms from EN turn on. The soft starting on the enabling Enhanced LPM does not allow this controller.*
- *In Enhanced LPM, maximum loading current is less than critical current of "Discontinuous Conductive Mode", in other words "pulse skip mode".*



9.1 Ultra Low Quiescent Current

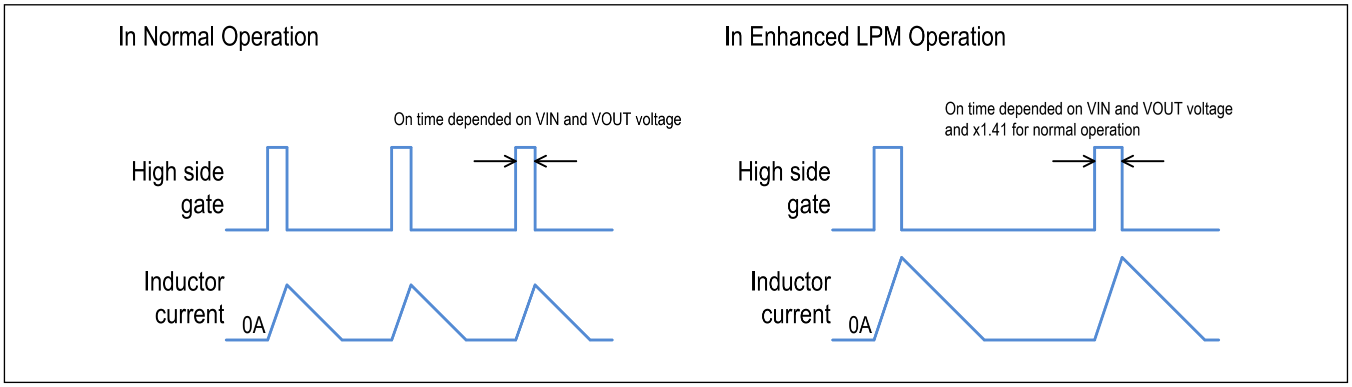
(MB39C502/C503/C504)

This controller has the feature of “Ultra low quiescent current” 30uA in enhanced LPM. So that the IC power loss is effectively improved efficiency in DCDC light load.

9.2 Extended On Time

(MB39C502/C503/C504)

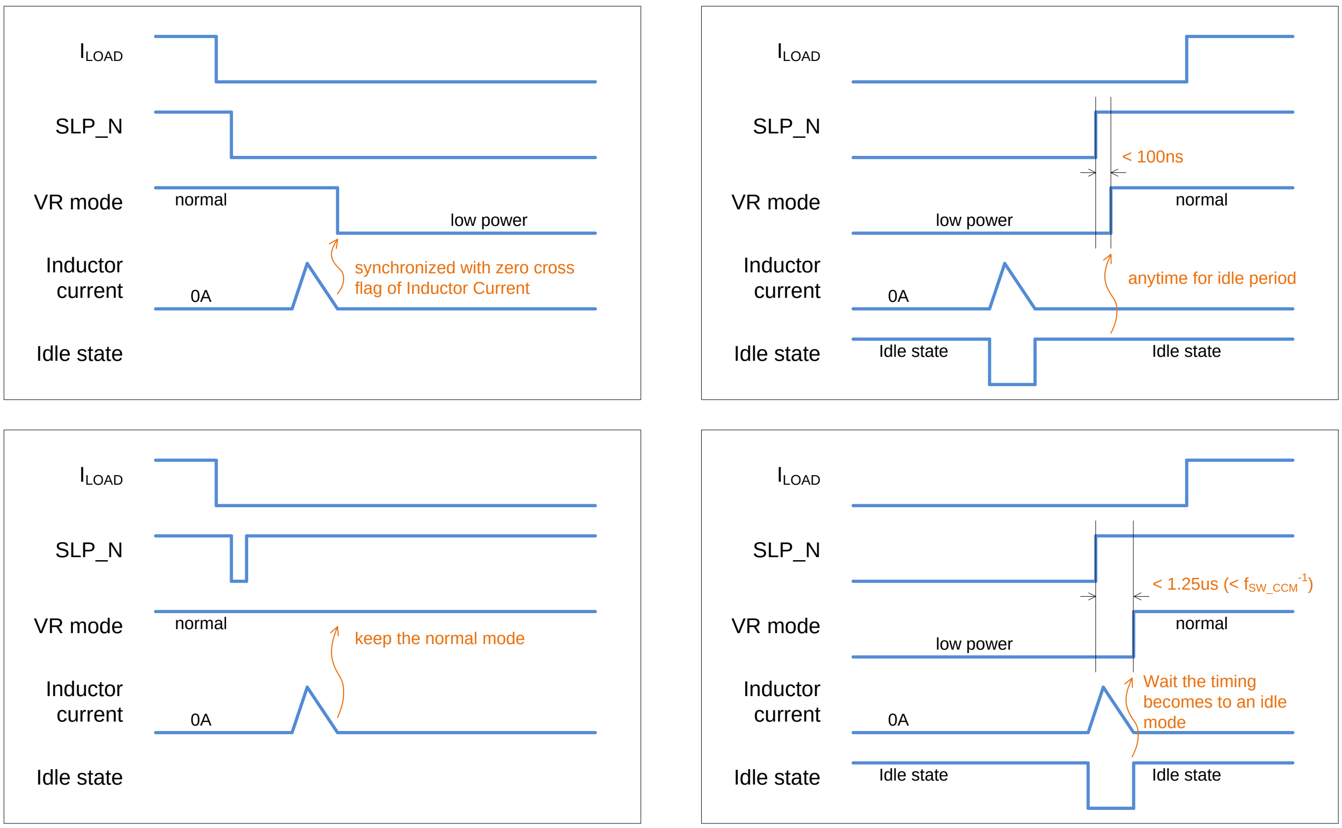
This controller uses feed forward on-time architecture with the information of input and output voltage. And this controller is transferred “Extended on-time” keeping the input and output voltage information in enhanced LPM. BY the on time is extended, gate drive loss is reduced by decreasing the switching frequency.



9.3 Timing Chart of Enhanced LPM

(MB39C502/C503/C504)

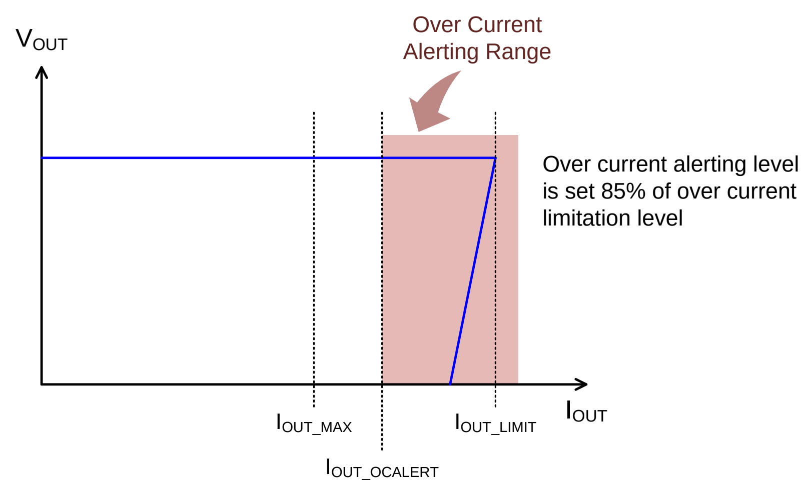
This controller is transferred to enhanced LPM synchronized the zero crossing of inductor current, and transferred to normal operation with 100ns propagation delay avoid the switching period.



10. Over Current Alerting Description

(MB39C502/C503)

This controller has “Over Current Alerting” function. In near over current limitation range, the ALERT_N with Nch open drain terminal is change to “L” level. Over current alerting level is set 85% for over current limitation level.



11. Application Note

11.1 Setting Operating Conditions

11.1.1 Setting Output Voltage

The output voltage can be set by adjusting the setting output voltage resister ratio. Setting output voltage is calculated by the following formula.

(MB39C502)

$$V_{OUT} = \frac{R1+R2}{R2} \times 0.7$$

(MB39C503/C504)

$$V_{OUT} = \frac{R1+R2}{R2} \times 1.0$$

V_{OUT} : output setting voltage (V)

R1, R2 : Feedback resistor (Ω)

The total resistor value (*R1*+*R2*) of the setting output resistor should be selected up to 300kΩ.

When the output voltage setting value is higher than 1.2V, select resistance that the current of 300μA or more flows into feedback resistor.

11.1.2 Setting Over Current Limitation and Over Current Alerting

The over current limitation value can be set by adjusting the current sense resistor. Calculate the resister value by the following formula.

(MB39C502)

$$R_{SENSE} = 0.024 \times \left(I_{LIMIT} - \frac{\Delta I_L}{2} - \frac{V_{OUT} \times 300 \times 10^{-9}}{L} \right)^{-1}$$

(MB39C503/C504)

$$R_{SENSE} = 0.025 \times \left(I_{LIMIT} - \frac{\Delta I_L}{2} - \frac{V_{OUT} \times 300 \times 10^{-9}}{L} \right)^{-1}$$

R_{SENSE} : Over current limitation value setting resister (Ω)

I_{LIMIT} : Over current limitation value (A)

ΔI_L : Inductor ripple current peak to peak value (A)

V_{OUT} : Output Voltage (V)

L : Inductance (H)

The over current limitation value needs to set a sufficient margin against the maximum load current.

The over current alerting value is set with over current limitation value as following formula.

(MB39C503/C504)

$$I_{ALERT} = \left(\frac{0.024}{R_{SENSE}} - \frac{V_{OUT} \times 300 \times 10^{-9}}{2 \times L} \right) \times 0.85 + \frac{\Delta I_L}{2}$$

R_{SENSE} : Over current limitation value setting resister (Ω)

I_{ALERT} : Over current Alerting value (A)

ΔI_L : Inductor ripple current peak to peak value (A)

V_{OUT} : Output Voltage (V)

L : Inductance (H)

11.2 Selection Parts

11.2.1 Selection of Smoothing Inductor

(MB39C502/C503/C504)

As a rough guide, inductance of an inductor should keep the peak to peak value of inductor ripple current below 50% of the maximum output current. The inductance fulfilling the above condition can be found by the following formula.

$$L \geq \frac{V_{IN} - V_{OUT}}{LOR \times I_{OUT\_MAX}} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

L : Inductance (H)

I_{OUT_MAX} : Maximum load current

LOR : Inductor ripple current peak to peak value – Maximum output current ratio (less than 0.5)

V_{IN} : Power supply voltage (V)

V_{OUT} : Output Voltage (V)

f_{SW} : Switching frequency (Hz)

The minimum output current (critical current) in the condition that inductor current does not flow in reverse can be found by the following formula.

$$I_{OC} = \frac{V_{OUT}}{2 \times L} \times \frac{V_{IN} - V_{OUT}}{V_{IN} \times f_{SW}}$$

I_{OC} : Critical current (A)

L : Inductance (H)

V_{IN} : Power supply voltage (V)

V_{OUT} : Output voltage (V)

f_{SW} : Switching frequency (Hz)

The maximum value of the current flowing through the inductor needs to be found in order to determine whether the current flowing through the inductor is within the rated value. The maximum current flowing through the inductor can be found by the following formula.

$$I_{L\_MAX} \geq I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

I_{L_MAX} : Maximum inductor current (A)

I_{OUT_MAX} : Maximum load current (A)

ΔI_L : Inductor ripple current peak to peak value (A)

11.2.2 Selection of Switching FET

(MB39C502/C503/C504)

In general, MOSFET should be used with a 30V absolute maximum rating. Obtain the maximum value of the current flowing through the switching FET in order to determine whether the current flowing through the switching FET is within the rated value. The maximum current flowing through the switching FET can be found by the following formula.

$$I_{D\_MAX} \geq I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

I_{D_MAX} : Maximum switching FET drain current (A)

I_{OUT_MAX} : Maximum load current (A)

ΔI_L : Inductor ripple current peak to peak value (A)

In addition, find the loss of the switching FET in order to determine whether the allowable loss of the switching is within the rated value. The allowable loss of the high side FET can be found by the following formula.

$$P_{FET\_HS} = P_{RON\_HS} + R_{SW\_HS}$$

P_{FET_HS} : Overall Loss of high side FET (W)

P_{RON_HS} : Conduction loss of high side FET (W)

P_{SW_HS} : Switching loss of high side FET (W)

The conduction loss of high side is followed as.

$$P_{RON\_HS} = I_{OUT\_MAX}{}^2 \times \frac{V_{OUT}}{V_{IN}} \times R_{ON\_HS}$$

P_{RON_HS} : Conduction loss of high side FET (W)

I_{OUT_MAX} : Maximum load current (A)

V_{IN} : Power supply voltage (V)

V_{OUT} : Output voltage (V)

R_{ON_HS} : On resistance of high side FET (Ω)

The switching loss of high side is followed as.

$$P_{SW\_HS} = 1.56 \times V_{IN} \times f_{SW} \times I_{OUT\_MAX} \times Q_{SW}$$

P_{SW_HS} : Switching loss of high side FET (W)

V_{IN} : Power supply voltage (V)

f_{SW} : Switching frequency (Hz)

I_{OUT_MAX} : Maximum load current (A)

Q_{SW} : Amount of high side FET gate switch electric charge (C)

MOSFET has a tendency where the gate drive loss increases because lower voltage product has the bigger amount of gate electric charge (Q_G). Normally, we recommend a 4V drive product, however, the idle period at light load (both the high side FET and the low side FET is off period) get longer and the gate drive voltage of the high side FET may decrease, in the automatic PFM/PWM transition. The voltage drops most at no load mode. At the time, confirm that the boost voltage (voltage between BST-LX pins) is a big enough value for the gate threshold value voltage of the high side FET.

If it is not enough, consider adding the boost diode, increasing the capacitor value of the capacitor or using a 2.5V (or 1.8V) drive product to the high side FET.

The allowable loss of the low side FET can be found by the following formula.

$$P_{FET\_LS} = P_{RON\_LS} = I_{OUT\_MAX}{}^{2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ON\_LS}$$

P_{FET_LS} : Overall loss of low side FET (W)

P_{RON_LS} : Conduction loss of low side FET (W)

I_{OUT_MAX} : Maximum output current (A)

V_{IN} : Switching power supply voltage (V)

V_{OUT} : Output voltage (V)

R_{ON_LS} : On resistance of low side FET (Ω)

In switching of low side FET, the transiting voltage between drain to source is generally small. The switching FET loss is omitted in this document as it is negligible.

11.2.3 Selection of Fly Back Diode

(MB39C502/C503/C504)

This device is improved by adding the fly back diode when the conversion efficiency improvement or the suppression of the low side FET fever is desired, although those are unnecessary to execute normally. The effect is achieved in the condition where the switching frequency is high or output voltage is lower. Select period for the electric current flow into fly back diode is limited to dead time period because the synchronous rectification system is adopted (as for the dead time, see “Electrical Characteristics”). Each rating for the fly back diode can be calculated by the following formula.

$$I_D \geq I_{OUT\_MAX} \times f_{SW} \times \left(t_{D1} + t_{D2}\right)$$

I_D : Forward current rating of SBD (A)

I_{OUT_MAX} : Maximum load current (A)

f_{SW} : Switching frequency (Hz)

t_{D1}, t_{D2} : Dead times (s)

$$I_{FSM} \geq I_{OUT\_MAX} + \frac{\Delta I_L}{2}$$

I_{FSM} : Rated value of fly back diode (V)

I_{OUT_MAX} : Maximum output current (A)

ΔI_L : Inductor ripple current peak to peak value (A)

$$V_{R\_FLY} > V_{IN}$$

V_{R_FLY} : DC reversing voltage of fly back diode (V)

V_{IN} : Switching power supply voltage (V)

11.2.4 Selection of Boost Diode

(MB39C502)

Select a schottky barrier diode (SBD) that has a small forward voltage drop. The current to drive the gate of High-side FET flows to the SBD of the boost circuit. The average current can be found by the following formula. Select a boost diode that keep the average current below the current rating.

$$I_D \geq Q_{G\_HS} \times f_{SW}$$

I_D : Forward current (A)

Q_{G_HS} : Total gate electric charge of high-side FET (C)

f_{SW} : Switching Frequency (Hz)

The rating of the boost diode can be found by the following formula.

$$V_{R\_BOOST} > V_{IN}$$

V_{R_BOOST} : Boost Diode DC reverse voltage (V)

V_{IN} : Switching power supply voltage (V)

11.2.5 Selection of Input Capacitor

(MB39C502/C503/C504)

Select the input capacitor whose ESR is as small as possible. The ceramic capacitor is an ideal. Use the tantalum capacitor and the polymer capacitor of low ESR when a mass capacitor is needed as the ceramic capacitor cannot support.

The ripple voltage is generated in the power supply voltage by the switching operation. Calculate the lower bound of input capacitor according to an allowable ripple voltage. Calculate the ripple voltage of the power supply from the following formula.

$$\Delta V_{IN} = \frac{I_{OUT\_MAX}}{C_{IN}} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}} + ESR \times \left(I_{OUT\_MAX} + \frac{\Delta I_L}{2} \right)$$

ΔV_{IN} : Power supply ripple voltage peak to peak value (V)

I_{OUT_MAX} : Maximum load current (A)

C_{IN} : Input capacitance (F)

V_{IN} : Power supply voltage (V)

V_{OUT} : Output voltage (V)

f_{SW} : Switching frequency (Hz)

ESR : Series resistance component of input capacitor (Ω)

ΔI_L : Ripple current peak to peak value of inductor (A)

Capacitor has frequency characteristics, the temperature characteristics, and the voltage characteristics, etc. The effective capacitance might become extremely small depending on the use conditions. Note the effective capacitance in the use conditions.

Calculate ratings of the input capacitor by following formula.

$$V_{CIN} > V_{IN}$$

V_{CIN} : Withstand voltage of the input capacitor (V)

V_{IN} : Power supply voltage (V)

$$Irms \geq I_{OUT\_MAX} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

$Irms$: Allowable ripple current of input capacitor (effective value) (A)

I_{OUT_MAX} : Maximum load current (A)

V_{IN} : Power supply voltage (V)

V_{OUT} : Output voltage (V)

11.2.6 Selection of Output Capacitor

Since a high ESR causes the output ripple voltage to increase, a low ESR capacitor is needs to be used in order to reduce the output ripple voltage. Generally, the ceramic capacitor is used as the output capacitor. With the switching ripple voltage taken consideration, the minimum capacitance required can be found by the following formula.

(MB39C502/C503/C504)

$$C_{OUT} \geq \frac{1}{2\pi \times f_{SW} \times \left(\Delta V_{OUT} / \Delta I_L - ESR\right)}$$

C_{OUT} : Output capacitance (F)

ESR : Series resistance element of output capacitor (Ω)

ΔV_{OUT} : Output ripple voltage (V)

ΔI_L : Inductor ripple current peak to peak value (A)

Also, it is necessary to unite a pole by the output capacitor and the output load with a zero by the internal compensation circuit, and to limit the crossover frequency. The minimum capacitance required can be found by the following formula.

(MB39C502)

$$C_{OUT} \geq 42.5 \times 10^{-6} \times \frac{I_{OUT\_MAX}}{V_{OUT}}$$

(MB39C503)

$$C_{OUT} \geq 49.0 \times 10^{-6} \times \frac{I_{OUT\_MAX}}{V_{OUT}}$$

(MB39C504)

$$C_{OUT} \geq 21.7 \times 10^{-6} \times I_{OUT\_MAX}$$

(MB39C502)

$$C_{OUT} \geq 0.59 \times 10^{-6} \times \frac{1}{R_{SENSE} \times V_{OUT}}$$

(MB39C503)

$$C_{OUT} \geq 0.67 \times 10^{-6} \times \frac{1}{R_{SENSE} \times V_{OUT}}$$

(MB39C504)

$$C_{OUT} \geq 0.27 \times 10^{-6} \times \frac{1}{R_{SENSE}}$$

I_{OUT_MAX} : Maximum output load current (A)

V_{OUT} : Output voltage (V)

R_{SENSE} : Over current limitation value setting resister (Ω)

Moreover, the output capacitance is also derived from the allowable amount of overshoot and under shoot. Adjust the capacitance so that the overshoot/undershoot voltage should not exceed the target voltage range.

11.2.7 Selection of Boost Capacitor

To drive the gate of high side FET, the boost capacitor must have enough stored charge. 0.47μF is assumed to be standard; however, it is necessary to adjust it when the high side FET Q_G is big. Consider the capacitance calculated by the following formula as the lowest value for the boost capacitance and select a thing anymore.

(MB39C502/C503/C504)

$$C_{BST} \geq 10 \times Q_{G\_HS}$$

C_{BST} : Boost capacitance (F)

Q_{G_HS} : Amount of high side FET gate charge (C)

Calculate ratings of the boost capacitor by the following formula.

(MB39C502/C503)

$$V_{CBST} > V_{VDD}$$

(MB39C504)

$$V_{CBST} > V_{LDO5}$$

V_{CBST} : Withstand voltage of the boost capacitor (V)

V_{VDD} : Input voltage of VDD terminal (V)

V_{LDO5} : Input voltage of LDO5 terminal (V)

11.2.8 Selection of VDD Capacitor

4.7μF is assumed to be a standard, and when Q_G of switching FET used large, it is necessary to adjust it. To suppress the ripple voltage by the switching FET gate drive, consider the capacitance calculated by the following formula as the lowest value for VDD Capacitor and select a thing any more.

Calculate ratings of the VDD terminal capacitor by the following formula.

(MB39C502/C503)

$$C_{VDD} \geq 50 \times Q_G$$

(MB39C504)

$$C_{LDO5} \geq 50 \times Q_G$$

C_{VDD} : VDD pin capacitance (F)

C_{LDO5} : LDO5 pin capacitance (F)

Q_G : Total amount of high and low side FETs gate charge (C)

Calculate ratings of the VDD terminal capacitor by the following formula.

(MB39C502/C503)

$$V_{CVDD} > V_{VDD}$$

(MB39C504)

$$V_{CLDO5} > V_{LDO5}$$

V_{CVDD} : Withstand voltage of the VDD terminal capacitor (V)

V_{VDD} : Input voltage of VDD terminal (V)

V_{CLDO5} : Withstand voltage of the LDO5 terminal capacitor (V)

V_{LDO5} : Input voltage of LDO5 terminal (V)

11.2.9 Selection of VCC Capacitor and Resistor

(MB39C502/C503)

Connect 1.0μF between VCC to AGND terminal. Connect 10Ω between VCC to VDD terminal.

(MB39C504)

Connect 1.0μF between VCC to AGND terminal. Connect 10Ω between VCC to LDO5 terminal.

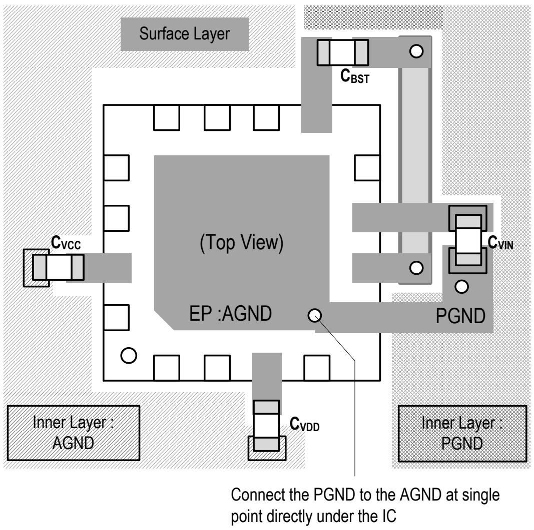
11.3 Layout

(MB39C502/C503)

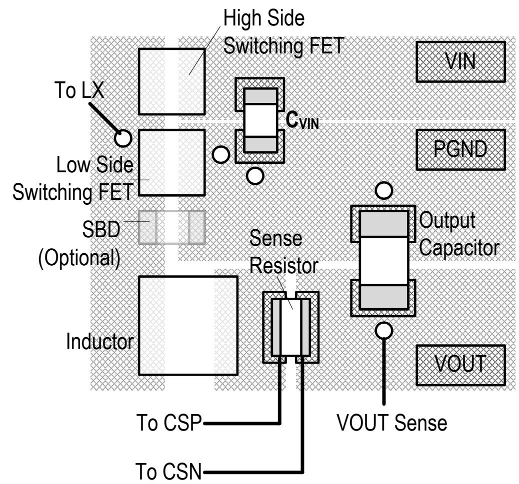
Consider the points listed below and do the layout design.

- Provide the ground plane as much as possible on the IC mounted face. Connect bypass capacitor connected with the VCC and VDD pins, and AGND pin of the switching system parts with switching system GND (PGND). Connect other GND connection pins with control system GND (AGND), and separate each GND, and try not to pass the heavy current path through the control system GND (AGND) as much as possible. In that case, connect control system GND (AGND) and switching system GND (PGND) at the single point of GND (PGND) directly below IC. Switching system parts are Input capacitor (C_{IN}), Switching FET, fly back diode (SBD), inductor (L) and Output capacitor (C_{OUT}).
- Connect the switching system parts as much as possible on the surface. Avoid the connection through the through hole as much as possible.
- As for AGND pins of the switching system parts, provide the through hole at the proximal place, and connect it with GND of internal layer.
- Pay the most attention to the loop composed of input capacitor (C_{IN}), switching FET, and fly back diode (SBD). Consider parts are disposed mutually to be near for making the current loop as small as possible.
- Place the bootstrap capacitor (C_{BST}) proximal to BST and LX pins of IC as much as possible.
- Connect the line to the LX pin proximal to the drain pin of low-side FET. Also large electric current flows momentary in this net. Wire the line of width of about 0.8 mm as standard, and as short as possible.
- Large electric current flows momentary in the net of DRVH and DRVL pins connected with the gate of switching FET. Wire the line width of about 0.8 mm to be a standard, as short as possible. Take special care about the line of the DRVL pin, and wire the line as short as possible.
- By-pass capacitor (C_{VCC}, C_{VDD}) connected with VCC, and VDD should be placed close to the pin as much as possible. Also connect the GND pin of the bypass capacitor with GND of internal layer in the proximal through-hole.
- Pull the feedback line to be connected to the FB pin of the IC separately from near the output capacitor pin, whenever possible. Consider the line connected with FB pins to keep away from a switching system parts as much as possible because it is sensitive to the noise.
  Also, place the output voltage setting resistor connected to this line near IC, and try to shorten the line to the FB pin.
  In addition, for the internal layer right under the component mounting place, provide the control system GND (AGND) of few ripple and few spike noises, or provide the ground plane of the power supply as much as possible.
  Consider that the discharge current momentary flows into the CSN pin (about 10mA at 1.0V output voltage) when the DC/DC operation stops, and then sustain the width for the feedback line.
  There is leaked magnetic flux around the inductor or backside of place equipped with inductor. Line and parts sensitive to noise should be considered to be placed away from the inductor (or backside of place equipped with inductor).

GND routing example



Layout example of switching components

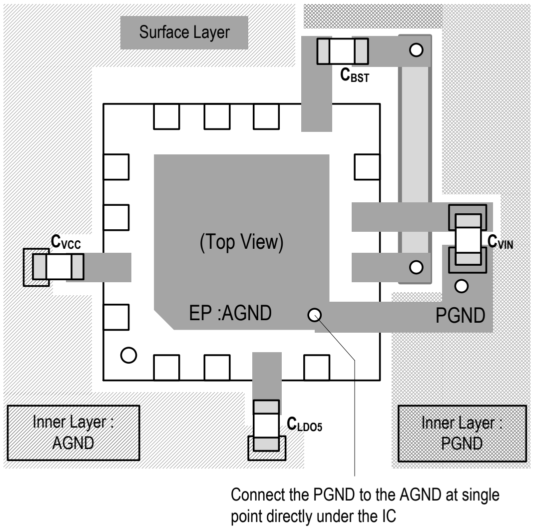


(MB39C504)

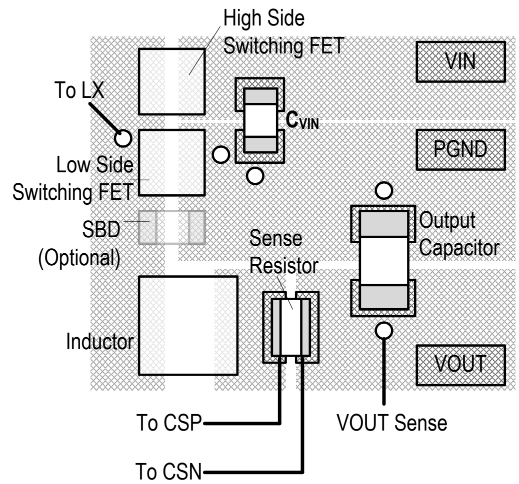
Consider the points listed below and do the layout design.

- Provide the ground plane as much as possible on the IC mounted face. Connect bypass capacitor connected with the VCC and LDO5 pins, and AGND pin of the switching system parts with switching system GND (PGND). Connect other GND connection pins with control system GND (AGND), and separate each GND, and try not to pass the heavy current path through the control system GND (AGND) as much as possible. In that case, connect control system GND (AGND) and switching system GND (PGND) at the single point of GND (PGND) directly below IC. Switching system parts are Input capacitor (C_{IN}), Switching FET, fly back diode (SBD), inductor (L) and Output capacitor (C_{OUT}).
- Connect the switching system parts as much as possible on the surface. Avoid the connection through the through hole as much as possible.
- As for AGND pins of the switching system parts, provide the through hole at the proximal place, and connect it with GND of internal layer.
- Pay the most attention to the loop composed of input capacitor (C_{IN}), switching FET, and fly back diode (SBD). Consider parts are disposed mutually to be near for making the current loop as small as possible.
- Place the bootstrap capacitor (C_{BST}) proximal to BST and LX pins of IC as much as possible.
- Connect the line to the LX pin proximal to the drain pin of low-side FET. Also large electric current flows momentary in this net. Wire the line of width of about 0.8 mm as standard, and as short as possible.
- Large electric current flows momentary in the net of DRVH and DRVL pins connected with the gate of switching FET. Wire the line width of about 0.8 mm to be a standard, as short as possible. Take special care about the line of the DRVL pin, and wire the line as short as possible.
- By-pass capacitor (C_{VCC}, C_{LDO5}) connected with VCC, and LDO5 should be placed close to the pin as much as possible. Also connect the GND pin of the bypass capacitor with GND of internal layer in the proximal through-hole.
- Pull the feedback line to be connected to the FB pin of the IC separately from near the output capacitor pin, whenever possible. Consider the line connected with FB pins to keep away from a switching system parts as much as possible because it is sensitive to the noise.
  Also, place the output voltage setting resistor connected to this line near IC, and try to shorten the line to the FB pin. In addition, for the internal layer right under the component mounting place, provide the control system GND (AGND) of few ripple and few spike noises, or provide the ground plane of the power supply as much as possible. Consider that the discharge current momentary flows into the CSN pin (about 10mA at 1.0V output voltage) when the DC/DC operation stops, and then sustain the width for the feedback line.
  There is leaked magnetic flux around the inductor or backside of place equipped with inductor. Line and parts sensitive to noise should be considered to be placed away from the inductor (or backside of place equipped with inductor).

GND routing example



Layout example of switching components

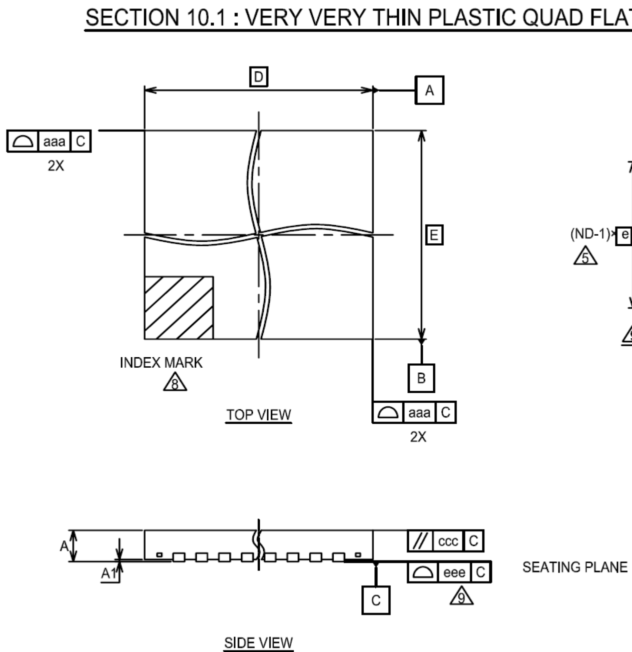


12. Ordering Information

Table 12-1 Ordering information

Part number	Package	Remarks
MB39C502WQN-G-AMERE1	16-pin plastic QFN (WN2016)	
MB39C503WQN-G-AMERE1		
MB39C504WQN-G-AMERE1		

13. Package Dimensions



SYMBOL	MILLIMETER			NOTE
	MIN.	NOM.	MAX.	
A	—	—	0.75	PROFILE
A_1	0.00	—	0.05	TERMINAL HEIGHT
$\boxed{D}$	3.00 BSC.			BODY SIZE
$\boxed{E}$	3.00 BSC.			BODY SIZE
b	0.20	0.25	0.30	TERMINAL WIDTH
$\boxed{D_2}$	1.90 BSC.			EXPOSED PAD SIZE
$\boxed{E_2}$	1.90 BSC.			EXPOSED PAD SIZE
$\boxed{e}$	0.50 BSC.			TERMINAL PITCH
n	16			TERMINAL COUNT
L	0.18	0.25	0.32	TERMINAL LENGTH
C	C0.30			EXPOSED PAD CHAMFER
aaa	0.07			
bbb	0.10			
ccc	0.10			
ddd	0.05			
eee	0.05			
fff	0.10			

1. DIMENSIONING AND TOLERANCINC CONFORMS TO ASME Y14.5-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL. THE DIMENSION "b"SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND REFER TO THE NUMBER OF TERMINALS ON D OR E SIDE.
6. MAX. PACKAGE WARPAGE IS 0.05mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LOCATED WITHIN INDICATED ZONE.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

14. Major Changes

Spansion Publication Number: MB39C502_DS405-00020-1v0-E

Page	Section	Change Results
Revision 1.0		
-	-	Initial release

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB39C502/503/504 High Efficiency Step Down DC/DC Controller Datasheet
Document Number: 002-08449

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	–	TAOA	09/09/2014	Migrated to Cypress and assigned document number 002-08449. No change to document contents or format.
*A	5127378	TAOA	02/12/2016	Updated to Cypress template

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc
Memory	cypress.com/go/memory
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless
Spansion Products	cypress.com/spansion products

PSoC® Solutions

psoc.cypress.com/solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Community | Forums | Blogs | Video | Training

Technical Support

cypress.com/go/support

ООО «ЛайфЭлектроникс» "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru