# 74LVTN16244B

3.3 V 16-bit buffer/driver; 3-state

Rev. 6 — 4 October 2018

**Product data sheet** 

### 1. General description

The 74LVTN16244B is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V.

This device is a 16-bit buffer and line driver featuring non-inverting 3-state bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

#### 2. Features and benefits

- · 16-bit bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- · TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Power-up 3-state
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- · Latch-up protection
  - JESD78B Class II exceeds 500 mA
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

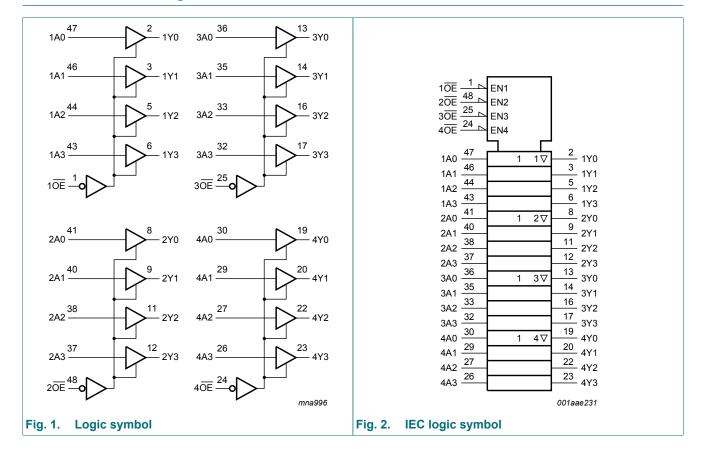
### 3. Ordering information

#### **Table 1. Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74LVTN16244BDGG	-40 °C to +85 °C		plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

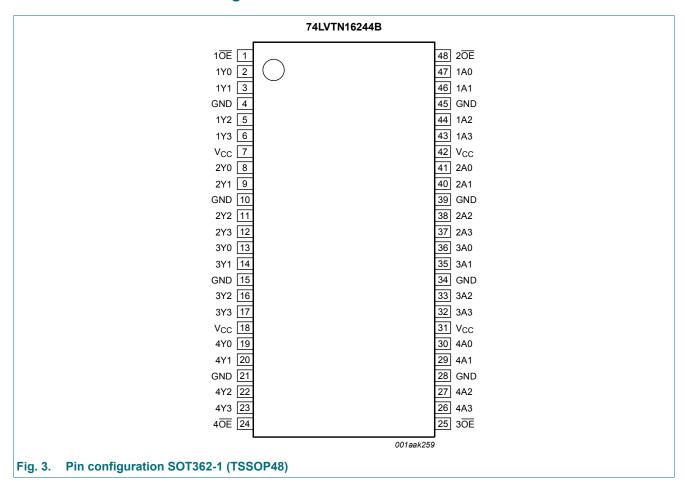


# 4. Functional diagram



# 5. Pinning information

### 5.1. Pinning



### 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1 <del>OE</del> , 2 <del>OE</del> ,3 <del>OE</del> , 4 <del>OE</del>	1, 48, 25, 24	output enable input (active LOW)
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	data output
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	data output
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	data output
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	data output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	data input
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	data input
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	data input
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	data input

# 6. Functional description

#### Table 3. Function table

 $H = HIGH \text{ voltage level}; L = LOW \text{ voltage level}; X = don't care; Z = high-impedance OFF-state.}$ 

	Input	Output
nŌE	nAn	nYn
L	L	L
L	Н	Н
Н	X	Z

# 7. Limiting values

#### **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
VI	input voltage	[1]	-0.5	+7.0	V
Vo	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
Io	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature	[2]	-	150	°C
P <sub>tot</sub>	total power dissipation	$T_{amb} = -40  ^{\circ}\text{C to } +85  ^{\circ}\text{C};$ [3]	-	500	mW

<sup>[1]</sup> The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

# 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		2.7	-	3.6	V
VI	input voltage		0	-	5.5	V
V <sub>IH</sub>	HIGH-level input voltage		2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage		-	-	0.8	V
I <sub>OH</sub>	HIGH-level output current		-32	-	-	mA
I <sub>OL</sub>	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f <sub>i</sub> ≥ 1 kHz	-	-	64	mA
T <sub>amb</sub>	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

<sup>[3]</sup> Above 60 °C the value of Ptot derates linearly with 5.5 mW/K.

### 9. Static characteristics

#### **Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb}$  = -40 °C to +85 °C .

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V <sub>IK</sub>	input clamping voltage	V <sub>CC</sub> = 2.7 V; I <sub>IK</sub> = -18 mA	-1.2	-0.85	-	V
V <sub>OH</sub>	HIGH-level output	I <sub>OH</sub> = -100 μA; V <sub>CC</sub> = 2.7 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
	voltage	I <sub>OH</sub> = -8 mA; V <sub>CC</sub> = 2.7 V	2.4	2.5	-	V
		I <sub>OH</sub> = -32 mA; V <sub>CC</sub> = 3.0 V	2.0	2.3	-	V
$V_{OL}$	LOW-level output	V <sub>CC</sub> = 2.7 V				
	voltage	I <sub>OL</sub> = 100 μA	-	0.07	0.2	V
		I <sub>OL</sub> = 24 mA	-	0.3	0.5	V
		V <sub>CC</sub> = 3.0 V				
		I <sub>OL</sub> = 16 mA	-	0.25	0.4	V
		I <sub>OL</sub> = 32 mA	-	0.3	0.5	V
		I <sub>OL</sub> = 64 mA	-	0.4	0.55	V
I <sub>I</sub>	input leakage current	all input pins; $V_{CC} = 0 \text{ V or } 3.6 \text{ V}$ ; $V_I = 5.5 \text{ V}$	-	0.1	10	μA
		control pins; V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	0.1	±1.0	μA
		data pins; unused pins at V <sub>CC</sub> or GND				
		V <sub>I</sub> = V <sub>CC</sub> ; V <sub>CC</sub> = 3.6 V	-	0.1	1	μA
		V <sub>I</sub> = 0 V; V <sub>CC</sub> = 3.6 V	-5	-0.1	-	μA
I <sub>OFF</sub>	power-off leakage current	$V_{CC} = 0 \text{ V}; V_{I} \text{ or } V_{O} = 0 \text{ V to } 4.5 \text{ V}$	-	0.1	±100	μΑ
I <sub>LO</sub>	output leakage current	output in HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5 \text{ V}$ ; $V_{CC} = 3.0 \text{ V}$	-	50	125	μΑ
I <sub>O(pu/pd)</sub>	power-up/ power-down output current	$V_{CC} \le 1.2 \text{ V}; V_O = 0.5 \text{ V to } V_{CC};$ [2] $V_I = \text{GND or } V_{CC}; \text{ nOE} = \text{don't care}$	-	1	±100	μА
l <sub>OZ</sub>	OFF-state output	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
ı	current	output HIGH: V <sub>O</sub> = 3.0 V	-	0.5	5	μA
l		output LOW: V <sub>O</sub> = 0.5 V	-5	+0.5	-	μA
I <sub>CC</sub>	supply current	$V_{CC} = 3.6 \text{ V}; V_{I} = \text{GND or } V_{CC}; I_{O} = 0 \text{ A}$				
		output HIGH	-	0.07	0.12	mA
		output LOW	-	4.0	6.0	mA
		outputs disabled [3]	-	0.07	0.12	mA
ΔI <sub>CC</sub>	additional supply current	per input pin; $V_{CC}$ = 3.0 V to 3.6 V; [4] one input at $V_{CC}$ - 0.6 V, other inputs at $V_{CC}$ or GND	-	0.1	0.2	mA
Cı	input capacitance	V <sub>I</sub> = 0 V or 3.0 V	-	3	-	pF
Co	output capacitance	outputs disabled; V <sub>O</sub> = 0 V or 3.0 V	-	9	-	pF

Typical values are measured at  $V_{CC}$  = 3.3 V and at  $T_{amb}$  = 25 °C. This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{CC}$  = 1.2 V to  $V_{CC}$  = 3.3 V ± 0.3 V a transition time of 100  $\mu s$  is permitted. This parameter is valid for  $T_{amb}$  = 25 °C only.  $I_{CC}$  is measured with outputs pulled to  $V_{CC}$  or GND.

This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND.

# 10. Dynamic characteristics

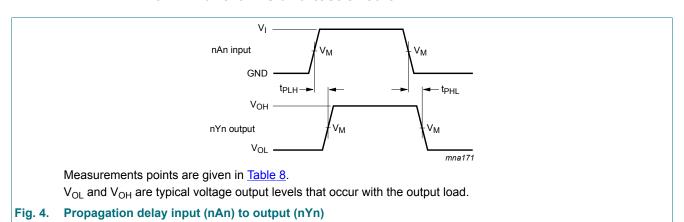
**Table 7. Dynamic characteristics** 

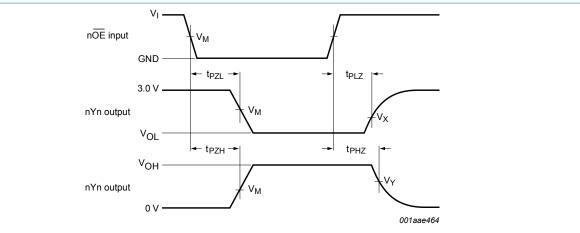
Voltages are referenced to GND (ground = 0 V); T<sub>amb</sub> = -40 °C to +85 °C; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t <sub>PLH</sub>	LOW to HIGH	nAn to nYn; see Fig. 4				
	propagation delay	V <sub>CC</sub> = 2.7 V	-	-	4.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	1.8	3.2	ns
t <sub>PHL</sub>	HIGH to LOW	nAn to nYn; see Fig. 4				
	propagation delay	V <sub>CC</sub> = 2.7 V	-	-	4.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	1.7	3.2	ns
t <sub>PZH</sub>	OFF-state to HIGH	nOE to nYn; see Fig. 5				
	propagation delay	V <sub>CC</sub> = 2.7 V	-	-	5.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.3	4.0	ns
t <sub>PZL</sub>	OFF-state to LOW	nOE to nYn; see Fig. 5				
	propagation delay	V <sub>CC</sub> = 2.7 V	-	-	5.3	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.1	4.0	ns
t <sub>PHZ</sub>	HIGH to OFF-state	nOE to nYn; see Fig. 5				
	propagation delay	V <sub>CC</sub> = 2.7 V	-	-	5.0	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.2	4.5	ns
t <sub>PLZ</sub>	LOW to OFF-state	nOE to nYn; see Fig. 5				
	propagation delay	V <sub>CC</sub> = 2.7 V	-	-	4.4	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	2.9	4.0	ns

<sup>[1]</sup> Typical values are measured at  $V_{CC}$  = 3.3 V and  $T_{amb}$  = 25 °C.

#### 10.1. Waveforms and test circuit





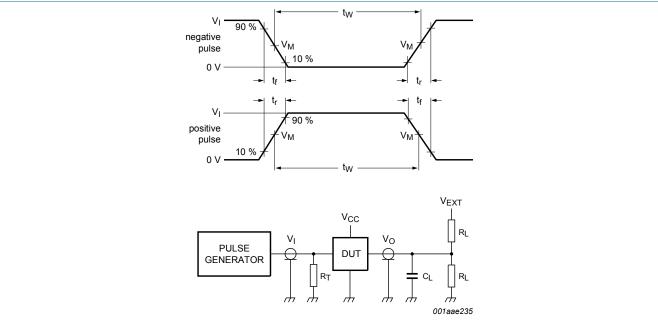
Measurements points are given in Table 8.

 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical voltage output levels that occur with the output load.

Fig. 5. 3-state output enable and disable times

**Table 8. Measurement points** 

Input	Output		
V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R<sub>L</sub> = Load resistance.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_T$  = Termination resistance should be equal to output impedance  $Z_0$  of the pulse generator.

V<sub>EXT</sub> = External voltage for measuring switching times.

#### Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Input			Load		V <sub>EXT</sub>			
VI	f <sub>i</sub>	t <sub>W</sub>	t <sub>r</sub> , t <sub>f</sub>	CL	$R_L$	t <sub>PHZ</sub> , t <sub>PZH</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

# 11. Package outline

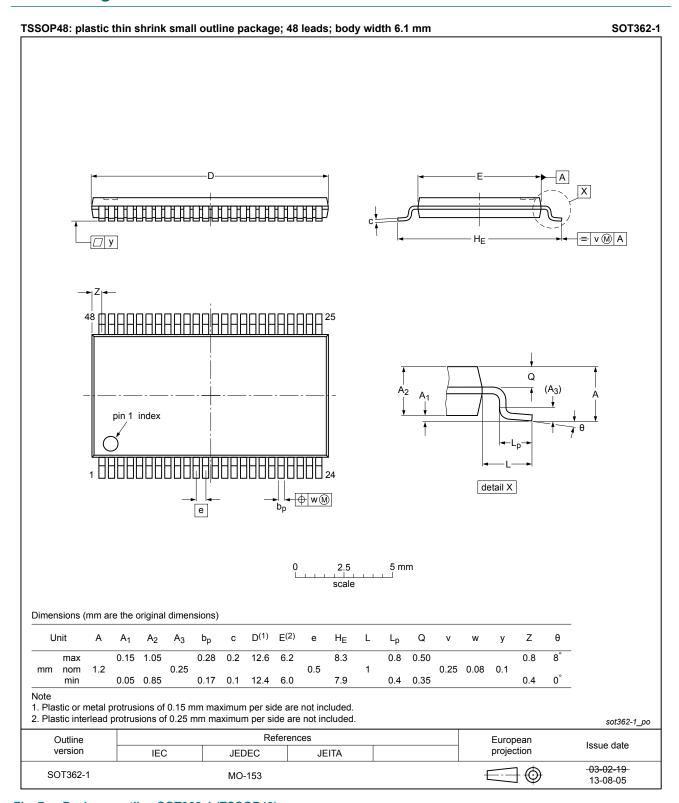


Fig. 7. Package outline SOT362-1 (TSSOP48)

# 12. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 13. Revision history

#### **Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74LVTN16244B v.6	20181004	Product data sheet	-	74LVTN16244B v.5		
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74LVTN16244BBX (SOT1134-2) removed.</li> <li>Package outline drawing SOT362-1 updated</li> </ul>					
74LVTN16244B v.5	20120402	Product data sheet	-	74LVTN16244B v.4		
Modifications:	For type num	nber 74LVTN16244BBX the	sot code has cha	anged to SOT1134-2.		
74LVTN16244B v.4	20111122	Product data sheet	-	74LVTN16244B v.3		
Modifications:	Legal pages	updated.				
74LVTN16244B v.3	20110614	Product data sheet	-	74LVTN16244B v.2		
74LVTN16244B v.2	20100323	Product data sheet	-	74LVTN16244B v.1		
74LVTN16244B v.1	20090713	Product data sheet	-	-		

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Document status [1][2]	Product status [3]	Definition
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