# STM32H747xI/G

## Dual 32-bit Arm® Cortex®-M7 up to 480MHz and -M4 MCUs, up to 2MB Flash, 1MB RAM, 46 com. and analog interfaces, SMPS, DSI

**Datasheet - production data**

## Features

### Dual core

- 32-bit Arm® Cortex®-M7 core with double-precision FPU and L1 cache: 16 Kbytes of data and 16 Kbytes of instruction cache; frequency up to 480 MHz, MPU, 1027 DMIPS/ 2.14 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- 32-bit Arm® 32-bit Cortex®-M4 core with FPU, Adaptive real-time accelerator (ART Accelerator™) for internal Flash memory and external memories, frequency up to 240 MHz, MPU, 300 DMIPS/1.25 DMIPS /MHz (Dhrystone 2.1), and DSP instructions

### Memories

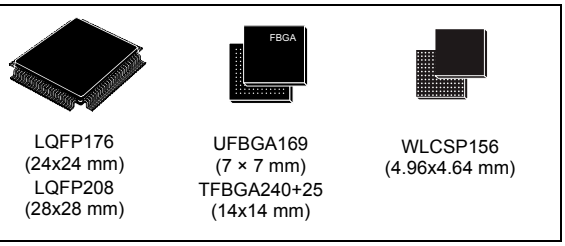
- Up to 2 Mbytes of Flash memory with read-while-write support
- 1 Mbyte of RAM: 192 Kbytes of TCM RAM (inc. 64 Kbytes of ITCM RAM + 128 Kbytes of DTCM RAM for time critical routines), 864 Kbytes of user SRAM, and 4 Kbytes of SRAM in Backup domain
- Dual mode Quad-SPI memory interface running up to 133 MHz
- Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, NOR/NAND Flash memory clocked up to 125 MHz in Synchronous mode
- CRC calculation unit

### Security

- ROP, PC-ROP, active tamper

### General-purpose input/outputs

- Up to 168 I/O ports with interrupt capability




LQFP176 (24x24 mm) LQFP208 (28x28 mm) | UFBGA169 (7 × 7 mm) TFBGA240+25 (14x14 mm) | WLCSP156 (4.96x4.64 mm)

### Reset and power management

- 3 separate power domains which can be independently clock-gated or switched off:
  - D1: high-performance capabilities
  - D2: communication peripherals and timers
  - D3: reset/clock control/power management
- 1.62 to 3.6 V application supply and I/Os
- POR, PDR, PVD and BOR
- Dedicated USB power embedding a 3.3 V internal regulator to supply the internal PHYs
- Embedded regulator (LDO) to supply the digital circuitry
- High power-efficiency SMPS step-down converter regulator to directly supply $V_{CORE}$ and/or external circuitry
- Voltage scaling in Run and Stop mode (6 configurable ranges)
- Backup regulator (~0.9 V)
- Voltage reference for analog peripheral/$V_{REF+}$
- 1.2 to 3.6 V $V_{BAT}$ supply
- Low-power modes: Sleep, Stop, Standby and $V_{BAT}$ supporting battery charging

### Low-power consumption

- $V_{BAT}$ battery operating mode with charging capability
- CPU and domain power state monitoring pins
- 2.95 µA in Standby mode (Backup SRAM OFF, RTC/LSE ON)



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### Clock management

- Internal oscillators: 64 MHz HSI, 48 MHz HSI48, 4 MHz CSI, 32 kHz LSI
- External oscillators: 4-48 MHz HSE, 32.768 kHz LSE
- 3× PLLs (1 for the system clock, 2 for kernel clocks) with Fractional mode

### Interconnect matrix

- 3 bus matrices (1 AXI and 2 AHB)
- Bridges (5× AHB2-APB, 2× AXI2-AHB)

### 4 DMA controllers to unload the CPU

- 1× high-speed master direct memory access controller (MDMA) with linked list support
- 2× dual-port DMAs with FIFO
- 1× basic DMA with request router capabilities

### Up to 35 communication peripherals

- 4× I2Cs FM+ interfaces (SMBus/PMBus)
- 4× USARTs/4x UARTs (ISO7816 interface, LIN, IrDA, up to 12.5 Mbit/s) and 1x LPUART
- 6× SPIs, 3 with muxed duplex I2S audio class accuracy via internal audio PLL or external clock, 1x I2S in LP domain (up to 150 MHz)
- 4x SAIs (serial audio interface)
- SPDIFRX interface
- SWPMI single-wire protocol master I/F
- MDIO Slave interface
- 2× SD/SDIO/MMC interfaces (up to 125 MHz)
- 2× CAN controllers: 2 with CAN FD, 1 with time-triggered CAN (TT-CAN)
- 2× USB OTG interfaces (1FS, 1HS/FS) crystal-less solution with LPM and BCD
- Ethernet MAC interface with DMA controller
- HDMI-CEC
- 8- to 14-bit camera interface (up to 80 MHz)

### 11 analog peripherals

- 3× ADCs with 16-bit max. resolution (up to 36 channels, up to 3.6 MSPS)
- 1× temperature sensor
- 2× 12-bit D/A converters (1 MHz)
- 2× ultra-low-power comparators
- 2× operational amplifiers (7.3 MHz bandwidth)
- 1× digital filters for sigma delta modulator (DFSDM) with 8 channels/4 filters

### Graphics

- LCD-TFT controller up to XGA resolution
- MIPI DSI host including an MIPI D-PHY to interface with low-pin count large displays
- Chrom-ART graphical hardware Accelerator™ (DMA2D) to reduce CPU load
- Hardware JPEG Codec

### Up to 22 timers and watchdogs

- 1× high-resolution timer (2.1 ns max resolution)
- 2× 32-bit timers with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input (up to 240 MHz)
- 2× 16-bit advanced motor control timers (up to 240 MHz)
- 10× 16-bit general-purpose timers (up to 240 MHz)
- 5× 16-bit low-power timers (up to 240 MHz)
- 4× watchdogs (independent and window)
- 2× SysTick timers
- RTC with sub-second accuracy and hardware calendar

### Debug mode

- SWD & JTAG interfaces
- 4-Kbyte Embedded Trace Buffer

### True random number generators (3 oscillators each)

### 96-bit unique ID

### All packages are ECOPACK®2 compliant

**Table 1. Device summary**

| Reference | Part number |
|---|---|
| STM32H747 xI | STM32H747AI, STM32H747BI, STM32H747II, STM32H747XI, STM32H747ZI |
| STM32H747 xG | STM32H747AG, STM32H747BG, STM32H747IG, STM32H747XG |

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# 1 Introduction

This document provides information on STM32H747xI/G microcontrollers, such as description, functional overview, pin assignment and definition, electrical characteristics, packaging, and ordering information.

This document should be read in conjunction with the STM32H747xI/G reference manual (RM0399), available from the STMicroelectronics website *www.st.com*.

For information on the Arm®(a) Cortex®-M7 core and Arm® Cortex®-M4 core, please refer to the Cortex®-M7 Technical Reference Manual, available from the http://www.arm.com website.

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

# 2 Description

STM32H747xI/G devices are based on the high-performance Arm® Cortex®-M7 and Cortex®-M4 32-bit RISC cores. The Cortex®-M7 core operates at up to 480 MHz and the Cortex®-M4 core at up to 240 MHz. Both cores feature a floating point unit (FPU) which supports Arm® single- and double-precision (Cortex®-M7 core) operations and conversions (IEEE 754 compliant), including a full set of DSP instructions and a memory protection unit (MPU) to enhance application security.

STM32H747xI/G devices incorporate high-speed embedded memories with a dual-bank Flash memory of up to 2 Mbytes, up to 1 Mbyte of RAM (including 192 Kbytes of TCM RAM, up to 864 Kbytes of user SRAM and 4 Kbytes of backup SRAM), as well as an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses, 2x32-bit multi-AHB bus matrix and a multi layer AXI interconnect supporting internal and external memory access.

All the devices offer three ADCs, two DACs, two ultra-low power comparators, a low-power RTC, a high-resolution timer, 12 general-purpose 16-bit timers, two PWM timers for motor control, five low-power timers, a true random number generator (RNG). The devices support four digital filters for external sigma-delta modulators (DFSDM). They also feature standard and advanced communication interfaces.

- Standard peripherals
  - Four $I^2Cs$
  - Four USARTs, four UARTs and one LPUART
  - Six SPIs, three $I^2Ss$ in Half-duplex mode. To achieve audio class accuracy, the $I^2S$ peripherals can be clocked by a dedicated internal audio PLL or by an external clock to allow synchronization.
  - Four SAI serial audio interfaces
  - One SPDIFRX interface
  - One SWPMI (Single Wire Protocol Master Interface)
  - Management Data Input/Output (MDIO) slaves
  - Two SDMMC interfaces
  - A USB OTG full-speed and a USB OTG high-speed interface with full-speed capability (with the ULPI)
  - One FDCAN plus one TT-FDCAN interface
  - An Ethernet interface
  - Chrom-ART Accelerator™
  - HDMI-CEC
- Advanced peripherals including
  - A flexible memory control (FMC) interface
  - A Quad-SPI Flash memory interface
  - A camera interface for CMOS sensors
  - An LCD-TFT display controller
  - A JPEG hardware compressor/decompressor
  - A DSI Host interface.

Refer to *Table 1: STM32H747xI/G features and peripheral counts* for the list of peripherals available on each part number.

STM32H747xI/G devices operate in the –40 to +85 °C temperature range from a 1.62 to 3.6 V power supply. The supply voltage can drop down to 1.62 V by using an external power supervisor (see *Section 3.5.2: Power supply supervisor)* and connecting the PDR_ON pin to $V_{SS}$. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.

Dedicated supply inputs for USB (OTG_FS and OTG_HS) are available on all packages to allow a greater power supply choice.

A comprehensive set of power-saving modes allows the design of low-power applications.

STM32H747xI/G devices are offered in 5 packages ranging from 156 pins to 240 pins/balls. The set of included peripherals changes with the device chosen.

These features make STM32H747xI/G microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile applications, Internet of Things
- Wearable devices: smart watches.

*Figure 1* shows the device block diagram.

**Table 1. STM32H747xI/G features and peripheral counts**

| Peripherals | | STM32H747AG | STM32H747IG | STM32H747BG | STM32H747XG | STM32H747ZI | STM32H747AI | STM32H747II | STM32H747BI | STM32H747XI |
|---|---|---|---|---|---|---|---|---|---|---|
| Flash memory in Kbytes | | 2 x 512 Kbytes | | | | 2 x 1 Mbyte | | | | |
| SRAM in Kbytes | SRAM mapped onto AXI bus | 512 | | | | | | | | |
| | SRAM1 (D2 domain) | 128 | | | | | | | | |
| | SRAM2 (D2 domain) | 128 | | | | | | | | |
| | SRAM3 (D2 domain) | 32 | | | | | | | | |
| | SRAM4 (D3 domain) | 64 | | | | | | | | |
| TCM RAM in Kbytes | ITCM RAM (instruction) | 64 | | | | | | | | |
| | DTCM RAM (data) | 128 | | | | | | | | |
| Backup SRAM (Kbytes) | | 4 | | | | | | | | |
| FMC | | Yes | | | | | | | | |
| General-purpose input/outputs | | 112 | 119 | 148 | 168 | 99 | 112 | 119 | 148 | 168 |
| Quad-SPI | | Yes | | | | | | | | |
| Ethernet | | Yes | | | | | | | | |
| Timers | High-resolution | 1 | | | | | | | | |
| | General-purpose | 10 | | | | | | | | |
| | Advanced-control (PWM) | 2 | | | | | | | | |
| | Basic | 2 | | | | | | | | |
| | Low-power | 5 | | | | | | | | |
| Wakeup pins<br>Tamper pins | | 4<br>2 | | 6<br>3 | | 4<br>2 | | | 6<br>3 | |
| Random number generator | | Yes | | | | | | | | |

**Table 1. STM32H747xI/G features and peripheral counts (continued)**

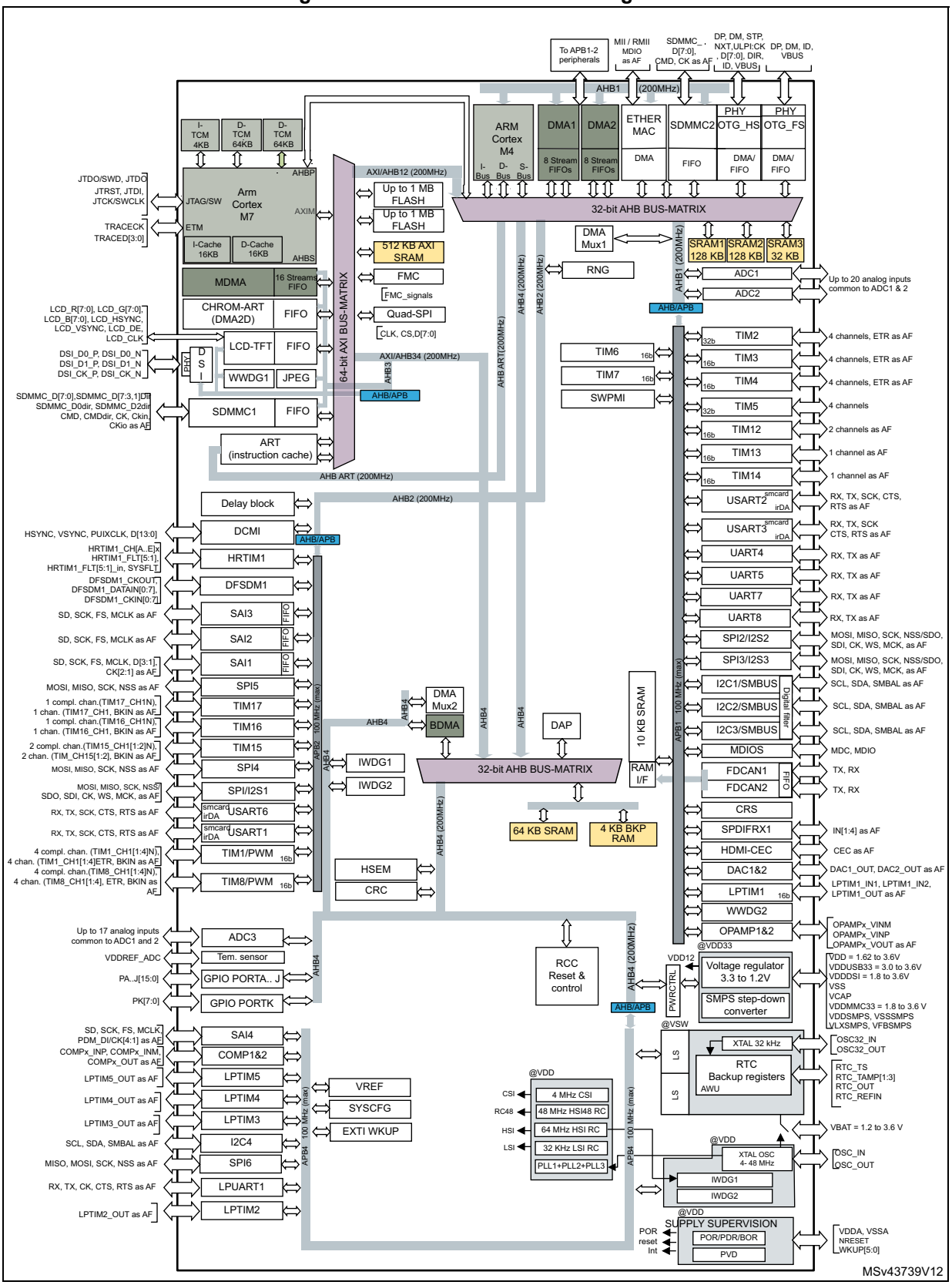
| Peripherals | | STM32H747AG | STM32H747IG | STM32H747BG | STM32H747XG | STM32H747ZI | STM32H747AI | STM32H747II | STM32H747BI | STM32H747XI |
|---|---|---|---|---|---|---|---|---|---|---|
| Communication interfaces | SPI / $I^2S$ | 6/3[1] | | | | | | | | |
| | $I^2C$ | 4 | | | | | | | | |
| | USART/UART /LPUART | 4/4 /1 | | | | | | | | |
| | SAI | 4 | | | | | | | | |
| | SPDIFRX | 4 inputs | | | | | | | | |
| | SWPMI | Yes | | | | | | | | |
| | MDIO | Yes | | | | | | | | |
| | SDMMC | 2 | | | | | | | | |
| | FDCAN/TT-FDCAN | 1/1 | | | | | | | | |
| | USB OTG_FS | Yes | | | | | | | | |
| | USB OTG_HS | Yes | | | | | | | | |
| Ethernet and camera interface | | Yes | | | | | | | | |
| LCD-TFT | | Yes | | | | | | | | |
| MIPI-DSI Host | | Yes | | | | | | | | |
| JPEG Codec | | Yes | | | | | | | | |
| Chrom-ART Accelerator™ (DMA2D) | | Yes | | | | | | | | |
| GPIOs | | Up to 168 | | | | | | | | |
| 16-bit ADCs | | 3 | | | | | | | | |
| Number of Direct channels | | 2 | | 2 | | 4 | | 2 | | 2 |
| Number of Fast channels | | 9 | | 9 | | 9 | | 7 | | 9 |
| Number of Slow channels | | 17 | | 21 | | 23 | | 14 | | 17 |
| 12-bit DAC | | Yes | | | | | | | | |
| Number of channels | | 2 | | | | | | | | |
| Comparators | | 2 | | | | | | | | |
| Operational amplifiers | | 2 | | | | | | | | |
| DFSDM | | Yes | | | | | | | | |
| Maximum CPU frequency | | 480 MHz | | | | | | | | |

**Table 1. STM32H747xI/G features and peripheral counts (continued)**

| Peripherals | STM32H747AG | STM32H747IG | STM32H747BG | STM32H747XG | STM32H747ZI | STM32H747AI | STM32H747II | STM32H747BI | STM32H747XI |
|---|---|---|---|---|---|---|---|---|---|
| Operating voltage | 1.62 to 3.6 V(2) | | | | | | | | |
| Operating temperatures | Ambient temperatures: –40 up to +85 °C(3) | | | | | | | | |
| | Junction temperature: –40 to + 125 °C | | | | | | | | |
| Package | UFBGA 169 | LQFP 176 | LQFP 208 | TFBGA 240+25 | WLCSP 156 | UFBGA169 | LQFP 176 | LQFP 208 | TFBGA 240+25 |

1. The SPI1, SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I2S audio mode.
2. $V_{DD}/V_{DDA}$ can drop down to 1.62 V by using an external power supervisor (see *Section 3.5.2: Power supply supervisor)* and connecting PDR_ON pin to $V_{SS}$. Otherwise the supply voltage must stay above 1.71 V with the embedded power voltage detector enabled.
3. The product junction temperature must be kept within the –40 to +125 °C range.

**Figure 1. STM32H747xI/G block diagram**



## Compatibility throughout the family

STM32H747xI/G devices are not pin-to-pin compatible with STM32H7x3 devices (single core line):

- The TFBGA240+25 ballout is compatible with STM32H7x3 devices, except for a few I/O balls as shown in *Figure 2*.
- LQFP208 and LQFP176 pinouts, as well as UFBGA176+25 ballout are not compatible with STM32H7x3 devices.

**Figure 2. TFBGA240+25 ball assignment differences**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | PI6 | PI5 | PI4 | PB5 | VDDLDO | VCAP | PK5 | PG10 | PG9 | PD5 | PD4 | PC10 | PA15 | PI1 | PI0 | VSS |
| B | VBAT | VSS | PI7 | PE1 | PB6 | VSS | PB4 | PK4 | PG11 | PJ15 | PD6 | PD3 | PC11 | PA14 | PI2 | PH15 | PH14 |
| C | PC15-OSC32_OUT | PC14-OSC32_IN | PE2 | PE0 | PB7 | PB3 | PK6 | PK3 | PG12 | VSS | PD7 | PC12 | VSS | PI3 | PA13 | VSS | VDDLDO |
| D | PE5 | PE4 | PE3 | PB9 | PB8 | PG15 | PK7 | PG14 | PG13 | PJ14 | PJ12 | PD2 | PD0 | PA10 | PA9 | PH13 | VCAP |
| E | | PI9 | PC13 | PI8 | PE6 | VDD | PDR_ON | BOOT0 | VDD | PJ13 | VDD | PD1 | PC8 | PC9 | PA8 | PA12 | PA11 |
| F | | | PI10 | PI11 | VDD | | | | | | | | PC7 | PC6 | PG8 | PG7 | VDD33USB |
| G | PF2 | | PF1 | PF0 | VDD | | VSS | VSS | VSS | VSS | VSS | | VDD | PG5 | PG6 | VSS | VDD5USB |
| H | PI12 | PI13 | PI14 | PF3 | VDD | | VSS | VSS | VSS | VSS | VSS | | VDD | PG4 | PG3 | PG2 | PK2 |
| J | PH1-OSC_OUT | PH0-OSC_IN | VSS | PF5 | PF4 | | VSS | VSS | VSS | VSS | VSS | | VDD | PK0 | PK1 | VSS DSI | VSSDSI |
| K | NRST | PF6 | PF7 | PF8 | VDD | | VSS | VSS | VSS | VSS | VSS | | VDD | PJ11 | | | |
| L | VDDA | PC0 | PF10 | PF9 | VDD | | VSS | VSS | VSS | VSS | VSS | | VDD | PJ10 | | | |
| M | VREF+ | PC1 | PC2 | PC3 | VDD | | | | | | | | VDD | PJ9 | | | |
| N | VREF- | PH2 | PA2 | PA1 | PA0 | PJ0 | VDD | VDD | PE10 | VDD | VDD | VDD | PJ8 | PJ7 | PJ6 | VSS | |
| P | VSSA | PH3 | PH4 | PH5 | PI15 | PJ1 | PF13 | PF14 | PE9 | PE11 | PB10 | PB11 | PH10 | PH11 | PD15 | PD14 | |
| R | PC2_C | PC3_C | PA6 | VSS | PA7 | PB2 | PF12 | VSS | PF15 | PE12 | PE15 | PJ5 | PH9 | PH12 | PD11 | PD12 | PD13 |
| T | PA0_C | PA1_C | PA5 | PC4 | PB1 | PJ2 | PF11 | PG0 | PE8 | PE13 | PH6 | VSS | PH8 | PB12 | PB15 | PD10 | PD9 |
| U | VSS | PA3 | PA4 | PC5 | PB0 | PJ3 | PJ4 | PG1 | PE7 | PE14 | VCAP | VDDLDO | PH7 | PB13 | PB14 | PD8 | VSS |

STM32H7x7

| | | | | |
|---|---|---|---|---|
| VLX SMPS | PI9 | VSSDSI | DSI_D1P | DSI_D1N |
| VDD SMPS | VSS SMPS | VSSDSI | DSI_CKP | DSI_CKN |
| PF2 | VFB SMPS | VSSDSI | DSI_D0P | DSI_D0N |
| | | PJ6 | VSS | VDDCAP DSI |
| | | PD15 | PD14 | VDDDSI |

STM32H7x3

| | | | | |
|---|---|---|---|---|
| NC | PI9 | VSS | NC | NC |
| NC | NC | VSS | NC | NC |
| PF2 | NC | VSS | NC | NC |
| | | PJ6 | VSS | NC |
| | | PD15 | PD14 | VDD |

MSv48802V2

1. The balls highlighted in gray correspond to different signals on STM32H747xI/G and STM32H7x3 devices.

# 3 Functional overview

## 3.1 Dual Arm® Cortex® cores

The dual-core MIPI-DSI STM32H747xI/G devices embed two Arm® cores, a Cortex®-M7 and a Cortex®-M4. The Cortex®-M4 offers optimal performance for real-time applications while the Cortex®-M7 core can execute high-performance tasks in parallel.

The two cores belong to separate power domains. This allows designing gradual high-power efficiency solutions in combination with the low-power modes already available on all STM32 microcontrollers.

### 3.1.1 Arm® Cortex®-M7 with FPU

The Arm® Cortex®-M7 with double-precision FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and optimized power consumption, while delivering outstanding computational performance and low interrupt latency.

The Cortex®-M7 processor is a highly efficient high-performance featuring:

- Six-stage dual-issue pipeline
- Dynamic branch prediction
- Harvard architecture with L1 caches (16 Kbytes of I-cache and 16 Kbytes of D-cache)
- 64-bit AXI interface
- 64-bit ITCM interface
- 2x32-bit DTCM interfaces

The following memory interfaces are supported:

- Separate Instruction and Data buses (Harvard Architecture) to optimize CPU latency
- Tightly Coupled Memory (TCM) interface designed for fast and deterministic SRAM accesses
- AXI Bus interface to optimize Burst transfers
- Dedicated low-latency AHB-Lite peripheral bus (AHBP) to connect to peripherals.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

It also supports single and double precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

*Figure 1* shows the general block diagram of the STM32H747xI/G family.

*Note: Cortex®-M7 with FPU core is binary compatible with the Cortex®-M4 core.*

### 3.1.2 Arm® Cortex®-M4 with FPU

The Arm® Cortex®-M4 processor is a high-performance embedded processor which supports DSP instructions. It was developed to provide an optimized power consumption MCU, while delivering outstanding computational performance and low interrupt latency.

The Arm® Cortex®-M4 processor is a highly efficient MCU featuring:

- 3-stage pipeline with branch prediction
- Harvard architecture
- 32-bit System (S-BUS) interface
- 32-bit I-BUS interface
- 32-bit D-BUS interface

The Arm® Cortex®-M4 processor also features a dedicated hardware adaptive real-time accelerator (ART Accelerator™). This is an instruction cache memory composed of sixty-four 256-bit lines, a 256-bit cache buffer connected to the 64-bit AXI interface and a 32-bit interface for non-cacheable accesses.

## 3.2 Memory protection unit (MPU)

The devices feature two memory protection units. Each MPU manages the CPU access rights and the attributes of the system resources. It has to be programmed and enabled before use. Its main purposes are to prevent an untrusted user program to accidentally corrupt data used by the OS and/or by a privileged task, but also to protect data processes or read-protect memory regions.

The MPU defines access rules for privileged accesses and user program accesses. It allows defining up to 16 protected regions that can in turn be divided into up to 8 independent subregions, where region address, size, and attributes can be configured. The protection area ranges from 32 bytes to 4 Gbytes of addressable memory.

When an unauthorized access is performed, a memory management exception is generated.

## 3.3 Memories

### 3.3.1 Embedded Flash memory

The STM32H747xI/G devices embed up to 2 Mbytes of Flash memory that can be used for storing programs and data.

The Flash memory is organized as 266-bit Flash words memory that can be used for storing both code and data constants. Each word consists of:

- One Flash word (8 words, 32 bytes or 256 bits)
- 10 ECC bits.

The Flash memory is divided into two independent banks. Each bank is organized as follows:

- A user Flash memory block of 512 Kbytes (STM32H7xxxG) or 1-Mbyte (STM32H7xxxI) containing eight user sectors of 128 Kbytes (4 K Flash memory words)
- 128 Kbytes of System Flash memory from which the device can boot
- 2 Kbytes (64 Flash words) of user option bytes for user configuration

### 3.3.2 Embedded SRAM

All devices feature around 1 Mbyte of RAM with hardware ECC. The RAM is divided as follows:

- 512 Kbytes of AXI-SRAM mapped onto AXI bus on D1 domain.
- SRAM1 mapped on D2 domain: 128 Kbytes
- SRAM2 mapped on D2 domain: 128 Kbytes
- SRAM3 mapped on D2 domain: 32 Kbytes
- SRAM4 mapped on D3 domain: 64 Kbytes
- 4 Kbytes of backup SRAM

  The content of this area is protected against possible unwanted write accesses, and is retained in Standby or $V_{BAT}$ mode.
- RAM mapped to TCM interface (ITCM and DTCM):

  Both ITCM and DTCM RAMs are 0 wait state memories. They can be accessed either from the Arm® Cortex®-M7 CPU or the MDMA (even in Sleep mode) through a specific AHB slave of the Cortex®-M7(AHBS):

  – 64 Kbytes of ITCM-RAM (instruction RAM)

    This RAM is connected to ITCM 64-bit interface designed for execution of critical real-times routines by the Cortex®-M7.

  – 128 Kbytes of DTCM-RAM (2x 64-Kbyte DTCM-RAMs on 2x32-bit DTCM ports)

    The DTCM-RAM could be used for critical real-time data, such as interrupt service routines or stack/heap memory. Both DTCM-RAMs can be used in parallel (for load/store operations) thanks to the Cortex®-M7 dual issue capability.

  The MDMA can be used to load code or data in ITCM or DTCM RAMs.

### Error code correction (ECC)

Over the product lifetime, and/or due to external events such as radiations, invalid bits in memories may occur. They can be detected and corrected by ECC. This is an expected behavior that has to be managed at final-application software level in order to ensure data integrity through ECC algorithms implementation.

SRAM data are protected by ECC:

- 7 ECC bits are added per 32-bit word.
- 8 ECC bits are added per 64-bit word for AXI-SRAM and ITCM-RAM.

The ECC mechanism is based on the SECDED algorithm. It supports single-error correction and double-error detection.

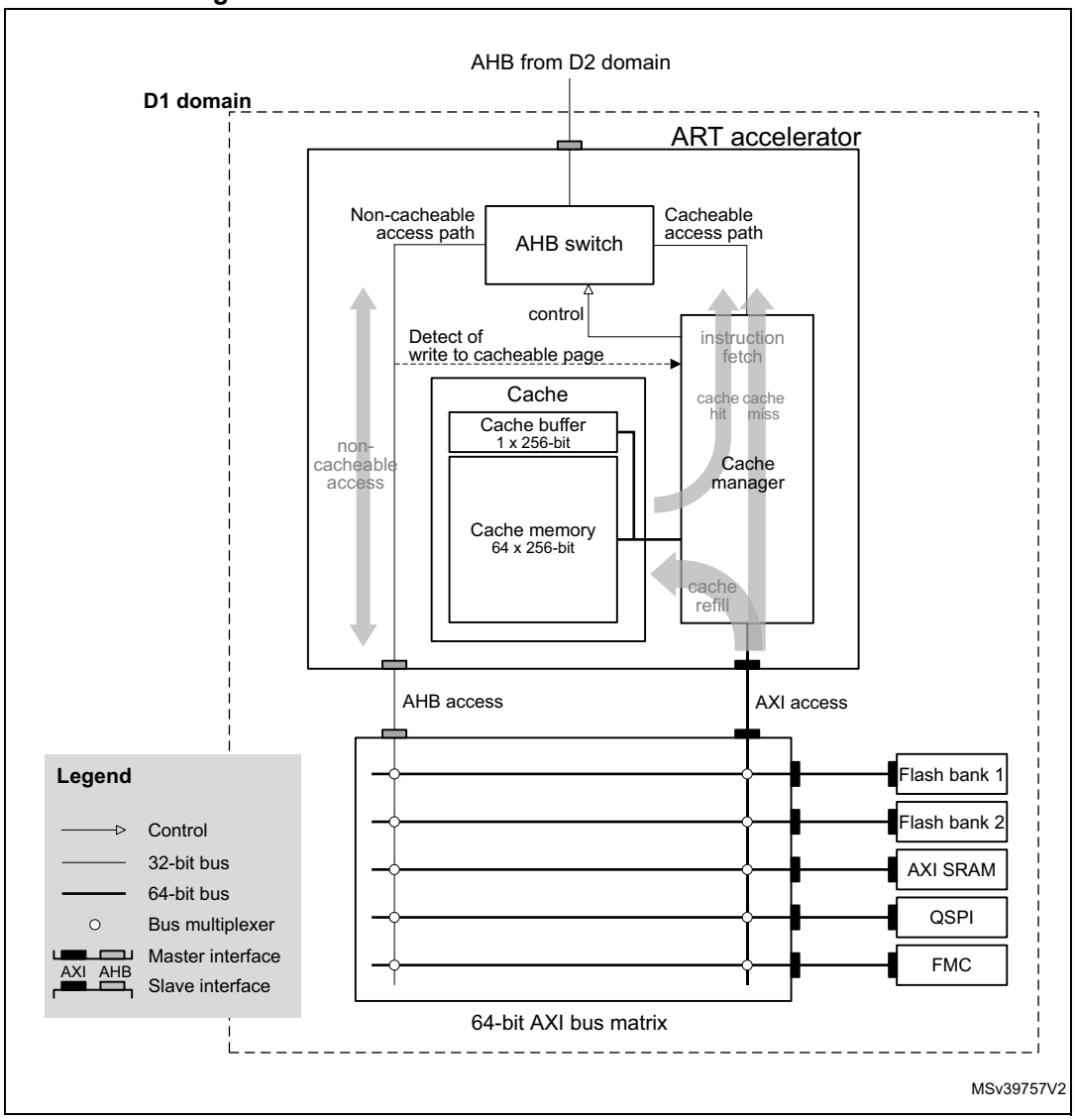
## 3.3.3 ART™ accelerator

The ART™ (adaptive real-time) accelerator block speeds up instruction fetch accesses of the Cortex®-M4 core from D1-domain internal memories (Flash memory bank 1, Flash memory bank 2, AXI SRAM) and from D1-domain external memories attached via Quad-SPI controller and Flexible memory controller (FMC).

The ART™ accelerator is a 256-bit cache line using 64-bit WRAP4 accesses from the 64-bit AXI D1 domain. The acceleration is achieved by loading selected code into an embedded cache and making it instantly available to Cortex®-M4 core, thus avoiding latency due to memory wait states.

*Figure 3*. shows the block schematic and the environment of the ART accelerator.

**Figure 3. ART™ accelerator schematic and environment**




## 3.4 Boot modes

By default, the boot codes are executed simultaneously by both cores. However, by programming the appropriate Flash user option byte, it is possible to boot from one core while clock-gating the other core.

At startup, the boot memory space is selected by the BOOT pin and BOOT_ADDx option bytes, allowing to program any boot memory address from 0x0000 0000 to 0x3FFF FFFF which includes:

- All Flash address space
- Flash memory and SRAMs (except for ITCM /DTCM RAMs which cannot be accessed by the Cortex®-M4 core)

The bootloader is located in non-user System memory. It is used to reprogram the Flash memory through a serial interface (USART, I2C, SPI, USB-DFU). Refer to *STM32 microcontroller System memory Boot mode* application note (AN2606) for details.

## 3.5 Power supply management

### 3.5.1 Power supply scheme

STM32H747xI/G power supply voltages are the following:

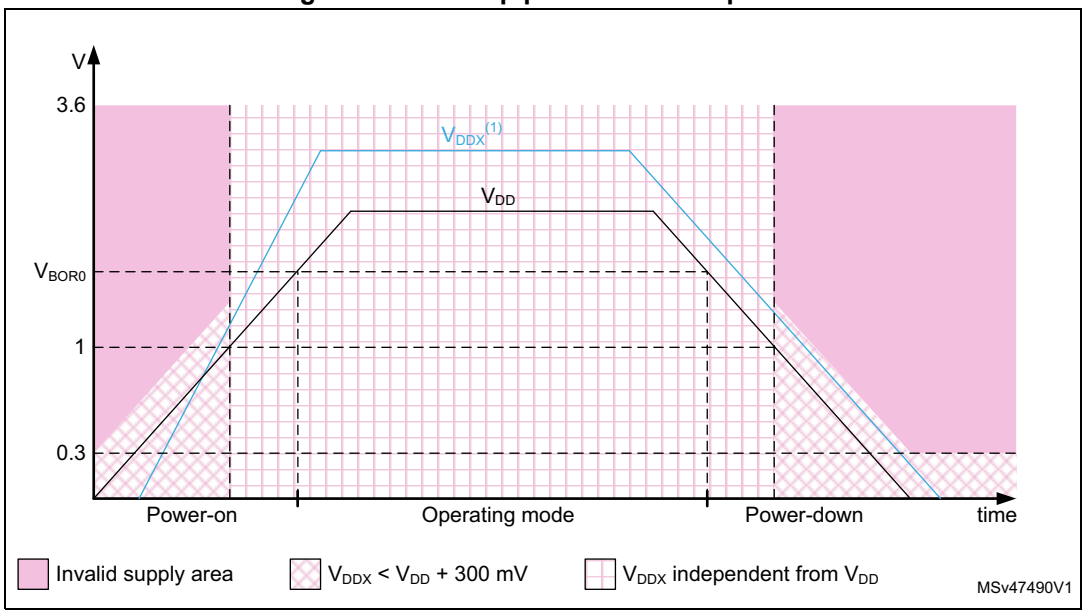
- $V_{DD}$ = 1.62 to 3.6 V: external power supply for I/Os, provided externally through $V_{DD}$ pins.
- $V_{DDLDO}$ = 1.62 to 3.6 V: supply voltage for the internal regulator supplying $V_{CORE}$
- $V_{DDA}$ = 1.62 to 3.6 V: external analog power supplies for ADC, DAC, COMP and OPAMP.
- $V_{DD33USB}$ and $V_{DD50USB}$:
  $V_{DD50USB}$ can be supplied through the USB cable to generate the $V_{DD33USB}$ via the USB internal regulator. This allows supporting a $V_{DD}$ supply different from 3.3 V.
  The USB regulator can be bypassed to supply directly $V_{DD33USB}$ if $V_{DD}$ = 3.3 V.
- $V_{BAT}$ = 1.2 to 3.6 V: power supply for the $V_{SW}$ domain when $V_{DD}$ is not present.
- $V_{CAP}$: $V_{CORE}$ supply voltage, which values depend on voltage scaling (1.0 V, 1.1 V, 1.2 V or 1.35 V). They are configured through VOS bits in PWR_D3CR register and ODEN bit in the SYSCFG_PWRCR register. The $V_{CORE}$ domain is split into the following power domains that can be independently switch off.
  - D1 domain containing some peripherals and the Cortex®-M7 core.
  - D2 domain containing a large part of the peripherals and the Cortex®-M4 core.
  - D3 domain containing some peripherals and the system control.
- $V_{DDSMPS}$= 1.62 V to 3.6 V: SMPS step-down converter power supply
  $V_{DDSMPS}$ must be kept at the same voltage level as $V_{DD}$.
- $V_{LXSMPS}$ = SMPS step-down converter output coupled to an inductor.
- $V_{FBSMPS}$ = $V_{CORE}$, 1.8 V or 2.5 V external SMPS step-down converter feedback voltage sense input.
- $V_{DDDSI}$ = 1.62 to 3.6 V: supply voltage for the DSI internal regulator
- $V_{DD12DSI}$ = 1.15 to 1.3 V: optional supply voltage for the DSI PHY (DSI regulator off)
- $V_{CAPDSI}$: DSI regulator supply output

During power-up and power-down phases, the following power sequence requirements must be respected (see *Figure 4*):

- When $V_{DD}$ is below 1 V, other power supplies ($V_{DDA}$, $V_{DD33USB}$, $V_{DD50USB}$, $V_{DDDSI}$) must remain below $V_{DD}$ + 300 mV.
- When $V_{DD}$ is above 1 V, all power supplies are independent (except for $V_{DDSMPS}$, which must remain at the same level as $V_{DD}$).

During the power-down phase, $V_{DD}$ can temporarily become lower than other supplies only if the energy provided to the microcontroller remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase.

**Figure 4. Power-up/power-down sequence**




1. $V_{DDx}$ refers to any power supply among $V_{DDA}$, $V_{DD33USB}$, $V_{DD50USB}$ and $V_{DDDSI}$.
2. $V_{DD}$ and $V_{DDSMPS}$ must be wired together into order to follow the same voltage sequence.

### 3.5.2 Power supply supervisor

The devices have an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry:

- Power-on reset (POR)

  The POR supervisor monitors $V_{DD}$ power supply and compares it to a fixed threshold. The devices remain in Reset mode when $V_{DD}$ is below this threshold,
- Power-down reset (PDR)

  The PDR supervisor monitors $V_{DD}$ power supply. A reset is generated when $V_{DD}$ drops below a fixed threshold.

  The PDR supervisor can be enabled/disabled through PDR_ON pin.
- Brownout reset (BOR)

  The BOR supervisor monitors $V_{DD}$ power supply. Three BOR thresholds (from 2.1 to 2.7 V) can be configured through option bytes. A reset is generated when $V_{DD}$ drops below this threshold.

### 3.5.3 Voltage regulator (SMPS step-down converter and LDO)

The same voltage regulator supplies the 3 power domains (D1, D2 and D3). D1 and D2 can be independently switched off.

Voltage regulator output can be adjusted according to application needs through 6 power supply levels:

- Run mode (VOS0 to VOS3)
  - Scale 0: boosted performance (available only with LDO regulator)
  - Scale 1: high performance
  - Scale 2: medium performance and consumption
  - Scale 3: optimized performance and low-power consumption

*Note: For STM32H7x7xIT3 sales types (industrial temperature range) the voltage regulator output can be set only to VOS2 or VOS3 in Run mode (VOS1 is not available for industrial temperature range).*

- Stop mode (SVOS3 to SVOS5)
  - Scale 3: peripheral with wakeup from Stop mode capabilities (UART, SPI, I2C, LPTIM) are operational
  - Scale 4 and 5 where the peripheral with wakeup from Stop mode is disabled

    The peripheral functionality is disabled but wakeup from Stop mode is possible through GPIO or asynchronous interrupt.

### 3.5.4 SMPS step-down converter

The built-in SMPS step-down converter is a highly power-efficient DC/DC non-linear switching regulator that provides lower power consumption than a conventional voltage regulator (LDO).

The SMPS step-down converter can be used for the following purposes:

- Direct supply of the $V_{CORE}$ domain
  - the SMPS step-down converter operating modes follow the device system operating modes (Run, Stop, Standby).
  - the SMPS step-down converter output voltage are set according to the selected VOS and SVOS bits (voltage scaling)
- Delivery of an intermediate voltage level to supply the internal voltage regulator (LDO)
  - SMPS step-down converter operating modes

    When the SDEXTHP bit is equal to 0 in the PWR_CR3 register, the SMPS step-down converter follows the device system operating modes (Run, Stop and Standby).

    When the SDEXTHP bit is equal to 1 in PWR_CR3, the SMPS step-down converter is forced to High-performance mode and does not follow the device system operating modes (Run, Stop and Standby).
  - The SMPS step-down converter output equals 1.8 V or 2.5 V according to the selected SD level
- Delivery of an external supply
  - The SMPS step-down converter is forced to High-performance mode (provided SDEXTHP bit is equal to 1 in PWR_CR3)
  - The SMPS step-down converter output equals 1.8 V or 2.5 V according to the selected SD level

## 3.6 Low-power strategy

There are several ways to reduce power consumption on STM32H747xI/G:

- Select the SMPS step-down converter as $V_{CORE}$ supply voltage source, as it allows to enhance power efficiency.
- Select the adequate voltage scaling
- Decrease the dynamic power consumption by slowing down the system clocks even in Run mode, and by individually clock gating the peripherals that are not used.
- Save power consumption when one or both CPUs are idle, by selecting among the available low-power mode according to the user application needs. This allows achieving the best compromise between short startup time, low-power consumption, as well as available wakeup sources.

The devices feature several low-power modes:

- CSleep (CPU clock stopped)
- CStop (CPU sub-system clock stopped)
- DStop (Domain bus matrix clock stopped)
- Stop (System clock stopped)
- DStandby (Domain powered down)
- Standby (System powered down)

CSleep and CStop low-power modes are entered by the MCU when executing the WFI (Wait for Interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit of the Cortex®-Mx core is set after returning from an interrupt service routine.

A domain can enter low-power mode (DStop or DStandby) when the processor, its subsystem and the peripherals allocated in the domain enter low-power mode. For instance D1 or D2 domain enters DStop/DStandby mode when the CPU of the domain is in CStop mode AND the other CPU has no peripheral allocated in that domain, or if it is in CStop mode too. D3 domain can enter DStop/DStandby mode if both core subsystems do not have active peripherals in D3 domain, and D3 is not forced in Run mode.

If part of the domain is not in low-power mode, the domain remains in the current mode.

Finally the system can enter Stop or Standby when all EXTI wakeup sources are cleared and the power domains are in DStop or DStandby mode.

The clock system can be re-initialize by a master CPU (either the Cortex®-M4 or -M7) after exiting Stop mode while the slave CPU is held in low-power mode. Once the master CPU has re-initialized the system, the slave CPU can receive a wakeup interrupt and proceed with the interrupt service routine.

**Table 2. System vs domain low-power mode**

| System power mode | D1 domain power mode | D2 domain power mode | D3 domain power mode |
|---|---|---|---|
| Run | DRun/DStop/DStandby | DRun/DStop/DStandby | DRun |
| Stop | DStop/DStandby | DStop/DStandby | DStop |
| Standby | DStandby | DStandby | DStandby |

## 3.7 Reset and clock controller (RCC)

The clock and reset controller is located in D3 domain. The RCC manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides a high flexibility in the choice of clock sources and allows to apply clock ratios to improve the power consumption. In addition, on some communication peripherals that are capable to work with two different clock domains (either a bus interface clock or a kernel peripheral clock), the system frequency can be changed without modifying the baudrate.

### 3.7.1 Clock management

The devices embed four internal oscillators, two oscillators with external crystal or resonator, two internal oscillators with fast startup time and three PLLs.

The RCC receives the following clock source inputs:

- Internal oscillators:
  - 64 MHz HSI clock
  - 48 MHz RC oscillator
  - 4 MHz CSI clock
  - 32 kHz LSI clock
- External oscillators:
  - HSE clock: 4-50 MHz (generated from an external source) or 4-48 MHz(generated from a crystal/ceramic resonator)
  - LSE clock: 32.768 kHz

The RCC provides three PLLs: one for system clock, two for kernel clocks.

The system starts on the HSI clock. The user application can then select the clock configuration.

### 3.7.2 System reset sources

Power-on reset initializes all registers while system reset reinitializes the system except for the debug, part of the RCC and power controller status registers, as well as the backup power domain.

A system reset is generated in the following cases:

- Power-on reset (pwr_por_rst)
- Brownout reset
- Low level on NRST pin (external reset)
- Independent watchdog 1 (from D1 domain)
- Independent watchdog 2 (from D2 domain)
- Window watchdog 1 (from D1 domain)
- Window watchdog 2 (from D2 domain)
- Software reset
- Low-power mode security reset
- Exit from Standby

## 3.8 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

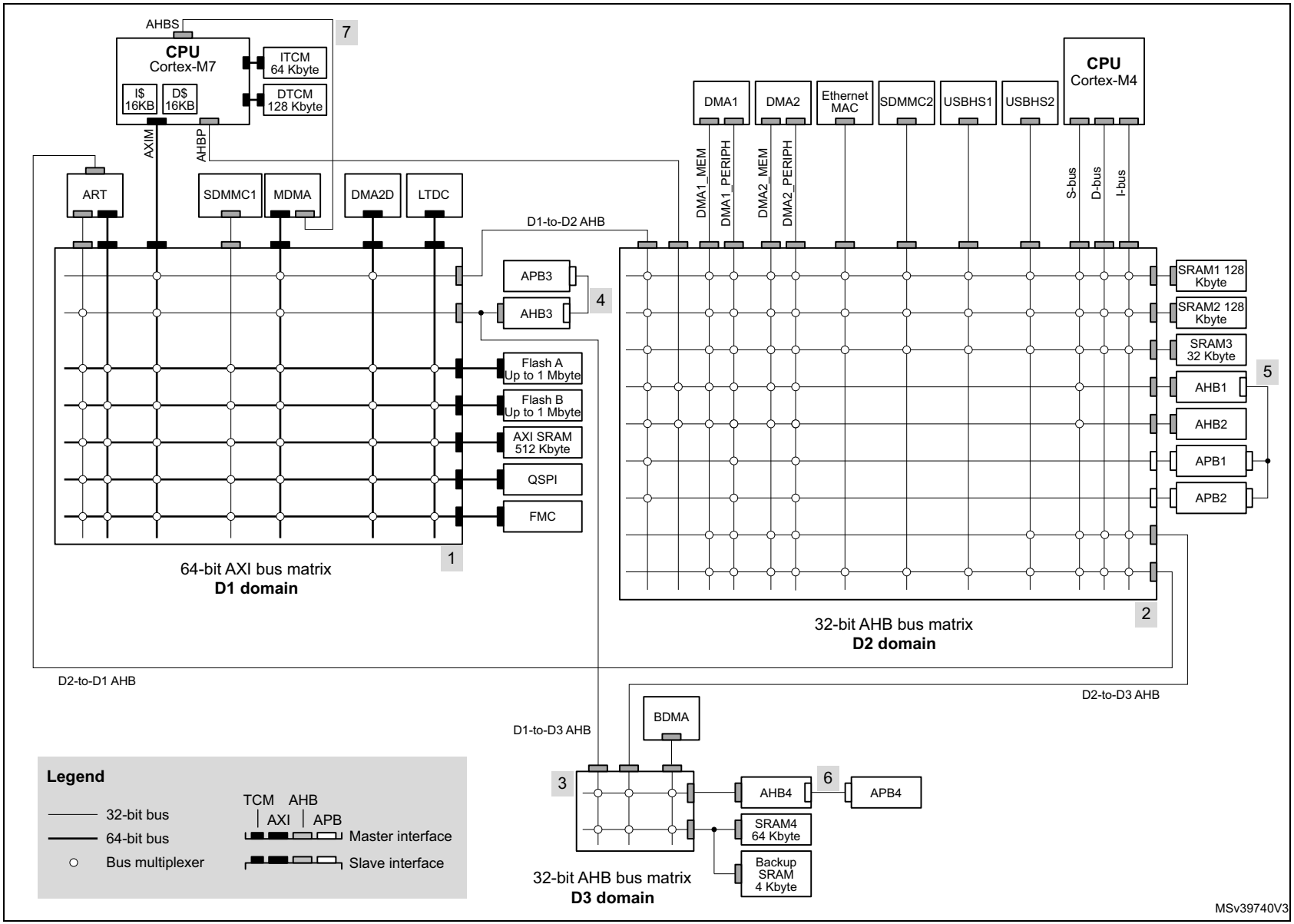
After reset, all GPIOs (except debug pins) are in Analog mode to reduce power consumption (refer to GPIOs register reset values in the device reference manual).

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

## 3.9 Bus-interconnect matrix

The devices feature an AXI bus matrix, two AHB bus matrices and bus bridges that allow interconnecting bus masters with bus slaves (see *Figure 5*).

**Figure 5. STM32H747xI/G bus matrix**



## 3.10 DMA controllers

The devices feature four DMA instances to unload CPU activity:

- A master direct memory access (MDMA)

  The MDMA is a high-speed DMA controller, which is in charge of all types of memory transfers (peripheral to memory, memory to memory, memory to peripheral), without any CPU action. It features a master AXI interface and a dedicated AHB interface to access Cortex®-M7 TCM memories.

  The MDMA is located in D1 domain. It is able to interface with the other DMA controllers located in D2 domain to extend the standard DMA capabilities, or can manage peripheral DMA requests directly.

  Each of the 16 channels can perform single block transfers, repeated block transfers and linked list transfers.
- Two dual-port DMAs (DMA1, DMA2) located in D2 domain, with FIFO and request router capabilities.
- One basic DMA (BDMA) located in D3 domain, with request router capabilities.

The DMA request router could be considered as an extension of the DMA controller. It routes the DMA peripheral requests to the DMA controller itself. This allowing managing the DMA requests with a high flexibility, maximizing the number of DMA requests that run concurrently, as well as generating DMA requests from peripheral output trigger or DMA event.

## 3.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphical accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables. The DMA2D also supports block based YCbCr to handle JPEG decoder output.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

## 3.12 Nested vectored interrupt controller (NVIC)

Both Cortex®-M7 (CPU1) and Cortex®-M4 (CPU2) cores have their own nested vector interrupt controller (respectively NVIC1 and NVIC2). Each NVIC instance is able to manage 16 priority levels, and handle up to 150 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M7 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor context automatically saved on interrupt entry, and restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

## 3.13 Extended interrupt and event controller (EXTI)

The EXTI controller performs interrupt and event management. In addition, it can wake up the processors, power domains and/or D3 domain from Stop mode.

The EXTI handles up to 89 independent event/interrupt lines split as 28 configurable events and 61 direct events (including two interrupt lines for inter-core management).

Configurable events have dedicated pending flags, active edge selection, and software trigger capable.

Direct events provide interrupts or events from peripherals having a status flag.

## 3.14 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code using a programmable polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

## 3.15 Flexible memory controller (FMC)

The FMC controller main features are the following:

- Interface with static-memory mapped devices including:
  - Static random access memory (SRAM)
  - NOR Flash memory/OneNAND Flash memory
  - PSRAM (4 memory banks)
  - NAND Flash memory with ECC hardware to check up to 8 Kbytes of data
- Interface with synchronous DRAM (SDRAM/Mobile LPSDR SDRAM) memories
- 8-,16-,32-bit data bus width
- Independent Chip Select control for each memory bank
- Independent configuration for each memory bank
- Write FIFO
- Read FIFO for SDRAM controller
- The maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is the FMC kernel clock divided by 2.

## 3.16 Quad-SPI memory interface (QUADSPI)

All devices embed a Quad-SPI memory interface, which is a specialized communication interface targeting Single, Dual or Quad-SPI Flash memories. It supports both single and double datarate operations.

It can operate in any of the following modes:

- Direct mode through registers
- External Flash status register polling mode
- Memory mapped mode.

Up to 256 Mbytes of external Flash memory can be mapped, and 8-, 16- and 32-bit data accesses are supported as well as code execution.

The opcode and the frame format are fully programmable.

## 3.17 Analog-to-digital converters (ADCs)

The STM32H747xI/G devices embed three analog-to-digital converters, which resolution can be configured to 16, 14, 12, 10 or 8 bits.

Each ADC shares up to 20 external channels, performing conversions in the Single-shot or Scan mode. In Scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold

The ADC can be served by the DMA controller, thus allowing to automatically transfer ADC converted values to a destination location without any software action.

In addition, an analog watchdog feature can accurately monitor the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4, TIM6, TIM8, TIM15, HRTIM1 and LPTIM1 timer.

## 3.18 Temperature sensor

STM32H747xI/G devices embed a temperature sensor that generates a voltage ($V_{TS}$) that varies linearly with the temperature. This temperature sensor is internally connected to ADC3_IN18. The conversion range is between 1.7 V and 3.6 V. It can measure the device junction temperature ranging from − 40 up to +125 °C.

The temperature sensor have a good linearity, but it has to be calibrated to obtain a good overall accuracy of the temperature measurement. As the temperature sensor offset varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only. To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the System memory area, which is accessible in Read-only mode.

## 3.19 $V_{BAT}$ operation

The $V_{BAT}$ power domain contains the RTC, the backup registers and the backup SRAM.

To optimize battery duration, this power domain is supplied by $V_{DD}$ when available or by the voltage applied on VBAT pin (when $V_{DD}$ supply is not present). $V_{BAT}$ power is switched when the PDR detects that $V_{DD}$ dropped below the PDR level.

The voltage on the VBAT pin could be provided by an external battery, a supercapacitor or directly by $V_{DD}$, in which case, the $V_{BAT}$ mode is not functional.

$V_{BAT}$ operation is activated when $V_{DD}$ is not present.

The $V_{BAT}$ pin supplies the RTC, the backup registers and the backup SRAM.

*Note: When the microcontroller is supplied from $V_{BAT}$, external interrupts and RTC alarm/events do not exit it from $V_{BAT}$ operation.*

*When PDR_ON pin is connected to $V_{SS}$ (Internal Reset OFF), the $V_{BAT}$ functionality is no more available and $V_{BAT}$ pin should be connected to $V_{DD}$.*

## 3.20 Digital-to-analog converters (DAC)

The two 12-bit buffered DAC channels can be used to convert two digital signals into two analog voltage signal outputs.

This dual digital Interface supports the following features:

- two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- left or right data alignment in 12-bit mode
- synchronized update capability
- noise-wave generation
- triangular-wave generation
- dual DAC channel independent or simultaneous conversions
- DMA capability for each channel including DMA underrun error detection
- external triggers for conversion
- input voltage reference $V_{REF+}$ or internal VREFBUF reference.

The DAC channels are triggered through the timer update outputs that are also connected to different DMA streams.

## 3.21 Ultra-low-power comparators (COMP)

STM32H747xI/G devices embed two rail-to-rail comparators (COMP1 and COMP2). They feature programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) as well as selectable output polarity.

The reference voltage can be one of the following:

- An external I/O
- A DAC output channel
- An internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers, and be combined into a window comparator.

## 3.22 Operational amplifiers (OPAMP)

STM32H747xI/G devices embed two rail-to-rail operational amplifiers (OPAMP1 and OPAMP2) with external or internal follower routing and PGA capability.

The operational amplifier main features are:

- PGA with a non-inverting gain ranging of 2, 4, 8 or 16 or inverting gain ranging of -1, -3, -7 or -15
- One positive input connected to DAC
- Output connected to internal ADC
- Low input bias current down to 1 nA
- Low input offset voltage down to 1.5 mV
- Gain bandwidth up to 7.3 MHz

The devices embeds two operational amplifiers (OPAMP1 and OPAMP2) with two inputs and one output each. These three I/Os can be connected to the external pins, thus enabling any type of external interconnections. The operational amplifiers can be configured internally as a follower, as an amplifier with a non-inverting gain ranging from 2 to 16 or with inverting gain ranging from -1 to -15.

## 3.23 Digital filter for sigma-delta modulators (DFSDM)

The devices embed one DFSDM with 4 digital filters modules and 8 external input serial channels (transceivers) or alternately 8 internal parallel inputs support.

The DFSDM peripheral is dedicated to interface the external ΣΔ modulators to microcontroller and then to perform digital filtering of the received data streams (which represent analog value on ΣΔ modulators inputs). DFSDM can also interface PDM (Pulse Density Modulation) microphones and perform PDM to PCM conversion and filtering in hardware. DFSDM features optional parallel data stream inputs from internal ADC peripherals or microcontroller memory (through DMA/CPU transfers into DFSDM).

DFSDM transceivers support several serial interface formats (to support various ΣΔ modulators). DFSDM digital filter modules perform digital processing according user selected filter parameters with up to 24-bit final ADC resolution.

The DFSDM peripheral supports:

- 8 multiplexed input digital serial channels:
  - configurable SPI interface to connect various SD modulator(s)
  - configurable Manchester coded 1 wire interface support
  - PDM (Pulse Density Modulation) microphone input support
  - maximum input clock frequency up to 20 MHz (10 MHz for Manchester coding)
  - clock output for SD modulator(s): 0..20 MHz
- alternative inputs from 8 internal digital parallel channels (up to 16 bit input resolution):
  - internal sources: ADC data or memory data streams (DMA)
- 4 digital filter modules with adjustable digital signal processing:
  - $Sinc^x$ filter: filter order/type (1..5), oversampling ratio (up to 1..1024)
  - integrator: oversampling ratio (1..256)
- up to 24-bit output data resolution, signed output data format
- automatic data offset correction (offset stored in register by user)
- continuous or single conversion
- start-of-conversion triggered by:
  - software trigger
  - internal timers
  - external events
  - start-of-conversion synchronously with first digital filter module (DFSDM0)
- analog watchdog feature:
  - low value and high value data threshold registers
  - dedicated configurable Sincx digital filter (order = 1..3, oversampling ratio = 1..32)
  - input from final output data or from selected input digital serial channels
  - continuous monitoring independently from standard conversion

- short circuit detector to detect saturated analog input values (bottom and top range):
  - up to 8-bit counter to detect 1..256 consecutive 0's or 1's on serial data stream
  - monitoring continuously each input serial channel
- break signal generation on analog watchdog event or on short circuit detector event
- extremes detector:
  - storage of minimum and maximum values of final conversion data
  - refreshed by software
- DMA capability to read the final conversion data
- interrupts: end of conversion, overrun, analog watchdog, short circuit, input serial channel clock absence
- "regular" or "injected" conversions:
  - "regular" conversions can be requested at any time or even in Continuous mode without having any impact on the timing of "injected" conversions
  - "injected" conversions for precise timing and with high conversion priority

**Table 3. DFSDM implementation**

| DFSDM features | DFSDM1 |
|---|---|
| Number of filters | 4 |
| Number of input transceivers/channels | 8 |
| Internal ADC parallel input | X |
| Number of external triggers | 16 |
| Regular channel information in identification register | X |

## 3.24 Digital camera interface (DCMI)

The devices embed a camera interface that can connect with camera modules and CMOS sensors through an 8-bit to 14-bit parallel interface, to receive video data. The camera interface can achieve a data transfer rate up to 140 Mbyte/s using a 80 MHz pixel clock. It features:

- Programmable polarity for the input pixel clock and synchronization signals
- Parallel data communication can be 8-, 10-, 12- or 14-bit
- Supports 8-bit progressive video monochrome or raw bayer format, YCbCr 4:2:2 progressive video, RGB 565 progressive video or compressed data (like JPEG)
- Supports Continuous mode or Snapshot (a single frame) mode
- Capability to automatically crop the image

## 3.25 LCD-TFT controller

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 display layers with dedicated FIFO (64x64-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events
- AXI master interface with burst of 16 words

## 3.26 DSI Host (DSI)

The DSI Host is a dedicated peripheral for interfacing with MIPI® DSI compliant displays. It includes a dedicated video interface internally connected to the LTDC, a generic APB interface that can be used to transmit information to the display, and Video mode pattern generator:

- LTDC interface

  It is used to transmit information in Video mode, in which the transfers from the host processor to the peripheral take the form of a real-time pixel stream (DPI).

  This interface can also be used to transmit information in full bandwidth in the Adapted Command mode (DBI).
- APB slave interface

  The APB slave interface allows transmitting generic information in Command mode though a proprietary register interface. It can operate concurrently with the LTDC interface either in Video or Adapted Command mode.
- The Video mode pattern generator allows transmitting horizontal/vertical color bar and D-PHY BER testing pattern without any kind of stimuli.

The DSI Host main features are the following:

- Compliance with MIPI® Alliance standards
- Interface with MIPI® D-PHY
- Support for all commands defined in the MIPI® Alliance specification for DCS:
  - Transmission of all Command mode packets through the APB interface
  - Transmission of commands in low-power and high-speed during Video mode
- Support for up to two D-PHY data lanes
- Bidirectional communication and Escape mode support through data lane 0
- Support for non-continuous clock in D-PHY clock lane for additional power saving
- Support for Ultra Low-Power mode with PLL disabled
- ECC and Checksum capabilities
- Support for End of Transmission Packet (EoTp)
- Fault recovery schemes

- 3D transmission support
- Configurable selection of system interfaces
  - AMBA APB for control and optional support for Generic and DCS commands
  - Video mode interface through LTDC
  - Adapted Command mode interface through LTDC
  - Independently programmable Virtual Channel ID in Video, Adapted Command or APB Slave mode
- Video mode interfaces features
  - LTDC interface color coding mappings into 24-bit interface:
    16-bit RGB, configurations 1, 2, and 3
    18-bit RGB, configurations 1 and 2
    24-bit RGB
  - Programmable polarity of all LTDC interface signals
  - Extended resolutions beyond the DPI standard maximum resolution of 800x480 pixels; the maximum resolution is limited by the available DSI physical link bandwidth:
    Number of lanes: 2
    Maximum speed per lane: 1 Gbps
- Adapted interface features
  - Support for sending large amounts of data through the *memory_write_start* (WMS) and *memory_write_continue* (WMC) DCS commands
  - LTDC interface color coding mappings into 24-bit interface:
    16-bit RGB, configurations 1, 2, and 3
    18-bit RGB, configurations 1 and 2
    24-bit RGB
- Video mode pattern generator
  - Vertical and horizontal color bar generation without LTDC stimuli
  - BER pattern without LTDC stimuli

## 3.27 JPEG Codec (JPEG)

The JPEG Codec can encode and decode a JPEG stream as defined in the ***ISO/IEC 10918-1*** specification. It provides an fast and simple hardware compressor and decompressor of JPEG images with full management of JPEG headers.

The JPEG codec main features are as follows:

- 8-bit/channel pixel depths
- Single clock per pixel encoding and decoding
- Support for JPEG header generation and parsing
- Up to four programmable quantization tables
- Fully programmable Huffman tables (two AC and two DC)
- Fully programmable minimum coded unit (MCU)
- Encode/decode support (non simultaneous)
- Single clock Huffman coding and decoding
- Two-channel interface: Pixel/Compress In, Pixel/Compressed Out
- Support for single greyscale component
- Ability to enable/disable header processing
- Fully synchronous design
- Configuration for High-speed decode mode

## 3.28 Random number generator (RNG)

All devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit.

## 3.29 Timers and watchdogs

The devices include one high-resolution timer, two advanced-control timers, ten general-purpose timers, two basic timers, five low-power timers, two watchdogs and a SysTick timer.

All timer counters can be frozen in Debug mode.

*Table 4* compares the features of the advanced-control, general-purpose and basic timers.

**Table 4. Timer feature comparison**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Comple-mentary output | Max interface clock (MHz) | Max timer clock (MHz) (1) |
|---|---|---|---|---|---|---|---|---|---|
| High-resolution timer | HRTIM1 | 16-bit | Up | /1 /2 /4 (x2 x4 x8 x16 x32, with DLL) | Yes | 10 | Yes | 480 | 480 |
| Advanced -control | TIM1, TIM8 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | Yes | 120 | 240 |

**Table 4. Timer feature comparison (continued)**

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/ compare channels | Comple-mentary output | Max interface clock (MHz) | Max timer clock (MHz) (1) |
|---|---|---|---|---|---|---|---|---|---|
| General purpose | TIM2, TIM5 | 32-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 120 | 240 |
| | TIM3, TIM4 | 16-bit | Up, Down, Up/down | Any integer between 1 and 65536 | Yes | 4 | No | 120 | 240 |
| | TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No | 120 | 240 |
| | TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No | 120 | 240 |
| | TIM15 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 2 | 1 | 120 | 240 |
| | TIM16, TIM17 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 1 | 1 | 120 | 240 |
| Basic | TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No | 120 | 240 |
| Low-power timer | LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5 | 16-bit | Up | 1, 2, 4, 8, 16, 32, 64, 128 | No | 0 | No | 120 | 240 |

1. The maximum timer clock is up to 480 MHz depending on TIMPRE bit in the RCC_CFGR register and D2PRE1/2 bits in RCC_D2CFGR register.

### 3.29.1 High-resolution timer (HRTIM1)

The high-resolution timer (HRTIM1) allows generating digital signals with high-accuracy timings, such as PWM or phase-shifted pulses.

It consists of 6 timers, 1 master and 5 slaves, totaling 10 high-resolution outputs, which can be coupled by pairs for deadtime insertion. It also features 5 fault inputs for protection purposes and 10 inputs to handle external events such as current limitation, zero voltage or zero current switching.

The HRTIM1 timer is made of a digital kernel clocked at 480 MHz The high-resolution is available on the 10 outputs in all operating modes: variable duty cycle, variable frequency, and constant ON time.

The slave timers can be combined to control multiswitch complex converters or operate independently to manage multiple independent converters.

The waveforms are defined by a combination of user-defined timings and external events such as analog or digital feedbacks signals.

HRTIM1 timer includes options for blanking and filtering out spurious events or faults. It also offers specific modes and features to offload the CPU: DMA requests, Burst mode controller, Push-pull and Resonant mode.

It supports many topologies including LLC, Full bridge phase shifted, buck or boost converters, either in voltage or current mode, as well as lighting application (fluorescent or LED). It can also be used as a general purpose timer, for instance to achieve high-resolution PWM-emulated DAC.

### 3.29.2 Advanced-control timers (TIM1, TIM8)

The advanced-control timers (TIM1, TIM8) can be seen as three-phase PWM generators multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead times. They can also be considered as complete general-purpose timers. Their 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (Edge- or Center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, they have the same features as the general-purpose TIMx timers. If configured as 16-bit PWM generators, they have full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 and TIM8 support independent DMA request generation.

### 3.29.3 General-purpose timers (TIMx)

There are ten synchronizable general-purpose timers embedded in the STM32H747xI/G devices (see *Table 4* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The devices include 4 full-featured general-purpose timers: TIM2, TIM3, TIM4 and TIM5. TIM2 and TIM5 are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler while TIM3 and TIM4 are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. All timers feature 4 independent channels for input capture/output compare, PWM or One-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  TIM2, TIM3, TIM4 and TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM12, TIM13, TIM14, TIM15, TIM16, TIM17**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13, TIM14, TIM16 and TIM17 feature one independent channel, whereas TIM12 and TIM15 have two independent channels for input capture/output compare, PWM or One-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers or used as simple timebases.

### 3.29.4 Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger and waveform generation. They can also be used as a generic 16-bit time base.

TIM6 and TIM7 support independent DMA request generation.

### 3.29.5 Low-power timers (LPTIM1, LPTIM2, LPTIM3, LPTIM4, LPTIM5)

The low-power timers have an independent clock and is running also in Stop mode if it is clocked by LSE, LSI or an external clock. It is able to wakeup the devices from Stop mode.

This low-power timer supports the following features:

- 16-bit up counter with 16-bit autoreload register
- 16-bit compare register
- Configurable output: pulse, PWM
- Continuous / One-shot mode
- Selectable software / hardware input trigger
- Selectable clock source:
- Internal clock source: LSE, LSI, HSI or APB clock
- External clock source over LPTIM input (working even with no internal clock source running, used by the Pulse Counter Application)
- Programmable digital glitch filter
- Encoder mode

### 3.29.6 Independent watchdogs

There are two independent watchdogs, one per domain. Each independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

### 3.29.7 Window watchdogs

There are two window watchdogs, one per domain. Each window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device or each respective domain (configurable in the RCC register), when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in Debug mode.

### 3.29.8 SysTick timer

The devices feature two SysTick timers, one per CPU. These timers are dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

## 3.30 Real-time clock (RTC), backup SRAM and backup registers

The RTC is an independent BCD timer/counter. It supports the following features:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Two programmable alarms.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy.
- Three anti-tamper detection pins with programmable filter.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event, or by a switch to $V_{BAT}$ mode.
- 17-bit auto-reload wakeup timer (WUT) for periodic events with programmable resolution and period.

The RTC and the 32 backup registers are supplied through a switch that takes power either from the $V_{DD}$ supply when present or from the $V_{BAT}$ pin.

The backup registers are 32-bit registers used to store 128 bytes of user application data when $V_{DD}$ power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC clock sources can be:

- A 32.768 kHz external crystal (LSE)
- An external resonator or oscillator (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 kHz)
- The high-speed external clock (HSE) divided by 32.

The RTC is functional in $V_{BAT}$ mode and in all low-power modes when it is clocked by the LSE. When clocked by the LSI, the RTC is not functional in $V_{BAT}$ mode, but is functional in all low-power modes.

All RTC events (Alarm, Wakeup Timer, Timestamp or Tamper) can generate an interrupt and wakeup the device from the low-power modes.

## 3.31 Inter-integrated circuit interface (I2C)

STM32H747xI/G devices embed four $I^2C$ interfaces.

The $I^2C$ bus interface handles communications between the microcontroller and the serial $I^2C$ bus. It controls all $I^2C$ bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

- $I^2C$-bus specification and user manual rev. 5 compatibility:
  - Slave and Master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming.
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

## 3.32 Universal synchronous/asynchronous receiver transmitter (USART)

STM32H747xI/G devices have four embedded universal synchronous receiver transmitters (USART1, USART2, USART3 and USART6) and four universal asynchronous receiver transmitters (UART4, UART5, UART7 and UART8). Refer to *Table 5* for a summary of USARTx and UARTx features.

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire Half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 12.5 Mbit/s.

USART1, USART2, USART3 and USART6 also provide Smartcard mode (ISO 7816 compliant) and SPI-like communication capability.

The USARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

All USART have a clock domain independent from the CPU clock, allowing the USARTx to wake up the MCU from Stop mode.The wakeup from Stop mode is programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

All USART interfaces can be served by the DMA controller.

**Table 5. USART features**

| USART modes/features(1) | USART1/2/3/6 | UART4/5/7/8 |
|---|---|---|
| Hardware flow control for modem | X | X |
| Continuous communication using DMA | X | X |
| Multiprocessor communication | X | X |
| Synchronous mode (Master/Slave) | X | - |
| Smartcard mode | X | - |
| Single-wire Half-duplex communication | X | X |
| IrDA SIR ENDEC block | X | X |
| LIN mode | X | X |
| Dual clock domain and wakeup from low power mode | X | X |
| Receiver timeout interrupt | X | X |
| Modbus communication | X | X |
| Auto baud rate detection | X | X |
| Driver Enable | X | X |
| USART data length | 7, 8 and 9 bits | |
| Tx/Rx FIFO | X | X |
| Tx/Rx FIFO size | 16 | |

1. X = supported.

## 3.33 Low-power universal asynchronous receiver transmitter (LPUART)

The device embeds one Low-Power UART (LPUART1). The LPUART supports asynchronous serial communication with minimum power consumption. It supports half duplex single wire communication and modem operations (CTS/RTS). It allows multiprocessor communication.

The LPUARTs embed a Transmit FIFO (TXFIFO) and a Receive FIFO (RXFIFO). FIFO mode is enabled by software and is disabled by default.

The LPUART has a clock domain independent from the CPU clock, and can wakeup the system from Stop mode. The wakeup from Stop mode are programmable and can be done on:

- Start bit detection
- Any received data frame
- A specific programmed data frame
- Specific TXFIFO/RXFIFO status when FIFO mode is enabled.

Only a 32.768 kHz clock (LSE) is needed to allow LPUART communication up to 9600 baud. Therefore, even in Stop mode, the LPUART can wait for an incoming frame while having an extremely low energy consumption. Higher speed clock can be used to reach higher baudrates.

LPUART interface can be served by the DMA controller.

## 3.34 Serial peripheral interface (SPI)/inter- integrated sound interfaces (I2S)

The devices feature up to six SPIs (SPI2S1, SPI2S2, SPI2S3, SPI4, SPI5 and SPI6) that allow communicating up to 150 Mbits/s in Master and Slave modes, in Half-duplex, Full-duplex and Simplex modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable from 4 to 16 bits. All SPI interfaces support NSS pulse mode, TI mode, Hardware CRC calculation and 8x 8-bit embedded Rx and Tx FIFOs with DMA capability.

Three standard $I^2S$ interfaces (multiplexed with SPI1, SPI2 and SPI3) are available. They can be operated in Master or Slave mode, in Simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the $I^2S$ interfaces is/are configured in Master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency. All $I^2S$ interfaces support 16x 8-bit embedded Rx and Tx FIFOs with DMA capability.

## 3.35 Serial audio interfaces (SAI)

The devices embed 4 SAIs (SAI1, SAI2, SAI3 and SAI4) that allow designing many stereo or mono audio protocols such as I2S, LSB or MSB-justified, PCM/DSP, TDM or AC’97. An SPDIF output is available when the audio block is configured as a transmitter. To bring this level of flexibility and reconfigurability, the SAI contains two independent audio sub-blocks. Each block has it own clock generator and I/O line controller.
Audio sampling frequencies up to 192 kHz are supported.
In addition, up to 8 microphones can be supported thanks to an embedded PDM interface.
The SAI can work in master or slave configuration. The audio sub-blocks can be either receiver or transmitter and can work synchronously or asynchronously (with respect to the other one). The SAI can be connected with other SAIs to work synchronously.

## 3.36 SPDIFRX Receiver Interface (SPDIFRX)

The SPDIFRX peripheral is designed to receive an S/PDIF flow compliant with IEC-60958 and IEC-61937. These standards support simple stereo streams up to high sample rate, and compressed multi-channel surround sound, such as those defined by Dolby or DTS (up to 5.1).

The main SPDIFRX features are the following:

- Up to 4 inputs available
- Automatic symbol rate detection
- Maximum symbol rate: 12.288 MHz
- Stereo stream from 32 to 192 kHz supported
- Supports Audio IEC-60958 and IEC-61937, consumer applications
- Parity bit management
- Communication using DMA for audio samples
- Communication using DMA for control and user channel information
- Interrupt capabilities

The SPDIFRX receiver provides all the necessary features to detect the symbol rate, and decode the incoming data stream. The user can select the wanted SPDIF input, and when a valid signal will be available, the SPDIFRX will re-sample the incoming signal, decode the Manchester stream, recognize frames, sub-frames and blocks elements. It delivers to the CPU decoded data, and associated status flags.

The SPDIFRX also offers a signal named spdif_frame_sync, which toggles at the S/PDIF sub-frame rate that will be used to compute the exact sample rate for clock drift algorithms.

## 3.37 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- Full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

## 3.38 Management Data Input/Output (MDIO) slaves

The devices embed an MDIO slave interface it includes the following features:

- 32 MDIO Registers addresses, each of which is managed using separate input and output data registers:
  - 32 x 16-bit firmware read/write, MDIO read-only output data registers
  - 32 x 16-bit firmware read-only, MDIO write-only input data registers
- Configurable slave (port) address
- Independently maskable interrupts/events:
  - MDIO Register write
  - MDIO Register read
  - MDIO protocol error
- Able to operate in and wake up from Stop mode

## 3.39 SD/SDIO/MMC card host interfaces (SDMMC)

Two SDMMC host interfaces are available. They support *MultiMediaCard System Specification Version 4.51* in three different databus modes: 1 bit (default), 4 bits and 8 bits.

Both interfaces support the *SD memory card specifications version 4.1.* and the *SDIO card specification version 4.0.* in two different databus modes: 1 bit (default) and 4 bits.

Each SDMMC host interface supports only one SD/SDIO/MMC card at any one time and a stack of MMC Version 4.51 or previous.

The SDMMC host interface embeds a dedicated DMA controller allowing high-speed transfers between the interface and the SRAM.

## 3.40 Controller area network (FDCAN1, FDCAN2)

The controller area network (CAN) subsystem consists of two CAN modules, a shared message RAM memory and a clock calibration unit.

Both CAN modules (FDCAN1 and FDCAN2) are compliant with ISO 11898-1 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0.

FDCAN1 supports time triggered CAN (TT-FDCAN) specified in ISO 11898-4, including event synchronized time-triggered communication, global system time, and clock drift compensation. The FDCAN1 contains additional registers, specific to the time triggered feature. The CAN FD option can be used together with event-triggered and time-triggered CAN communication.

A 10-Kbyte message RAM memory implements filters, receive FIFOs, receive buffers, transmit event FIFOs, transmit buffers (and triggers for TT-FDCAN). This message RAM is shared between the two FDCAN1 and FDCAN2 modules.

The common clock calibration unit is optional. It can be used to generate a calibrated clock for both FDCAN1 and FDCAN2 from the HSI internal RC oscillator and the PLL, by evaluating CAN messages received by the FDCAN1.

## 3.41 Universal serial bus on-the-go high-speed (OTG_HS)

The devices embed two USB OTG high-speed (up to 480 Mbit/s) device/host/OTG peripheral. OTG-HS1 supports both full-speed and high-speed operations, while OTG-HS2 supports only full-speed operations. They both integrate the transceivers for full-speed operation (12 Mbit/s) and are able to operate from the internal HSI48 oscillator. OTG-HS1 features a UTMI low-pin interface (ULPI) for high-speed operation (480 Mbit/s). When using the USB OTG-HS1 in HS mode, an external PHY device connected to the ULPI is required.

The USB OTG HS peripherals are compliant with the USB 2.0 specification and with the OTG 2.0 specification. They have software-configurable endpoint setting and supports suspend/resume. The USB OTG controllers require a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator.

The main features are:

- Combined Rx and Tx FIFO size of 4 Kbytes with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 9 bidirectional endpoints (including EP0)
- 16 host channels with periodic OUT support
- Software configurable to OTG1.3 and OTG2.0 modes of operation
- USB 2.0 LPM (Link Power Management) support
- Battery Charging Specification Revision 1.2 support
- Internal FS OTG PHY support
- External HS or HS OTG operation supporting ULPI in SDR mode (OTG_HS1 only)

  The OTG PHY is connected to the microcontroller ULPI port through 12 signals. It can be clocked using the 60 MHz output.
- Internal USB DMA
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

## 3.42 Ethernet MAC interface with dedicated DMA controller (ETH)

The devices provide an IEEE-802.3-2002-compliant media access controller (MAC) for ethernet LAN communications through an industry-standard medium-independent interface (MII) or a reduced medium-independent interface (RMII). The microcontroller requires an external physical interface device (PHY) to connect to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the device MII port using 17 signals for MII or 9 signals for RMII, and can be clocked using the 25 MHz (MII) from the microcontroller.

The devices include the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller allowing high-speed transfers between the dedicated SRAM and the descriptors
- Tagged MAC frame support (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operation
- MAC control sublayer (control frames) support
- 32-bit CRC generation and removal
- Several address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal FIFOs to buffer transmit and receive frames. The transmit FIFO and the receive FIFO are both 2 Kbytes.
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588 2008 (PTP V2) with the time stamp comparator connected to the TIM2 input
- Triggers interrupt when system time becomes greater than target time

## 3.43 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The devices embed a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI-CEC controller to wakeup the MCU from Stop mode on data reception.

## 3.44 Debug infrastructure

The devices offer a comprehensive set of debug and trace features on both cores to support software development and system integration.

- Breakpoint debugging
- Code execution tracing
- Software instrumentation
- JTAG debug port
- Serial-wire debug port
- Trigger input and output
- Serial-wire trace port
- Trace port
- Arm® CoreSight™ debug and trace components

The debug can be controlled via a JTAG/Serial-wire debug access port, using industry standard debugging tools. The debug infrastructure allows debugging one core at a time, or both cores in parallel.

The trace port performs data capture for logging and analysis.

A 4-Kbyte embedded trace FIFO (ETF) allows recording data and sending them to any com port. In Trace mode, the trace is transferred by DMA to system RAM or to a high-speed interface (such as SPI or USB). It can even be monitored by a software running on one of the cores. Unlike hardware FIFO mode, this mode is invasive since it uses system resources which are shared by the processors.

# 4 Memory mapping

Refer to the product line reference manual for details on the memory mapping as well as the boundary addresses for all peripherals.

# 5 Pin descriptions

**Figure 6. WLCSP156 ballout**

| | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | DNC(1) | VDDLDO | VCAP | PB8 | VDD | PB4 | PG15 | VDD | PD4 | PD0 | PA15 | VDDLDO | VSS |
| B | VBAT | PE4 | VDD | PE0 | VSS | PB5 | PB3 | VSS | PD3 | PC12 | VDD | VCAP | PA12 |
| C | PC14-OSC32_IN | PC15-OSC32_OUT | PE5 | VSS | PB9 | PB7 | PB6 | PD6 | PC11 | VSS | PA13 | PA10 | PA11 |
| D | VDD | VSS SMPS | VSS | PE3 | PE2 | PE1 | BOOT0 | PD7 | PC10 | PA9 | PA8 | PC9 | PC8 |
| E | VDD SMPS | VLX SMPS | VFB SMPS | PF0 | PC13 | PE6 | PDR_ON | PD2 | PA14 | PC7 | VDD50 USB | VDD | VDD33 USB |
| F | PF3 | PF2 | PF4 | PF5 | PF1 | PF11 | PD5 | PD1 | PC6 | PG4 | VSS | PG8 | PG5 |
| G | VDD | VSS | PC0 | PC1 | PA6 | PF12 | PE10 | PE11 | PD8 | PG3 | PG2 | DSI_D1P | DSI_D1N |
| H | PH1-OSC_OUT | PH0-OSC_IN | NRST | PA5 | PB1 | PF13 | PE7 | PB10 | PB13 | PD14 | VSSDSI | DSI_CKP | DSI_CKN |
| J | VSSA | VREF+ | VDDA | PA3 | PA7 | PF15 | PE8 | PE12 | PB12 | PD11 | PD15 | DSI_D0P | DSI_D0N |
| K | PC2_C | PC3_C | PA2 | PA4 | PB0 | PF14 | PE9 | PE13 | PB11 | PD9 | PD13 | VDD | VCAP DSI |
| L | PA0 | PA1 | VSS | PC5 | VSS | PG0 | VSS | PE15 | VSS | VDDLDO | PD10 | PD12 | VSS |
| M | VSS | VDD | PC4 | PB2 | VDD | PG1 | VDD | PE14 | VCAP | VDD | PB14 | PB15 | VSS |

MSv43741V5

1. The DNC ball must neither be connected to GND nor to $V_{DD}$.
2. The above figure shows the package top view.

**Figure 7. UFBGA169 ballout**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | PE2 | VDDLDO | VCAP | PB5 | PB3 | VSS | PD7 | VDD | PD3 | PA14 | VSS | PA10 |
| B | VBAT | VDD | PDR_ ON | VSS | BOOT0 | PB4 | VDD | PD6 | VSS | PA15 | PA13 | VDD | VDDLDO |
| C | PC14_ OSC32_ IN | PE6 | PE3 | PE1 | PB7 | PG15 | PG9 | PD5 | PD1 | PD0 | PC10 | VSS | VCAP |
| D | VSS | PC15_ OSC32_ OUT | PE4 | PE0 | PB8 | PB9 | PG10 | PD4 | PC12 | PA8 | PA9 | PA11 | PA12 |
| E | VLX SMPS | VDD | PC13 | PE5 | PB6 | PG14 | PG11 | PD2 | PC11 | PC7 | PC9 | VDD | VSS |
| F | VDD SMPS | VSS SMPS | VFB SMPS | PF0 | PF1 | PF2 | PG13 | PG7 | PG8 | PC8 | PC6 | VDD50_ USB | VDD33_ USB |
| G | PF4 | PF3 | PF5 | PF6 | PF7 | PF8 | PG12 | PG3 | PG5 | PG4 | PG6 | VSSDSI | VSSDSI |
| H | VDD | VSS | PF9 | PF10 | NRST | PB1 | PG2 | PE13 | PD14 | PD15 | VSS DSI | DSI_ D1P | DSI_ D1N |
| J | PH1_ OSCOUT | PH0_ OSCIN | PC1 | PC0 | PA5 | PF12 | PG1 | PE12 | PD13 | PD12 | VSS DSI | DSI_ CKP | DSI_ CKN |
| K | PC2_C | PC3_C | PA0 | PA7 | PC5 | PF11 | PE7 | PE15 | PB10 | PD11 | VSS DSI | DSI_ D0P | DSI_ D0N |
| L | VSSA_ VREF- | VDDA | PA1 | PC4 | PB2 | PG0 | PE10 | PE8 | VDD | PB12 | VDD | VCAP DSI | VSS |
| M | VREF+ | VDD | PA2 | PA6 | PF13 | VSS | PF15 | PE14 | VSS | PB13 | PB15 | PD9 | VDD DSI |
| N | VSS | PA3 | PA4 | PB0 | PF14 | PE9 | PE11 | PB11 | VCAP | VDDLDO | PB14 | PD8 | PD10 |

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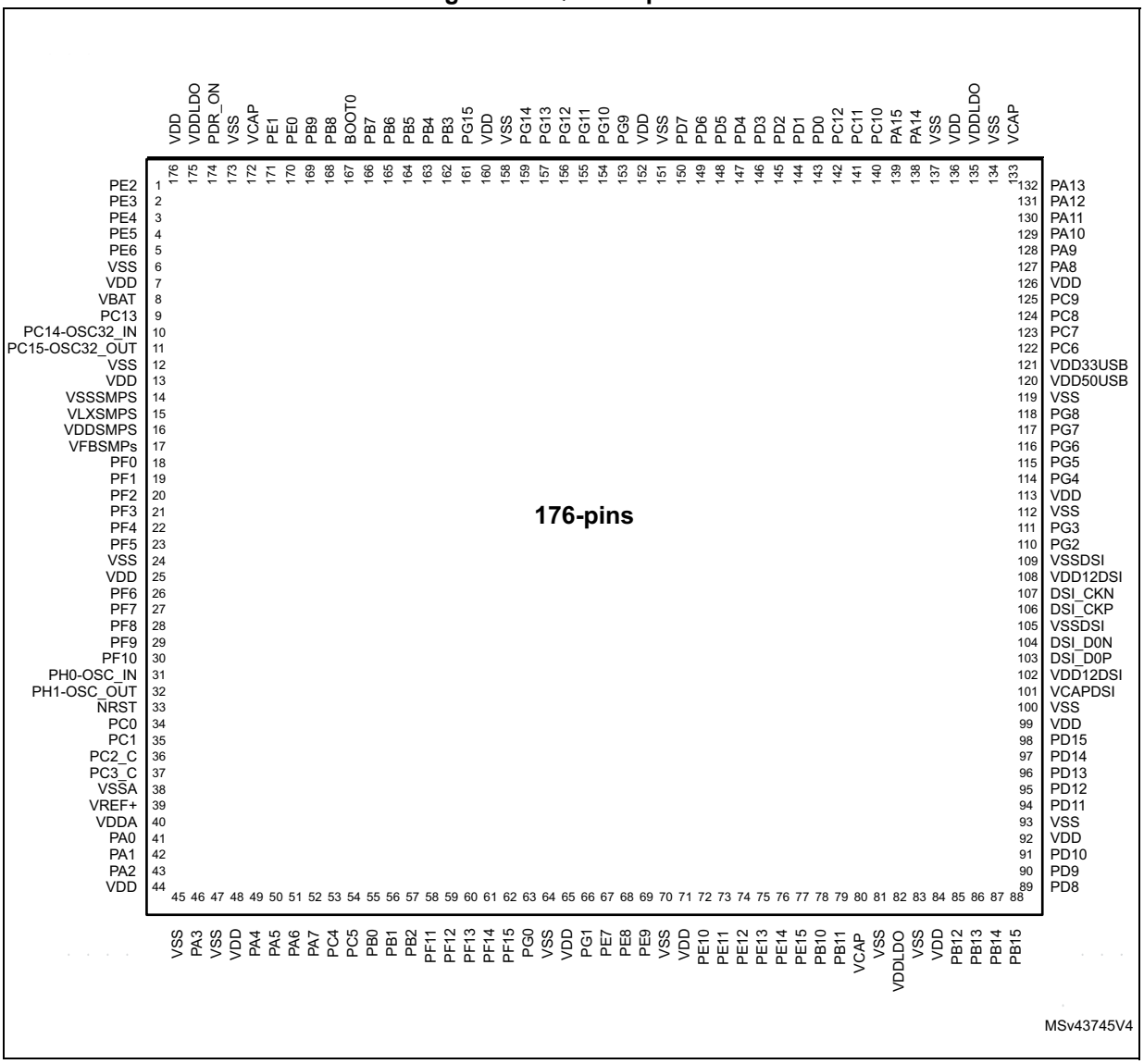
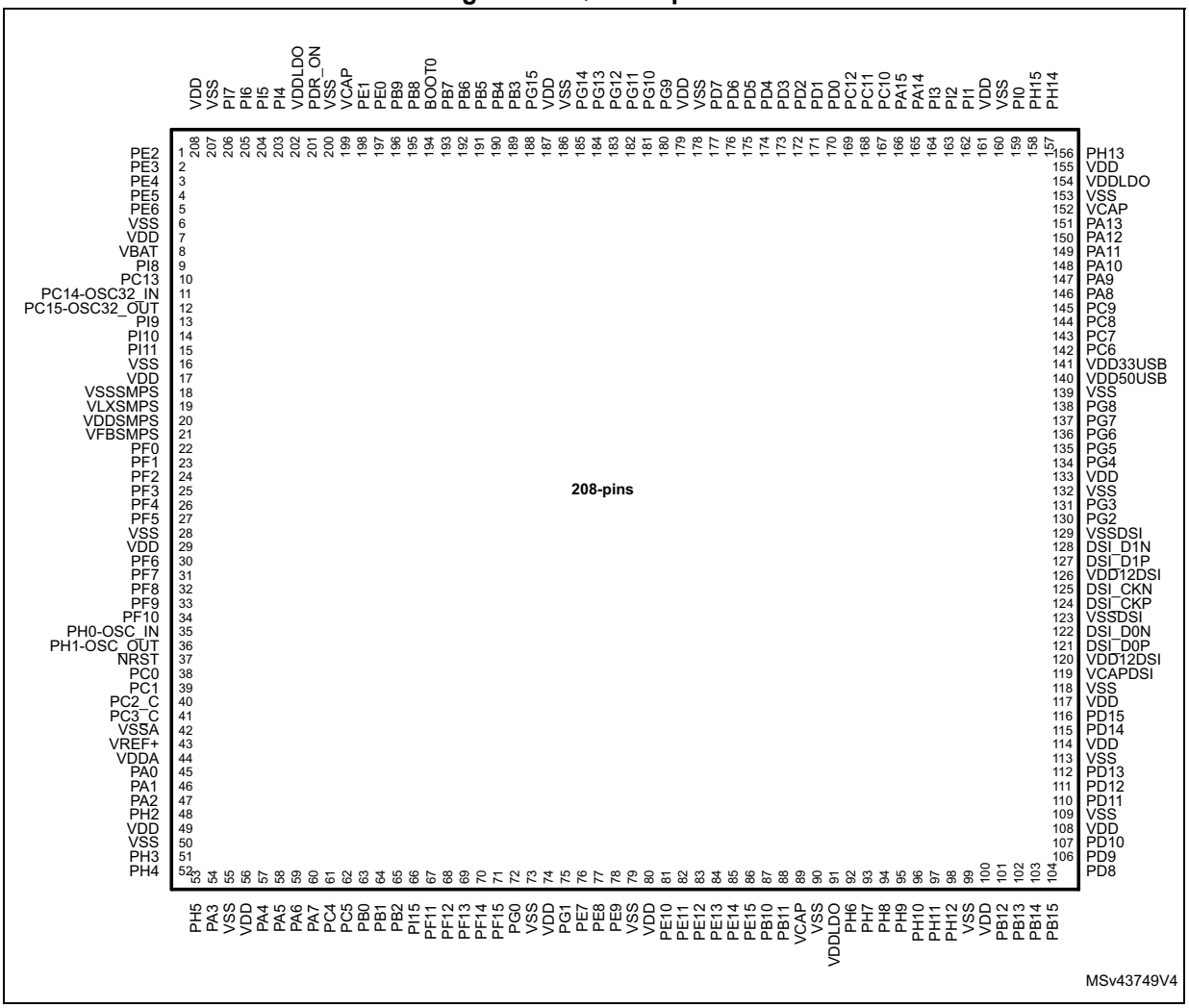
1. The above figure shows the package top view.

**Figure 8. LQFP176 pinout**



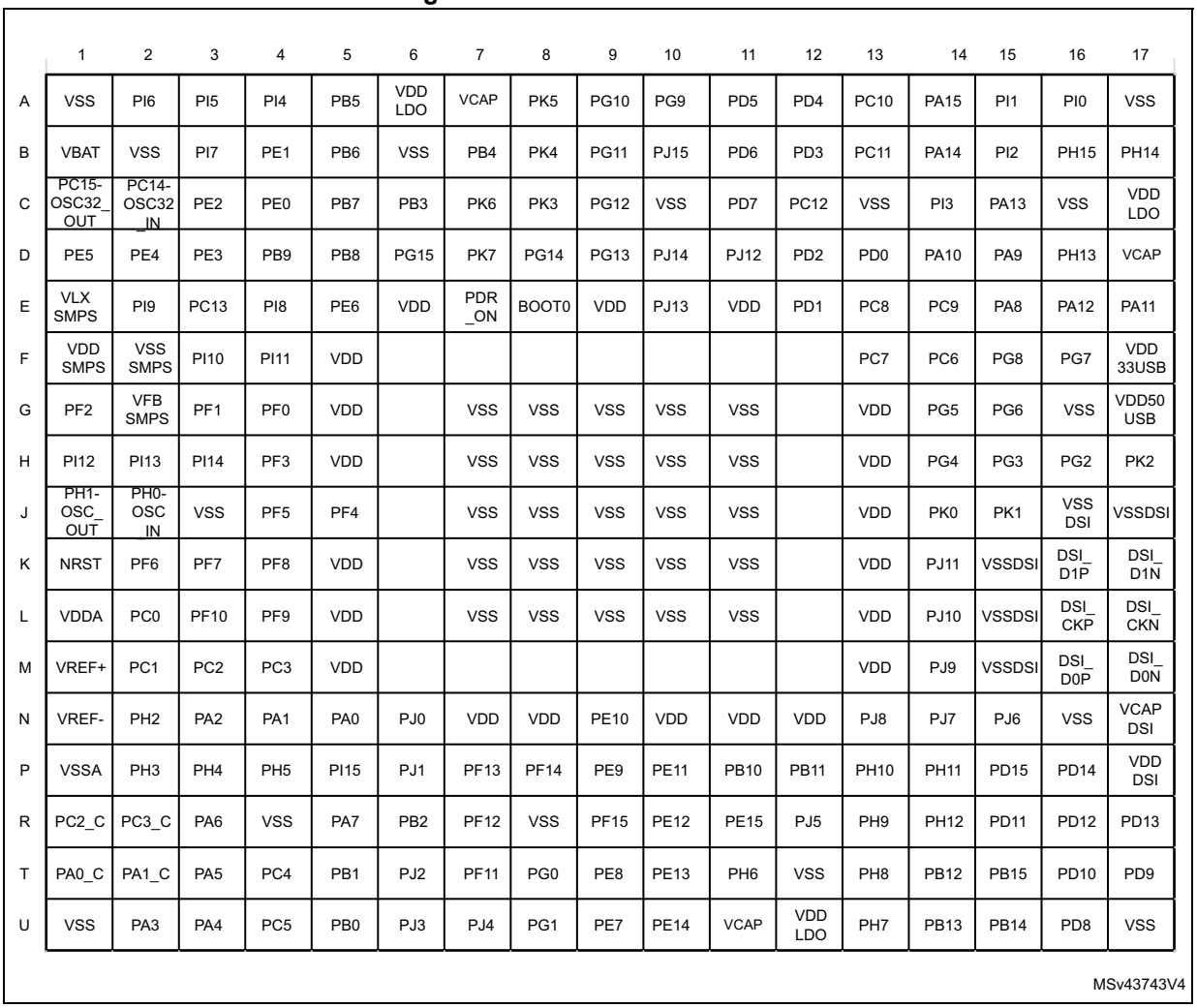

1. The above figure shows the package top view.

**Figure 9. LQFP208 pinout**




1. The above figure shows the package top view.

**Figure 10. TFBGA240+25 ballout**



| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS | PI6 | PI5 | PI4 | PB5 | VDD LDO | VCAP | PK5 | PG10 | PG9 | PD5 | PD4 | PC10 | PA15 | PI1 | PI0 | VSS |
| B | VBAT | VSS | PI7 | PE1 | PB6 | VSS | PB4 | PK4 | PG11 | PJ15 | PD6 | PD3 | PC11 | PA14 | PI2 | PH15 | PH14 |
| C | PC15-OSC32_OUT | PC14-OSC32_IN | PE2 | PE0 | PB7 | PB3 | PK6 | PK3 | PG12 | VSS | PD7 | PC12 | VSS | PI3 | PA13 | VSS | VDD LDO |
| D | PE5 | PE4 | PE3 | PB9 | PB8 | PG15 | PK7 | PG14 | PG13 | PJ14 | PJ12 | PD2 | PD0 | PA10 | PA9 | PH13 | VCAP |
| E | VLX SMPS | PI9 | PC13 | PI8 | PE6 | VDD | PDR_ON | BOOT0 | VDD | PJ13 | VDD | PD1 | PC8 | PC9 | PA8 | PA12 | PA11 |
| F | VDD SMPS | VSS SMPS | PI10 | PI11 | VDD | | | | | | | | PC7 | PC6 | PG8 | PG7 | VDD 33USB |
| G | PF2 | VFB SMPS | PF1 | PF0 | VDD | | VSS | VSS | VSS | VSS | VSS | | VDD | PG5 | PG6 | VSS | VDD50 USB |
| H | PI12 | PI13 | PI14 | PF3 | VDD | | VSS | VSS | VSS | VSS | VSS | | VDD | PG4 | PG3 | PG2 | PK2 |
| J | PH1-OSC_OUT | PH0-OSC_IN | VSS | PF5 | PF4 | | VSS | VSS | VSS | VSS | VSS | | VDD | PK0 | PK1 | VSS DSI | VSSDSI |
| K | NRST | PF6 | PF7 | PF8 | VDD | | VSS | VSS | VSS | VSS | VSS | | VDD | PJ11 | VSSDSI | DSI_D1P | DSI_D1N |
| L | VDDA | PC0 | PF10 | PF9 | VDD | | VSS | VSS | VSS | VSS | VSS | | VDD | PJ10 | VSSDSI | DSI_CKP | DSI_CKN |
| M | VREF+ | PC1 | PC2 | PC3 | VDD | | | | | | | | VDD | PJ9 | VSSDSI | DSI_D0P | DSI_D0N |
| N | VREF- | PH2 | PA2 | PA1 | PA0 | PJ0 | VDD | VDD | PE10 | VDD | VDD | VDD | PJ8 | PJ7 | PJ6 | VSS | VCAP DSI |
| P | VSSA | PH3 | PH4 | PH5 | PI15 | PJ1 | PF13 | PF14 | PE9 | PE11 | PB10 | PB11 | PH10 | PH11 | PD15 | PD14 | VDD DSI |
| R | PC2_C | PC3_C | PA6 | VSS | PA7 | PB2 | PF12 | VSS | PF15 | PE12 | PE15 | PJ5 | PH9 | PH12 | PD11 | PD12 | PD13 |
| T | PA0_C | PA1_C | PA5 | PC4 | PB1 | PJ2 | PF11 | PG0 | PE8 | PE13 | PH6 | VSS | PH8 | PB12 | PB15 | PD10 | PD9 |
| U | VSS | PA3 | PA4 | PC5 | PB0 | PJ3 | PJ4 | PG1 | PE7 | PE14 | VCAP | VDD LDO | PH7 | PB13 | PB14 | PD8 | VSS |

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1. The above figure shows the package top view.

**Table 6. Legend/abbreviations used in the pinout table**

| Name | | Abbreviation | Definition |
|---|---|---|---|
| Pin name | | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | | S | Supply pin |
| | | I | Input only pin |
| | | I/O | Input / output pin |
| | | ANA | Analog-only Input |
| I/O structure | | FT | 5 V tolerant I/O |
| | | TT | 3.3 V tolerant I/O |
| | | B | Dedicated BOOT0 pin |
| | | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| | | **Option for TT and FT I/Os** | |
| | | _f | I2C FM+ option |
| | | _a | analog option (supplied by $V_{DDA}$) |
| | | _u | USB option (supplied by $V_{DD33USB}$) |
| | | _h | High-speed low-voltage I/O |
| Notes | | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset. | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers | |
| | Additional functions | Functions directly selected/enabled through peripheral registers | |

**Table 7. STM32H747xI/G pin/ball definition**

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| D9 | A2 | 1 | 1 | C3 | PE2 | I/O | FT_h | - | TRACECLK, SAI1_CK1, SPI4_SCK, SAI1_MCLK_A, SAI4_MCLK_A, QUADSPI_BK1_IO2, SAI4_CK1, ETH_MII_TXD3, FMC_A23, EVENTOUT | - |
| D10 | C3 | 2 | 2 | D3 | PE3 | I/O | FT_h | - | TRACED0, TIM15_BKIN, SAI1_SD_B, SAI4_SD_B, FMC_A19, EVENTOUT | - |
| B12 | D3 | 3 | 3 | D2 | PE4 | I/O | FT_h | - | TRACED1, SAI1_D2, DFSDM1_DATIN3, TIM15_CH1N, SPI4_NSS, SAI1_FS_A, SAI4_FS_A, SAI4_D2, FMC_A20, DCMI_D4, LCD_B0, EVENTOUT | - |
| C11 | E4 | 4 | 4 | D1 | PE5 | I/O | FT_h | - | TRACED2, SAI1_CK2, DFSDM1_CKIN3, TIM15_CH1, SPI4_MISO, SAI1_SCK_A, SAI4_SCK_A, SAI4_CK2, FMC_A21, DCMI_D6, LCD_G0, EVENTOUT | - |
| E8 | C2 | 5 | 5 | E5 | PE6 | I/O | FT_h | - | TRACED3, TIM1_BKIN2, SAI1_D1, TIM15_CH2, SPI4_MOSI, SAI1_SD_A, SAI4_SD_A, SAI4_D1, SAI2_MCLK_B, TIM1_BKIN2_COMP12, FMC_A22, DCMI_D7, LCD_G1, EVENTOUT | - |
| - | A1 | 6 | 6 | A1 | VSS | S | - | - | - | - |
| - | A9 | 7 | 7 | - | VDD | S | - | - | - | - |
| B13 | B1 | 8 | 8 | B1 | VBAT | S | - | - | - | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| D11 | - | - | - | B2 | VSS | S | - | - | - | - |
| - | - | - | 9 | E4 | PI8 | I/O | FT | - | EVENTOUT | RTC_TAMP2/ WKUP3 |
| E9 | E3 | 9 | 10 | E3 | PC13 | I/O | FT | - | EVENTOUT | RTC_TAMP1/ RTC_TS/WKUP2 |
| C13 | C1 | 10 | 11 | C2 | PC14-OSC32_IN (OSC32_IN)(1) | I/O | FT | - | EVENTOUT | OSC32_IN |
| C12 | D2 | 11 | 12 | C1 | PC15-OSC32_OUT( OSC32_OUT) (1) | I/O | FT | - | EVENTOUT | OSC32_OUT |
| - | - | - | 13 | E2 | PI9 | I/O | FT_h | - | UART4_RX, FDCAN1_RX, FMC_D30, LCD_VSYNC, EVENTOUT | - |
| - | - | - | 14 | F3 | PI10 | I/O | FT_h | - | FDCAN1_RXFD_MODE, ETH_MII_RX_ER, FMC_D31, LCD_HSYNC, EVENTOUT | - |
| - | - | - | 15 | F4 | PI11 | I/O | FT | - | LCD_G6, OTG_HS_ULPI_DIR, EVENTOUT | WKUP4 |
| - | B4 | 12 | 16 | A17 | VSS | S | - | - | - | - |
| D13 | E2 | 13 | 17 | E6 | VDD | S | - | - | - | - |
| D12 | F2 | 14 | 18 | F2 | VSSSMPS | S | - | - | - | - |
| E12 | E1 | 15 | 19 | E1 | VLXSMPS | S | - | - | - | - |
| E13 | F1 | 16 | 20 | F1 | VDDSMPS | S | - | - | - | - |
| E11 | F3 | 17 | 21 | G2 | VFBSMPS | S | - | - | - | - |
| E10 | F4 | 18 | 22 | G4 | PF0 | I/O | FT_f | - | I2C2_SDA, FMC_A0, EVENTOUT | - |
| F9 | F5 | 19 | 23 | G3 | PF1 | I/O | FT_f | - | I2C2_SCL, FMC_A1, EVENTOUT | - |
| F12 | F6 | 20 | 24 | G1 | PF2 | I/O | FT | - | I2C2_SMBA, FMC_A2, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| - | - | - | - | H1 | PI12 | I/O | FT | - | LCD_HSYNC, EVENTOUT | - |
| - | - | - | - | H2 | PI13 | I/O | FT | - | LCD_VSYNC, EVENTOUT | - |
| - | - | - | - | H3 | PI14 | I/O | FT_h | - | LCD_CLK, EVENTOUT | - |
| F13 | G2 | 21 | 25 | H4 | PF3 | I/O | FT_ha | - | FMC_A3, EVENTOUT | ADC3_INP5 |
| F11 | G1 | 22 | 26 | J5 | PF4 | I/O | FT_ha | - | FMC_A4, EVENTOUT | ADC3_INN5, ADC3_INP9 |
| F10 | G3 | 23 | 27 | J4 | PF5 | I/O | FT_ha | - | FMC_A5, EVENTOUT | ADC3_INP4 |
| G12 | - | 24 | 28 | C10 | VSS | S | | - | - | - |
| G13 | H1 | 25 | 29 | E9 | VDD | S | | - | - | - |
| - | G4 | 26 | 30 | K2 | PF6 | I/O | FT_ha | - | TIM16_CH1, SPI5_NSS, SAI1_SD_B, UART7_RX, SAI4_SD_B, QUADSPI_BK1_IO3, EVENTOUT | ADC3_INN4, ADC3_INP8 |
| - | G5 | 27 | 31 | K3 | PF7 | I/O | FT_ha | - | TIM17_CH1, SPI5_SCK, SAI1_MCLK_B, UART7_TX, SAI4_MCLK_B, QUADSPI_BK1_IO2, EVENTOUT | ADC3_INP3 |
| - | G6 | 28 | 32 | K4 | PF8 | I/O | FT_ha | - | TIM16_CH1N, SPI5_MISO, SAI1_SCK_B, UART7_RTS/UART7_DE, SAI4_SCK_B, TIM13_CH1, QUADSPI_BK1_IO0, EVENTOUT | ADC3_INN3, ADC3_INP7 |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| - | H3 | 29 | 33 | L4 | PF9 | I/O | FT_ha | - | TIM17_CH1N, SPI5_MOSI, SAI1_FS_B, UART7_CTS, SAI4_FS_B, TIM14_CH1, QUADSPI_BK1_IO1, EVENTOUT | ADC3_INP2 |
| - | H4 | 30 | 34 | L3 | PF10 | I/O | FT_ha | - | TIM16_BKIN, SAI1_D3, QUADSPI_CLK, SAI4_D3, DCMI_D11, LCD_DE, EVENTOUT | ADC3_INN2, ADC3_INP6 |
| H12 | J2 | 31 | 35 | J2 | PH0-OSC_IN(PH0) | I/O | FT | - | EVENTOUT | OSC_IN |
| H13 | J1 | 32 | 36 | J1 | PH1-OSC_OUT(PH1) | I/O | FT | - | EVENTOUT | OSC_OUT |
| H11 | H5 | 33 | 37 | K1 | NRST | I/O | RST | - | - | - |
| G11 | J4 | 34 | 38 | L2 | PC0 | I/O | FT_a | - | DFSDM1_CKIN0, DFSDM1_DATIN4, SAI2_FS_B, OTG_HS_ULPI_STP, FMC_SDNWE, LCD_R5, EVENTOUT | ADC123_INP10 |
| G10 | J3 | 35 | 39 | M2 | PC1 | I/O | FT_ha | - | TRACED0, SAI1_D1, DFSDM1_DATIN0, DFSDM1_CKIN4, SPI2_MOSI/I2S2_SDO, SAI1_SD_A, SAI4_SD_A, SDMMC2_CK, SAI4_D1, ETH_MDC, MDIOS_MDC, EVENTOUT | ADC123_INN10, ADC123_INP11, RTC_TAMP3/WKUP5 |
| - | - | - | - | M3(2) | PC2 | I/O | FT_a | - | C1DSLEEP, DFSDM1_CKIN1, SPI2_MISO/I2S2_SDI, DFSDM1_CKOUT, OTG_HS_ULPI_DIR, ETH_MII_TXD2, FMC_SDNE0, EVENTOUT | ADC123_INN11, ADC123_INP12 |
| K13(3) | K1(3) | 36(3) | 40(3) | R1(1) | PC2_C | ANA | TT_a | - | | ADC3_INN1, ADC3_INP0 |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| - | - | - | - | M4(1) | PC3 | I/O | FT_a | - | C1SLEEP, DFSDM1_DATIN1, SPI2_MOSI/I2S2_SDO, OTG_HS_ULPI_NXT, ETH_MII_TX_CLK, FMC_SDCKE0, EVENTOUT | ADC12_INN12, ADC12_INP13 |
| K12(3) | K2(3) | 37(3) | 41(3) | R2(1) | PC3_C | ANA | TT_a | - | | ADC3_INP1 |
| - | M2 | - | - | E11 | VDD | S | - | - | - | - |
| - | C12 | - | - | C13 | VSS | S | - | - | - | - |
| J13 | - | 38 | 42 | P1 | VSSA | S | - | - | - | - |
| - | L1 | - | - | N1 | VREF- | S | - | - | - | - |
| J12 | M1 | 39 | 43 | M1 | VREF+ | S | - | - | - | - |
| J11 | L2 | 40 | 44 | L1 | VDDA | S | - | - | - | - |
| L13 | K3 | 41 | 45 | N5(1) | PA0 | I/O | FT_a | - | TIM2_CH1/TIM2_ETR, TIM5_CH1, TIM8_ETR, TIM15_BKIN, USART2_CTS/USART2_NSS, UART4_TX, SDMMC2_CMD, SAI2_SD_B, ETH_MII_CRS, EVENTOUT | ADC1_INP16, WKUP0 |
| - | - | - | - | T1(1) | PA0_C | ANA | TT_a | - | | ADC12_INN1, ADC12_INP0 |
| L12 | L3 | 42 | 46 | N4(1) | PA1 | I/O | FT_ha | - | TIM2_CH2, TIM5_CH2, LPTIM3_OUT, TIM15_CH1N, USART2_RTS/USART2_DE, UART4_RX, QUADSPI_BK1_IO3, SAI2_MCLK_B, ETH_MII_RX_CLK/ETH_RMII_REF_CLK, LCD_R2, EVENTOUT | ADC1_INN16, ADC1_INP17 |
| - | - | - | - | T2(1) | PA1_C | ANA | TT_a | - | | ADC12_INP1 |
| K11 | M3 | 43 | 47 | N3 | PA2 | I/O | FT_a | - | TIM2_CH3, TIM5_CH3, LPTIM4_OUT, TIM15_CH1, USART2_TX, SAI2_SCK_B, ETH_MDIO, MDIOS_MDIO, LCD_R1, EVENTOUT | ADC12_INP14, WKUP1 |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| - | - | - | 48 | N2 | PH2 | I/O | FT_ha | - | LPTIM1_IN2, QUADSPI_BK2_IO0, SAI2_SCK_B, ETH_MII_CRS, FMC_SDCKE0, LCD_R0, EVENTOUT | ADC3_INP13 |
| - | - | 44 | 49 | F5 | VDD | S | - | - | - | - |
| - | N1 | 45 | 50 | C16 | VSS | S | - | - | - | - |
| - | - | - | 51 | P2 | PH3 | I/O | FT_ha | - | QUADSPI_BK2_IO1, SAI2_MCLK_B, ETH_MII_COL, FMC_SDNE0, LCD_R1, EVENTOUT | ADC3_INN13, ADC3_INP14 |
| - | - | - | 52 | P3 | PH4 | I/O | FT_fa | - | I2C2_SCL, LCD_G5, OTG_HS_ULPI_NXT, LCD_G4, EVENTOUT | ADC3_INN14, ADC3_INP15 |
| - | - | - | 53 | P4 | PH5 | I/O | FT_fa | - | I2C2_SDA, SPI5_NSS, FMC_SDNWE, EVENTOUT | ADC3_INN15, ADC3_INP16 |
| J10 | N2 | 46 | 54 | U2 | PA3 | I/O | FT_ha | - | TIM2_CH4, TIM5_CH4, LPTIM5_OUT, TIM15_CH2, USART2_RX, LCD_B2, OTG_HS_ULPI_D0, ETH_MII_COL, LCD_B5, EVENTOUT | ADC12_INP15 |
| L11 | - | 47 | 55 | - | VSS | S | - | - | - | - |
| M12 | - | 48 | 56 | G5 | VDD | S | - | - | - | - |
| K10 | N3 | 49 | 57 | U3 | PA4 | I/O | TT_a | - | D1PWREN, TIM5_ETR, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, USART2_CK, SPI6_NSS, OTG_HS_SOF, DCMI_HSYNC, LCD_VSYNC, EVENTOUT | ADC12_INP18, DAC1_OUT1 |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| H10 | J5 | 50 | 58 | T3 | PA5 | I/O | TT_ha | - | D2PWREN, TIM2_CH1/TIM2_ETR, TIM8_CH1N, SPI1_SCK/I2S1_CK, SPI6_SCK, OTG_HS_ULPI_CK, LCD_R4, EVENTOUT | ADC12_INN18, ADC12_INP19, DAC1_OUT2 |
| G9 | M4 | 51 | 59 | R3 | PA6 | I/O | FT_a | - | TIM1_BKIN, TIM3_CH1, TIM8_BKIN, SPI1_MISO/I2S1_SDI, SPI6_MISO, TIM13_CH1, TIM8_BKIN_COMP12, MDIOS_MDC, TIM1_BKIN_COMP12, DCMI_PIXCLK, LCD_G2, EVENTOUT | ADC12_INP3 |
| J9 | K4 | 52 | 60 | R5 | PA7 | I/O | TT_a | - | TIM1_CH1N, TIM3_CH2, TIM8_CH1N, SPI1_MOSI/I2S1_SDO, SPI6_MOSI, TIM14_CH1, ETH_MII_RX_DV/ETH_RMII_CRS_DV, FMC_SDNWE, EVENTOUT | ADC12_INN3, ADC12_INP7, OPAMP1_VINM |
| M11 | L4 | 53 | 61 | T4 | PC4 | I/O | TT_a | - | C2DSLEEP, DFSDM1_CKIN2, I2S1_MCK, SPDIFRX1_IN3, ETH_MII_RXD0/ETH_RMII_RXD0, FMC_SDNE0, EVENTOUT | ADC12_INP4, OPAMP1_VOUT, COMP1_INM |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| L10 | K5 | 54 | 62 | U4 | PC5 | I/O | TT_a | - | C2SLEEP, SAI1_D3, DFSDM1_DATIN2, SPDIFRX1_IN4, SAI4_D3, ETH_MII_RXD1/ETH_RMII_RXD1, FMC_SDCKE0, COMP1_OUT, EVENTOUT | ADC12_INN4, ADC12_INP8, OPAMP1_VINM |
| - | - | - | - | G13 | VDD | S | - | - | - | - |
| - | H2 | - | - | R4 | VSS | S | - | - | - | - |
| K9 | N4 | 55 | 63 | U5 | PB0 | I/O | FT_a | - | TIM1_CH2N, TIM3_CH3, TIM8_CH2N, DFSDM1_CKOUT, UART4_CTS, LCD_R3, OTG_HS_ULPI_D1, ETH_MII_RXD2, LCD_G1, EVENTOUT | ADC12_INN5, ADC12_INP9, OPAMP1_VINP, COMP1_INP |
| H9 | H6 | 56 | 64 | T5 | PB1 | I/O | TT_u | - | TIM1_CH3N, TIM3_CH4, TIM8_CH3N, DFSDM1_DATIN1, LCD_R6, OTG_HS_ULPI_D2, ETH_MII_RXD3, LCD_G0, EVENTOUT | ADC12_INP5, COMP1_INM |
| M10 | L5 | 57 | 65 | R6 | PB2 | I/O | FT_ha | - | RTC_OUT, SAI1_D1, DFSDM1_CKIN1, SAI1_SD_A, SPI3_MOSI/I2S3_SDO, SAI4_SD_A, QUADSPI_CLK, SAI4_D1, EVENTOUT | COMP1_INP |
| - | - | - | 66 | P5 | PI15 | I/O | FT | - | LCD_G2, LCD_R0, EVENTOUT | - |
| - | - | - | - | N6 | PJ0 | I/O | FT | - | LCD_R7, LCD_R1, EVENTOUT | - |
| - | - | - | - | P6 | PJ1 | I/O | FT | - | LCD_R2, EVENTOUT | - |
| - | - | - | - | T6 | PJ2 | I/O | FT | - | DSI_TE, LCD_R3, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| - | - | - | - | U6 | PJ3 | I/O | FT | - | LCD_R4, EVENTOUT | - |
| - | - | - | - | U7 | PJ4 | I/O | FT | - | LCD_R5, EVENTOUT | - |
| F8 | K6 | 58 | 67 | T7 | PF11 | I/O | FT_a | - | SPI5_MOSI, SAI2_SD_B, FMC_SDNRAS, DCMI_D12, EVENTOUT | ADC1_INP2 |
| G8 | J6 | 59 | 68 | R7 | PF12 | I/O | FT_ha | - | FMC_A6, EVENTOUT | ADC1_INN2, ADC1_INP6 |
| L9 | - | - | - | J3 | VSS | S | | - | - | - |
| M9 | - | - | - | H5 | VDD | S | | - | - | - |
| H8 | M5 | 60 | 69 | P7 | PF13 | I/O | FT_ha | - | DFSDM1_DATIN6, I2C4_SMBA, FMC_A7, EVENTOUT | ADC2_INP2 |
| K8 | N5 | 61 | 70 | P8 | PF14 | I/O | FT_fha | - | DFSDM1_CKIN6, I2C4_SCL, FMC_A8, EVENTOUT | ADC2_INN2, ADC2_INP6 |
| J8 | M7 | 62 | 71 | R9 | PF15 | I/O | FT_fh | - | I2C4_SDA, FMC_A9, EVENTOUT | - |
| L8 | L6 | 63 | 72 | T8 | PG0 | I/O | FT_h | - | FMC_A10, EVENTOUT | - |
| - | M9 | 64 | 73 | J16 | VSS | S | | - | - | - |
| - | - | 65 | 74 | H13 | VDD | S | | - | - | - |
| M8 | J7 | 66 | 75 | U8 | PG1 | I/O | TT_h | - | FMC_A11, EVENTOUT | OPAMP2_VINM |
| H7 | K7 | 67 | 76 | U9 | PE7 | I/O | TT_ha | - | TIM1_ETR, DFSDM1_DATIN2, UART7_RX, QUADSPI_BK2_IO0, FMC_D4/FMC_DA4, EVENTOUT | OPAMP2_VOUT, COMP2_INM |
| J7 | L8 | 68 | 77 | T9 | PE8 | I/O | TT_ha | - | TIM1_CH1N, DFSDM1_CKIN2, UART7_TX, QUADSPI_BK2_IO1, FMC_D5/FMC_DA5, COMP2_OUT, EVENTOUT | OPAMP2_VINM |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| K7 | N6 | 69 | 78 | P9 | PE9 | I/O | TT_ha | - | TIM1_CH1, DFSDM1_CKOUT, UART7_RTS/UART7_DE, QUADSPI_BK2_IO2, FMC_D6/FMC_DA6, EVENTOUT | OPAMP2_VINP, COMP2_INP |
| L7 | M6 | 70 | 79 | J17 | VSS | S | - | - | - | - |
| M7 | - | 71 | 80 | J13 | VDD | S | - | - | - | - |
| G7 | L7 | 72 | 81 | N9 | PE10 | I/O | FT_ha | - | TIM1_CH2N, DFSDM1_DATIN4, UART7_CTS, QUADSPI_BK2_IO3, FMC_D7/FMC_DA7, EVENTOUT | COMP2_INM |
| G6 | N7 | 73 | 82 | P10 | PE11 | I/O | FT_ha | - | TIM1_CH2, DFSDM1_CKIN4, SPI4_NSS, SAI2_SD_B, FMC_D8/FMC_DA8, LCD_G3, EVENTOUT | COMP2_INP |
| J6 | J8 | 74 | 83 | R10 | PE12 | I/O | FT_h | - | TIM1_CH3N, DFSDM1_DATIN5, SPI4_SCK, SAI2_SCK_B, FMC_D9/FMC_DA9, COMP1_OUT, LCD_B4, EVENTOUT | - |
| K6 | H8 | 75 | 84 | T10 | PE13 | I/O | FT_h | - | TIM1_CH3, DFSDM1_CKIN5, SPI4_MISO, SAI2_FS_B, FMC_D10/FMC_DA10, COMP2_OUT, LCD_DE, EVENTOUT | - |
| - | H2 | - | - | T12 | VSS | S | - | - | - | - |
| - | - | - | - | K13 | VDD | S | | - | - | - |
| M6 | M8 | 76 | 85 | U10 | PE14 | I/O | FT_h | - | TIM1_CH4, SPI4_MOSI, SAI2_MCLK_B, FMC_D11/FMC_DA11, LCD_CLK, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| L6 | K8 | 77 | 86 | R11 | PE15 | I/O | FT_h | - | TIM1_BKIN, COMP_TIM1_BKIN, FMC_D12/FMC_DA12, TIM1_BKIN_COMP12, LCD_R7, EVENTOUT | - |
| H6 | K9 | 78 | 87 | P11 | PB10 | I/O | FT_f | - | TIM2_CH3, HRTIM_SCOUT, LPTIM2_IN1, I2C2_SCL, SPI2_SCK/I2S2_CK, DFSDM1_DATIN7, USART3_TX, QUADSPI_BK1_NCS, OTG_HS_ULPI_D3, ETH_MII_RX_ER, LCD_G4, EVENTOUT | - |
| K5 | N8 | 79 | 88 | P12 | PB11 | I/O | FT_f | - | TIM2_CH4, HRTIM_SCIN, LPTIM2_ETR, I2C2_SDA, DFSDM1_CKIN7, USART3_RX, OTG_HS_ULPI_D4, ETH_MII_TX_EN/ETH_RMII_TX_EN, DSI_TE, LCD_G5, EVENTOUT | - |
| M5 | N9 | 80 | 89 | U11 | VCAP | S | - | - | - | - |
| L5 | - | 81 | 90 | - | VSS | S | - | - | - | - |
| L4 | N10 | 82 | 91 | U12 | VDDLDO | S | - | - | - | - |
| M4 | - | - | - | L13 | VDD | S | - | - | - | - |
| - | - | - | - | R12 | PJ5 | I/O | FT | - | LCD_R6, EVENTOUT | - |
| - | - | - | 92 | T11 | PH6 | I/O | FT | - | TIM12_CH1, I2C2_SMBA, SPI5_SCK, ETH_MII_RXD2, FMC_SDNE1, DCMI_D8, EVENTOUT | - |
| - | - | - | 93 | U13 | PH7 | I/O | FT_fa | - | I2C3_SCL, SPI5_MISO, ETH_MII_RXD3, FMC_SDCKE1, DCMI_D9, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| - | - | - | 94 | T13 | PH8 | I/O | FT_fha | - | TIM5_ETR, I2C3_SDA, FMC_D16, DCMI_HSYNC, LCD_R2, EVENTOUT | - |
| - | E13 | - | - | - | VSS | S | - | - | - | - |
| M4 | L9 | - | - | M13 | VDD | S | - | - | - | - |
| - | - | - | 95 | R13 | PH9 | I/O | FT_h | - | TIM12_CH2, I2C3_SMBA, FMC_D17, DCMI_D0, LCD_R3, EVENTOUT | - |
| - | - | - | 96 | P13 | PH10 | I/O | FT_h | - | TIM5_CH1, I2C4_SMBA, FMC_D18, DCMI_D1, LCD_R4, EVENTOUT | - |
| - | - | - | 97 | P14 | PH11 | I/O | FT_fh | - | TIM5_CH2, I2C4_SCL, FMC_D19, DCMI_D2, LCD_R5, EVENTOUT | - |
| - | - | - | 98 | R14 | PH12 | I/O | FT_fh | - | TIM5_CH3, I2C4_SDA, FMC_D20, DCMI_D3, LCD_R6, EVENTOUT | - |
| - | D1 | 83 | 99 | N16 | VSS | S | - | - | - | - |
| M4 | - | 84 | 100 | - | VDD | S | - | - | - | - |
| J5 | L10 | 85 | 101 | T14 | PB12 | I/O | FT_u | - | TIM1_BKIN, I2C2_SMBA, SPI2_NSS/I2S2_WS, DFSDM1_DATIN1, USART3_CK, FDCAN2_RX, OTG_HS_ULPI_D5, ETH_MII_TXD0/ETH_RMII_TXD0, OTG_HS_ID, TIM1_BKIN_COMP12, UART5_RX, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| H5 | M10 | 86 | 102 | U14 | PB13 | I/O | FT_u | - | TIM1_CH1N, LPTIM2_OUT, SPI2_SCK/I2S2_CK, DFSDM1_CKIN1, USART3_CTS/USART3_NSS, FDCAN2_TX, OTG_HS_ULPI_D6, ETH_MII_TXD1/ETH_RMII_TXD1, UART5_TX, EVENTOUT | OTG_HS_VBUS |
| M3 | N11 | 87 | 103 | U15 | PB14 | I/O | FT_u | - | TIM1_CH2N, TIM12_CH1, TIM8_CH2N, USART1_TX, SPI2_MISO/I2S2_SDI, DFSDM1_DATIN2, USART3_RTS/USART3_DE, UART4_RTS/UART4_DE, SDMMC2_D0, OTG_HS_DM, EVENTOUT | - |
| M2 | M11 | 88 | 104 | T15 | PB15 | I/O | FT_u | - | RTC_REFIN, TIM1_CH3N, TIM12_CH2, TIM8_CH3N, USART1_RX, SPI2_MOSI/I2S2_SDO, DFSDM1_CKIN2, UART4_CTS, SDMMC2_D1, OTG_HS_DP, EVENTOUT | - |
| G5 | N12 | 89 | 105 | U16 | PD8 | I/O | FT_h | - | DFSDM1_CKIN3, SAI3_SCK_B, USART3_TX, SPDIFRX1_IN2, FMC_D13/FMC_DA13, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| K4 | M12 | 90 | 106 | T17 | PD9 | I/O | FT_h | - | DFSDM1_DATIN3, SAI3_SD_B, USART3_RX, FDCAN2_RXFD_MODE, FMC_D14/FMC_DA14, EVENTOUT | - |
| L3 | N13 | 91 | 107 | T16 | PD10 | I/O | FT_h | - | DFSDM1_CKOUT, SAI3_FS_B, USART3_CK, FDCAN2_TXFD_MODE, FMC_D15/FMC_DA15, LCD_B3, EVENTOUT | |
| - | L11 | 92 | 108 | N12 | VDD | S | - | - | - | - |
| M1 | L13 | 93 | 109 | U17 | VSS | S | - | - | - | - |
| J4 | K10 | 94 | 110 | R15 | PD11 | I/O | FT_h | - | LPTIM2_IN2, I2C4_SMBA, USART3_CTS/USART3_NSS, QUADSPI_BK1_IO0, SAI2_SD_A, FMC_A16, EVENTOUT | - |
| L2 | J10 | 95 | 111 | R16 | PD12 | I/O | FT_fh | - | LPTIM1_IN1, TIM4_CH1, LPTIM2_IN1, I2C4_SCL, USART3_RTS/ USART3_DE, QUADSPI_BK1_IO1, SAI2_FS_A, FMC_A17, EVENTOUT | - |
| K3 | J9 | 96 | 112 | R17 | PD13 | I/O | FT_fh | - | LPTIM1_OUT, TIM4_CH2, I2C4_SDA, QUADSPI_BK1_IO3, SAI2_SCK_A, FMC_A18, EVENTOUT | - |
| L1 | - | - | 113 | - | VSS | S | - | - | - | - |
| - | - | - | 114 | N11 | VDD | S | - | - | - | - |
| H4 | H9 | 97 | 115 | P16 | PD14 | I/O | FT_h | - | TIM4_CH3, SAI3_MCLK_B, UART8_CTS, FMC_D0/FMC_DA0, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| J3 | H10 | 98 | 116 | P15 | PD15 | I/O | FT_h | - | TIM4_CH4, SAI3_MCLK_A, UART8_RTS/ UART8_DE, FMC_D1/FMC_DA1, EVENTOUT | - |
| - | - | - | - | N15 | PJ6 | I/O | FT | - | TIM8_CH2, LCD_R7, EVENTOUT | - |
| - | - | - | - | N14 | PJ7 | I/O | FT | - | TRGIN, TIM8_CH2N, LCD_G0, EVENTOUT | - |
| K2 | - | - | - | N10 | VDD | S | - | - | - | - |
| - | C12 | - | - | R8 | VSS | S | - | - | - | - |
| - | - | - | - | N13 | PJ8 | I/O | FT | - | TIM1_CH3N, TIM8_CH1, UART8_TX, LCD_G1, EVENTOUT | - |
| - | - | - | - | M14 | PJ9 | I/O | FT | - | TIM1_CH3, TIM8_CH1N, UART8_RX, LCD_G2, EVENTOUT | - |
| - | - | - | - | L14 | PJ10 | I/O | FT | - | TIM1_CH2N, TIM8_CH2, SPI5_MOSI, LCD_G3, EVENTOUT | - |
| - | - | - | - | K14 | PJ11 | I/O | FT | - | TIM1_CH2, TIM8_CH2N, SPI5_MISO, LCD_G4, EVENTOUT | - |
| - | - | 99 | 117 | N8 | VDD | S | | - | - | - |
| - | M13 | - | - | P17 | VDDDSI | S | | - | - | - |
| - | - | 100 | 118 | U1 | VSS | S | | - | - | - |
| K1 | L12 | 101 | 119 | N17 | VCAPDSI | S | | - | - | - |
| - | - | 102 | 120 | - | VDD12DSI | S | | - | - | - |
| J2 | K12 | 103 | 121 | M16 | DSI_D0P | I/O | TT | - | - | - |
| J1 | K13 | 104 | 122 | M17 | DSI_D0N | I/O | TT | - | - | - |
| H3 | G12 | 105 | 123 | K15 | VSSDSI | S | | - | - | - |
| H2 | J12 | 106 | 124 | L16 | DSI_CKP | I/O | TT | - | - | - |
| H1 | J13 | 107 | 125 | L17 | DSI_CKN | I/O | TT | - | - | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| - | - | 108 | 126 | - | VDD12DSI | S | - | - | - | - |
| G2 | H12 | - | 127 | K16 | DSI_D1P | I/O | TT | - | - | - |
| G1 | H13 | - | 128 | K17 | DSI_D1N | I/O | TT | - | - | - |
| - | G13 | 109 | 129 | L15 | VSSDSI | S | - | - | - | - |
| - | - | - | - | J14 | PK0 | I/O | FT | - | TIM1_CH1N, TIM8_CH3, SPI5_SCK, LCD_G5, EVENTOUT | - |
| - | - | - | - | J15 | PK1 | I/O | FT | - | TIM1_CH1, TIM8_CH3N, SPI5_NSS, LCD_G6, EVENTOUT | - |
| - | - | - | - | H17 | PK2 | I/O | FT | - | TIM1_BKIN, TIM8_BKIN, TIM8_BKIN_COMP12, TIM1_BKIN_COMP12, LCD_G7, EVENTOUT | - |
| G3 | H7 | 110 | 130 | H16 | PG2 | I/O | FT_h | - | TIM8_BKIN, TIM8_BKIN_COMP12, FMC_A12, EVENTOUT | - |
| G4 | G8 | 111 | 131 | H15 | PG3 | I/O | FT_h | - | TIM8_BKIN2, TIM8_BKIN2_COMP12, FMC_A13, EVENTOUT | - |
| - | - | 112 | 132 | - | VSS | S | - | - | - | - |
| - | E12 | 113 | 133 | N7 | VDD | S | - | - | - | - |
| F4 | G10 | 114 | 134 | H14 | PG4 | I/O | FT_h | - | TIM1_BKIN2, TIM1_BKIN2_COMP12, FMC_A14/FMC_BA0, EVENTOUT | - |
| F1 | G9 | 115 | 135 | G14 | PG5 | I/O | FT_h | - | TIM1_ETR, FMC_A15/FMC_BA1, EVENTOUT | - |
| - | G11 | 116 | 136 | G15 | PG6 | I/O | FT_h | - | TIM17_BKIN, HRTIM_CHE1, QUADSPI_BK1_NCS, FMC_NE3, DCMI_D12, LCD_R7, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| - | F8 | 117 | 137 | F16 | PG7 | I/O | FT_h | - | HRTIM_CHE2, SAI1_MCLK_A, USART6_CK, FMC_INT, DCMI_D13, LCD_CLK, EVENTOUT | - |
| F2 | F9 | 118 | 138 | F15 | PG8 | I/O | FT_h | - | TIM8_ETR, SPI6_NSS, USART6_RTS/USART6_DE, SPDIFRX1_IN3, ETH_PPS_OUT, FMC_SDCLK, LCD_G7, EVENTOUT | - |
| F3 | - | 119 | 139 | G16 | VSS | S | - | - | - | - |
| E3 | F12 | 120 | 140 | G17 | VDD50USB | S | - | - | - | - |
| E1 | F13 | 121 | 141 | F17 | VDD33USB | S | - | - | - | - |
| E2 | - | - | - | M5 | VDD | S | - | - | - | - |
| F5 | F11 | 122 | 142 | F14 | PC6 | I/O | FT_h | - | HRTIM_CHA1, TIM3_CH1, TIM8_CH1, DFSDM1_CKIN3, I2S2_MCK, USART6_TX, SDMMC1_D0DIR, FMC_NWAIT, SDMMC2_D6, SDMMC1_D6, DCMI_D0, LCD_HSYNC, EVENTOUT | SWPMI_IO |
| E4 | E10 | 123 | 143 | F13 | PC7 | I/O | FT_h | - | TRGIO, HRTIM_CHA2, TIM3_CH2, TIM8_CH2, DFSDM1_DATIN3, I2S3_MCK, USART6_RX, SDMMC1_D123DIR, FMC_NE1, SDMMC2_D7, SWPMI_TX, SDMMC1_D7, DCMI_D1, LCD_G6, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| D1 | F10 | 124 | 144 | E13 | PC8 | I/O | FT_h | - | TRACED1, HRTIM_CHB1, TIM3_CH3, TIM8_CH3, USART6_CK, UART5_RTS/ UART5_DE, FMC_NE2/FMC_NCE, SWPMI_RX, SDMMC1_D0, DCMI_D2, EVENTOUT | - |
| D2 | E11 | 125 | 145 | E14 | PC9 | I/O | FT_fh | - | MCO2, TIM3_CH4, TIM8_CH4, I2C3_SDA, I2S_CKIN, UART5_CTS, QUADSPI_BK1_IO0, LCD_G3, SWPMI_SUSPEND, SDMMC1_D1, DCMI_D3, LCD_B2, EVENTOUT | - |
| - | - | 126 | - | L5 | VDD | S | - | - | - | - |
| D3 | D10 | 127 | 146 | E15 | PA8 | I/O | FT_fha | - | MCO1, TIM1_CH1, HRTIM_CHB2, TIM8_BKIN2, I2C3_SCL, USART1_CK, OTG_FS_SOF, UART7_RX, TIM8_BKIN2_COMP12, LCD_B3, LCD_R6, EVENTOUT | - |
| D4 | D11 | 128 | 147 | D15 | PA9 | I/O | FT_u | - | TIM1_CH2, HRTIM_CHC1, LPUART1_TX, I2C3_SMBA, SPI2_SCK/I2S2_CK, USART1_TX, FDCAN1_RXFD_MODE, DCMI_D0, LCD_R5, EVENTOUT | OTG_FS_VBUS |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| C2 | A13 | 129 | 148 | D14 | PA10 | I/O | FT_u | - | TIM1_CH3, HRTIM_CHC2, LPUART1_RX, USART1_RX, FDCAN1_TXFD_MODE, OTG_FS_ID, MDIOS_MDIO, LCD_B4, DCMI_D1, LCD_B1, EVENTOUT | - |
| C1 | D12 | 130 | 149 | E17 | PA11 | I/O | FT_u | - | TIM1_CH4, HRTIM_CHD1, LPUART1_CTS, SPI2_NSS/I2S2_WS, UART4_RX, USART1_CTS/USART1_NSS, FDCAN1_RX, OTG_FS_DM, LCD_R4, EVENTOUT | - |
| B1 | D13 | 131 | 150 | E16 | PA12 | I/O | FT_u | - | TIM1_ETR, HRTIM_CHD2, LPUART1_RTS/ LPUART1_DE, SPI2_SCK/I2S2_CK, UART4_TX, USART1_RTS/ USART1_DE, SAI2_FS_B, FDCAN1_TX, OTG_FS_DP, LCD_R5, EVENTOUT | - |
| C3 | B11 | 132 | 151 | C15 | PA13(JTMS/ SWDIO) | I/O | FT | - | JTMS-SWDIO, EVENTOUT | - |
| B2 | C13 | 133 | 152 | D17 | VCAP | S | - | - | - | - |
| A1 | - | 134 | 153 | - | VSS | S | - | - | - | - |
| A2 | B13 | 135 | 154 | C17 | VDDLDO | | - | - | - | - |
| B3 | - | 136 | 155 | K5 | VDD | S | - | - | - | - |
| - | - | - | 156 | D16 | PH13 | I/O | FT_h | - | TIM8_CH1N, UART4_TX, FDCAN1_TX, FMC_D21, LCD_G2, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| - | - | - | 157 | B17 | PH14 | I/O | FT_h | - | TIM8_CH2N, UART4_RX, FDCAN1_RX, FMC_D22, DCMI_D4, LCD_G3, EVENTOUT | - |
| - | - | - | 158 | B16 | PH15 | I/O | FT_h | - | TIM8_CH3N, FDCAN1_TXFD_MODE, FMC_D23, DCMI_D11, LCD_G4, EVENTOUT | - |
| - | - | - | 159 | A16 | PI0 | I/O | FT_h | - | TIM5_CH4, SPI2_NSS/I2S2_WS, FDCAN1_RXFD_MODE, FMC_D24, DCMI_D13, LCD_G5, EVENTOUT | - |
| - | - | - | 160 | - | VSS | S | | - | - | - |
| - | B12 | - | 161 | VDD | VDD | S | | - | - | - |
| - | - | - | 162 | A15 | PI1 | I/O | FT_h | - | TIM8_BKIN2, SPI2_SCK/I2S2_CK, TIM8_BKIN2_COMP12, FMC_D25, DCMI_D8, LCD_G6, EVENTOUT | - |
| - | - | - | 163 | B15 | PI2 | I/O | FT_h | - | TIM8_CH4, SPI2_MISO/I2S2_SDI, FMC_D26, DCMI_D9, LCD_G7, EVENTOUT | - |
| - | - | - | 164 | C14 | PI3 | I/O | FT_h | - | TIM8_ETR, SPI2_MOSI/I2S2_SDO, FMC_D27, DCMI_D10, EVENTOUT | - |
| C4 | - | 137 | - | - | VSS | S | - | - | - | - |
| B3 | - | - | - | VDD | VDD | S | - | - | - | - |
| E5 | A11 | 138 | 165 | B14 | PA14(JTCK/SWCLK) | I/O | FT | - | JTCK-SWCLK, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| A3 | B10 | 139 | 166 | A14 | PA15(JTDI) | I/O | FT | - | JTDI, TIM2_CH1/TIM2_ETR, HRTIM_FLT1, CEC, SPI1_NSS/I2S1_WS, SPI3_NSS/I2S3_WS, SPI6_NSS, UART4_RTS/UART4_DE, UART7_TX, DSI_TE, EVENTOUT | - |
| D5 | C11 | 140 | 167 | A13 | PC10 | I/O | FT_ha | - | HRTIM_EEV1, DFSDM1_CKIN5, SPI3_SCK/I2S3_CK, USART3_TX, UART4_TX, QUADSPI_BK1_IO1, SDMMC1_D2, DCMI_D8, LCD_R2, EVENTOUT | - |
| C5 | E9 | 141 | 168 | B13 | PC11 | I/O | FT_h | - | HRTIM_FLT2, DFSDM1_DATIN5, SPI3_MISO/I2S3_SDI, USART3_RX, UART4_RX, QUADSPI_BK2_NCS, SDMMC1_D3, DCMI_D4, EVENTOUT | - |
| B4 | D9 | 142 | 169 | C12 | PC12 | I/O | FT_h | - | TRACED3, HRTIM_EEV2, SPI3_MOSI/I2S3_SDO, USART3_CK, UART5_TX, SDMMC1_CK, DCMI_D9, EVENTOUT | - |
| - | A7 | - | - | - | VSS | S | - | - | - | - |
| - | - | - | - | VDD | VDD | S | - | - | - | - |
| A4 | C10 | 143 | 170 | D13 | PD0 | I/O | FT_h | - | DFSDM1_CKIN6, SAI3_SCK_A, UART4_RX, FDCAN1_RX, FMC_D2/FMC_DA2, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| F6 | C9 | 144 | 171 | E12 | PD1 | I/O | FT_h | - | DFSDM1_DATIN6, SAI3_SD_A, UART4_TX, FDCAN1_TX, FMC_D3/FMC_DA3, EVENTOUT | - |
| E6 | E8 | 145 | 172 | D12 | PD2 | I/O | FT_h | - | TRACED2, TIM3_ETR, UART5_RX, SDMMC1_CMD, DCMI_D11, EVENTOUT | - |
| B5 | A10 | 146 | 173 | B12 | PD3 | I/O | FT_h | - | DFSDM1_CKOUT, SPI2_SCK/I2S2_CK, USART2_CTS/USART2_NSS, FMC_CLK, DCMI_D5, LCD_G7, EVENTOUT | - |
| A5 | D8 | 147 | 174 | A12 | PD4 | I/O | FT_h | - | HRTIM_FLT3, SAI3_FS_A, USART2_RTS/USART2_DE, FDCAN1_RXFD_MODE, FMC_NOE, EVENTOUT | - |
| F7 | C8 | 148 | 175 | A11 | PD5 | I/O | FT_h | - | HRTIM_EEV3, USART2_TX, FDCAN1_TXFD_MODE, FMC_NWE, EVENTOUT | - |
| B6 | - | - | - | - | VSS | S | - | - | - | - |
| A6 | B2 | - | - | VDD | VDD | S | - | - | - | - |
| C6 | B8 | 149 | 176 | B11 | PD6 | I/O | FT_h | - | SAI1_D1, DFSDM1_CKIN4, DFSDM1_DATIN1, SPI3_MOSI/I2S3_SDO, SAI1_SD_A, USART2_RX, SAI4_SD_A, FDCAN2_RXFD_MODE, SAI4_D1, SDMMC2_CK, FMC_NWAIT, DCMI_D10, LCD_B2, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| D6 | A8 | 150 | 177 | C11 | PD7 | I/O | FT_h | - | DFSDM1_DATIN4, SPI1_MOSI/I2S1_SDO, DFSDM1_CKIN1, USART2_CK, SPDIFRX1_IN0, SDMMC2_CMD, FMC_NE1, EVENTOUT | - |
| - | - | - | - | D11 | PJ12 | I/O | FT | - | TRGOUT, LCD_G3, LCD_B0, EVENTOUT | - |
| - | - | - | - | E10 | PJ13 | I/O | FT | - | LCD_B4, LCD_B1, EVENTOUT | - |
| - | - | - | - | D10 | PJ14 | I/O | FT | - | LCD_B2, EVENTOUT | - |
| - | - | - | - | B10 | PJ15 | I/O | FT | - | LCD_B3, EVENTOUT | - |
| B9 | B9 | 151 | 178 | - | VSS | S | - | - | - | - |
| - | - | 152 | 179 | VDD | VDD | S | - | - | - | - |
| - | C7 | 153 | 180 | A10 | PG9 | I/O | FT_h | - | SPI1_MISO/I2S1_SDI, USART6_RX, SPDIFRX1_IN4, QUADSPI_BK2_IO2, SAI2_FS_B, FMC_NE2/FMC_NCE, DCMI_VSYNC, EVENTOUT | - |
| - | D7 | 154 | 181 | A9 | PG10 | I/O | FT_h | - | HRTIM_FLT5, SPI1_NSS/I2S1_WS, LCD_G3, SAI2_SD_B, FMC_NE3, DCMI_D2, LCD_B2, EVENTOUT | - |
| - | E7 | 155 | 182 | B9 | PG11 | I/O | FT_h | - | LPTIM1_IN2, HRTIM_EEV4, SPI1_SCK/I2S1_CK, SPDIFRX1_IN1, SDMMC2_D2, ETH_MII_TX_EN/ETH_RMII_TX_EN, DCMI_D3, LCD_B3, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| - | G7 | 156 | 183 | C9 | PG12 | I/O | FT_h | - | LPTIM1_IN1, HRTIM_EEV5, SPI6_MISO, USART6_RTS/USART6_DE, SPDIFRX1_IN2, LCD_B4, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_NE4, LCD_B1, EVENTOUT | - |
| - | F7 | 157 | 184 | D9 | PG13 | I/O | FT_h | - | TRACED0, LPTIM1_OUT, HRTIM_EEV10, SPI6_SCK, USART6_CTS/USART6_NSS, ETH_MII_TXD0/ETH_RMII_TXD0, FMC_A24, LCD_R0, EVENTOUT | - |
| - | E6 | 158 | 185 | D8 | PG14 | I/O | FT_h | - | TRACED1, LPTIM1_ETR, SPI6_MOSI, USART6_TX, QUADSPI_BK2_IO3, ETH_MII_TXD1/ETH_RMII_TXD1, FMC_A25, LCD_B0, EVENTOUT | - |
| - | - | 159 | 186 | - | VSS | S | - | - | - | - |
| - | - | 160 | 187 | VDD | VDD | S | - | - | - | - |
| - | - | - | - | C8 | PK3 | I/O | FT | - | LCD_B4, EVENTOUT | - |
| - | - | - | - | B8 | PK4 | I/O | FT | - | LCD_B5, EVENTOUT | - |
| - | - | - | - | A8 | PK5 | I/O | FT | - | LCD_B6, EVENTOUT | - |
| - | - | - | - | C7 | PK6 | I/O | FT | - | LCD_B7, EVENTOUT | - |
| - | - | - | - | D7 | PK7 | I/O | FT | - | LCD_DE, EVENTOUT | - |
| - | B7 | - | - | VDD | VDD | S | | - | - | - |
| A7 | C6 | 161 | 188 | D6 | PG15 | I/O | FT_h | - | USART6_CTS/USART6_NSS, FMC_SDNCAS, DCMI_D13, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| B7 | A6 | 162 | 189 | C6 | PB3(JTDO/TRACESWO) | I/O | FT | - | JTDO/TRACESWO, TIM2_CH2, HRTIM_FLT4, SPI1_SCK/I2S1_CK, SPI3_SCK/I2S3_CK, SPI6_SCK, SDMMC2_D2, CRS_SYNC, UART7_RX, EVENTOUT | - |
| A8 | B6 | 163 | 190 | B7 | PB4(NJTRST) | I/O | FT | - | NJTRST, TIM16_BKIN, TIM3_CH1, HRTIM_EEV6, SPI1_MISO/I2S1_SDI, SPI3_MISO/I2S3_SDI, SPI2_NSS/I2S2_WS, SPI6_MISO, SDMMC2_D3, UART7_TX, EVENTOUT | - |
| B8 | A5 | 164 | 191 | A5 | PB5 | I/O | FT | - | TIM17_BKIN, TIM3_CH2, HRTIM_EEV7, I2C1_SMBA, SPI1_MOSI/I2S1_SDO, I2C4_SMBA, SPI3_MOSI/I2S3_SDO, SPI6_MOSI, FDCAN2_RX, OTG_HS_ULPI_D7, ETH_PPS_OUT, FMC_SDCKE1, DCMI_D10, UART5_RX, EVENTOUT | - |
| A9 | - | - | - | VDD | VDD | S | - | - | - | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| C7 | E5 | 165 | 192 | B5 | PB6 | I/O | FT_f | - | TIM16_CH1N, TIM4_CH1, HRTIM_EEV8, I2C1_SCL, CEC, I2C4_SCL, USART1_TX, LPUART1_TX, FDCAN2_TX, QUADSPI_BK1_NCS, DFSDM1_DATIN5, FMC_SDNE1, DCMI_D5, UART5_TX, EVENTOUT | - |
| C8 | C5 | 166 | 193 | C5 | PB7 | I/O | FT_fa | - | TIM17_CH1N, TIM4_CH2, HRTIM_EEV9, I2C1_SDA, I2C4_SDA, USART1_RX, LPUART1_RX, FDCAN2_TXFD_MODE, DFSDM1_CKIN5, FMC_NL, DCMI_VSYNC, EVENTOUT | PVD_IN |
| D7 | B5 | 167 | 194 | E8 | BOOT0 | I | B | - | - | VPP |
| A10 | D5 | 168 | 195 | D5 | PB8 | I/O | FT_fh | - | TIM16_CH1, TIM4_CH3, DFSDM1_CKIN7, I2C1_SCL, I2C4_SCL, SDMMC1_CKIN, UART4_RX, FDCAN1_RX, SDMMC2_D4, ETH_MII_TXD3, SDMMC1_D4, DCMI_D6, LCD_B6, EVENTOUT | - |

Table 7. STM32H747xI/G pin/ball definition (continued)

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| C9 | D6 | 169 | 196 | D4 | PB9 | I/O | FT_fh | - | TIM17_CH1, TIM4_CH4, DFSDM1_DATIN7, I2C1_SDA, SPI2_NSS/I2S2_WS, I2C4_SDA, SDMMC1_CDIR, UART4_TX, FDCAN1_TX, SDMMC2_D5, I2C4_SMBA, SDMMC1_D5, DCMI_D7, LCD_B7, EVENTOUT | - |
| B10 | D4 | 170 | 197 | C4 | PE0 | I/O | FT_h | - | LPTIM1_ETR, TIM4_ETR, HRTIM_SCIN, LPTIM2_ETR, UART8_RX, FDCAN1_RXFD_MODE, SAI2_MCLK_A, FMC_NBL0, DCMI_D2, EVENTOUT | - |
| D8 | C4 | 171 | 198 | B4 | PE1 | I/O | FT_h | - | LPTIM1_IN2, HRTIM_SCOUT, UART8_TX, FDCAN1_TXFD_MODE, FMC_NBL1, DCMI_D3, EVENTOUT | - |
| A11 | A4 | 172 | 199 | A7 | VCAP | S | - | - | - | - |
| C10 | - | 173 | 200 | B6 | VSS | S | - | - | - | - |
| E7 | B3 | 174 | 201 | E7 | PDR_ON | I | FT | - | - | - |
| A12 | A3 | 175 | 202 | A6 | VDDLDO | S | - | - | - | - |
| B11 | - | - | - | VDD | VDD | S | - | - | - | - |
| - | - | - | 203 | A4 | PI4 | I/O | FT_h | - | TIM8_BKIN, SAI2_MCLK_A, TIM8_BKIN_COMP12, FMC_NBL2, DCMI_D5, LCD_B4, EVENTOUT | - |

**Table 7. STM32H747xI/G pin/ball definition (continued)**

| Pin/ball name | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Alternate functions | Additional functions |
|---|---|---|---|---|---|---|---|---|---|---|
| WLCSP156 | UFBGA169 | LQFP176 | LQFP208 | TFBGA240+25 | | | | | | |
| - | - | - | 204 | A3 | PI5 | I/O | FT_h | - | TIM8_CH1, SAI2_SCK_A, FMC_NBL3, DCMI_VSYNC, LCD_B5, EVENTOUT | - |
| - | - | - | 205 | A2 | PI6 | I/O | FT_h | - | TIM8_CH2, SAI2_SD_A, FMC_D28, DCMI_D6, LCD_B6, EVENTOUT | - |
| - | - | - | 206 | B3 | PI7 | I/O | FT_h | - | TIM8_CH3, SAI2_FS_A, FMC_D29, DCMI_D7, LCD_B7, EVENTOUT | - |
| - | - | - | 207 | - | VSS | S | - | - | - | - |
| B11 | - | 176 | 208 | VDD | VDD | S | - | - | - | - |
| M13 | - | - | - | - | VSS | S | - | - | - | - |
| A13 | - | - | - | - | DNC | | - | - | - | - |
| - | - | - | - | M15 | VSSDSI | S | - | - | - | - |

1. When this pin/ball was previously configured as an oscillator, the oscillator function is kept during and after a reset. This is valid for all resets except for power-on reset.
2. Pxy_C and Pxy pins/balls are two separate pads (analog switch open). The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.
3. There is a direct path between Pxy_C and Pxy pins/balls, through an analog switch. Pxy alternate functions are available on Pxy_C when the analog switch is closed. The analog switch is configured through a SYSCFG register. Refer to the product reference manual for a detailed description of the switch configuration bits.

## Table 8. Port A alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port A | PA0 | - | TIM2_CH1/TIM2_ETR | TIM5_CH1 | TIM8_ETR | TIM15_BKIN | - | - | USART2_CTS/USART2_NSS | UART4_TX | SDMMC2_CMD | SAI2_SD_B | ETH_MII_CRS | - | - | - | EVENTOUT |
| | PA1 | - | TIM2_CH2 | TIM5_CH2 | LPTIM3_OUT | TIM15_CH1N | - | - | USART2_RTS/USART2_DE | UART4_RX | QUADSPI_BK1_IO3 | SAI2_MCLK_B | ETH_MII_RX_CLK/ETH_RMII_REF_CLK | - | - | LCD_R2 | EVENTOUT |
| | PA2 | | TIM2_CH3 | TIM5_CH3 | LPTIM4_OUT | TIM15_CH1 | - | - | USART2_TX | SAI2_SCK_B | - | - | ETH_MDIO | MDIOS_MDIO | - | LCD_R1 | EVENTOUT |
| | PA3 | | TIM2_CH4 | TIM5_CH4 | LPTIM5_OUT | TIM15_CH2 | - | - | USART2_RX | - | LCD_B2 | OTG_HS_ULPI_D0 | ETH_MII_COL | - | - | LCD_B5 | EVENTOUT |
| | PA4 | D1PWRE | - | TIM5_ETR | - | - | SPI1_NSS/I2S1_WS | SPI3_NSS/I2S3_WS | USART2_CK | SPI6_NSS | - | - | - | OTG_HS_SOF | DCMI_HSYNC | LCD_VSYNC | EVENTOUT |
| | PA5 | D2PWRE | TIM2_CH1/TIM2_ETR | - | TIM8_CH1N | - | SPI1_SCK/I2S1_CK | - | - | SPI6_SCK | - | OTG_HS_ULPI_CK | - | - | - | LCD_R4 | EVENTOUT |
| | PA6 | - | TIM1_BKIN | TIM3_CH1 | TIM8_BKIN | - | SPI1_MISO/I2S1_SDI | - | - | SPI6_MISO | TIM13_CH1 | TIM8_BKIN_COMP12 | MDIOS_MDC | TIM1_BKIN_COMP12 | DCMI_PIXCLK | LCD_G2 | EVENTOUT |
| | PA7 | - | TIM1_CH1N | TIM3_CH2 | TIM8_CH1N | - | SPI1_MOSI/I2S1_SDO | - | - | SPI6_MOSI | TIM14_CH1 | | ETH_MII_RX_DV/ETH_RMII_CRS_DV | FMC_SDNWE | - | - | EVENTOUT |
| | PA8 | MCO1 | TIM1_CH1 | HRTIM_CHB2 | TIM8_BKIN2 | I2C3_SCL | - | - | USART1_CK | - | - | OTG_FS_SOF | UART7_RX | TIM8_BKIN2_COMP12 | LCD_B3 | LCD_R6 | EVENTOUT |
| | PA9 | - | TIM1_CH2 | HRTIM_CHC1 | LPUART1_TX | I2C3_SMBA | SPI2_SCK/I2S2_CK | - | USART1_TX | - | FDCAN1_RXFD_MODE | - | ETH_TX_ER | - | DCMI_D0 | LCD_R5 | EVENTOUT |
| | PA10 | - | TIM1_CH3 | HRTIM_CHC2 | LPUART1_RX | - | - | - | USART1_RX | - | FDCAN1_TXFD_MODE | OTG_FS_ID | MDIOS_MDIO | LCD_B4 | DCMI_D1 | LCD_B1 | EVENTOUT |
| | PA11 | - | TIM1_CH4 | HRTIM_CHD1 | LPUART1_CTS | - | SPI2_NSS/I2S2_WS | UART4_RX | USART1_CTS/USART1_NSS | - | FDCAN1_RX | OTG_FS_DM | - | - | - | LCD_R4 | EVENTOUT |
| | PA12 | - | TIM1_ETR | HRTIM_CHD2 | LPUART1_RTS/LPUART1_DE | - | SPI2_SCK/I2S2_CK | UART4_TX | USART1_RTS/USART1_DE | SAI2_FS_B | FDCAN1_TX | OTG_FS_DP | - | - | - | LCD_R5 | EVENTOUT |

**Table 8. Port A alternate functions (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port A | PA13 | JTMS/SWDIO | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT OUT |
| | PA14 | JTCK/SWCLK | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT OUT |
| | PA15 | JTDI | TIM2_CH1/TIM2_ETR | HRTIM_FLT1 | - | CEC | SPI1_NSS/I2S1_WS | SPI3_NSS/I2S3_WS | SPI6_NSS | UART4_RTS/UART4_DE | - | - | UART7_TX | - | DSI_TE | - | EVENT OUT |

## Table 9. Port B alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD/CRS | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port B | PB0 | - | TIM1_CH2N | TIM3_CH3 | TIM8_CH2N | - | - | DFSDM1_CKOUT | - | UART4_CTS | LCD_R3 | OTG_HS_ULPI_D1 | ETH_MII_RXD2 | - | - | LCD_G1 | EVENTOUT |
| | PB1 | - | TIM1_CH3N | TIM3_CH4 | TIM8_CH3N | - | - | DFSDM1_DATIN1 | - | - | LCD_R6 | OTG_HS_ULPI_D2 | ETH_MII_RXD3 | - | - | LCD_G0 | EVENTOUT |
| | PB2 | RTC_OUT | - | SAI1_D1 | - | DFSDM1_CKIN1 | - | SAI1_SD_A | SPI3_MOSI/I2S3_SDO | SAI4_SD_A | QUADSPI_CLK | SAI4_D1 | - | - | - | - | EVENTOUT |
| | PB3 | JTDO/TRACESWO | TIM2_CH2 | HRTIM_FLT4 | - | - | SPI1_SCK/I2S1_CK | SPI3_SCK/I2S3_CK | - | SPI6_SCK | SDMMC2_D2 | CRS_SYNC | UART7_RX | - | - | - | EVENTOUT |
| | PB4 | NJTRST | TIM16_BKIN | TIM3_CH1 | HRTIM_EEV6 | - | SPI1_MISO/I2S1_SDI | SPI3_MISO/I2S3_SDI | SPI2_NSS/I2S2_WS | SPI6_MISO | SDMMC2_D3 | - | UART7_TX | - | - | - | EVENTOUT |
| | PB5 | - | TIM17_BKIN | TIM3_CH2 | HRTIM_EEV7 | I2C1_SMBA | SPI1_MOSI/I2S1_SDO | I2C4_SMBA | SPI3_MOSI/I2S3_SDO | SPI6_MOSI | FDCAN2_RX | OTG_HS_ULPI_D7 | ETH_PPS_OUT | FMC_SDCKE1 | DCMI_D10 | UART5_RX | EVENTOUT |
| | PB6 | - | TIM16_CH1N | TIM4_CH1 | HRTIM_EEV8 | I2C1_SCL | CEC | I2C4_SCL | USART1_TX | LPUART1_TX | FDCAN2_TX | QUADSPI_BK1_NCS | DFSDM1_DATIN5 | FMC_SDNE1 | DCMI_D5 | UART5_TX | EVENTOUT |
| | PB7 | - | TIM17_CH1N | TIM4_CH2 | HRTIM_EEV9 | I2C1_SDA | - | I2C4_SDA | USART1_RX | LPUART1_RX | FDCAN2_TXFD_MODE | - | DFSDM1_CKIN5 | FMC_NL | DCMI_VSYNC | - | EVENTOUT |
| | PB8 | - | TIM16_CH1 | TIM4_CH3 | DFSDM1_CKIN7 | I2C1_SCL | - | I2C4_SCL | SDMMC1_CKIN | UART4_RX | FDCAN1_RX | SDMMC2_D4 | ETH_MII_TXD3 | SDMMC1_D4 | DCMI_D6 | LCD_B6 | EVENTOUT |

**Table 9. Port B alternate functions (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD/CRS | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port B | PB9 | - | TIM17_CH1 | TIM4_CH4 | DFSDM1_DATIN7 | I2C1_SDA | SPI2_NSS/I2S2_WS | I2C4_SDA | SDMMC1_CDIR | UART4_TX | FDCAN1_TX | SDMMC2_D5 | I2C4_SMBA | SDMMC1_D5 | DCMI_D7 | LCD_B7 | EVENTOUT |
| | PB10 | - | TIM2_CH3 | HRTIM_SCOUT | LPTIM2_IN1 | I2C2_SCL | SPI2_SCK/I2S2_CK | DFSDM1_DATIN7 | USART3_TX | - | QUADSPI_BK1_NCS | OTG_HS_ULPI_D3 | ETH_MII_RX_ER | - | - | LCD_G4 | EVENTOUT |
| | PB11 | - | TIM2_CH4 | HRTIM_SCIN | LPTIM2_ETR | I2C2_SDA | - | DFSDM1_CKIN7 | USART3_RX | - | - | OTG_HS_ULPI_D4 | ETH_MII_TX_EN/ETH_RMII_TX_EN | - | DSI_TE | LCD_G5 | EVENTOUT |
| | PB12 | - | TIM1_BKIN | - | - | I2C2_SMBA | SPI2_NSS/I2S2_WS | DFSDM1_DATIN1 | USART3_CK | - | FDCAN2_RX | OTG_HS_ULPI_D5 | ETH_MII_TXD0/ETH_RMII_TXD0 | OTG_HS_ID | TIM1_BKIN_COMP12 | UART5_RX | EVENTOUT |
| | PB13 | - | TIM1_CH1N | - | LPTIM2_OUT | - | SPI2_SCK/I2S2_CK | DFSDM1_CKIN1 | USART3_CTS/USART3_NSS | - | FDCAN2_TX | OTG_HS_ULPI_D6 | ETH_MII_TXD1/ETH_RMII_TXD1 | - | - | UART5_TX | EVENTOUT |
| | PB14 | - | TIM1_CH2N | - | TIM8_CH2N | USART1_TX | SPI2_MISO/I2S2_SDI | DFSDM1_DATIN2 | USART3_RTS/USART3_DE | UART4_RTS/UART4_DE | SDMMC2_D0 | - | - | OTG_HS_DM | - | | EVENTOUT |
| | PB15 | RTC_REFIN | TIM1_CH3N | - | TIM8_CH3N | USART1_RX | SPI2_MOSI/I2S2_SDO | DFSDM1_CKIN2 | - | UART4_CTS | SDMMC2_D1 | - | - | OTG_HS_DP | - | | EVENTOUT |

## Table 10. Port C alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port C | PC0 | - | - | - | DFSDM1_CKIN0 | - | - | DFSDM1_DATIN4 | - | SAI2_FS_B | - | OTG_HS_ULPI_STP | - | FMC_SDNWE | - | LCD_R5 | EVENTOUT |
| | PC1 | TRACED0 | - | SAI1_D1 | DFSDM1_DATIN0 | DFSDM1_CKIN4 | SPI2_MOSI/I2S2_SDO | SAI1_SD_A | - | SAI4_SD_A | SDMMC2_CK | SAI4_D1 | ETH_MDC | MDIOS_MDC | - | - | EVENTOUT |
| | PC2 | C1DSLEEP | - | - | DFSDM1_CKIN1 | - | SPI2_MISO/I2S2_SDI | DFSDM1_CKOUT | - | - | - | OTG_HS_ULPI_DIR | ETH_MII_TXD2 | FMC_SDNE0 | - | - | EVENTOUT |
| | PC3 | C1SLEEP | - | - | DFSDM1_DATIN1 | - | SPI2_MOSI/I2S2_SDO | - | - | - | - | OTG_HS_ULPI_NXT | ETH_MII_TX_CLK | FMC_SDCKE0 | - | - | EVENTOUT |
| | PC4 | C2DSLEEP | - | - | DFSDM1_CKIN2 | - | I2S1_MCK | - | - | | SPDIFRX1_IN3 | - | ETH_MII_RXD0/ETH_RMII_RXD0 | FMC_SDNE0 | - | - | EVENTOUT |
| | PC5 | C2SLEEP | - | SAI1_D3 | DFSDM1_DATIN2 | - | - | - | - | - | SPDIFRX1_IN4 | SAI4_D3 | ETH_MII_RXD1/ETH_RMII_RXD1 | FMC_SDCKE0 | COMP1_OUT | - | EVENTOUT |
| | PC6 | - | HRTIM_CHA1 | TIM3_CH1 | TIM8_CH1 | DFSDM1_CKIN3 | I2S2_MCK | - | USART6_TX | SDMMC1_D0DIR | FMC_NWAIT | SDMMC2_D6 | - | SDMMC1_D6 | DCMI_D0 | LCD_HSYNC | EVENTOUT |
| | PC7 | TRGIO | HRTIM_CHA2 | TIM3_CH2 | TIM8_CH2 | DFSDM1_DATIN3 | - | I2S3_MCK | USART6_RX | SDMMC1_D123DIR | FMC_NE1 | SDMMC2_D7 | SWPMI_TX | SDMMC1_D7 | DCMI_D1 | LCD_G6 | EVENTOUT |
| | PC8 | TRACED1 | HRTIM_CHB1 | TIM3_CH3 | TIM8_CH3 | - | - | - | USART6_CK | UART5_RTS/UART5_DE | FMC_NE2/FMC_NCE | - | SWPMI_RX | SDMMC1_D0 | DCMI_D2 | - | EVENTOUT |
| | PC9 | MCO2 | - | TIM3_CH4 | TIM8_CH4 | I2C3_SDA | I2S_CKIN | - | - | UART5_CTS | QUADSPI_BK1_IO0 | LCD_G3 | SWPMI_SUSPEND | SDMMC1_D1 | DCMI_D3 | LCD_B2 | EVENTOUT |
| | PC10 | - | - | HRTIM_EEV1 | DFSDM1_CKIN5 | - | - | SPI3_SCK/I2S3_CK | USART3_TX | UART4_TX | QUADSPI_BK1_IO1 | - | - | SDMMC1_D2 | DCMI_D8 | LCD_R2 | EVENTOUT |
| | PC11 | - | - | HRTIM_FLT2 | DFSDM1_DATIN5 | - | - | SPI3_MISO/I2S3_SDI | USART3_RX | UART4_RX | QUADSPI_BK2_NCS | - | - | SDMMC1_D3 | DCMI_D4 | - | EVENTOUT |
| | PC12 | TRACED3 | - | HRTIM_EEV2 | - | - | - | SPI3_MOSI/I2S3_SDO | USART3_CK | UART5_TX | - | - | - | SDMMC1_CK | DCMI_D9 | - | EVENTOUT |
| | PC13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |
| | PC15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENTOUT |

## Table 11. Port D alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port D | PD0 | - | - | - | DFSDM1_CKIN6 | - | - | SAI3_SCK_A | - | UART4_RX | FDCAN1_RX | - | - | FMC_D2/FMC_DA2 | - | - | EVENTOUT |
| | PD1 | - | - | - | DFSDM1_DATIN6 | - | - | SAI3_SD_A | - | UART4_TX | FDCAN1_TX | - | - | FMC_D3/FMC_DA3 | - | - | EVENTOUT |
| | PD2 | TRACED2 | - | TIM3_ETR | - | - | - | - | - | UART5_RX | - | - | - | SDMMC1_CMD | DCMI_D11 | - | EVENTOUT |
| | PD3 | - | - | - | DFSDM1_CKOUT | - | SPI2_SCK/I2S2_CK | - | USART2_CTS/USART2_NSS | - | - | - | - | FMC_CLK | DCMI_D5 | LCD_G7 | EVENTOUT |
| | PD4 | - | - | HRTIM_FLT3 | - | - | - | SAI3_FS_A | USART2_RTS/USART2_DE | - | FDCAN1_RXFD_MODE | - | - | FMC_NOE | - | - | EVENTOUT |
| | PD5 | - | - | HRTIM_EEV3 | - | - | - | | USART2_TX | - | FDCAN1_TXFD_MODE | - | - | FMC_NWE | - | - | EVENTOUT |
| | PD6 | - | - | SAI1_D1 | DFSDM1_CKIN4 | DFSDM1_DATIN1 | SPI3_MOSI/I2S3_SDO | SAI1_SD_A | USART2_RX | SAI4_SD_A | FDCAN2_RXFD_MODE | SAI4_D1 | SDMMC2_CK | FMC_NWAIT | DCMI_D10 | LCD_B2 | EVENTOUT |
| | PD7 | - | - | - | DFSDM1_DATIN4 | - | SPI1_MOSI/I2S1_SDO | DFSDM1_CKIN1 | USART2_CK | - | SPDIFRX1_IN1 | - | SDMMC2_CMD | FMC_NE1 | - | - | EVENTOUT |
| | PD8 | - | - | - | DFSDM1_CKIN3 | - | - | SAI3_SCK_B | USART3_TX | - | SPDIFRX1_IN2 | - | - | FMC_D13/FMC_DA13 | - | - | EVENTOUT |
| | PD9 | - | - | - | DFSDM1_DATIN3 | - | - | SAI3_SD_B | USART3_RX | - | FDCAN2_RXFD_MODE | - | - | FMC_D14/FMC_DA14 | - | - | EVENTOUT |
| | PD10 | - | - | - | DFSDM1_CKOUT | - | - | SAI3_FS_B | USART3_CK | - | FDCAN2_TXFD_MODE | - | - | FMC_D15/FMC_DA15 | - | LCD_B3 | EVENTOUT |
| | PD11 | - | - | - | LPTIM2_IN2 | I2C4_SMBA | - | - | USART3_CTS/USART3_NSS | - | QUADSPI_BK1_IO0 | SAI2_SD_A | - | FMC_A16 | - | - | EVENTOUT |
| | PD12 | - | LPTIM1_IN1 | TIM4_CH1 | LPTIM2_IN1 | I2C4_SCL | - | - | USART3_RTS/USART3_DE | - | QUADSPI_BK1_IO1 | SAI2_FS_A | - | FMC_A17 | - | - | EVENTOUT |
| | PD13 | - | LPTIM1_OUT | TIM4_CH2 | | I2C4_SDA | - | - | | | QUADSPI_BK1_IO3 | SAI2_SCK_A | - | FMC_A18 | - | - | EVENTOUT |

**Table 11. Port D alternate functions (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port D | PD14 | - | | TIM4_CH3 | - | - | - | SAI3_MCLK_B | - | UART8_CTS | - | - | - | FMC_D0/FMC_DA0 | - | - | EVENT OUT |
| | PD15 | - | | TIM4_CH4 | - | - | - | SAI3_MCLK_A | - | UART8_RTS/UART8_DE | - | - | - | FMC_D1/FMC_DA1 | - | - | EVENT OUT |

## Table 12. Port E alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port E | PE0 | - | LPTIM1_ETR | TIM4_ETR | HRTIM_SCIN | LPTIM2_ETR | - | - | - | UART8_RX | FDCAN1_RXFD_MODE | SAI2_MCLK_A | - | FMC_NBL0 | DCMI_D2 | - | EVENTOUT |
| | PE1 | - | LPTIM1_IN2 | - | HRTIM_SCOUT | - | - | - | - | UART8_TX | FDCAN1_TXFD_MODE | - | - | FMC_NBL1 | DCMI_D3 | - | EVENTOUT |
| | PE2 | TRACECLK | - | SAI1_CK1 | - | - | SPI4_SCK | SAI1_MCLK_A | - | SAI4_MCLK_A | QUADSPI_BK1_IO2 | SAI4_CK1 | ETH_MII_TXD3 | FMC_A23 | - | - | EVENTOUT |
| | PE3 | TRACED0 | - | - | - | TIM15_BKIN | - | SAI1_SD_B | - | SAI4_SD_B | - | - | - | FMC_A19 | - | - | EVENTOUT |
| | PE4 | TRACED1 | - | SAI1_D2 | DFSDM1_DATIN3 | TIM15_CH1N | SPI4_NSS | SAI1_FS_A | - | SAI4_FS_A | - | SAI4_D2 | - | FMC_A20 | DCMI_D4 | LCD_B0 | EVENTOUT |
| | PE5 | TRACED2 | - | SAI1_CK2 | DFSDM1_CKIN3 | TIM15_CH1 | SPI4_MISO | SAI1_SCK_A | - | SAI4_SCK_A | - | SAI4_CK2 | - | FMC_A21 | DCMI_D6 | LCD_G0 | EVENTOUT |
| | PE6 | TRACED3 | TIM1_BKIN2 | SAI1_D1 | - | TIM15_CH2 | SPI4_MOSI | SAI1_SD_A | - | SAI4_SD_A | SAI4_D1 | SAI2_MCLK_B | TIM1_BKIN2_COMP12 | FMC_A22 | DCMI_D7 | LCD_G1 | EVENTOUT |
| | PE7 | - | TIM1_ETR | - | DFSDM1_DATIN2 | - | - | - | UART7_RX | - | - | QUADSPI_BK2_IO0 | - | FMC_D4/FMC_DA4 | - | - | EVENTOUT |
| | PE8 | - | TIM1_CH1N | - | DFSDM1_CKIN2 | - | - | - | UART7_TX | - | - | QUADSPI_BK2_IO1 | - | FMC_D5/FMC_DA5 | COMP2_OUT | - | EVENTOUT |
| | PE9 | - | TIM1_CH1 | - | DFSDM1_CKOUT | - | - | - | UART7_RTS/UART7_DE | - | - | QUADSPI_BK2_IO2 | - | FMC_D6/FMC_DA6 | - | - | EVENTOUT |
| | PE10 | - | TIM1_CH2N | - | DFSDM1_DATIN4 | - | - | - | UART7_CTS | - | - | QUADSPI_BK2_IO3 | - | FMC_D7/FMC_DA7 | - | - | EVENTOUT |
| | PE11 | - | TIM1_CH2 | - | DFSDM1_CKIN4 | - | SPI4_NSS | - | - | - | - | SAI2_SD_B | - | FMC_D8/FMC_DA8 | - | LCD_G3 | EVENTOUT |
| | PE12 | - | TIM1_CH3N | - | DFSDM1_DATIN5 | - | SPI4_SCK | - | - | - | - | SAI2_SCK_B | - | FMC_D9/FMC_DA9 | COMP1_OUT | LCD_B4 | EVENTOUT |
| | PE13 | - | TIM1_CH3 | - | DFSDM1_CKIN5 | - | SPI4_MISO | - | - | - | - | SAI2_FS_B | - | FMC_D10/FMC_DA10 | COMP2_OUT | LCD_DE | EVENTOUT |
| | PE14 | - | TIM1_CH4 | - | - | - | SPI4_MOSI | - | - | - | - | SAI2_MCLK_B | - | FMC_D11/FMC_DA11 | - | LCD_CLK | EVENTOUT |
| | PE15 | - | TIM1_BKIN | - | - | - | TIM1_BKIN | - | - | - | - | - | - | FMC_D12/FMC_DA12 | TIM1_BKIN_COMP12/COMP_TIM1_BKIN | LCD_R7 | EVENTOUT |

## Table 13. Port F alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port F | PF0 | - | - | - | - | I2C2_SDA | - | - | - | - | - | - | - | FMC_A0 | - | - | EVENT OUT |
| | PF1 | - | - | - | - | I2C2_SCL | - | - | - | - | - | - | - | FMC_A1 | - | - | EVENT OUT |
| | PF2 | - | - | - | - | I2C2_SMBA | - | - | - | - | - | - | - | FMC_A2 | - | - | EVENT OUT |
| | PF3 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A3 | - | - | EVENT OUT |
| | PF4 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A4 | - | - | EVENT OUT |
| | PF5 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A5 | - | - | EVENT OUT |
| | PF6 | - | TIM16_CH1 | - | - | - | SPI5_NSS | SAI1_SD_B | UART7_RX | SAI4_SD_B | QUADSPI_BK1_IO3 | - | - | - | - | - | EVENT OUT |
| | PF7 | - | TIM17_CH1 | - | - | - | SPI5_SCK | SAI1_MCLK_B | UART7_TX | SAI4_MCLK_B | QUADSPI_BK1_IO2 | - | - | - | - | - | EVENT OUT |
| | PF8 | - | TIM16_CH1N | - | - | - | SPI5_MISO | SAI1_SCK_B | UART7_RTS/UART7_DE | SAI4_SCK_B | TIM13_CH1 | QUADSPI_BK1_IO0 | - | - | - | - | EVENT OUT |
| | PF9 | - | TIM17_CH1N | - | - | - | SPI5_MOSI | SAI1_FS_B | UART7_CTS | SAI4_FS_B | TIM14_CH1 | QUADSPI_BK1_IO1 | - | - | - | - | EVENT OUT |
| | PF10 | - | TIM16_BKIN | SAI1_D3 | - | - | - | - | - | - | QUADSPI_CLK | SAI4_D3 | - | - | DCMI_D11 | LCD_DE | EVENT OUT |
| | PF11 | - | - | - | - | - | SPI5_MOSI | - | - | - | - | SAI2_SD_B | | FMC_SDNRAS | DCMI_D12 | - | EVENT OUT |
| | PF12 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A6 | - | - | EVENT OUT |
| | PF13 | - | - | - | DFSDM1_DATIN6 | I2C4_SMBA | - | - | - | - | - | - | - | FMC_A7 | - | - | EVENT OUT |
| | PF14 | - | - | - | DFSDM1_CKIN6 | I2C4_SCL | - | - | - | - | - | - | - | FMC_A8 | - | - | EVENT OUT |
| | PF15 | - | - | - | - | I2C4_SDA | - | - | - | - | - | - | - | FMC_A9 | - | - | EVENT OUT |

## Table 14. Port G alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port G | PG0 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A10 | - | - | EVENTOUT |
| | PG1 | - | - | - | - | - | - | - | - | - | - | - | - | FMC_A11 | - | - | EVENTOUT |
| | PG2 | - | - | - | TIM8_BKIN | - | - | - | - | - | - | - | TIM8_BKIN_COMP12 | FMC_A12 | - | - | EVENTOUT |
| | PG3 | - | - | - | TIM8_BKIN2 | - | - | - | - | - | - | - | TIM8_BKIN2_COMP12 | FMC_A13 | - | - | EVENTOUT |
| | PG4 | - | TIM1_BKIN2 | - | - | - | - | - | - | - | - | - | TIM1_BKIN2_COMP12 | FMC_A14/FMC_BA0 | - | - | EVENTOUT |
| | PG5 | - | TIM1_ETR | - | - | - | - | - | - | - | - | - | - | FMC_A15/FMC_BA1 | - | - | EVENTOUT |
| | PG6 | - | TIM17_BKIN | HRTIM_CHE1 | - | - | - | - | - | - | - | QUADSPI_BK1_NCS | - | FMC_NE3 | DCMI_D12 | LCD_R7 | EVENTOUT |
| | PG7 | - | | HRTIM_CHE2 | | | | SAI1_MCLK_A | USART6_CK | - | - | - | - | FMC_INT | DCMI_D13 | LCD_CLK | EVENTOUT |
| | PG8 | - | - | - | TIM8_ETR | - | SPI6_NSS | - | USART6_RTS/USART6_DE | SPDIFRX1_IN3 | - | - | ETH_PPS_OUT | FMC_SDCLK | - | LCD_G7 | EVENTOUT |
| | PG9 | - | - | - | - | - | SPI1_MISO/I2S1_SDI | - | USART6_RX | SPDIFRX1_IN4 | QUADSPI_BK2_IO2 | SAI2_FS_B | - | FMC_NE2/FMC_NCE | DCMI_VSYNC | - | EVENTOUT |
| | PG10 | - | | HRTIM_FLT5 | - | - | SPI1_NSS/I2S1_WS | - | - | - | LCD_G3 | SAI2_SD_B | - | FMC_NE3 | DCMI_D2 | LCD_B2 | EVENTOUT |
| | PG11 | - | LPTIM1_IN2 | HRTIM_EEV4 | - | - | SPI1_SCK/I2S1_CK | - | - | SPDIFRX1_IN1 | - | SDMMC2_D2 | ETH_MII_TX_EN/ETH_RMII_TX_EN | - | DCMI_D3 | LCD_B3 | EVENTOUT |
| | PG12 | | LPTIM1_IN1 | HRTIM_EEV5 | - | - | SPI6_MISO | - | USART6_RTS/USART6_DE | SPDIFRX1_IN2 | LCD_B4 | - | ETH_MII_TXD1/ETH_RMII_TXD1 | FMC_NE4 | - | LCD_B1 | EVENTOUT |
| | PG13 | TRACED0 | LPTIM1_OUT | HRTIM_EEV10 | - | - | SPI6_SCK | - | USART6_CTS/USART6_NSS | - | - | - | ETH_MII_TXD0/ETH_RMII_TXD0 | FMC_A24 | - | LCD_R0 | EVENTOUT |

**Table 14. Port G alternate functions (continued)**

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port G | PG14 | TRACED1 | LPTIM1_ETR | - | - | - | SPI6_MOSI | - | USART6_TX | - | QUADSPI_BK2_IO3 | - | ETH_MII_TXD1/ETH_RMII_TXD1 | FMC_A25 | - | LCD_B0 | EVENTOUT |
| | PG15 | - | - | - | - | - | - | - | USART6_CTS/USART6_NSS | - | - | - | - | FMC_SDNCAS | DCMI_D13 | - | EVENTOUT |

## Table 15. Port H alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port H | PH0 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT OUT |
| | PH1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT OUT |
| | PH2 | - | LPTIM1_IN2 | - | - | - | - | - | - | - | QUADSPI_BK2_IO0 | SAI2_SCK_B | ETH_MII_CRS | FMC_SDCKE0 | - | LCD_R0 | EVENT OUT |
| | PH3 | - | - | - | - | - | - | - | - | - | QUADSPI_BK2_IO1 | SAI2_MCLK_B | ETH_MII_COL | FMC_SDNE0 | - | LCD_R1 | EVENT OUT |
| | PH4 | - | - | - | - | I2C2_SCL | - | - | - | - | LCD_G5 | OTG_HS_ULPI_NXT | - | | - | LCD_G4 | EVENT OUT |
| | PH5 | - | - | - | - | I2C2_SDA | SPI5_NSS | - | - | - | - | - | - | FMC_SDNWE | - | - | EVENT OUT |
| | PH6 | - | - | - | - | I2C2_SMBA | SPI5_SCK | - | - | - | - | - | ETH_MII_RXD2 | FMC_SDNE1 | DCMI_D8 | - | EVENT OUT |
| | PH7 | - | - | - | - | I2C3_SCL | SPI5_MISO | - | - | - | - | - | ETH_MII_RXD3 | FMC_SDCKE1 | DCMI_D9 | - | EVENT OUT |
| | PH8 | - | - | TIM5_ETR | - | I2C3_SDA | - | - | - | - | - | - | - | FMC_D16 | DCMI_HSYNC | LCD_R2 | EVENT OUT |
| | PH9 | - | - | - | - | I2C3_SMBA | - | - | - | - | - | - | - | FMC_D17 | DCMI_D0 | LCD_R3 | EVENT OUT |
| | PH10 | - | - | TIM5_CH1 | - | I2C4_SMBA | - | - | - | - | - | - | - | FMC_D18 | DCMI_D1 | LCD_R4 | EVENT OUT |
| | PH11 | - | - | TIM5_CH2 | - | I2C4_SCL | - | - | - | - | - | - | - | FMC_D19 | DCMI_D2 | LCD_R5 | EVENT OUT |
| | PH12 | - | - | TIM5_CH3 | - | I2C4_SDA | - | - | - | - | - | - | - | FMC_D20 | DCMI_D3 | LCD_R6 | EVENT OUT |
| | PH13 | - | - | - | TIM8_CH1N | - | - | - | - | UART4_TX | FDCAN1_TX | - | - | FMC_D21 | - | LCD_G2 | EVENT OUT |
| | PH14 | - | - | - | TIM8_CH2N | - | - | - | - | UART4_RX | FDCAN1_RX | - | - | FMC_D22 | DCMI_D4 | LCD_G3 | EVENT OUT |
| | PH15 | - | - | - | TIM8_CH3N | - | - | - | - | - | FDCAN1_TXFD_MODE | - | - | FMC_D23 | DCMI_D11 | LCD_G4 | EVENT OUT |

## Table 16. Port I alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/ HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/ TIM8/LPTIM2/3/4/5/ HRTIM1/ DFSDM1 | I2C1/2/3/4/USART1/ TIM15/ LPTIM2/ DFSDM1/ CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM1 | SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/ SDMMC1/ SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/ FMC/SDMMC2/LCD/ SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/ OTG1_HS/ OTG2_FS/ LCD | I2C4/UART7/SWPMI1/ TIM1/8/ DFSDM1/ SDMMC2/ MDIOS/ ETH | TIM1/8/FMC/SDMMC1/ MDIOS/ OTG1_FS/ LCD | TIM1/DCMI/ LCD/DSI/ COMP | UART5/ LCD | SYS |
| Port I | PI0 | - | - | TIM5_CH4 | - | - | SPI2_NSS/ I2S2_WS | - | - | - | FDCAN1_ RXFD_ MODE | - | - | FMC_D24 | DCMI_D13 | LCD_G5 | EVENT OUT |
| | PI1 | - | - | - | TIM8_BKIN2 | - | SPI2_SCK/ I2S2_CK | - | - | - | - | - | TIM8_BKIN 2_COMP12 | FMC_D25 | DCMI_D8 | LCD_G6 | EVENT OUT |
| | PI2 | - | - | - | TIM8_CH4 | - | SPI2_MISO /I2S2_SDI | - | - | - | - | - | - | FMC_D26 | DCMI_D9 | LCD_G7 | EVENT OUT |
| | PI3 | - | - | - | TIM8_ETR | - | SPI2_MOSI /I2S2_SDO | - | - | - | - | - | - | FMC_D27 | DCMI_D10 | - | EVENT OUT |
| | PI4 | - | - | - | TIM8_BKIN | - | - | - | - | - | - | SAI2_MCLK _A | TIM8_BKIN _COMP12 | FMC_NBL2 | DCMI_D5 | LCD_B4 | EVENT OUT |
| | PI5 | - | - | - | TIM8_CH1 | - | - | - | - | - | - | SAI2_SCK_ A | - | FMC_NBL3 | DCMI_VSY NC | LCD_B5 | EVENT OUT |
| | PI6 | - | - | - | TIM8_CH2 | - | - | - | - | - | - | SAI2_SD_A | - | FMC_D28 | DCMI_D6 | LCD_B6 | EVENT OUT |
| | PI7 | - | - | - | TIM8_CH3 | - | - | - | - | - | - | SAI2_FS_A | - | FMC_D29 | DCMI_D7 | LCD_B7 | EVENT OUT |
| | PI8 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | EVENT OUT |
| | PI9 | - | - | - | - | - | - | - | - | UART4_RX | FDCAN1_ RX | - | - | FMC_D30 | - | LCD_ VSYNC | EVENT OUT |
| | PI10 | - | - | - | - | - | - | - | - | - | FDCAN1_ RXFD_ MODE | - | ETH_MII_ RX_ER | FMC_D31 | - | LCD_ HSYNC | EVENT OUT |
| | PI11 | - | - | - | - | - | - | - | - | - | LCD_G6 | OTG_HS_U LPI_DIR | - | - | - | | EVENT OUT |
| | PI12 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_HSY NC | EVENT OUT |
| | PI13 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_VSY NC | EVENT OUT |
| | PI14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_CLK | EVENT OUT |
| | PI15 | - | - | - | - | - | - | - | - | - | LCD_G2 | - | - | - | - | LCD_R0 | EVENT OUT |

## Table 17. Port J alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/TIM8/LPTIM2/3/4/5/HRTIM1/DFSDM1 | I2C1/2/3/4/USART1/TIM15/LPTIM2/DFSDM1/CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/UART4/DFSDM1 | SPI2/3/6/USART1/2/3/6/UART7/SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/SDMMC1/SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/FMC/SDMMC2/LCD/SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/OTG1_HS/OTG2_FS/LCD | I2C4/UART7/SWPMI1/TIM1/8/DFSDM1/SDMMC2/MDIOS/ETH | TIM1/8/FMC/SDMMC1/MDIOS/OTG1_FS/LCD | TIM1/DCMI/LCD/DSI/COMP | UART5/LCD | SYS |
| Port J | PJ0 | - | - | - | - | - | - | - | - | - | LCD_R7 | - | - | - | - | LCD_R1 | EVENTOUT |
| | PJ1 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R2 | EVENTOUT |
| | PJ2 | - | - | - | - | - | - | - | - | - | - | - | - | - | DSI_TE | LCD_R3 | EVENTOUT |
| | PJ3 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R4 | EVENTOUT |
| | PJ4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R5 | EVENTOUT |
| | PJ5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_R6 | EVENTOUT |
| | PJ6 | - | - | - | TIM8_CH2 | - | - | - | - | - | - | - | - | - | - | LCD_R7 | EVENTOUT |
| | PJ7 | TRGIN | - | - | TIM8_CH2N | - | - | - | - | - | - | - | - | - | - | LCD_G0 | EVENTOUT |
| | PJ8 | - | TIM1_CH3N | - | TIM8_CH1 | - | - | - | - | UART8_TX | - | - | - | - | - | LCD_G1 | EVENTOUT |
| | PJ9 | - | TIM1_CH3 | - | TIM8_CH1N | - | - | - | - | UART8_RX | - | - | - | - | - | LCD_G2 | EVENTOUT |
| | PJ10 | - | TIM1_CH2N | - | TIM8_CH2 | - | SPI5_MOSI | - | - | - | - | - | - | - | - | LCD_G3 | EVENTOUT |
| | PJ11 | - | TIM1_CH2 | - | TIM8_CH2N | - | SPI5_MISO | - | - | - | - | - | - | - | - | LCD_G4 | EVENTOUT |
| | PJ12 | TRGOUT | - | - | - | - | - | - | - | - | LCD_G3 | - | - | - | - | LCD_B0 | EVENTOUT |
| | PJ13 | - | - | - | - | - | - | - | - | - | LCD_B4 | - | - | - | - | LCD_B1 | EVENTOUT |
| | PJ14 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B2 | EVENTOUT |
| | PJ15 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B3 | EVENTOUT |

## Table 18. Port K alternate functions

| Port | | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 | AF8 | AF9 | AF10 | AF11 | AF12 | AF13 | AF14 | AF15 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | SYS | TIM1/2/16/17/LPTIM1/ HRTIM1 | SAI1/TIM3/4/5/HRTIM1 | LPUART/ TIM8/LPTIM2/3/4/5/ HRTIM1/ DFSDM1 | I2C1/2/3/4/USART1/ TIM15/ LPTIM2/ DFSDM1/ CEC | SPI1/2/3/4/5/6/CEC | SPI2/3/SAI1/3/I2C4/ UART4/ DFSDM1 | SPI2/3/6/ USART1/2/3/6/UART7/ SDMMC1 | SPI6/SAI2/4/UART4/5/8/LPUART/ SDMMC1/ SPDIFRX1 | SAI4/FDCAN1/FDACN2/TIM13/14/QUADSPI/ FMC/SDMMC2/LCD/ SPDIFRX1 | SAI2/4/TIM8/QUADSPI/SDMMC2/ OTG1_HS/ OTG2_FS/ LCD | I2C4/UART7/SWPMI1/ TIM1/8/ DFSDM1/ SDMMC2/ MDIOS/ ETH | TIM1/8/FMC/SDMMC1/ MDIOS/ OTG1_FS/ LCD | TIM1/DCMI/ LCD/DSI/ COMP | UART5/ LCD | SYS |
| Port K | PK0 | - | TIM1_CH1N | - | TIM8_CH3 | - | SPI5_SCK | - | - | - | - | - | - | - | - | LCD_G5 | EVENT OUT |
| | PK1 | - | TIM1_CH1 | - | TIM8_CH3N | - | SPI5_NSS | - | - | - | - | - | - | - | - | LCD_G6 | EVENT OUT |
| | PK2 | - | TIM1_BKIN | - | TIM8_BKIN | - | - | - | - | - | - | TIM8_BKIN_COMP12 | TIM1_BKIN_COMP12 | - | - | LCD_G7 | EVENT OUT |
| | PK3 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B4 | EVENT OUT |
| | PK4 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B5 | EVENT OUT |
| | PK5 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B6 | EVENT OUT |
| | PK6 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_B7 | EVENT OUT |
| | PK7 | - | - | - | - | - | - | - | - | - | - | - | - | - | - | LCD_DE | EVENT OUT |

# 6 Electrical characteristics

## 6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to $V_{SS}$.

### 6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of junction temperature, supply voltage and frequencies by tests in production on 100% of the devices with an junction temperature at $T_J$ = 25 °C and $T_J$ = $T_{Jmax}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

### 6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_J$ = 25 °C, $V_{DD}$ = 3.3 V (for the 1.7 V ≤ $V_{DD}$ ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

### 6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

### 6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

### 6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

**Figure 11. Pin loading conditions**

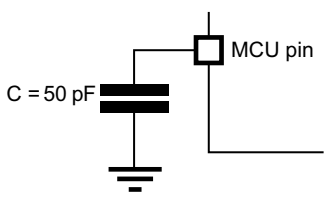
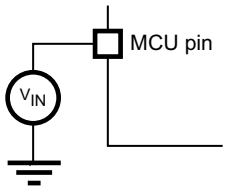
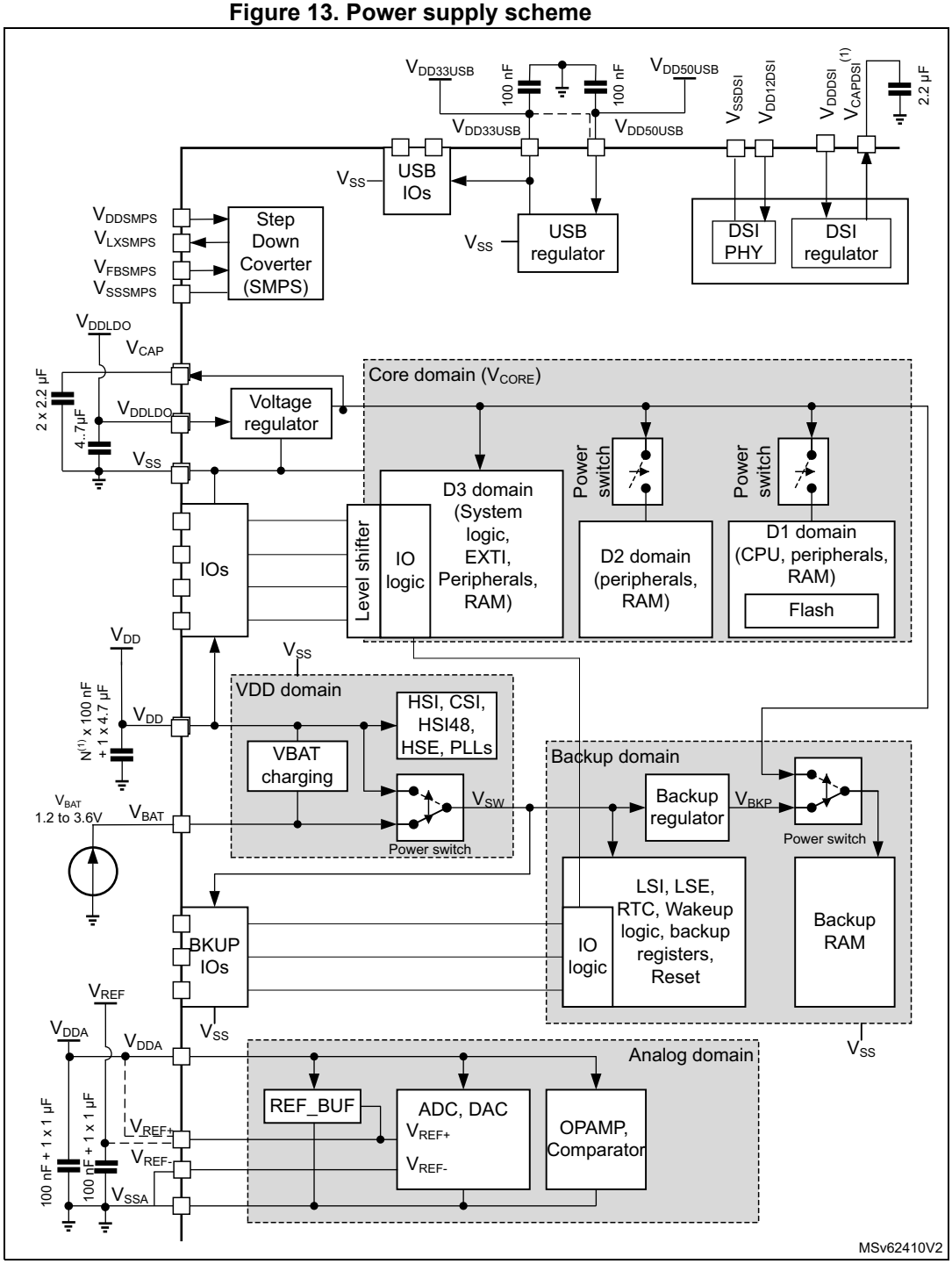



**Figure 12. Pin input voltage**



### 6.1.6 Power supply scheme

**Figure 13. Power supply scheme**



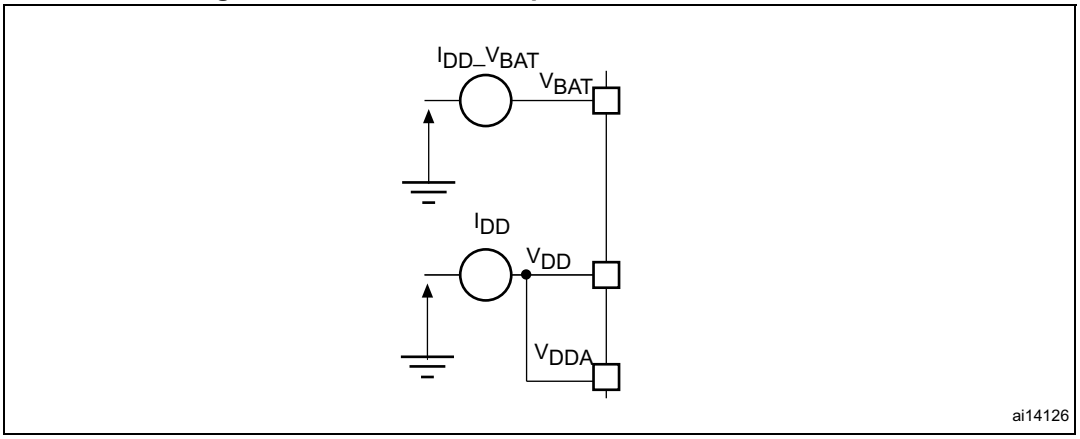

1. N corresponds to the number of VDD pins available on the package.
2. A tolerance of +/- 20% is acceptable on decoupling capacitors.
3. VCAPDSI pin must be externally connected to VDD12DSI pin.

**Caution:** Each power supply pair ($V_{DD}/V_{SS}$, $V_{DDA}/V_{SSA}$ ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or

below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

### 6.1.7 Current consumption measurement

**Figure 14. Current consumption measurement scheme**




## 6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 19: Voltage characteristics*, *Table 20: Current characteristics*, and *Table 21: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and the functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 19. Voltage characteristics (1)**

| Symbols | Ratings | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DDX}$ - $V_{SS}$ | External main supply voltage (including $V_{DD}$, $V_{DDLDO}$, $V_{DDSMPS}$, $V_{DDA}$, $V_{DD33USB}$, $V_{BAT}$) | −0.3 | 4.0 | V |
| $V_{IN}$(2) | Input voltage on FT_xxx pins | $V_{SS}$−0.3 | Min($V_{DD}$, $V_{DDA}$, $V_{DD33USB}$, $V_{BAT}$) +4.0(3)(4) | V |
| | Input voltage on TT_xx pins | $V_{SS}$-0.3 | 4.0 | V |
| | Input voltage on BOOT0 pin | $V_{SS}$ | 9.0 | V |
| | Input voltage on any other pins | $V_{SS}$-0.3 | 4.0 | V |
| $\lvert\Delta V_{DDX}\rvert$ | Variations between different $V_{DDX}$ power pins of the same domain | - | 50 | mV |
| $\lvert V_{SSx}-V_{SS}\rvert$ | Variations between all the different ground pins | - | 50 | mV |

1. All main power ($V_{DD}$, $V_{DDA}$, $V_{DD33USB}$, $V_{DDSMPS}$, $V_{BAT}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supply, in the permitted range.
2. $V_{IN}$ maximum must always be respected. Refer to *Table 70: I/O current injection susceptibility* for the maximum allowed injected current values.
3. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.

4. To sustain a voltage higher than 4V the internal pull-up/pull-down resistors must be disabled.

**Table 20. Current characteristics**

| Symbols | Ratings | Max | Unit |
|---|---|---|---|
| $\Sigma IV_{DD}$ | Total current into sum of all $V_{DD}$ power lines (source)(1) | 620 | mA |
| $\Sigma IV_{SS}$ | Total current out of sum of all $V_{SS}$ ground lines (sink)(1) | 620 | |
| $IV_{DD}$ | Maximum current into each $V_{DD}$ power pin (source)(1) | 100 | |
| $IV_{SS}$ | Maximum current out of each $V_{SS}$ ground pin (sink)(1) | 100 | |
| $I_{IO}$ | Output current sunk by any I/O and control pin | 20 | |
| $\Sigma I_{(PIN)}$ | Total output current sunk by sum of all I/Os and control pins(2) | 140 | |
| | Total output current sourced by sum of all I/Os and control pins(2) | 140 | |
| $I_{INJ(PIN)}$(3)(4) | Injected current on FT_xxx, TT_xx, RST and B pins except PA4, PA5 | −5/+0 | |
| | Injected current on PA4, PA5 | −0/0 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/Os and control pins)(5) | ±25 | |

1. All main power ($V_{DD}$, $V_{DDA}$, $V_{DD33USB}$) and ground ($V_{SS}$, $V_{SSA}$) pins must always be connected to the external power supplies, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
4. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 19: Voltage characteristics* for the maximum allowed input voltage values.
5. When several inputs are submitted to a current injection, the maximum $\sum I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

**Table 21. Thermal characteristics**

| Symbol | Ratings | Value | Unit |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | − 65 to +150 | °C |
| $T_J$ | Maximum junction temperature | 125 | |

# 6.3 Operating conditions

## 6.3.1 General operating conditions

**Table 22. General operating conditions**

| Symbol | Parameter | Operating conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Standard operating voltage | - | 1.62(1) | - | 3.6 | V |
| $V_{DDLDO}$ | Supply voltage for the internal regulator | $V_{DDLDO} \leq V_{DD}$ | 1.62(1) | - | 3.6 | V |
| | | | 1.2(2) | - | 3.6 | |
| $V_{DDSMPS}$ | Supply voltage for the internal SMPS Step-down converter | $V_{DDSMPS} = V_{DD}$ | 1.62(1) | - | 3.6 | V |
| $V_{DD33USB}$ | Standard operating voltage, USB domain | USB used | 3.0 | - | 3.6 | V |
| | | USB not used | 0 | - | 3.6 | |
| $V_{DDA}$ | Analog operating voltage | ADC or COMP used | 1.62 | - | 3.6 | |
| | | DAC used | 1.8 | - | | |
| | | OPAMP used | 2.0 | - | | |
| | | VREFBUF used | 1.8 | - | | |
| | | ADC, DAC, OPAMP, COMP, VREFBUF not used | 0 | - | | |
| $V_{IN}$ | I/O Input voltage | TT_xx I/O | −0.3 | - | $V_{DD}$+0.3 | |
| | | BOOT0 | 0 | - | 9 | |
| | | All I/O except BOOT0 and TT_xx | −0.3 | - | Min($V_{DD}$, $V_{DDA}$, $V_{DD33USB}$) +3.6V < 5.5V(3)(4) | |

**Table 22. General operating conditions (continued)**

| Symbol | Parameter | Operating conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CORE}$ | Internal regulator ON (LDO) | VOS3 (max frequency 200 MHz) | 0.95 | 1.0 | 1.26 | V |
| | | VOS2 (max frequency 300 MHz) | 1.05 | 1.10 | 1.26 | |
| | | VOS1 (max frequency 400 MHz) | 1.15 | 1.20 | 1.26 | |
| | | VOS0(5) (max frequency 480 MHz(6)) | 1.26 | 1.35 | 1.40 | |
| | Internal regulator ON (SMPS step-down converter)(7) | VOS3 (max frequency 200 MHz) | 0.95 | 1.0 | 1.26 | |
| | | VOS2 (max frequency 300 MHz) | 1.05 | 1.10 | 1.26 | |
| | | VOS1 (max frequency 400 MHz) | 1.15 | 1.20 | 1.26 | |
| | Regulator OFF: external $V_{CORE}$ voltage must be supplied from external regulator on two VCAP pins | VOS3 (max frequency 200 MHz) | 0.98 | 1.03 | 1.26 | |
| | | VOS2 (max frequency 300 MHz) | 1.08 | 1.13 | 1.26 | |
| | | VOS1 (max frequency 400 MHz) | 1.17 | 1.23 | 1.26 | |
| | | VOS0 (max frequency 480 MHz(6)) | 1.37 | 1.38 | 1.40 | |

**Table 22. General operating conditions (continued)**

| Symbol | Parameter | Operating conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CPU1}$ | Arm® Cortex®-M7 clock frequency | VOS3 | - | - | 200 | MHz |
| | | VOS2 | - | - | 300 | |
| | | VOS1 | - | - | 400 | |
| | | VOS0 | - | - | 480(6) | |
| $f_{CPU2}$ | Arm® Cortex®-M4 clock frequency | VOS3 | - | - | 200 | |
| | | VOS2 | - | - | 150 | |
| | | VOS1 | - | - | 200 | |
| | | VOS0 | - | - | 240(6) | |
| $f_{ACLK}$ | AXI clock frequency | VOS3 | - | - | 100 | |
| | | VOS2 | - | - | 150 | |
| | | VOS1 | - | - | 200 | |
| | | VOS0 | - | - | 240(6) | |
| $f_{HCLK}$ | AHB clock frequency | VOS3 | - | - | 100 | |
| | | VOS2 | - | - | 150 | |
| | | VOS1 | - | - | 200 | |
| | | VOS0 | - | - | 240(6) | |
| $f_{PCLK}$ | APB clock frequency | VOS3 | - | - | 50(8) | |
| | | VOS2 | - | - | 75 | |
| | | VOS1 | - | - | 100 | |
| | | VOS0 | - | - | 120(6) | |

1. When RESET is released functionality is guaranteed down to $V_{BOR0}$ min
2. Only for power-up sequence when the SMPS step-down converter is configured to supply the LDO and $T_{JMax}$ = 105 °C.
3. This formula has to be applied on power supplies related to the IO structure described by the pin definition table.
4. For operation with voltage higher than Min ($V_{DD}$, $V_{DDA}$, $V_{DD33USB}$) +0.3V, the internal Pull-up and Pull-Down resistors must be disabled.
5. VOS0 is available only when the LDO regulator is ON.
6. $T_{Jmax}$ = 105 °C.
7. At startup, the external $V_{CORE}$ voltage must remain higher or equal to 1.10 V before disabling the internal regulator (LDO).
8. Maximum APB clock frequency when at least one peripheral is enabled.

**Table 23. Supply voltage and maximum frequency configuration**

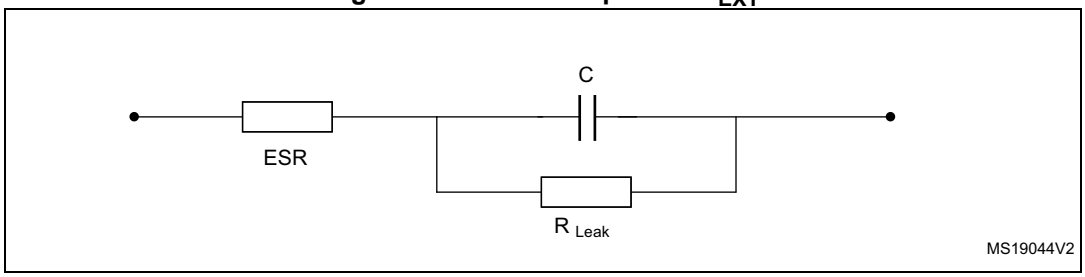
| Power scale | $V_{CORE}$ source | Max $T_J$ (°C) | Max frequency (MHz) | Min $V_{DD}$ (V) |
|---|---|---|---|---|
| VOS0 | LDO | 105 | 480 | 1.7 |
| | SMPS step-down converter(1) | - | - | - |
| VOS1 | LDO | 125 | 400 | 1.62 |
| | SMPS step-down converter | | | |
| VOS2 | LDO | 125 | 300 | 1.62 |
| | SMPS step-down converter | 125 | | |
| VOS3 | LDO(2) | 105 | 64 | 1.2(2) |
| | LDO | 125 | 200 | 1.62 |
| | SMPS step-down converter | 125 | | |
| SVOS4 | LDO | 105 | N/A | 1.62 |
| | SMPS step-down converter | 125 | | |
| SVOS5 | LDO | 105 | N/A | 1.62 |
| | SMPS step-down converter | 125 | | |

1. VOS0 (power scale 0) is not available when the SMPS step-down converter directly supplies $V_{CORE}$.
2. Only for power-up sequence when the SMPS step-down converter supplies the LDO.

### 6.3.2 VCAP external capacitor

Stabilization for the main regulator is achieved by connecting an external capacitor $C_{EXT}$ to the VCAP pin. $C_{EXT}$ is specified in *Table 24*. Two external capacitors can be connected to VCAP pins.

**Figure 15. External capacitor $C_{EXT}$**




1. Legend: ESR is the equivalent series resistance.

**Table 24. VCAP operating conditions(1)**

| Symbol | Parameter | Conditions |
|---|---|---|
| CEXT | Capacitance of external capacitor | 2.2 µF(2) |
| ESR | ESR of external capacitor | < 100 mΩ |

1. When bypassing the voltage regulator, the two 2.2 µF $V_{CAP}$ capacitors are not required and should be replaced by two 100 nF decoupling capacitors.
2. This value corresponds to CEXT typical value. A variation of +/-20% is tolerated.

### 6.3.3 SMPS step-down converter

The devices embed a high power efficiency SMPS step-down converter. SMPS characteristics for external usage are given in *Table 26*. The SMPS step-down converter requires external components that are specified in *Figure 16* and *Table 25*.

**Figure 16. External components for SMPS step-down converter**

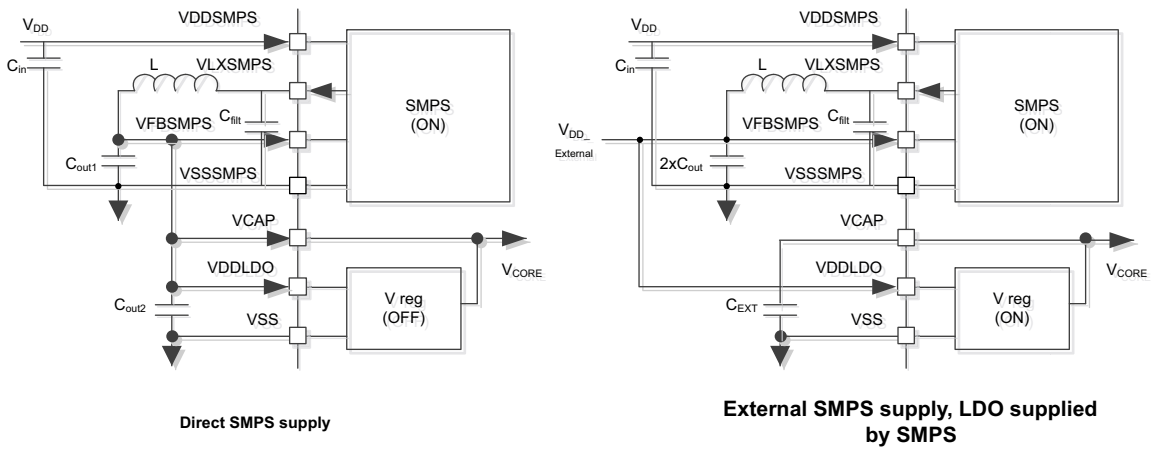



**Table 25. Characteristics of SMPS step-down converter external components**

| Symbol | Parameter | Conditions |
|---|---|---|
| $C_{in}$ | Capacitance of external capacitor on $V_{DDSMPS}$ | 4.7 µF |
| | ESR of external capacitor | 100 mΩ |
| $C_{filt}$ | Capacitance of external capacitor on $V_{LXSMPS}$ pin | 220 pF |
| $C_{OUT}$ | Capacitance of external capacitor on $V_{FBSMPS}$ pin | 10 µF |
| | ESR of external capacitor | 20 mΩ |
| L | Inductance of external Inductor on $V_{LXSMPS}$ pin | 2.2 µH |
| - | Serial DC resistor | 150 mΩ |

**Table 25. Characteristics of SMPS step-down converter external components**

| Symbol | Parameter | Conditions |
|---|---|---|
| $I_{SAT}$ | DC current at which the inductance drops 30% from its value without current. | 1.7 A |
| $I_{RMS}$ | Average current for a 40 °C rise: rated current for which the temperature of the inductor is raised 40°C by DC current | 1.4 A |

**Table 26. SMPS step-down converter characteristics for external usage**

| Parameters | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{DDSMPS}$(1) | $V_{OUT}$ = 1.8 V | 2.3 | - | 3.6 | V |
| | $V_{OUT}$ = 2.5 V | 3 | - | 3.6 | |
| $V_{OUT}$(2) | Iout=600 mA | 2.25 | 2.5 | 2.75 | V |
| | | 1.62 | 1.8 | 1.98 | |
| $I_{OUT}$ | internal and external usage | - | - | 600 | mA |
| | External usage only(3) | - | - | 600 | |
| $RDS_{ON}$ | - | - | 100 | 120 | mΩ |
| $I_{DDSMPS_Q}$ | Quiescent current | - | 220 | - | µA |
| $T_{SMPS_START}$ | $V_{OUT}$ = 1.8 V | - | - | 225 | µs |
| | $V_{OUT}$ = 2.5 V | - | - | 300 | |

1. The switching frequency is 2.4 MHz±10%
2. Including line transient and load transient.
3. These characteristics are given for SDEXTHP bit is set in the PWR_CR3 register.

### 6.3.4 Operating conditions at power-up / power-down

Subject to general operating conditions for $T_A$.

**Table 27. Operating conditions at power-up / power-down (regulator ON)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{VDD}$ | $V_{DD}$ rise time rate | 0 | ∞ | µs/V |
| | $V_{DD}$ fall time rate | 10 | ∞ | |
| $t_{VDDA}$ | $V_{DDA}$ rise time rate | 0 | ∞ | |
| | $V_{DDA}$ fall time rate | 10 | ∞ | |
| $t_{VDDUSB}$ | $V_{DDUSB}$ rise time rate | 0 | ∞ | |
| | $V_{DDUSB}$ fall time rate | 10 | ∞ | |

### 6.3.5 Embedded reset and power control block characteristics

The parameters given in *Table 28* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 28. Reset and power control block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{RSTTEMPO}$(1) | Reset temporization after BOR0 released | - | - | 377 | - | µs |
| $V_{BOR0}$ | Brown-out reset threshold 0 | Rising edge(1) | 1.62 | 1.67 | 1.71 | V |
| | | Falling edge | 1.58 | 1.62 | 1.68 | |
| $V_{BOR1}$ | Brown-out reset threshold 1 | Rising edge | 2.04 | 2.10 | 2.15 | |
| | | Falling edge | 1.95 | 2.00 | 2.06 | |
| $V_{BOR2}$ | Brown-out reset threshold 2 | Rising edge | 2.34 | 2.41 | 2.47 | |
| | | Falling edge | 2.25 | 2.31 | 2.37 | |
| $V_{BOR3}$ | Brown-out reset threshold 3 | Rising edge | 2.63 | 2.70 | 2.78 | |
| | | Falling edge | 2.54 | 2.61 | 2.68 | |
| $V_{PVD0}$ | Programmable Voltage Detector threshold 0 | Rising edge | 1.90 | 1.96 | 2.01 | |
| | | Falling edge | 1.81 | 1.86 | 1.91 | |
| $V_{PVD1}$ | Programmable Voltage Detector threshold 1 | Rising edge | 2.05 | 2.10 | 2.16 | |
| | | Falling edge | 1.96 | 2.01 | 2.06 | |
| $V_{PVD2}$ | Programmable Voltage Detector threshold 2 | Rising edge | 2.19 | 2.26 | 2.32 | |
| | | Falling edge | 2.10 | 2.15 | 2.21 | |
| $V_{PVD3}$ | Programmable Voltage Detector threshold 3 | Rising edge | 2.35 | 2.41 | 2.47 | |
| | | Falling edge | 2.25 | 2.31 | 2.37 | |
| $V_{PVD4}$ | Programmable Voltage Detector threshold 4 | Rising edge | 2.49 | 2.56 | 2.62 | |
| | | Falling edge | 2.39 | 2.45 | 2.51 | |
| $V_{PVD5}$ | Programmable Voltage Detector threshold 5 | Rising edge | 2.64 | 2.71 | 2.78 | |
| | | Falling edge | 2.55 | 2.61 | 2.68 | |
| $V_{PVD6}$ | Programmable Voltage Detector threshold 6 | Rising edge | 2.78 | 2.86 | 2.94 | |
| | | Falling edge in Run mode | 2.69 | 2.76 | 2.83 | |
| $V_{hyst_BOR_PVD}$ | Hysteresis voltage of BOR (unless BOR0) and PVD | Hysteresis in Run mode | - | 100 | - | mV |
| $I_{DD_BOR_PVD}$(1) | BOR(2) (unless BOR0) and PVD consumption from $V_{DD}$ | - | - | | 0.630 | µA |

**Table 28. Reset and power control block characteristics (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{AVM_0}$ | Analog voltage detector for $V_{DDA}$ threshold 0 | Rising edge | 1.66 | 1.71 | 1.76 | V |
| | | Falling edge | 1.56 | 1.61 | 1.66 | |
| $V_{AVM_1}$ | Analog voltage detector for $V_{DDA}$ threshold 1 | Rising edge | 2.06 | 2.12 | 2.19 | |
| | | Falling edge | 1.96 | 2.02 | 2.08 | |
| $V_{AVM_2}$ | Analog voltage detector for $V_{DDA}$ threshold 2 | Rising edge | 2.42 | 2.50 | 2.58 | |
| | | Falling edge | 2.35 | 2.42 | 2.49 | |
| $V_{AVM_3}$ | Analog voltage detector for $V_{DDA}$ threshold 3 | Rising edge | 2.74 | 2.83 | 2.91 | |
| | | Falling edge | 2.64 | 2.72 | 2.80 | |
| $V_{hyst_VDDA}$ | Hysteresis of $V_{DDA}$ voltage detector | - | - | 100 | - | mV |
| $I_{DD_PVM}$ | PVM consumption from $V_{DD}$(1) | - | - | - | 0.25 | µA |
| $I_{DD_VDDA}$ | Voltage detector consumption on $V_{DDA}$(1) | Resistor bridge | - | - | 2.5 | µA |

1. Guaranteed by design.
2. BOR0 is enabled in all modes and its consumption is therefore included in the supply current characteristics tables (refer to *Section 6.3.7: Supply current characteristics*).

## 6.3.6 Embedded reference voltage

The parameters given in *Table 29* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 29. Embedded reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltages | -40°C < TJ < 125 °C, $V_{DD}$ = 3.3 V | 1.180 | 1.216 | 1.255 | V |
| $t_{S_vrefint}$(1)(2) | ADC sampling time when reading the internal reference voltage | - | 4.3 | - | - | µs |
| $t_{S_vbat}$(1)(2) | VBAT sampling time when reading the internal VBAT reference voltage | - | 9 | - | - | |
| $I_{refbuf}$(2) | Reference Buffer consumption for ADC | $V_{DDA}$=3.3 V | 9 | 13.5 | 23 | µA |
| $\Delta V_{REFINT}$(2) | Internal reference voltage spread over the temperature range | -40°C < $T_J$ < 125 °C | - | 5 | 15 | mV |
| $T_{coeff}$(2) | Average temperature coefficient | Average temperature coefficient | - | 20 | 70 | ppm/°C |
| $V_{DDcoeff}$(2) | Average Voltage coefficient | 3.0V < $V_{DD}$ < 3.6V | - | 10 | 1370 | ppm/V |

**Table 29. Embedded reference voltage (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT_DIV1}$ | 1/4 reference voltage | - | - | 25 | - | % $V_{REFINT}$ |
| $V_{REFINT_DIV2}$ | 1/2 reference voltage | - | - | 50 | - | |
| $V_{REFINT_DIV3}$ | 3/4 reference voltage | - | - | 75 | - | |

1. The shortest sampling time for the application can be determined by multiple iterations.
2. Guaranteed by design.

**Table 30. Internal reference voltage calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| $V_{REFIN_CAL}$ | Raw data acquired at temperature of 30 °C, $V_{DDA}$ = 3.3 V | 1FF1E860 - 1FF1E861 |

## 6.3.7 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All the run-mode current consumption measurements given in this section are performed with a CoreMark code.

### Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted with the minimum wait states number, depending on the $f_{ACLK}$ frequency (refer to the table “Number of wait states according to CPU clock ($f_{rcc_c_ck}$) frequency and $V_{CORE}$ range” available in the reference manual).
- When the peripherals are enabled, the AHB clock frequency is the CPU1 frequency divided by 2 and the APB clock frequency is AHB clock frequency divided by 2.

The parameters given in the below tables are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 31. Typical and maximum current consumption in Run mode, code with data processing running from ITCM for Cortex-M7 core, and Flash memory for Cortex-M4 (ART accelerator ON), LDO regulator ON(1)(2)**

| Symbol | Parameter | Conditions | | Arm Cortex-M7 $f_{CPU1}$ (MHz) | Arm Cortex-M4 $f_{CPU2}$ (MHz) | Typ | Max(3) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Tj= 25 °C | Tj= 85 °C | Tj= 105°C | Tj= 125°C | |
| $I_{DD}$ | Supply current in Run mode | All peripherals disabled | VOS0 | 480 | 240 | 179 | 272 | 387 | 498 | | mA |
| | | | | 400 | 200 | 151 | - | - | - | | |
| | | | VOS1 | 400 | 200 | 132 | 181 | 292 | 382 | 502 | |
| | | | VOS2 | 300 | 150 | 91 | 122 | 211 | 281 | 377 | |
| | | | VOS3 | 200 | 100 | 56 | 79 | 150 | 206 | 284 | |
| | | All peripherals enabled | VOS0 | 480 | 240 | 247 | 374 | 462 | 571 | | |
| | | | | 400 | 200 | 208 | - | - | - | | |
| | | | VOS1 | 400 | 200 | 181 | 232 | 337 | 422 | 541 | |
| | | | VOS2 | 300 | 150 | 126 | 163 | 248 | 318 | 414 | |
| | | | VOS3 | 200 | 100 | 78 | 104 | 173 | 229 | 307 | |

1. Data are in DTCM for best computation performance, the cache has no influence on consumption in this case.
2. The grayed cells correspond to the forbidden configurations.
3. Guaranteed by characterization results, unless otherwise specified.

**Table 32. Typical and maximum current consumption in Run mode, code with data processing running from ITCM for Arm Cortex-M7 and Flash memory for Arm Cortex-M4, ART accelerator ON, SMPS regulator(1)**

| Symbol | Parameter | Conditions | | Arm Cortex-M7 $f_{CPU1}$ (MHz) | Arm Cortex-M4 $f_{CPU2}$ (MHz) | Typ | Max | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Tj= 25 °C | Tj= 85 °C | Tj= 105°C | Tj= 125°C | |
| $I_{DD}$ | Supply current in Run mode | All peripherals disabled | VOS1 | 400 | 200 | 58.3 | 79.0 | 129.0 | 175.1 | 236.0 | mA |
| | | | VOS2 | 300 | 150 | 37.0 | 50.2 | 84.7 | 115.6 | 161.1 | |
| | | | VOS3 | 200 | 100 | 21.5 | 29.9 | 56.1 | 77.1 | 107.6 | |
| | | All peripherals enabled | VOS1 | 400 | 200 | 78.1 | 100.1 | 148.9 | 193.4 | 254.3 | |
| | | | VOS2 | 300 | 150 | 51.2 | 65.5 | 100.8 | 130.9 | 176.9 | |
| | | | VOS3 | 200 | 100 | 29.5 | 39.4 | 63.9 | 86.7 | 116.3 | |

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors.

**Table 33. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, both cores running, cache ON, ART accelerator ON, LDO regulator ON(1)**

| Symbol | Parameter | Conditions | | Arm Cortex-M7 $f_{CPU1}$ (MHz) | Arm Cortex-M4 $f_{CPU2}$ (MHz) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Tj= 25 °C | Tj= 85 °C | Tj= 105°C | Tj= 125°C | |
| $I_{DD}$ | Supply current in Run mode | All peripherals disabled | VOS0 | 480 | 240 | 173 | 268 | 385 | 496 | | mA |
| | | | | 400 | 200 | 147 | - | - | - | | |
| | | | VOS1 | 400 | 200 | 128 | 175 | 288 | 379 | 499 | |
| | | | VOS2 | 300 | 150 | 88 | 120 | 209 | 279 | 374 | |
| | | | VOS3 | 200 | 100 | 55 | 77 | 149 | 205 | 283 | |
| | | All peripherals enabled | VOS0 | 480 | 240 | 242 | 368 | 459 | 569 | | |
| | | | VOS1 | 400 | 200 | 178 | 229(3) | 334 | 419(3) | 537 | |
| | | | VOS2 | 300 | 150 | 123 | 161 | 246 | 316 | 412 | |
| | | | VOS3 | 200 | 100 | 77 | 102 | 172 | 228 | 306 | |

1. The grayed cells correspond to the forbidden configurations.
2. Guaranteed by characterization results, unless otherwise specified.
3. Guaranteed by tests in production.

**Table 34. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, both cores running, cache OFF, ART accelerator OFF, LDO regulator ON(1)**

| Symbol | Parameter | Conditions | | Arm Cortex-M7 $f_{CPU1}$ (MHz) | Arm Cortex-M4 $f_{CPU2}$ (MHz) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Tj= 25 °C | Tj= 85 °C | Tj= 105°C | Tj= 125°C | |
| $I_{DD}$ | Supply current in Run mode | All peripherals disabled | VOS0 | 480 | 240 | 109 | 191 | 330 | 444 | | mA |
| | | | VOS1 | 400 | 200 | 96 | 149 | 256 | 347 | 468 | |
| | | | VOS2 | 300 | 150 | 67 | 95 | 187 | 257 | 354 | |
| | | | VOS3 | 200 | 100 | 43 | 62 | 136 | 192 | 270 | |
| | | All peripherals enabled | VOS0 | 480 | 240 | 178 | 291 | 403 | 517 | | |
| | | | VOS1 | 400 | 200 | 147 | 224 | 310 | 401 | 523 | |
| | | | VOS2 | 300 | 150 | 103 | 136 | 224 | 295 | 392 | |
| | | | VOS3 | 200 | 100 | 64 | 87 | 159 | 215 | 293 | |

1. The grayed cells correspond to the forbidden configurations.
2. Guaranteed by characterization results, unless otherwise specified.

**Table 35. Typical and maximum current consumption in Run mode, code with data processing running from ITCM, only Arm Cortex-M7 running, LDO regulator ON(1)(2)**

| Symbol | Parameter | Conditions | | $f_{CPU1}$ (MHz) | Typ | Max(3) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Tj=25 °C | Tj=85 °C | Tj=105 °C | Tj=125 °C | |
| $I_{DD}$ | Supply current in Run mode | All peripherals disabled | VOS0 | 480 | 148 | 226 | 307 | 390 | | mA |
| | | | | 400 | 125 | - | - | - | | |
| | | | VOS1 | 400 | 110 | 168 | 230 | 296 | 384 | |
| | | | | 300 | 84 | - | - | - | - | |
| | | | VOS2 | 300 | 76 | 114 | 170 | 224 | 297 | |
| | | | | 216 | 56 | 88 | 152 | 205 | 278 | |
| | | | | 200 | 53 | - | - | - | - | |
| | | | VOS3 | 200 | 47 | 71 | 121 | 164 | 223 | |
| | | | | 180 | 43 | 64 | 116 | 159 | 218 | |
| | | | | 168 | 40 | 63 | 115 | 158 | 217 | |
| | | | | 144 | 35 | 55 | 109 | 153 | 212 | |
| | | | | 60 | 16 | 36 | 92 | 135 | 194 | |
| | | | | 25 | 12 | 24 | 83 | 126 | 185 | |
| | | All peripherals enabled | VOS0 | 480 | 226 | 222 | 439 | 550 | | |
| | | | | 400 | 190 | - | - | - | | |
| | | | VOS1 | 400 | 167 | 222 | 327 | 416 | 536 | |
| | | | | 300 | 135 | - | - | - | - | |
| | | | VOS2 | 300 | 122 | 160 | 248 | 320 | 419 | |
| | | | | 200 | 85 | - | - | - | - | |
| | | | VOS3 | 200 | 76 | 103 | 174 | 233 | 313 | |

1. Data are in DTCM for best computation performance, the cache has no influence on consumption in this case.
2. The grayed cells correspond to the forbidden configurations.
3. Guaranteed by characterization results, unless otherwise specified.

**Table 36. Typical and maximum current consumption in Run mode, code with data processing running from ITCM, only Arm Cortex-M7 running, SMPS regulator(1)**

| Symbol | Parameter | Conditions | | $f_{CPU1}$ (MHz) | Typ | Max | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Tj=25 °C | Tj=85 °C | Tj=105 °C | Tj=125 °C | |
| $I_{DD}$ | Supply current in Run mode | All peripherals disabled | VOS1 | 400 | 48.6 | 73.3 | 100.4 | 132.4 | 176.0 | mA |
| | | | VOS2 | 300 | 31.3 | 46.3 | 68.3 | 90.0 | 122.2 | |
| | | | VOS3 | 200 | 18.0 | 26.9 | 45.3 | 60.6 | 82.4 | |
| | | All peripherals enabled | VOS1 | 400 | 72.9 | 95.8 | 144.5 | 190.7 | 252.0 | |
| | | | VOS2 | 300 | 49.6 | 64.3 | 99.6 | 131.7 | 179.1 | |
| | | | VOS3 | 200 | 28.8 | 38.5 | 64.3 | 88.3 | 118.6 | |

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors.

**Table 37. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, only Arm Cortex-M7 running, cache ON, LDO regulator ON(1)**

| Symbol | Parameter | Conditions | | $f_{CPU1}$ (MHz) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Tj=25 °C | Tj=85 °C | Tj=105 °C | Tj=125 °C | |
| $I_{DD}$ | Supply current in Run mode | All peripherals disabled | VOS0 | 480 | 110 | 222 | 304 | 388 | | mA |
| | | | | 400 | 91 | - | - | - | | |
| | | | VOS1 | 400 | 80 | 162 | 228 | 294 | 381 | |
| | | | | 300 | 61.5 | - | - | - | - | |
| | | | VOS2 | 216 | 55 | 111 | 168 | 222 | 294 | |
| | | | | 200 | 38.5 | - | - | - | - | |
| | | | VOS3 | 200 | 34.5 | 69 | 120 | 163 | 222 | |
| | | All peripherals enabled | VOS0 | 480 | 220 | 342 | 436 | 546 | | |
| | | | | 400 | 195 | - | - | - | | |
| | | | VOS1 | 400 | 175 | 264 | 336 | 424 | 544 | |
| | | | | 300 | 135 | - | - | - | - | |
| | | | VOS2 | 300 | 120 | 180 | 246 | 318 | 418 | |
| | | | | 200 | 83 | - | - | - | - | |
| | | | VOS3 | 200 | 75 | 114 | 173 | 232 | 312 | |

1. The grayed cells correspond to the forbidden configurations.
2. Guaranteed by characterization results, unless otherwise specified.

**Table 38. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, only Arm Cortex-M7 running, cache OFF, LDO regulator ON(1)**

| Symbol | Parameter | Conditions | | $f_{CPU1}$ (MHz) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Tj=25°C | Tj=85°C | Tj=105 °C | Tj=125 °C | |
| $I_{DD}$ | Supply current in Run mode | All peripherals disabled | VOS0 | 480 | 87 | 157 | 259 | 342 | | mA |
| | | | VOS1 | 400 | 73 | 123 | 201 | 267 | 355 | |
| | | | VOS2 | 300 | 52 | 85 | 150 | 204 | 277 | |
| | | | VOS3 | 200 | 34 | 54 | 109 | 152 | 212 | |
| | | All peripherals enabled | VOS0 | 480 | 168 | 276 | 390 | 504 | | |
| | | | VOS1 | 400 | 135 | 224 | 308 | 397 | 519 | |
| | | | VOS2 | 300 | 100 | 154 | 228 | 301 | 401 | |
| | | | VOS3 | 200 | 70 | 103 | 167 | 226 | 307 | |

1. The grayed cells correspond to the forbidden configurations.
2. Guaranteed by characterization results, unless otherwise specified.

**Table 39. Typical and maximum current consumption batch acquisition mode, LDO regulator ON**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ (MHz) | Typ | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Tj=25°C | Tj=85°C | Tj=105 °C | Tj=125 °C | |
| $I_{DD}$ | Supply current in batch acquisition mode | D1 Standby, D2 Standby, D3 Run | VOS3 | 64 | 2.7 | 4.7 | 12.9 | 19.0 | 27.5 | mA |
| | | | | 8 | 1.1 | - | - | - | - | |
| | | D1 Stop, D2 Stop, D3 Run | VOS3 | 64 | 5.4 | 18.4 | 83.7 | 132.6 | 202.4 | |
| | | | | 8 | 3.8 | - | - | - | - | |

1. Guaranteed by characterization results, unless otherwise specified.

**Table 40. Typical and maximum current consumption in Run mode, code with data processing running from Flash memory, only Arm Cortex-M4 running, ART accelerator ON, LDO regulator ON(1)**

| Symbol | Parameter | Conditions | | $f_{CPU2}$ (MHz) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Tj=25 °C | Tj=85 °C | Tj=105 °C | Tj=125 °C | |
| $I_{DD}$ | Supply current in Run mode | All peripherals disabled | VOS0 | 240 | 121 | 203 | 339 | 453 | | mA |
| | | | | 200 | 90 | - | - | - | | |
| | | | VOS1 | 200 | 79 | 123 | 234 | 323 | 444 | |
| | | | | 150 | 61 | - | - | - | - | |
| | | | VOS2 | 150 | 56 | 85 | 178 | 250 | 350 | |
| | | | VOS3 | 100 | 35 | 59 | 131 | 189 | 269 | |
| | | All peripherals enabled | VOS0 | 240 | 190 | 303 | 412 | 525 | | |
| | | | | 200 | 146 | - | - | - | | |
| | | | VOS1 | 200 | 129 | 195 | 287 | 376 | 499 | |
| | | | VOS2 | 150 | 90 | 134 | 214 | 287 | 386 | |
| | | | VOS3 | 100 | 61 | 100 | 158 | 216 | 297 | |

1. The grayed cells correspond to the forbidden configurations.
2. Guaranteed by characterization results, unless otherwise specified.

**Table 41. Typical and maximum current consumption in Run mode, code with data processing running from Flash bank 2, only Arm Cortex-M4 running, ART accelerator ON, SMPS regulator(1)**

| Symbol | Parameter | Conditions | | Typ | Max | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Tj=25 °C | Tj=85 °C | Tj=105 °C | Tj=125 °C | |
| $I_{DD}$ | Supply current in Run mode | All peripherals disabled | VOS1 | 35.3 | 54.3 | 102.1 | 144.4 | 203.5 | mA |
| | | | VOS2 | 23.3 | 35.0 | 70.6 | 99.2 | 145.8 | |
| | | | VOS3 | 13.6 | 22.3 | 49.0 | 69.8 | 101.9 | |
| | | All peripherals enabled | VOS1 | 57.0 | 84.1 | 126.8 | 172.3 | 234.6 | |
| | | | VOS2 | 36.6 | 54.5 | 84.9 | 118.1 | 165.0 | |
| | | | VOS3 | 23.1 | 37.4 | 58.4 | 79.8 | 112.5 | |

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors.

**Table 42. Typical and maximum current consumption in Stop, LDO regulator ON(1)**

| Symbol | Parameter | Conditions | | Typ | Max(2) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Tj=25°C | Tj=85°C | Tj=105 °C | Tj=125 °C | |
| $I_{DD\ (Stop)}$ | D1 Stop, D2 Stop, D3 Stop | Flash memory OFF, no IWDG | SVOS5 | 1.27 | 6.3 | 42.5 | 72.0 | | mA |
| | | | SVOS4 | 1.96 | 9.4 | 57.4 | 94.6 | | |
| | | | SVOS3 | 2.78 | 13.8(3) | 75.9 | 121.3(3) | 183.8 | |
| | | Flash memory ON, no IWDG | SVOS5 | 1.27 | 6.3 | 42.5 | 72.0 | | |
| | | | SVOS4 | 2.25 | 9.8 | 57.9 | 95.2 | | |
| | | | SVOS3 | 3.07 | 14.1 | 76.4 | 122.0 | 184.8 | |
| | D1 Stop, D2 Standby, D3 Stop | Flash memory OFF, no IWDG | SVOS5 | 0.91 | 4.6 | 30.4 | 51.2 | | |
| | | | SVOS4 | 1.42 | 6.8 | 41.1 | 67.3 | | |
| | | | SVOS3 | 2.02 | 10.0 | 54.4 | 86.6 | 130.0 | |
| | | Flash memory ON, no IWDG | SVOS5 | 0.91 | 4.6 | 30.4 | 51.2 | | |
| | | | SVOS4 | 1.70 | 7.2 | 41.5 | 67.9 | | |
| | | | SVOS3 | 2.31 | 10.3 | 54.9 | 87.1 | 130.8 | |
| | D1 Standby, D2 Stop, D3 Stop | Flash memory OFF, no IWDG | SVOS5 | 0.49 | 2.4 | 16.5 | 28.0 | | |
| | | | SVOS4 | 0.76 | 3.6 | 22.2 | 36.6 | | |
| | | | SVOS3 | 1.10 | 5.3 | 29.3 | 46.9 | 71.2 | |
| | D1 Standby, D2 Standby, D3 Stop | | SVOS5 | 0.15 | 0.7(3) | 4.3 | 7.3(3) | | |
| | | | SVOS4 | 0.22 | 1.0 | 5.8 | 9.6 | | |
| | | | SVOS3 | 0.35 | 1.5(3) | 7.8 | 12.3(3) | 18.6 | |

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors.
2. Guaranteed by characterization results, unless otherwise specified.
3. Guaranteed by tests in production.

**Table 43. Typical and maximum current consumption in Stop, SMPS regulator(1)**

| Symbol | Parameter | Conditions | | Typ | Max | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | Tj=25°C | Tj=85°C | Tj=105 °C | Tj=125 °C | |
| $I_{DD\ (Stop)}$ | D1 Stop, D2 Stop, D3 Stop | Flash OFF, no IWDG | SVOS5 | 0.36 | 1.73 | 11.91 | 21.53 | - | mA |
| | | | SVOS4 | 0.63 | 3.05 | 19.57 | 33.51 | - | |
| | | | SVOS3 | 1.00 | 4.98 | 29.11 | 47.13 | 68.76 | |
| | | Flash ON, no IWDG | SVOS5 | 0.36 | 1.73 | 11.91 | 21.53 | - | |
| | | | SVOS4 | 0.73 | 3.18 | 19.74 | 33.72 | - | |
| | | | SVOS3 | 1.11 | 5.09 | 29.31 | 47.40 | 69.14 | |
| | D1 Stop, D2 Standby, D3 Stop | Flash OFF, no IWDG | SVOS5 | 0.25 | 1.24 | 8.21 | 14.00 | - | |
| | | | SVOS4 | 0.46 | 2.21 | 14.01 | 22.94 | - | |
| | | | SVOS3 | 0.73 | 3.57 | 19.62 | 32.80 | 49.24 | |
| | | Flash ON, no IWDG | SVOS5 | 0.25 | 1.24 | 8.21 | 14.00 | - | |
| | | | SVOS4 | 0.55 | 2.34 | 14.15 | 23.15 | - | |
| | | | SVOS3 | 0.83 | 3.67 | 19.81 | 32.99 | 49.55 | |
| | D1 Standby, D2 Stop, D3 Stop | Flash OFF, no IWDG | SVOS5 | 0.15 | 0.67 | 4.51 | 7.85 | - | |
| | | | SVOS4 | 0.26 | 1.17 | 7.21 | 12.32 | - | |
| | | | SVOS3 | 0.40 | 1.90 | 10.57 | 17.12 | 26.97 | |
| | D1 Standby, D2 Standby, D3 Stop | Flash ON, no IWDG | SVOS5 | 0.06 | 0.20 | 1.18 | 2.05 | - | µA |
| | | | SVOS4 | 0.08 | 0.33 | 1.90 | 3.11 | - | |
| | | | SVOS3 | 0.13 | 0.54 | 2.80 | 4.47 | 6.77 | |

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors.

**Table 44. Typical and maximum current consumption in Sleep mode, LDO regulator (1)**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ (MHz) | Typ | Max(2) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Tj=25 °C | Tj=85 °C | Tj=105 °C | Tj=125 °C | |
| $I_{DD\ (Sleep)}$ | Supply current in Sleep mode | All peripherals disabled | VOS0 | 480 | 50.7 | 96.3 | 253.4 | 366.1 | | mA |
| | | | | 400 | 43.4 | 87.8 | 245.5 | 357.9 | | |
| | | | VOS1 | 400 | 35.3 | 66.5 | 181.3 | 265.8 | 379.6 | |
| | | | | 300 | 27.9 | - | - | - | - | |
| | | | VOS2 | 300 | 24.6 | 47.3 | 139.1 | 207.3 | 300.4 | |
| | | | | 200 | 18.8 | - | - | - | - | |
| | | | VOS3 | 200 | 16.5 | 33.6 | 106.4 | 160.9 | 236.1 | |
| | | All peripherals enabled | VOS0 | 480 | 136.0 | 194.7 | 348.5 | 464.4 | | |
| | | | | 400 | 115.0 | 169.0 | 325.9 | 441.7 | | |
| | | | VOS1 | 400 | 97.7 | 138.2 | 251.3 | 338.4 | 456.4 | |
| | | | | 300 | 74.9 | - | - | - | - | |
| | | | VOS2 | 300 | 67.3 | 95.8 | 187.6 | 257.9 | 354.1 | |
| | | | | 200 | 52.8 | - | - | - | - | |
| | | | VOS3 | 200 | 47.1 | 69.3 | 141.4 | 197.7 | 275.1 | |

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors.
2. Guaranteed by characterization results, unless otherwise specified.

**Table 45. Typical and maximum current consumption in Sleep mode, SMPS regulator(1)**

| Symbol | Parameter | Conditions | | $f_{HCLK}$ (MHz) | Typ | Max | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Tj=25 °C | Tj=85 °C | Tj=105 °C | Tj=125 °C | |
| $I_{DD\ (Sleep)}$ | Supply current in Sleep mode | All peripherals disabled | VOS1 | 400 | 15.93 | 29.69 | 79.01 | 118.72 | 173.80 | mA |
| | | | | 300 | 12.58 | - | - | - | - | |
| | | | VOS2 | 300 | 10.21 | 19.63 | 56.46 | 82.14 | 123.46 | |
| | | | | 200 | 7.89 | - | - | - | - | |
| | | | VOS3 | 200 | 6.50 | 12.98 | 39.73 | 59.35 | 87.10 | |
| | | All peripherals Enabled | VOS1 | 400 | 42.65 | 59.62 | 110.88 | 153.00 | 211.65 | |
| | | | VOS2 | 300 | 27.70 | 38.94 | 75.26 | 102.22 | 147.38 | |
| | | | VOS3 | 200 | 17.95 | 26.14 | 52.75 | 72.95 | 104.09 | |

1. The parameters given in the above table for the SMPS regulator are derived by extrapolation from the LDO consumption and typical SMPS efficiency factors.

**Table 46. Typical and maximum current consumption in Standby**

| Symbol | Parameter | Conditions | | Typ | | | | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 3 V | | | | |
| | | Backup SRAM | RTC and LSE | 1.62 V | 2.4 V | 3 V | 3.3 V | Tj=25 °C | Tj=85 °C | Tj=105 °C | Tj=125 °C | |
| $I_{DD}$ (Standby) | Supply current in Standby mode | OFF | OFF | 1,92 | 1,95 | 2,06 | 2,16 | 4 | 18 | 40 | 90 | µA |
| | | ON | OFF | 3,33 | 3,44 | 3,6 | 3,79 | 8.2 | 47 | 83 | 141 | |
| | | OFF | ON | 2,43 | 2,57 | 2,77 | 2,95 | - | - | - | - | |
| | | ON | ON | 3,82 | 4,05 | 4,31 | 4,55 | - | - | - | - | |

1. Guaranteed by characterization results, unless otherwise specified.

**Table 47. Typical and maximum current consumption in $V_{BAT}$ mode**

| Symbol | Parameter | Conditions | | Typ | | | | Max(1) | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | 3 V | | | | |
| | | Backup SRAM | RTC and LSE | 1.2 V | 2 V | 3 V | 3.4 V | Tj=25 °C | Tj=85 °C | Tj=105 °C | Tj=125 °C | |
| $I_{DD}$ (VBAT) | Supply current in $V_{BAT}$ mode | OFF | OFF | 0,02 | 0,02 | 0,03 | 0,05 | 0,5 | 4,1 | 10 | 24 | µA |
| | | ON | OFF | 1,33 | 1,45 | 1,58 | 1,7 | 4,4 | 22 | 48 | 87 | |
| | | OFF | ON | 0,46 | 0,57 | 0,75 | 0,87 | - | - | - | - | |
| | | ON | ON | 1,77 | 2 | 2,3 | 2,5 | - | - | - | - | |

1. Guaranteed by characterization results, unless otherwise specified.

### Typical SMPS efficiency versus load current and temperature

**Figure 17. Typical SMPS efficiency (%) vs load current (A) in Run mode at $T_J$ = 30 °C**

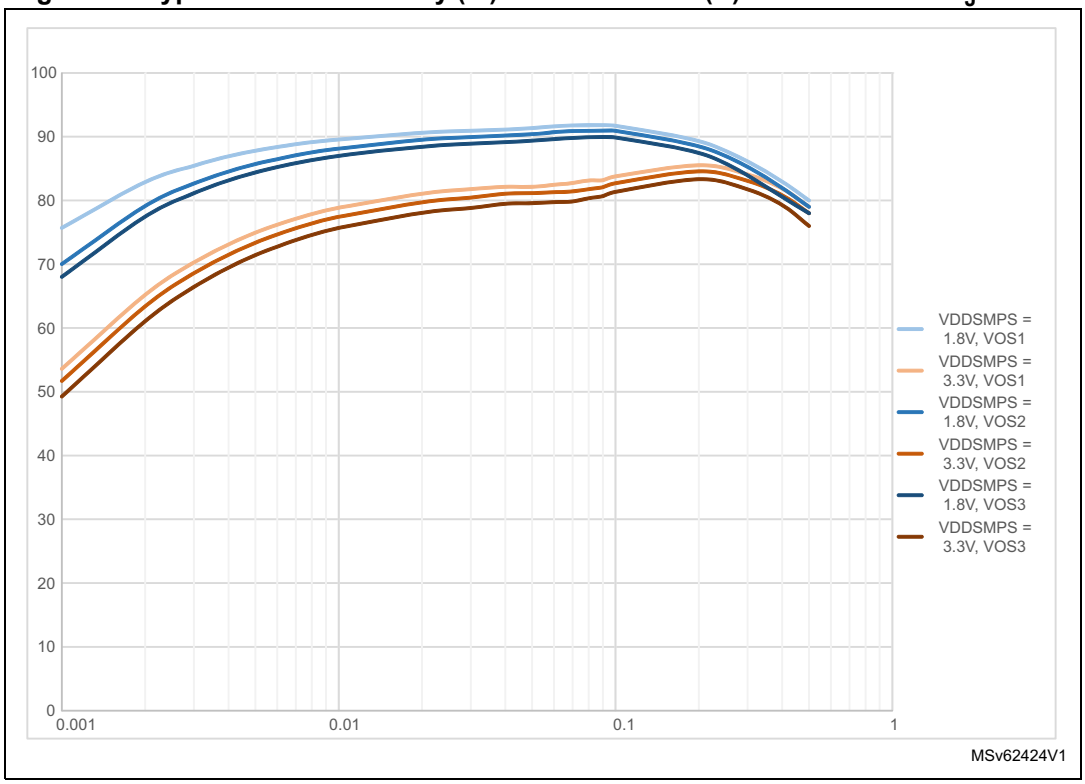



**Figure 18. Typical SMPS efficiency (%) vs load current (A) in Run mode at $T_J = T_{Jmax}$**

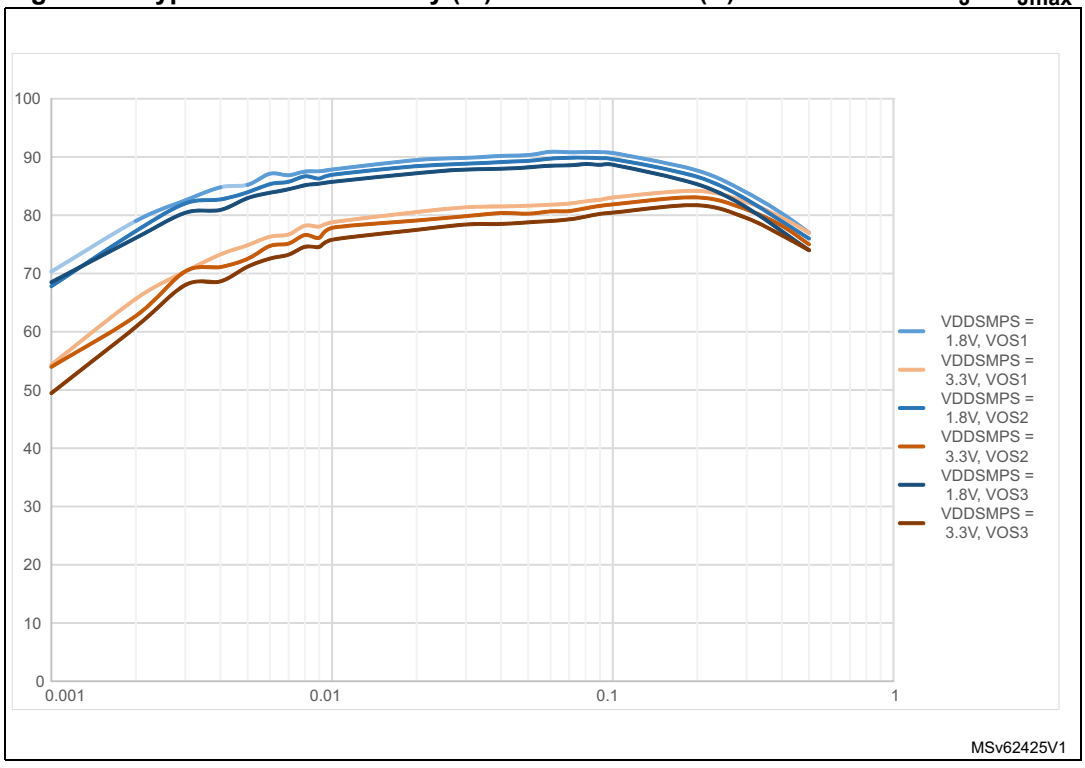


**Figure 19. Typical SMPS efficiency (%) vs load current (A) in low-power mode at $T_J$ = 30 °C**

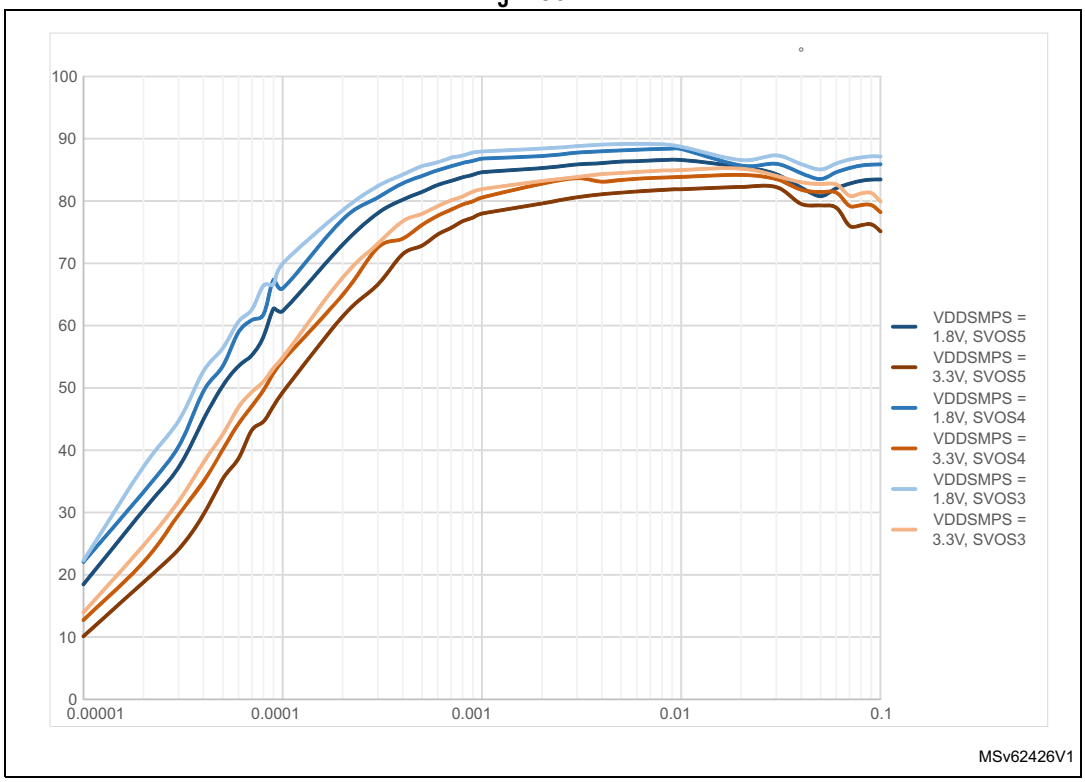
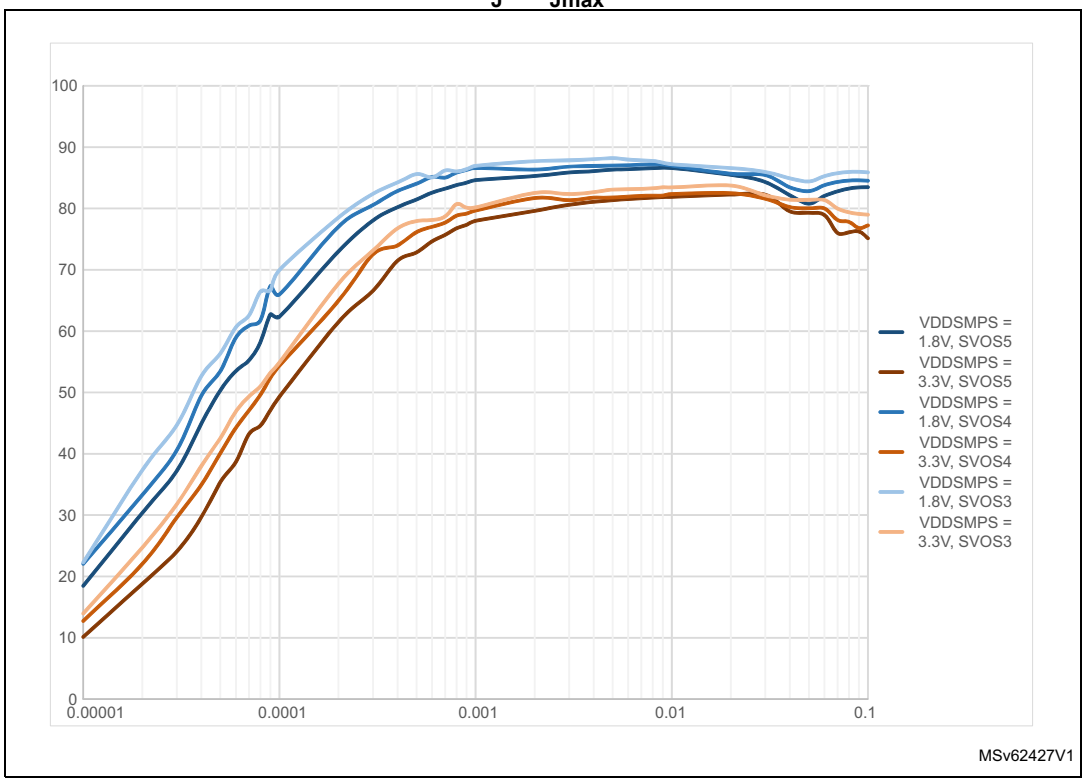


**Figure 20. Typical SMPS efficiency (%) vs load current (A) in low-power mode at $T_J = T_{Jmax}$**




## I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

### I/O static current consumption

All the I/Os used as inputs with pull-up generate a current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 71: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

An additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

**Caution:** Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid a current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

### I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 48: Peripheral current consumption in Run mode*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDx} \times f_{SW} \times C_L$$

where

$I_{SW}$ is the current sunk by a switching I/O to charge/discharge the capacitive load

$V_{DDx}$ is the MCU supply voltage

$f_{SW}$ is the I/O switching frequency

$C_L$ is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

## On-chip peripheral current consumption

The MCU is placed under the following conditions:

- At startup, all I/O pins are in analog input configuration.
- All peripherals are disabled unless otherwise mentioned.
- The I/O compensation cell is enabled.
- $f_{rcc_c_ck}$ is the CPU clock. $f_{PCLK} = f_{rcc_c_ck}/4$, and $f_{HCLK} = f_{rcc_c_ck}/2$.
  The given value is calculated by measuring the difference of current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
  - $f_{rcc_c_ck}$ = 480 MHz (Scale 0), $f_{rcc_c_ck}$ = 400 MHz (Scale 1), $f_{rcc_c_ck}$ = 300 MHz (Scale 2), $f_{rcc_c_ck}$ = 200 MHz (Scale 3)
- The ambient operating temperature is 25 °C and $V_{DD}$=3.3 V.

**Table 48. Peripheral current consumption in Run mode**

| Bus | Peripheral | VOS0 | VOS1 | VOS2 | VOS3 | Unit |
|---|---|---|---|---|---|---|
| AHB3 | MDMA | 4.6 | 3.8 | 3.4 | 3.2 | µA/MHz |
| | DMA2D | 2.9 | 2.4 | 2.1 | 1.9 | |
| | JPGDEC | 4.1 | 3.7 | 3.4 | 3.1 | |
| | FLASH | 17.0 | 15.0 | 14.0 | 12.0 | |
| | FMC registers | 0.9 | 1.1 | 0.9 | 0.8 | |
| | FMC kernel | 7.0 | 6.1 | 5.6 | 5.0 | |
| | QUADSPI registers | 1.5 | 1.5 | 1.4 | 1.3 | |
| | QSPI kernel | 1.0 | 0.9 | 0.8 | 0.7 | |
| | SDMMC1 registers | 8.2 | 7.2 | 6.7 | 6.0 | |
| | SDMMC1 kernel | 1.3 | 1.2 | 0.9 | 0.9 | |
| | DTCM1 | 7.9 | 6.8 | 6.0 | 5.3 | |
| | DTCM2 | 8.3 | 7.2 | 6.4 | 5.7 | |
| | ITCM | 7.0 | 6.3 | 5.6 | 5.1 | |
| | D1SRAM1 | 13.0 | 11.0 | 9.9 | 8.7 | |
| | AHB3 bridge | 35.0 | 32.0 | 29.0 | 26.0 | |
| | **Total AHB3** | **120** | **106** | **96** | **86** | |
| AHB1 | DMA1 | 54.0 | 48.0 | 41.0 | 37.0 | |
| | DMA2 | 55.0 | 49.0 | 42.0 | 37.0 | |
| | ADC12 registers | 4.5 | 4.1 | 3.7 | 3.3 | |
| | ADC12 kernel | 1.0 | 0.7 | 0.4 | 0.6 | |
| | ART accelerator | 4.1 | 3.7 | 3.2 | 2.9 | |
| | ETH1MAC | 17.0 | 15.0 | 14.0 | 12.0 | |
| | ETH1TX | 0.1 | 0.1 | 0.1 | 0.1 | |
| | ETH1RX | 0.1 | 0.1 | 0.1 | 0.1 | |
| | USB1 OTG registers | 23.0 | 21.0 | 19.0 | 17.0 | |
| | USB1 OTG kernel | 8.2 | 0.5 | 8.3 | 8.2 | |
| | USB1 ULPI | 0.1 | 0.1 | 0.1 | 0.1 | |
| | USB2 OTG registers | 21.0 | 19.0 | 17.0 | 15.0 | |
| | USB2 OTG kernel | 8.5 | 0.4 | 8.6 | 8.3 | |
| | USB2 ULPI | 23.0 | 19.0 | 20.0 | 19.0 | |
| | AHB1 bridge | 0.1 | 0.1 | 0.1 | 0.1 | |
| | **Total AHB1** | **220** | **181** | **178** | **161** | |

**Table 48. Peripheral current consumption in Run mode (continued)**

| Bus | Peripheral | VOS0 | VOS1 | VOS2 | VOS3 | Unit |
|---|---|---|---|---|---|---|
| AHB2 | DCMI | 2.1 | 1.9 | 1.8 | 1.6 | µA/MHz |
| | RNG registers | 1.7 | 2.0 | 1.3 | 1.2 | |
| | RNG kernel | 11.0 | 0.1 | 9.7 | 9.4 | |
| | SDMMC2 registers | 47.0 | 41.0 | 37.0 | 34.0 | |
| | SDMMC2 kernel | 1.7 | 1.2 | 1.1 | 1.0 | |
| | D2SRAM1 | 5.7 | 4.9 | 4.4 | 3.9 | |
| | D2SRAM2 | 5.2 | 4.5 | 4.0 | 3.5 | |
| | D2SRAM3 | 4.1 | 3.6 | 3.2 | 2.8 | |
| | AHB2 bridge | 0.1 | 0.1 | 0.1 | 0.1 | |
| | **Total AHB2** | **79** | **60** | **63** | **58** | |
| AHB4 | GPIOA | 1.5 | 1.3 | 1.3 | 1.1 | |
| | GPIOB | 1.2 | 1.0 | 1.0 | 0.9 | |
| | GPIOC | 0.8 | 0.7 | 0.7 | 0.6 | |
| | GPIOD | 1.1 | 1.0 | 1.0 | 0.9 | |
| | GPIOE | 0.7 | 0.7 | 0.7 | 0.6 | |
| | GPIOF | 0.8 | 0.8 | 0.7 | 0.6 | |
| | GPIOG | 0.9 | 0.8 | 0.8 | 0.7 | |
| | GPIOH | 1.1 | 1.0 | 1.0 | 0.9 | |
| | GPIOI | 0.9 | 0.9 | 0.8 | 0.7 | |
| | GPIOJ | 0.8 | 0.8 | 0.7 | 0.7 | |
| | GPIOK | 0.7 | 0.8 | 0.7 | 0.6 | |
| | CRC | 0.4 | 0.5 | 0.4 | 0.3 | |
| | BDMA | 6.6 | 5.9 | 5.3 | 4.8 | |
| | ADC3 registers | 1.7 | 1.5 | 1.2 | 1.2 | |
| | ADC3 kernel | 0.4 | 0.3 | 0.5 | 0.2 | |
| | BKPRAM | 2.3 | 1.9 | 1.7 | 1.5 | |
| | AHB4 bridge | 0.1 | 0.1 | 0.1 | 0.1 | |
| | **Total AHB4** | **22** | **20** | **19** | **16** | |
| APB3 | WWDG1 | 0.7 | 0.5 | 0.5 | 0.2 | µA/MHz |
| | LCD-TFT | 81.0 | 36.0 | 33.0 | 30.0 | |
| | DSI registers | 4.7 | 4.2 | 4.0 | 3.6 | |
| | DSI kernel | 0.1 | 0.1 | 0.1 | 0.1 | |
| | APB3 bridge | 0.3 | 0.2 | 0.1 | 0.1 | |
| | **Total APB3** | **87** | **41** | **38** | **34** | |

**Table 48. Peripheral current consumption in Run mode (continued)**

| Bus | Peripheral | VOS0 | VOS1 | VOS2 | VOS3 | Unit |
|---|---|---|---|---|---|---|
| APB1 | TIM2 | 7.7 | 3.6 | 3.3 | 3.0 | µA/MHz |
| | TIM3 | 6.7 | 3.2 | 3.0 | 2.7 | |
| | TIM4 | 6.3 | 3.1 | 2.8 | 2.5 | |
| | TIM5 | 7.4 | 3.5 | 3.2 | 2.8 | |
| | TIM6 | 1.4 | 0.7 | 0.8 | 0.6 | |
| | TIM7 | 1.4 | 0.7 | 0.7 | 0.6 | |
| | TIM12 | 3.2 | 1.5 | 1.5 | 1.3 | |
| | TIM13 | 2.3 | 1.1 | 1.1 | 0.9 | |
| | TIM14 | 2.1 | 1.1 | 1.1 | 0.9 | |
| | LPTIM1 registers | 0.7 | 0.5 | 0.8 | 0.7 | |
| | LPTIM1 kernel | 2.4 | 2.3 | 1.9 | 1.7 | |
| | WWDG2 | 0.6 | 0.5 | 0.5 | 0.4 | |
| | SPI2 registers | 2.0 | 1.8 | 1.7 | 1.4 | |
| | SPI2 kernel | 0.8 | 0.6 | 0.5 | 0.6 | |
| | SPI3 registers | 1.8 | 1.6 | 1.6 | 1.3 | |
| | SPI3 kernel | 0.7 | 0.9 | 0.7 | 0.7 | |
| | SPDIFRX1 registers | 0.5 | 0.7 | 0.7 | 0.6 | |
| | SPDIFRX1 kernel | 3.5 | 2.8 | 2.4 | 2.2 | |
| | USART2 registers | 1.9 | 1.7 | 1.4 | 1.3 | |
| | USART2 kernel | 4.3 | 3.9 | 3.6 | 3.2 | |
| | USART3 registers | 1.9 | 1.7 | 1.4 | 1.3 | |
| | USART3 kernel | 4.4 | 3.9 | 3.5 | 3.2 | |
| | UART4 registers | 1.7 | 1.5 | 1.4 | 1.4 | |
| | UART4 kernel | 3.9 | 3.4 | 3.1 | 2.8 | |
| | UART5 registers | 1.6 | 1.4 | 1.4 | 1.3 | |
| | UART5 kernel | 3.8 | 3.4 | 3.0 | 2.7 | |
| | I2C1 registers | 1.1 | 0.8 | 0.9 | 0.8 | |
| | I2C1 kernel | 2.5 | 2.3 | 2.0 | 1.9 | |
| | I2C2 registers | 1.0 | 0.8 | 0.9 | 0.8 | |

**Table 48. Peripheral current consumption in Run mode (continued)**

| Bus | Peripheral | VOS0 | VOS1 | VOS2 | VOS3 | Unit |
|---|---|---|---|---|---|---|
| APB1 (continued) | I2C2 kernel | 2.3 | 2.2 | 1.9 | 1.7 | µA/MHz |
| | I2C3 registers | 0.8 | 1.0 | 0.8 | 0.8 | |
| | I2C3 kernel | 2.4 | 1.9 | 1.8 | 1.6 | |
| | HDMI-CEC registers | 0.7 | 0.5 | 0.6 | 0.5 | |
| | HDMI-CEC kernel | 0.1 | 0.1 | 3.2 | 0.1 | |
| | DAC12 | 3.6 | 1.3 | 1.2 | 1.0 | |
| | USART7 registers | 1.8 | 1.8 | 1.6 | 1.4 | |
| | USART7 kernel | 4.0 | 3.3 | 3.0 | 2.8 | |
| | USART8 registers | 2.0 | 1.6 | 1.6 | 1.4 | |
| | USART8 kernel | 3.9 | 3.4 | 3.1 | 2.8 | |
| | CRS | 6.4 | 5.5 | 5.0 | 4.5 | |
| | SWPMI registers | 2.7 | 2.4 | 2.3 | 1.9 | |
| | SWPMI kernel | 0.1 | 0.1 | 0.1 | 0.1 | |
| | OPAMP | 0.2 | 0.3 | 0.3 | 0.2 | |
| | MDIO | 3.3 | 2.9 | 2.6 | 2.3 | |
| | FDCAN registers | 19.0 | 17.0 | 15.0 | 13.0 | |
| | FDCAN kernel | 9.1 | 7.9 | 6.9 | 6.4 | |
| | APB1 bridge | 0.1 | 0.1 | 0.1 | 0.1 | |
| | **Total APB1** | **142** | **108** | **102** | **88** | |
| APB2 | TIM1 | 11.0 | 5.0 | 4.5 | 4.0 | |
| | TIM8 | 10.0 | 4.7 | 4.3 | 3.8 | |
| | USART1 registers | 3.6 | 2.5 | 2.7 | 2.9 | |
| | USART1 kernel | 0.1 | 0.1 | 0.1 | 0.1 | |
| | USART6 registers | 4.5 | 3.0 | 3.1 | 3.4 | |
| | USART6 kernel | 0.1 | 0.1 | 0.1 | 0.1 | |
| | SPI1 registers | 2.0 | 1.7 | 1.6 | 1.4 | |
| | SPI1 kernel | 0.9 | 0.8 | 0.7 | 0.6 | |
| | SPI4 registers | 2.1 | 1.7 | 1.6 | 1.5 | |
| | SPI4 kernel | 0.6 | 0.5 | 0.5 | 0.3 | |
| | TIM15 | 5.5 | 2.5 | 2.3 | 2.1 | |
| | TIM16 | 4.1 | 2.0 | 1.8 | 1.7 | |
| | TIM17 | 4.1 | 1.9 | 1.8 | 1.6 | |
| | SPI5 registers | 2.0 | 1.8 | 1.6 | 1.3 | |
| | SPI5 kernel | 0.5 | 0.4 | 0.4 | 0.5 | |
| | SAI1 registers | 1.3 | 1.1 | 1.1 | 1.0 | |

**Table 48. Peripheral current consumption in Run mode (continued)**

| Bus | Peripheral | VOS0 | VOS1 | VOS2 | VOS3 | Unit |
|---|---|---|---|---|---|---|
| APB2 (continued) | SAI1 kernel | 1.4 | 1.1 | 1.0 | 0.8 | µA/MHz |
| | SAI2 registers | 1.5 | 1.3 | 1.2 | 1.0 | |
| | SAI2 kernel | 1.1 | 1.0 | 0.9 | 0.9 | |
| | SAI3 registers | 1.6 | 1.3 | 1.1 | 1.0 | |
| | SAI3 kernel | 1.1 | 1.2 | 1.1 | 0.9 | |
| | DFSDM1 registers | 6.5 | 5.8 | 5.2 | 4.7 | |
| | DFSDM1 kernel | 0.3 | 0.2 | 0.2 | 0.4 | |
| | HRTIM | 84.0 | 39.0 | 35.0 | 32.0 | |
| | APB2 bridge | 0.2 | 0.1 | 0.1 | 0.2 | |
| | **Total APB2** | **150** | **81** | **74** | **68** | |
| APB4 | SYSCFG | 0.9 | 1.0 | 0.7 | 0.8 | |
| | LPUART1 registers | 1.1 | 1.3 | 1.0 | 0.8 | |
| | LPUART1 kernel | 2.9 | 2.2 | 2.2 | 2.1 | |
| | SPI6 registers | 1.8 | 1.6 | 1.4 | 1.3 | |
| | SPI6 kernel | 0.4 | 0.4 | 0.5 | 0.3 | |
| | I2C4 registers | 0.9 | 0.7 | 0.7 | 0.4 | |
| | I2C4 kernel | 2.2 | 2.1 | 1.9 | 1.8 | |
| | LPTIM2 registers | 0.8 | 0.6 | 0.7 | 0.5 | |
| | LPTIM2 kernel | 2.3 | 2.1 | 1.8 | 1.4 | |
| | LPTIM3 registers | 0.7 | 0.7 | 0.7 | 0.4 | |
| | LPTIM3 kernel | 2.1 | 1.7 | 1.6 | 1.5 | |
| | LPTIM4 registers | 0.8 | 0.4 | 0.6 | 0.4 | |
| | LPTIM4 kernel | 2.2 | 2.0 | 1.7 | 1.5 | |
| | LPTIM5 registers | 0.5 | 0.4 | 0.6 | 0.4 | |
| | LPTIM5 kernel | 2.0 | 1.8 | 1.5 | 1.2 | |
| | COMP12 | 0.6 | 0.4 | 0.5 | 0.2 | |
| | VREF | 0.4 | 0.2 | 0.2 | 0.1 | |
| | RTC | 1.1 | 0.9 | 1.0 | 0.6 | |
| | SAI4 registers | 1.7 | 1.4 | 1.3 | 1.0 | |
| | SAI4 kernel | 2.0 | 2.0 | 1.8 | 1.6 | |
| | APB4 bridge | 0.1 | 0.1 | 0.1 | 0.1 | |
| | **Total APB4** | **28** | **24.4** | **22.4** | **18.9** | |

### 6.3.8 Wakeup time from low-power modes

The wakeup times given in *Table 49* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PC1) pin is used to wakeup from Standby, Stop and Sleep modes.

All timings are derived from tests performed under ambient temperature and $V_{DD}$=3.3 V.

**Table 49. Low-power mode wakeup timings(1)**

| Symbol | Parameter | Conditions | Typ(2) | Max(2) | Unit |
|---|---|---|---|---|---|
| $t_{WUSLEEP}$(3) | Wakeup from Sleep | - | 9 | 10 | CPU clock cycles |
| $t_{WUSTOP}$(3) | Wakeup from Stop | VOS3, HSI, Flash memory in normal mode | 4.4 | 5.6 | µs |
| | | VOS3, HSI, Flash memory in low-power mode | 12 | 15 | |
| | | VOS4, HSI, Flash memory in normal mode | 15 | 20 | |
| | | VOS4, HSI, Flash memory in low-power mode | 23 | 28 | |
| | | VOS5, HSI, Flash memory in normal mode | 39 | 71 | |
| | | VOS5, HSI, Flash memory in low-power mode | 39 | 47 | |
| | | VOS3, CSI, Flash memory in normal mode | 30 | 37 | |
| | | VOS3, CSI, Flash memory in low power mode | 36 | 50 | |
| | | VOS4, CSI, Flash memory in normal mode | 38 | 48 | |
| | | VOS4, CSI, Flash memory in low-power mode | 47 | 61 | |
| | | VOS5, CSI, Flash memory in normal mode | 68 | 75 | |
| | | VOS5, CSI, Flash memory in low-power mode | 68 | 77 | |
| $t_{WUSTOP_KERON}$(3) | Wakeup from Stop, clock kept running | VOS3, HSI, Flash memory in normal mode | 2.6 | 3.4 | |
| | | VOS3, CSI, Flash memory in normal mode | 26 | 36 | |
| $t_{WUSTDBY}$(3) | Wakeup from Standby mode | - | 390 | 500 | |

1. The wakeup timings is valid for both CPUs.
2. Guaranteed by characterization results.
3. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

### 6.3.9 External clock source characteristics

#### High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard I/O.

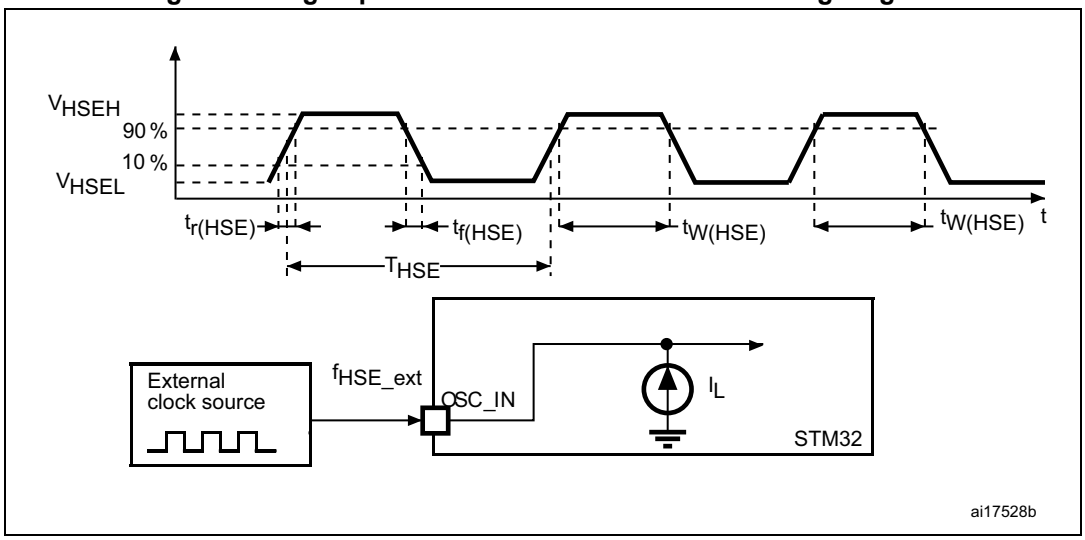
The external clock signal has to respect the *Table 71: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 21*.

**Table 50. High-speed external user clock characteristics(1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{HSE_ext}$ | User external clock source frequency | 4 | 25 | 50 | MHz |
| $V_{SW}$ ($V_{HSEH}$–$V_{HSEL}$) | OSC_IN amplitude | $0.7V_{DD}$ | - | $V_{DD}$ | V |
| $V_{DC}$ | OSC_IN input voltage | $V_{SS}$ | - | $0.3V_{SS}$ | |
| $t_{W(HSE)}$ | OSC_IN high or low time | 7 | - | - | ns |

1. Guaranteed by design.

**Figure 21. High-speed external clock source AC timing diagram**



### Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard I/O. The external clock signal has to respect the *Table 71: I/O static characteristics*. However, the recommended clock input waveform is shown in *Figure 22*.

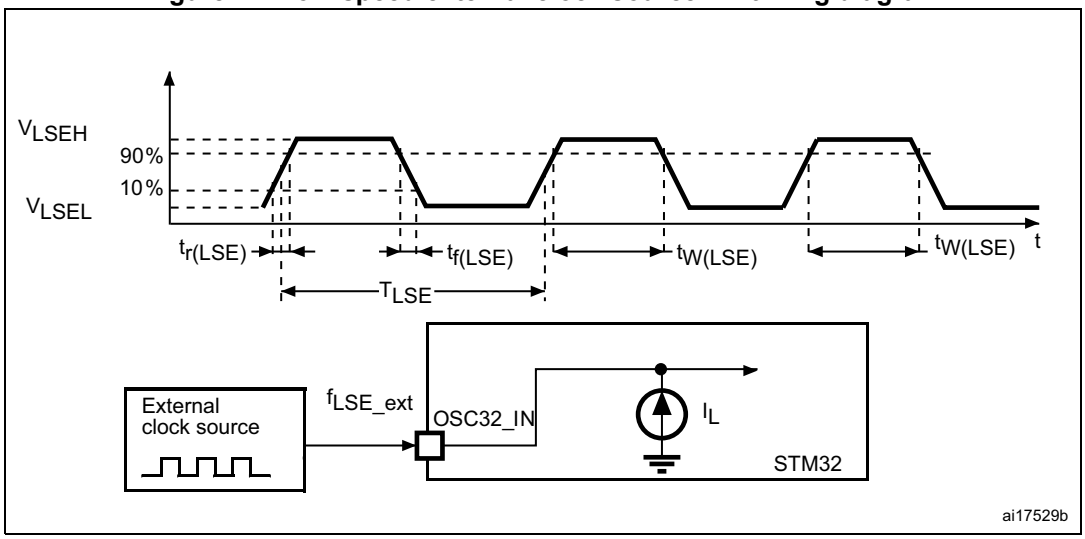
**Table 51. Low-speed external user clock characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSE_ext}$ | User external clock source frequency | - | - | 32.768 | 1000 | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | - | 0.7 $V_{DDIOx}$ | - | $V_{DDIOx}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low level voltage | - | $V_{SS}$ | - | 0.3 $V_{DDIOx}$ | |
| $t_{w(LSEH)}$ $t_{w(LSEL)}$ | OSC32_IN high or low time | - | 250 | - | - | ns |

1. Guaranteed by design.

*Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 22. Low-speed external clock source AC timing diagram**



### High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 52*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 52. 4-48 MHz HSE oscillator characteristics(1)**

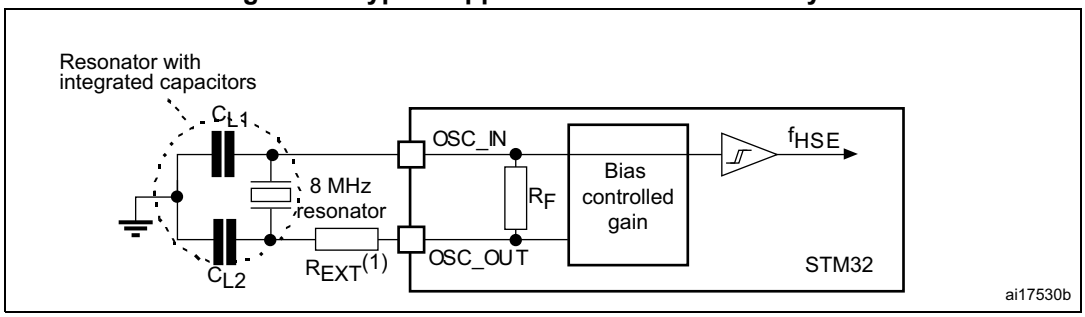
| Symbol | Parameter | Operating conditions(2) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| F | Oscillator frequency | - | 4 | - | 48 | MHz |
| $R_F$ | Feedback resistor | - | - | 200 | - | kΩ |
| $I_{DD(HSE)}$ | HSE current consumption | During startup(3) | - | - | 4 | mA |
| | | $V_{DD}$=3 V, Rm=30 Ω $C_L$=10pF@4MHz | - | 0.35 | - | |
| | | $V_{DD}$=3 V, Rm=30 Ω $C_L$=10 pF at 8 MHz | - | 0.40 | - | |
| | | $V_{DD}$=3 V, Rm=30 Ω $C_L$=10 pF at 16 MHz | - | 0.45 | - | |
| | | $V_{DD}$=3 V, Rm=30 Ω $C_L$=10 pF at 32 MHz | - | 0.65 | - | |
| | | $V_{DD}$=3 V, Rm=30 Ω $C_L$=10 pF at 48 MHz | - | 0.95 | - | |
| $Gm_{critmax}$ | Maximum critical crystal gm | Startup | - | - | 1.5 | mA/V |
| $t_{SU}$(4) | Start-up time | $V_{DD}$ is stabilized | - | 2 | - | ms |

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For $C_{L1}$ and $C_{L2}$, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typical), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 23*). $C_{L1}$ and $C_{L2}$ are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of $C_{L1}$ and $C_{L2}$. The PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing $C_{L1}$ and $C_{L2}$.

*Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 23. Typical application with an 8 MHz crystal**




1. $R_{EXT}$ value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 53*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

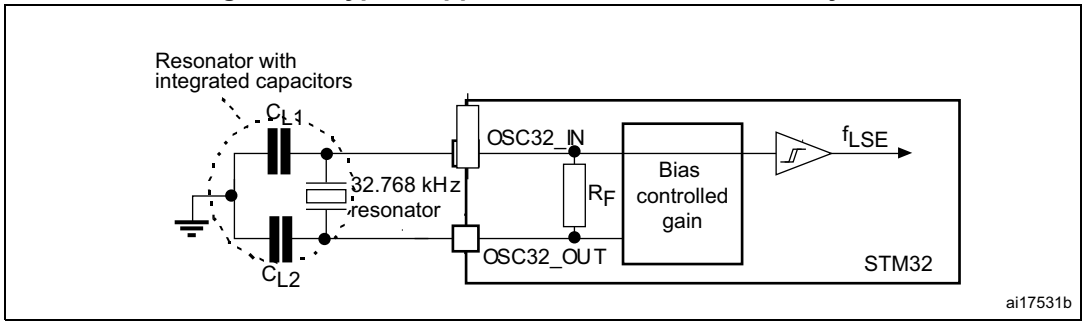
**Table 53. Low-speed external user clock characteristics(1)**

| Symbol | Parameter | Operating conditions(2) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| F | Oscillator frequency | - | - | 32.768 | - | kHz |
| $I_{DD}$ | LSE current consumption | LSEDRV[1:0] = 00, Low drive capability | - | 290 | - | nA |
| | | LSEDRV[1:0] = 01, Medium Low drive capability | - | 390 | - | |
| | | LSEDRV[1:0] = 10, Medium high drive capability | - | 550 | - | |
| | | LSEDRV[1:0] = 11, High drive capability | - | 900 | - | |
| $Gm_{critmax}$ | Maximum critical crystal gm | LSEDRV[1:0] = 00, Low drive capability | - | - | 0.5 | µA/V |
| | | LSEDRV[1:0] = 01, Medium Low drive capability | - | - | 0.75 | |
| | | LSEDRV[1:0] = 10, Medium high drive capability | - | - | 1.7 | |
| | | LSEDRV[1:0] = 11, High drive capability | - | - | 2.7 | |
| $t_{SU}$(3) | Startup time | VDD is stabilized | - | 2 | - | s |

1. Guaranteed by design.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers.
3. $t_{SU}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768k Hz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

*Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

**Figure 24. Typical application with a 32.768 kHz crystal**




1. *An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.*

## 6.3.10 Internal clock source characteristics

The parameters given in *Table 54* to *Table 57* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*.

### 48 MHz high-speed internal RC oscillator (HSI48)

**Table 54. HSI48 oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI48}$ | HSI48 frequency | $V_{DD}$=3.3 V, TJ=30 °C | 47.5(1) | 48 | 48.5(1) | MHz |
| TRIM(2) | USER trimming step | - | - | 0.175 | - | % |
| USER TRIM COVERAGE(3) | USER TRIMMING Coverage | ± 32 steps | ±4.79 | ±5.60 | - | % |
| DuCy(HSI48)(2) | Duty Cycle | - | 45 | - | 55 | % |
| ACCHSI48_REL(3)(4) | Accuracy of the HSI48 oscillator over temperature (factory calibrated) | $T_J$=-40 to 125 °C | –4.5 | - | 3.5 | % |
| $\Delta_{VDD}$(HSI48)(3) | HSI48 oscillator frequency drift with $V_{DD}$(5) | $V_{DD}$=3 to 3.6 V | - | 0.025 | 0.05 | % |
| | | $V_{DD}$=1.62 V to 3.6 V | - | 0.05 | 0.1 | |
| $t_{su(HSI48)}$(2) | HSI48 oscillator start-up time | - | - | 2.1 | 4.0 | µs |
| $I_{DD(HSI48)}$(2) | HSI48 oscillator power consumption | - | - | 350 | 400 | µA |
| $N_T$ jitter | Next transition jitter<br>Accumulated jitter on 28 cycles(6) | - | - | ± 0.15 | - | ns |
| $P_T$ jitter | Paired transition jitter<br>Accumulated jitter on 56 cycles(6) | - | - | ± 0.25 | - | ns |

1. Guaranteed by test in production.
2. Guaranteed by design.
3. Guaranteed by characterization.
4. ΔfHSI = ACCHSI48_REL + $\Delta_{VDD}$.

5. These values are obtained by using the formula: (Freq(3.6V) - Freq(3.0V)) / Freq(3.0V) or (Freq(3.6V) - Freq(1.62V)) / Freq(1.62V).
6. Jitter measurements are performed without clock source activated in parallel.

### 64 MHz high-speed internal RC oscillator (HSI)

**Table 55. HSI oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{HSI}$ | HSI frequency | $V_{DD}$=3.3 V, $T_J$=30 °C | 63.7(2) | 64 | 64.3(2) | MHz |
| TRIM | HSI user trimming step | Trimming is not a multiple of 32 | - | 0.24 | 0.32 | % |
| | | Trimming is 128, 256 and 384 | −5.2 | −1.8 | - | |
| | | Trimming is 64, 192, 320 and 448 | −1.4 | −0.8 | - | |
| | | Other trimming are a multiple of 32 (not including multiple of 64 and 128) | −0.6 | −0.25 | - | |
| DuCy(HSI) | Duty Cycle | - | 45 | - | 55 | % |
| $\Delta_{VDD\ (HSI)}$ | HSI oscillator frequency drift over $V_{DD}$ (reference is 3.3 V) | $V_{DD}$=1.62 to 3.6 V | −0.12 | - | 0.03 | % |
| $\Delta_{TEMP\ (HSI)}$ | HSI oscillator frequency drift over temperature (reference is 64 MHz) | $T_J$=-20 to 105 °C | −1(3) | - | 1(3) | % |
| | | $T_J$=−40 to $T_J$max °C | −2(3) | - | 1(3) | |
| $t_{su}$(HSI) | HSI oscillator start-up time | - | - | 1.4 | 2 | µs |
| $t_{stab}$(HSI) | HSI oscillator stabilization time | at 1% of target frequency | - | 4 | 8 | µs |
| $I_{DD}$(HSI) | HSI oscillator power consumption | - | - | 300 | 400 | µA |

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by test in production.
3. Guaranteed by characterization.

### 4 MHz low-power internal RC oscillator (CSI)

**Table 56. CSI oscillator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CSI}$ | CSI frequency | $V_{DD}$=3.3 V, $T_J$=30 °C | 3.96(2) | 4 | 4.04(2) | MHz |
| TRIM | Trimming step | - | - | 0.35 | - | % |
| DuCy(CSI) | Duty Cycle | - | 45 | - | 55 | % |
| $\Delta_{TEMP}$ (CSI) | CSI oscillator frequency drift over temperature | $T_J$ = 0 to 85 °C | - | −3.7(3) | 4.5(3) | % |
| | | $T_J$ = −40 to 125 °C | - | −11(3) | 7.5(3) | |
| $D_{VDD}$ (CSI) | CSI oscillator frequency drift over $V_{DD}$ | $V_{DD}$ = 1.62 to 3.6 V | - | −0.06 | 0.06 | % |

**Table 56. CSI oscillator characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{su(CSI)}$ | CSI oscillator startup time | - | - | 1 | 2 | µs |
| $t_{stab(CSI)}$ | CSI oscillator stabilization time (to reach ±3% of $f_{CSI}$) | - | - | - | 4 | cycle |
| $I_{DD(CSI)}$ | CSI oscillator power consumption | - | - | 23 | 30 | µA |

1. Guaranteed by design.
2. Guaranteed by test in production.
3. Guaranteed by characterization.

## Low-speed internal (LSI) RC oscillator

**Table 57. LSI oscillator characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LSI}$ | LSI frequency | $V_{DD}$ = 3.3 V, $T_J$ = 25 °C | 31.4(1) | 32 | 32.6(1) | kHz |
| | | $T_J$ = –40 to 110 °C, $V_{DD}$ = 1.62 to 3.6 V | 29.76(2) | - | 33.6(2) | |
| | | $T_J$ = –40 to 125 °C, $V_{DD}$ = 1.62 to 3.6 V | 29.4 | - | 33.6 | |
| $t_{su(LSI)}$(3) | LSI oscillator startup time | - | - | 80 | 130 | µs |
| $t_{stab(LSI)}$(3) | LSI oscillator stabilization time (5% of final value) | - | - | 120 | 170 | |
| $I_{DD(LSI)}$(3) | LSI oscillator power consumption | - | - | 130 | 280 | nA |

1. Guaranteed by test in production.
2. Guaranteed by characterization results.
3. Guaranteed by design.

### 6.3.11 PLL characteristics

The parameters given in *Table 58* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 58. PLL characteristics (wide VCO frequency range)(1)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{PLL_IN}$ | PLL input clock | - | | 2 | - | 16 | MHz |
| | PLL input clock duty cycle | - | | 10 | - | 90 | % |
| $f_{PLL_P_OUT}$ | PLL multiplier output clock P | VOS0 | | 1.5 | - | 480(2) | MHz |
| | | VOS1 | | 1.5 | - | 400(2) | |
| | | VOS2 | | 1.5 | - | 300(2) | |
| | | VOS3 | | 1.5 | - | 200(2) | |
| $f_{VCO_OUT}$ | PLL VCO output | - | | 192 | - | 960 | |
| $t_{LOCK}$ | PLL lock time | Normal mode | | - | 50(3) | 150(3) | µs |
| | | Sigma-delta mode (CKIN ≥ 8 MHz) | | - | 58(3) | 166(3) | |
| Jitter | Cycle-to-cycle jitter(4) | - | VCO = 192 MHz | - | 134 | - | ±ps |
| | | | VCO = 200 MHz | - | 134 | - | |
| | | | VCO = 400 MHz | - | 76 | - | |
| | | | VCO = 800 MHz | - | 39 | - | |
| | Long term jitter | Normal mode | VCO = 800 MHz | - | ±0.7 | - | % |
| | | Sigma-delta mode (CKIN = 16 MHz) | VCO = 800 MHz | - | ±0.8 | - | |
| $I_{DD(PLL)}$(3) | PLL power consumption on $V_{DD}$ | VCO freq = 836 MHz | $V_{DDA}$ | - | 590 | 1500 | µA |
| | | | $V_{CORE}$ | - | 720 | - | |
| | | VCO freq = 192 MHz | $V_{DDA}$ | - | 180 | 600 | |
| | | | $V_{CORE}$ | - | 280 | - | |

1. Guaranteed by design unless otherwise specified.
2. This value must be limited to the maximum frequency due to the product limitation (480 MHz for VOS0, 400 MHz for VOS1, 300 MHz for VOS2, 200 MHz for VOS3).
3. Guaranteed by characterization results.
4. Integer mode only.

**Table 59. PLL characteristics (medium VCO frequency range)(1)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{PLL_IN}$ | PLL input clock | - | | 1 | - | 2 | MHz |
| | PLL input clock duty cycle | - | | 10 | - | 90 | % |
| $f_{PLL_OUT}$ | PLL multiplier output clock P, Q, R | VOS1 | | 1.17 | - | 210 | MHz |
| | | VOS2 | | 1.17 | - | 210 | |
| | | VOS3 | | 1.17 | - | 200 | |
| $f_{VCO_OUT}$ | PLL VCO output | - | | 150 | - | 420 | |
| $t_{LOCK}$ | PLL lock time | Normal mode | | - | 60(2) | 100(2) | µs |
| | | Sigma-delta mode | | forbidden | | | |
| Jitter | Cycle-to-cycle jitter(3) | - | VCO = 150 MHz | - | 145 | - | ±ps |
| | | | VCO = 300 MHz | - | 91 | - | |
| | | | VCO = 400 MHz | - | 64 | - | |
| | | | VCO = 420 MHz | - | 63 | - | |
| | Period jitter | $f_{PLL_OUT}$ = 50 MHz | VCO = 150 MHz | - | 55 | - | ±-ps |
| | | | VCO = 400 MHz | - | 30 | - | |
| | Long term jitter | Normal mode | VCO = 400 MHz | - | ±0.3 | - | % |
| I(PLL)(2) | PLL power consumption on $V_{DD}$ | VCO freq = 420MHz | VDD | - | 440 | 1150 | µA |
| | | | VCORE | - | 530 | - | |
| | | VCO freq = 150MHz | VDD | - | 180 | 500 | |
| | | | VCORE | - | 200 | - | |

1. Guaranteed by design unless otherwise specified.
2. Guaranteed by characterization results.
3. Integer mode only.

## 6.3.12 MIPI D-PHY characteristics

The parameters given in *Table 60* and *Table 61* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 60. MIPI D-PHY characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Hi-Speed Input/Output Characteristics | | | | | | |
| $U_{INST}$ | UI instantaneous | - | 2 | - | 12.5 | ns |

**Table 60. MIPI D-PHY characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CMTX}$ | HS transmit common mode voltage | - | 150 | 200 | 250 | mV |
| $\|\Delta V_{CMTX}\|$ | $V_{CMTX}$ mismatch when output is Differential-1 or Differential-0 | - | - | - | 5 | |
| $\|V_{OD}\|$ | HS transmit differential voltage | - | 140 | 200 | 270 | |
| $\|\Delta V_{OD}\|$ | $V_{OD}$ mismatch when output is Differential-1 or Differential-0 | - | - | - | 14 | |
| $V_{OHHS}$ | HS output high voltage | - | - | - | 360 | |
| $Z_{OS}$ | Single ended output impedance | - | 40 | 50 | 62.5 | Ω |
| $\Delta Z_{OS}$ | Single ended output impedance mismatch | - | - | - | 10 | % |
| $t_{HSr}$ & $t_{HSf}$ | 20%-80% rise and fall time | - | 100 | - | 0.35*UI | ps |
| LP Receiver Input Characteristics | | | | | | |
| $V_{IL}$ | Logic 0 input voltage (not in ULP State) | - | - | - | 550 | mV |
| $V_{IL-ULPS}$ | Logic 0 input voltage in ULP State | - | - | - | 300 | |
| $V_{IH}$ | Input high level voltage | - | 880 | - | - | |
| $V_{hys}$ | Voltage hysteresis | - | 25 | - | - | |
| LP Emitter Output Characteristics | | | | | | |
| $V_{IL}$ | Output low level voltage | - | 1.1 | 1.2 | 1.2 | V |
| $V_{IL-ULPS}$ | Output high level voltage | - | -50 | - | 50 | mV |
| $V_{IH}$ | Output impedance of LP transmitter | - | 110 | - | - | Ω |
| $V_{hys}$ | 15%-85% rise and fall time | - | - | - | 25 | ns |
| LP Contention Detector Characteristics | | | | | | |
| $V_{ILCD}$ | Logic 0 contention threshold | - | - | - | 200 | mV |
| $V_{IHCD}$ | Logic 0 contention threshold | - | 450 | - | - | |

1. Guaranteed based on test during characterization.

**Table 61. MIPI D-PHY AC characteristics LP mode and HS/LP transitions(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $T_{LPX}$ | Transmitted length of any Low-Power state period | - | 50 | - | - | ns |
| $T_{CLK-PREPARE}$ | Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | - | 38 | - | 95 | |
| $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | Time that the transmitter drives the HS-0 state prior to starting the clock. | - | 300 | - | - | |
| $T_{CLK-PRE}$ | Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode. | - | 8 | - | - | UI |
| $T_{CLK-POST}$ | Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. | - | 62+52*UI | - | - | ns |
| $T_{CLK-TRAIL}$ | Time that the transmitter drives the HS-0 state after the last payload clock bit of an HS transmission burst. | - | 60 | - | - | |
| $T_{HS-PREPARE}$ | Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission. | - | 40+4*UI | - | 85+6*UI | |
| $T_{HS-PREPARE}$ + $T_{HS-ZERO}$ | $T_{HS-PREPARE+}$ Time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence. | - | 145+10*UI | - | - | |
| $T_{HS-TRAIL}$ | Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst. | - | Max (n*8*UI, 60+n*4*UI) | - | - | |
| $T_{HS-EXIT}$ | Time that the transmitter drives LP-11 following a HS burst. | - | 100 | - | - | |
| $T_{REOT}$ | 30%-85% rise time and fall time | - | - | - | 35 | |
| $T_{EOT}$ | Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst. | - | - | - | 105+ n*12UI | |

1. Guaranteed based on test during characterization.

**Figure 25. MIPI D-PHY HS/LP clock lane transition timing diagram**

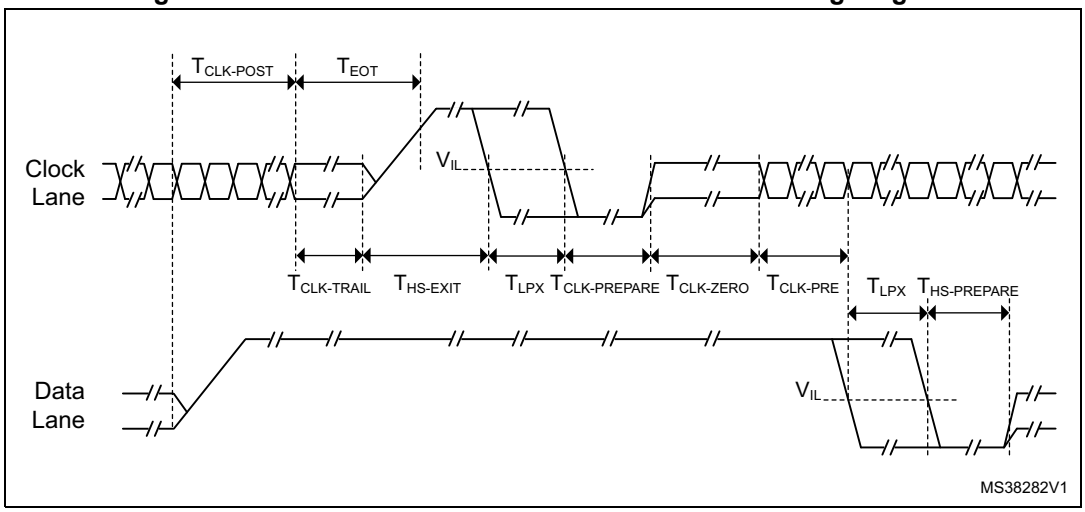
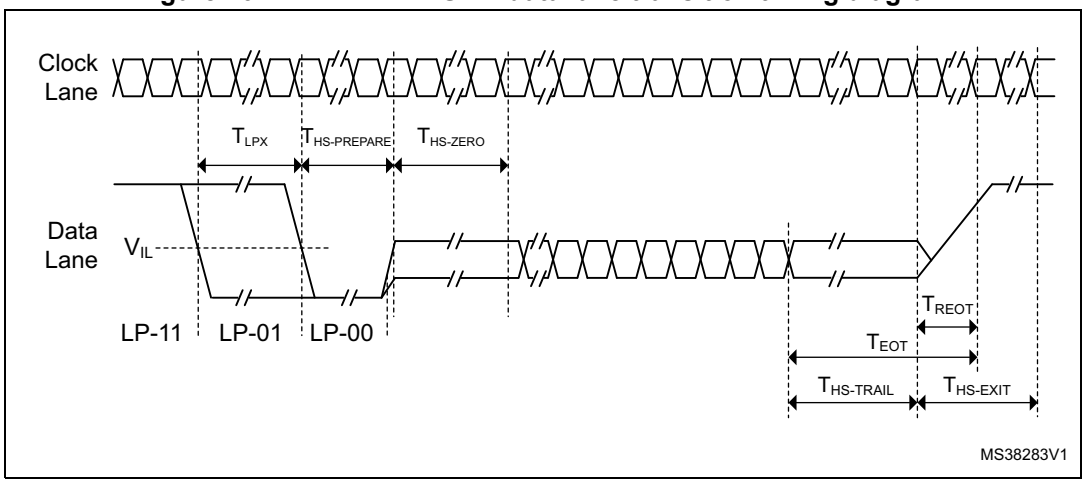



**Figure 26. MIPI D-PHY HS/LP data lane transition timing diagram**




## 6.3.13 MIPI D-PHY regulator characteristics

The parameters given in *Table 62* are derived from tests performed under temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 62. DSI regulator characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDDSI}$ | Regulator output voltage on $V_{DDDSI}$ | - | 1.62 | - | - | V |
| $V_{DD12DSI}$ | 1.2 V internal voltage on $V_{DD12DSI}$ | - | 1.15 | 1.20 | 1.26 | |
| $C_{EXT}$ | External capacitor on $V_{CAPDSI}$ | - | 0.5 | 2.2(2) | 3.3 | µF |
| ESR | External serial resistor | - | 0 | 25 | 600 | mΩ |
| $I_{LOAD}$ | Static load current | - | - | - | 50 | mA |
| $I_{DDDSIREG}$ | Regulator power consumption on $V_{DDDSI}$ | $I_{LOAD}$ = 0 mA | 110 | 170 | 220 | µA |
| | | $I_{LOAD}$ = 50 mA | 140 | 200 | 260 | |

**Table 62. DSI regulator characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{WAKEUP}$ | Startup delay | $C_{EXT}$ = 2.2 µF | - | 80 | - | µs |
| | | $C_{EXT}$ = 3.3 µF | - | - | 160 | |
| $I_{INRUSH}$ | Inrush current on $V_{DDDSI}$ | External capacitor load at start | - | 60 | 250 | mA |

1. Based on test during characterization.
2. $C_{EXT}$ recommended value is 2.2 µF to achieve a better dynamic performance of the regulator. A 1 µF capacitor can be used only if the minimum value does not drop below 0.5 µF.

## 6.3.14 Memory characteristics

### Flash memory

The characteristics are given at $T_J$ = –40 to 125 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

**Table 63. Flash memory characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply current | Write / Erase 8-bit mode | - | 6.5 | - | mA |
| | | Write / Erase 16-bit mode | - | 11.5 | - | |
| | | Write / Erase 32-bit mode | - | 20 | - | |
| | | Write / Erase 64-bit mode | - | 35 | - | |

**Table 64. Flash memory programming (single bank configuration nDBANK=1)**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $t_{prog}$ | Word (266 bits) programming time | Program/erase parallelism x 8 | - | 290 | 580(2) | µs |
| | | Program/erase parallelism x 16 | - | 180 | 360 | |
| | | Program/erase parallelism x 32 | - | 130 | 260 | |
| | | Program/erase parallelism x 64 | - | 100 | 200 | |
| $t_{ERASE128KB}$ | Sector (128 KB) erase time | Program/erase parallelism x 8 | - | 2 | 4 | s |
| | | Program/erase parallelism x 16 | - | 1.8 | 3.6 | |
| | | Program/erase parallelism x 32 | - | | | |
| $t_{ME}$ | Mass erase time | Program/erase parallelism x 8 | - | 13 | 26 | |
| | | Program/erase parallelism x 16 | - | 8 | 16 | |
| | | Program/erase parallelism x 32 | - | 6 | 12 | |
| | | Program/erase parallelism x 64 | - | 5 | 10 | |

**Table 64. Flash memory programming (single bank configuration nDBANK=1) (continued)**

| Symbol | Parameter | Conditions | Min(1) | Typ | Max(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{prog}$ | Programming voltage | Program parallelism x 8 | 1.62 | - | 3.6 | V |
| | | Program parallelism x 16 | | | | |
| | | Program parallelism x 32 | | | | |
| | | Program parallelism x 64 | 1.8 | - | 3.6 | |

1. Guaranteed by characterization results.
2. The maximum programming time is measured after 10K erase operations.

**Table 65. Flash memory endurance and data retention**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| | | | Min(1) | |
| $N_{END}$ | Endurance | $T_J$ = –40 to +125 °C (6 suffix versions) | 10 | kcycles |
| $t_{RET}$ | Data retention | 1 kcycle at $T_A$ = 85 °C | 30 | Years |
| | | 10 kcycles at $T_A$ = 55 °C | 20 | |

1. Guaranteed by characterization results.

## 6.3.15 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

### Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A burst of fast transient voltage (positive and negative) is applied to $V_{DD}$ and $V_{SS}$ through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 66*. They are based on the EMS levels and classes defined in application note AN1709.

**Table 66. EMS characteristics**

| Symbol | Parameter | Conditions | Level/ Class |
|---|---|---|---|
| $V_{FESD}$ | Voltage limits to be applied on any I/O pin to induce a functional disturbance | $V_{DD}$ = 3.3 V, $T_A$ = +25 °C, UFBGA240, $f_{rcc_c_ck}$ = 400 MHz, conforms to IEC 61000-4-2 | 3B |
| $V_{FTB}$ | Fast transient voltage burst limits to be applied through 100 pF on $V_{DD}$ and $V_{SS}$ pins to induce a functional disturbance | | 5A |

As a consequence, it is recommended to add a serial resistor (1 kΩ) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

### Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

#### Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

#### Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

### Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

**Table 67. EMI characteristics**

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [$f_{HSE}/f_{CPU}$] | Unit |
|---|---|---|---|---|---|
| | | | | 8/400 MHz | |
| $S_{EMI}$ | Peak level | $V_{DD}$ = 3.6 V, $T_A$ = 25 °C, UFBGA240 package, conforming to IEC61967-2 | 0.1 to 30 MHz | 11 | dBµV |
| | | | 30 to 130 MHz | 6 | |
| | | | 130 MHz to 1 GHz | 12 | |
| | | | 1 GHz to 2 GHz | 7 | |
| | | | EMI Level | 2.5 | - |

### 6.3.16 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

#### Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse) are applied to the pins of each sample according to each pin combination. This test conforms to the ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 standards.

**Table 68. ESD absolute maximum ratings**

| Symbol | Ratings | Conditions | Packages | Class | Maximum value(1) | Unit |
|---|---|---|---|---|---|---|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A$ = +25 °C conforming to ANSI/ESDA/JEDEC JS-001 | All | 1C | 1000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A$ = +25 °C conforming to ANSI/ESDA/JEDEC JS-002 | All | C1 | 250 | |

1. Guaranteed by characterization results.

#### Static latchup

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with JESD78 IC latchup standard.

**Table 69. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latchup class | $T_A$ = +25 °C conforming to JESD78 | II level A |

### 6.3.17 I/O current injection characteristics

As a general rule, a current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3.3 V-capable I/O pins) should be avoided during the normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when an abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during the device characterization.

#### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of –5 µA/+0 µA range), or other functional failure (for example reset, oscillator frequency deviation).

The following tables are the compilation of the SIC1/SIC2 and functional ESD results.

Negative induced A negative induced leakage current is caused by negative injection and positive induced leakage current by positive injection.

**Table 70. I/O current injection susceptibility(1)**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | PA7, PC5, PG1, PB14, PJ7, PA11, PA12, PA13, PA14, PA15, PJ12, PB4 | 5 | 0 | mA |
| | PA2, PH2, PH3, PE8, PA6, PA7, PC4, PE7, PE10, PE11 | 0 | NA | |
| | PA0, PA_C, PA1, PA1_C, PC2, PC2_C, PC3, PC3_C, PA4, PA5, PH4, PH5, BOOT0 | 0 | 0 | |
| | All other I/Os | 5 | NA | |

1. Guaranteed by characterization.

## 6.3.18 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 71: I/O static characteristics* are derived from tests performed under the conditions summarized in *Table 22: General operating conditions*. All I/Os are CMOS and TTL compliant (except for BOOT0).

**Table 71. I/O static characteristics**

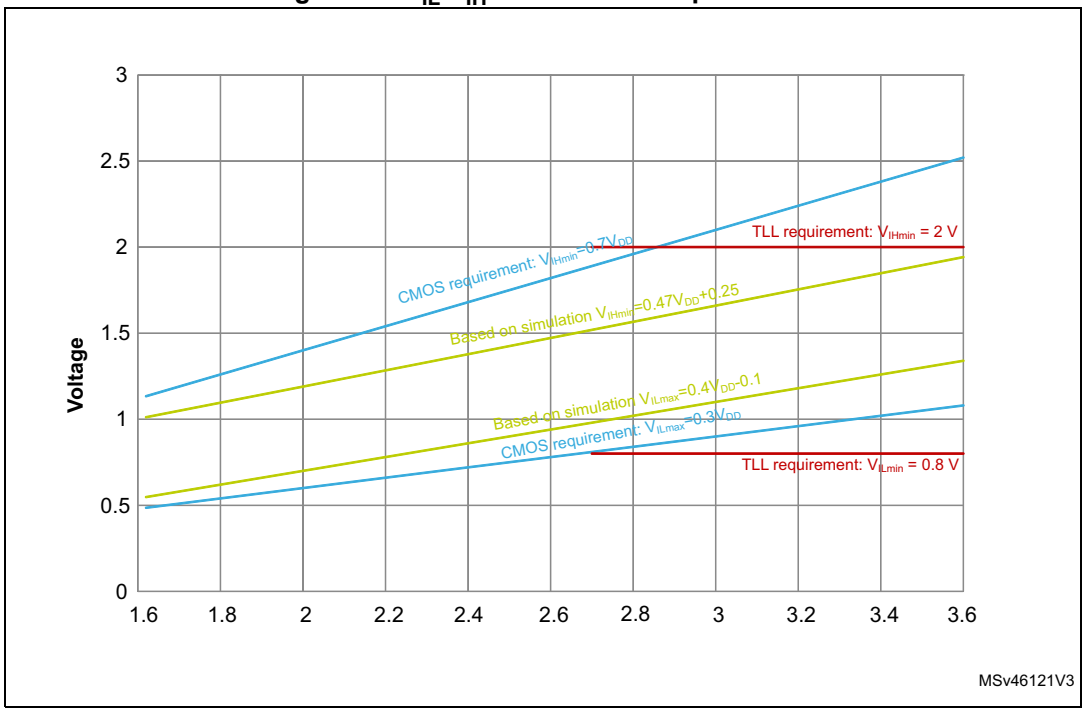
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | I/O input low level voltage except BOOT0 | 1.62 V<$V_{DDIOx}$<3.6 V | - | - | $0.3V_{DD}$(1) | V |
| | I/O input low level voltage except BOOT0 | | - | - | $0.4V_{DD}-0.1$(2) | |
| | BOOT0 I/O input low level voltage | | - | - | $0.19V_{DD}+0.1$(2) | |
| $V_{IH}$ | I/O input high level voltage except BOOT0 | 1.62 V<$V_{DDIOx}$<3.6 V | $0.7V_{DD}$(1) | - | - | V |
| | I/O input high level voltage except BOOT0(3) | | $0.47V_{DD}+0.25$(2) | - | - | |
| | BOOT0 I/O input high level voltage(3) | | $0.17V_{DD}+0.6$(2) | - | - | |
| $V_{HYS}$(2) | TT_xx, FT_xxx and NRST I/O input hysteresis | 1.62 V< $V_{DDIOx}$ <3.6 V | - | 250 | - | mV |
| | BOOT0 I/O input hysteresis | | - | 200 | - | |
| $I_{leak}$(4) | FT_xx Input leakage current(2) | 0< $V_{IN}$ ≤ Max($V_{DDXXX}$)(9) | - | - | +/-250 | nA |
| | | Max($V_{DDXXX}$) < $V_{IN}$ ≤ 5.5 V (5)(6)(9) | - | - | 1500 | |
| | FT_u IO | 0< $V_{IN}$ ≤ Max($V_{DDXXX}$)(9) | - | - | +/- 350 | |
| | | Max($V_{DDXXX}$) < $V_{IN}$ ≤ 5.5 V (5)(6)(9) | - | - | 5000(7) | |
| | TT_xx Input leakage current | 0< $V_{IN}$ ≤ Max($V_{DDXXX}$) (9) | - | - | +/-250 | |
| | VPP (BOOT0 alternate function) | 0< $V_{IN}$ ≤ $V_{DDIOX}$ | - | - | 15 | |
| | | $V_{DDIOX}$ < $V_{IN}$ ≤ 9 V | | | 35 | |
| $R_{PU}$ | Weak pull-up equivalent resistor(8) | $V_{IN}$=$V_{SS}$ | 30 | 40 | 50 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor(8) | $V_{IN}$=$V_{DD}$(9) | 30 | 40 | 50 | |
| $C_{IO}$ | I/O pin capacitance | - | - | 5 | - | pF |

1. Compliant with CMOS requirements.
2. Guaranteed by design.
3. $V_{DDIOx}$ represents $V_{DDIO1}$, $V_{DDIO2}$ or $V_{DDIO3}$. $V_{DDIOx}$= $V_{DD}$.
4. This parameter represents the pad leakage of the I/O itself. The total product pad leakage is provided by the following formula: $I_{Total_Ileak_max}$ = 10 µA + [number of I/Os where $V_{IN}$ is applied on the pad] x $I_{lkg(Max)}$.
5. All FT_xx IO except FT_lu, FT_u and PC3.

6. $V_{IN}$ must be less than Max(VDDXXX) + 3.6 V.
7. To sustain a voltage higher than MIN($V_{DD}$, $V_{DDA}$, $V_{DD33USB}$) +0.3 V, the internal pull-up and pull-down resistors must be disabled.
8. The pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).
9. Max(VDDXXX) is the maximum value of all the I/O supplies.

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements for FT I/Os is shown in *Figure 27*.

**Figure 27. $V_{IL}/V_{IH}$ for all I/Os except BOOT0**




## Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ±20 mA (with a relaxed $V_{OL}/V_{OH}$).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 6.2*. In particular:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating $\Sigma I_{VDD}$ (see *Table 20*).
- The sum of the currents sunk by all the I/Os on $V_{SS}$ plus the maximum Run consumption of the MCU sunk on $V_{SS}$ cannot exceed the absolute maximum rating $\Sigma I_{VSS}$ (see *Table 20*).

### Output voltage levels

Unless otherwise specified, the parameters given in *Table 72: Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8* and *Table 73: Output voltage characteristics for PC13, PC14, PC15 and PI8* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*. All I/Os are CMOS and TTL compliant.

**Table 72. Output voltage characteristics for all I/Os except PC13, PC14, PC15 and PI8(1)**

| Symbol | Parameter | Conditions(3) | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level voltage | CMOS port(2)<br>$I_{IO}$=8 mA<br>2.7 V≤ $V_{DD}$ ≤3.6 V | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage | CMOS port(2)<br>$I_{IO}$=-8 mA<br>2.7 V≤ $V_{DD}$ ≤3.6 V | $V_{DD}$−0.4 | - | |
| $V_{OL}$(3) | Output low level voltage | TTL port(2)<br>$I_{IO}$=8 mA<br>2.7 V≤ $V_{DD}$ ≤3.6 V | - | 0.4 | |
| $V_{OH}$(3) | Output high level voltage | TTL port(2)<br>$I_{IO}$=-8 mA<br>2.7 V≤ $V_{DD}$ ≤3.6 V | 2.4 | - | |
| $V_{OL}$(3) | Output low level voltage | $I_{IO}$=20 mA<br>2.7 V≤ $V_{DD}$ ≤3.6 V | - | 1.3 | |
| $V_{OH}$(3) | Output high level voltage | $I_{IO}$=-20 mA<br>2.7 V≤ $V_{DD}$ ≤3.6 V | $V_{DD}$−1.3 | - | |
| $V_{OL}$(3) | Output low level voltage | $I_{IO}$=4 mA<br>1.62 V≤ $V_{DD}$ ≤3.6 V | - | 0.4 | |
| $V_{OH}$ (3) | Output high level voltage | $I_{IO}$=-4 mA<br>1.62 V≤$V_{DD}$<3.6 V | $V_{DD}$−-0.4 | - | |
| $V_{OLFM+}$(3) | Output low level voltage for an FTf I/O pin in FM+ mode | $I_{IO}$= 20 mA<br>2.3 V≤ $V_{DD}$≤3.6 V | - | 0.4 | |
| | | $I_{IO}$= 10 mA<br>1.62 V≤ $V_{DD}$ ≤3.6 V | - | 0.4 | |

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 19: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

**Table 73. Output voltage characteristics for PC13, PC14, PC15 and PI8(1)**

| Symbol | Parameter | Conditions(3) | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level voltage | CMOS port(2)<br>$I_{IO}$=3 mA<br>2.7 V≤ $V_{DD}$ ≤3.6 V | - | 0.4 | V |
| $V_{OH}$ | Output high level voltage | CMOS port(2)<br>$I_{IO}$=-3 mA<br>2.7 V≤ $V_{DD}$ ≤3.6 V | $V_{DD}$−0.4 | - | |
| $V_{OL}$(3) | Output low level voltage | TTL port(2)<br>$I_{IO}$=3 mA<br>2.7 V≤ $V_{DD}$ ≤3.6 V | - | 0.4 | |
| $V_{OH}$(2) | Output high level voltage | TTL port(2)<br>$I_{IO}$=-3 mA<br>2.7 V≤ $V_{DD}$ ≤3.6 V | 2.4 | - | |
| $V_{OL}$(2) | Output low level voltage | $I_{IO}$=1.5 mA<br>1.62 V≤ $V_{DD}$ ≤3.6 V | - | 0.4 | |
| $V_{OH}$(2) | Output high level voltage | $I_{IO}$=-1.5 mA<br>1.62 V≤ $V_{DD}$ ≤3.6 V | $V_{DD}$−0.4 | - | |

1. The IIO current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 19: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣIIO.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

### Output buffer timing characteristics (HSLV option disabled)

The HSLV bit of SYSCFG_CCCSR register can be used to optimize the I/O speed when the product voltage is below 2.7 V.

**Table 74. Output timing characteristics (HSLV OFF)(1)(2)**

| Speed | Symbol | Parameter | conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 00 | $F_{max}$(3) | Maximum frequency | C=50 pF, 2.7 V≤ $V_{DD}$≤3.6 V | - | 12 | MHz |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 3 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V | - | 12 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 3 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V | - | 16 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 4 | |
| | $t_r/t_f$(4) | Output high to low level fall time and output low to high level rise time | C=50 pF, 2.7 V≤ $V_{DD}$≤3.6 V | - | 16.6 | ns |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 33.3 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V | - | 13.3 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 25 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V | - | 10 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 20 | |
| 01 | $F_{max}$(3) | Maximum frequency | C=50 pF, 2.7 V≤ $V_{DD}$≤3.6 V | - | 60 | MHz |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 15 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V | - | 80 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 15 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V | - | 110 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 20 | |
| | $t_r/t_f$(4) | Output high to low level fall time and output low to high level rise time | C=50 pF, 2.7 V≤ $V_{DD}$≤3.6 V | - | 5.2 | ns |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 10 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V | - | 4.2 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 7.5 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V | - | 2.8 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 5.2 | |

**Table 74. Output timing characteristics (HSLV OFF)(1)(2) (continued)**

| Speed | Symbol | Parameter | conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 10 | $F_{max}$(3) | Maximum frequency | C=50 pF, 2.7 V≤$V_{DD}$≤3.6 V(5) | - | 85 | MHz |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V(5) | - | 35 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V(5) | - | 110 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(5) | - | 40 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V(5) | - | 166 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V(5) | - | 100 | |
| | $t_r/t_f$(4) | Output high to low level fall time and output low to high level rise time | C=50 pF, 2.7 V≤$V_{DD}$≤3.6 V(5) | - | 3.8 | ns |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V(5) | - | 6.9 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V(5) | - | 2.8 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(5) | - | 5.2 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V(5) | - | 1.8 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V$^{v}$ | - | 3.3 | |
| 11 | $F_{max}$(3) | Maximum frequency | C=50 pF, 2.7 V≤$V_{DD}$≤3.6 V$^{v}$ | - | 100 | MHz |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V(5) | - | 50 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V$^{v}$ | - | 133 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(5) | - | 66 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V(5) | - | 220 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V(5) | - | 85 | |
| | $t_r/t_f$(4) | Output high to low level fall time and output low to high level rise time | C=50 pF, 2.7 V≤$V_{DD}$≤3.6 V(5) | - | 3.3 | ns |
| | | | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V(5) | - | 6.6 | |
| | | | C=30 pF, 2.7 V≤$V_{DD}$≤3.6 V(5) | - | 2.4 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(5) | - | 4.5 | |
| | | | C=10 pF, 2.7 V≤$V_{DD}$≤3.6 V(5) | - | 1.5 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V(5) | - | 2.7 | |

1. Guaranteed by design.
2. The frequency of the GPIOs that can be supplied in $V_{BAT}$ mode (PC13, PC14, PC15 and PI8) is limited to 2 MHz
3. The maximum frequency is defined with the following conditions:
   ($t_r$+$t_f$) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
4. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
5. Compensation system enabled.

## Output buffer timing characteristics (HSLV option enabled)

**Table 75. Output timing characteristics (HSLV ON)(1)**

| Speed | Symbol | Parameter | conditions | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 00 | $F_{max}$(2) | Maximum frequency | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 10 | MHz |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 10 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 10 | |
| | $t_r/t_f$(3) | Output high to low level fall time and output low to high level rise time | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 11 | ns |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 9 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 6.6 | |
| 01 | $F_{max}$(2) | Maximum frequency | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 50 | MHz |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 58 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 66 | |
| | $t_r/t_f$(3) | Output high to low level fall time and output low to high level rise time | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 6.6 | ns |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 4.8 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V | - | 3 | |
| 10 | $F_{max}$(2) | Maximum frequency | C=50 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 55 | MHz |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 80 | |
| | | | C=10 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 133 | |
| | $t_r/t_f$(3) | Output high to low level fall time and output low to high level rise time | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 5.8 | ns |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 4 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 2.4 | |
| 11 | $F_{max}$(2) | Maximum frequency | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 60 | MHz |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 90 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 175 | |
| | $t_r/t_f$(3) | Output high to low level fall time and output low to high level rise time | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 5.3 | ns |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 3.6 | |
| | | | C=30 pF, 1.62 V≤$V_{DD}$≤2.7 V(4) | - | 1.9 | |

1. Guaranteed by design.
2. The maximum frequency is defined with the following conditions:
   ($t_r$+$t_f$) ≤ 2/3 T
   Skew ≤ 1/20 T
   45%<Duty cycle<55%
3. The fall and rise times are defined between 90% and 10% and between 10% and 90% of the output waveform, respectively.
4. Compensation system enabled.

### 6.3.19 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 71: I/O static characteristics*).

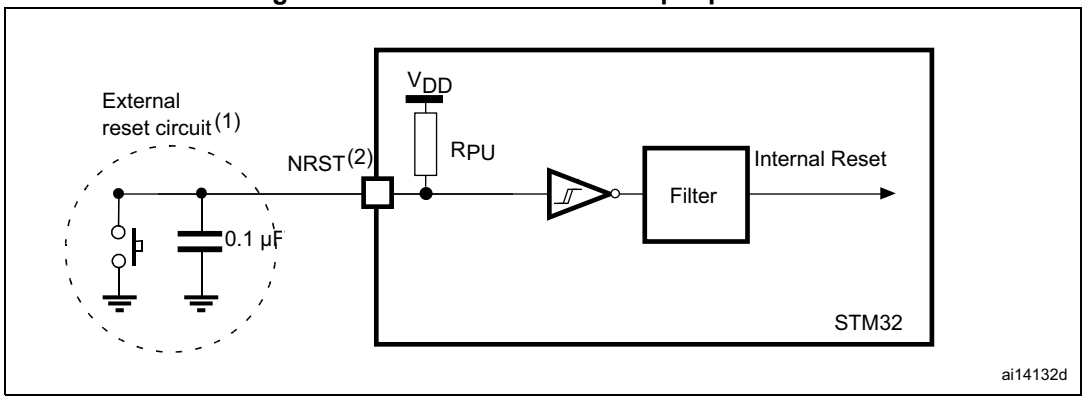
Unless otherwise specified, the parameters given in *Table 76* are derived from tests performed under the ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 76. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{PU}$(2) | Weak pull-up equivalent resistor(1) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$(2) | NRST Input filtered pulse | 1.71 V < $V_{DD}$ < 3.6 V | - | - | 50 | ns |
| $V_{NF(NRST)}$(2) | NRST Input not filtered pulse | 1.71 V < $V_{DD}$ < 3.6 V | 300 | - | - | |
| | | 1.62 V < $V_{DD}$ < 3.6 V | 1000 | - | - | |

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

**Figure 28. Recommended NRST pin protection**




1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 71*. Otherwise the reset is not taken into account by the device.

### 6.3.20 FMC characteristics

Unless otherwise specified, the parameters given in *Table 77* to *Table 90* for the FMC interface are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1.

Refer to *Section 6.3.18: I/O port characteristics* for more details on the input/output alternate function characteristics.

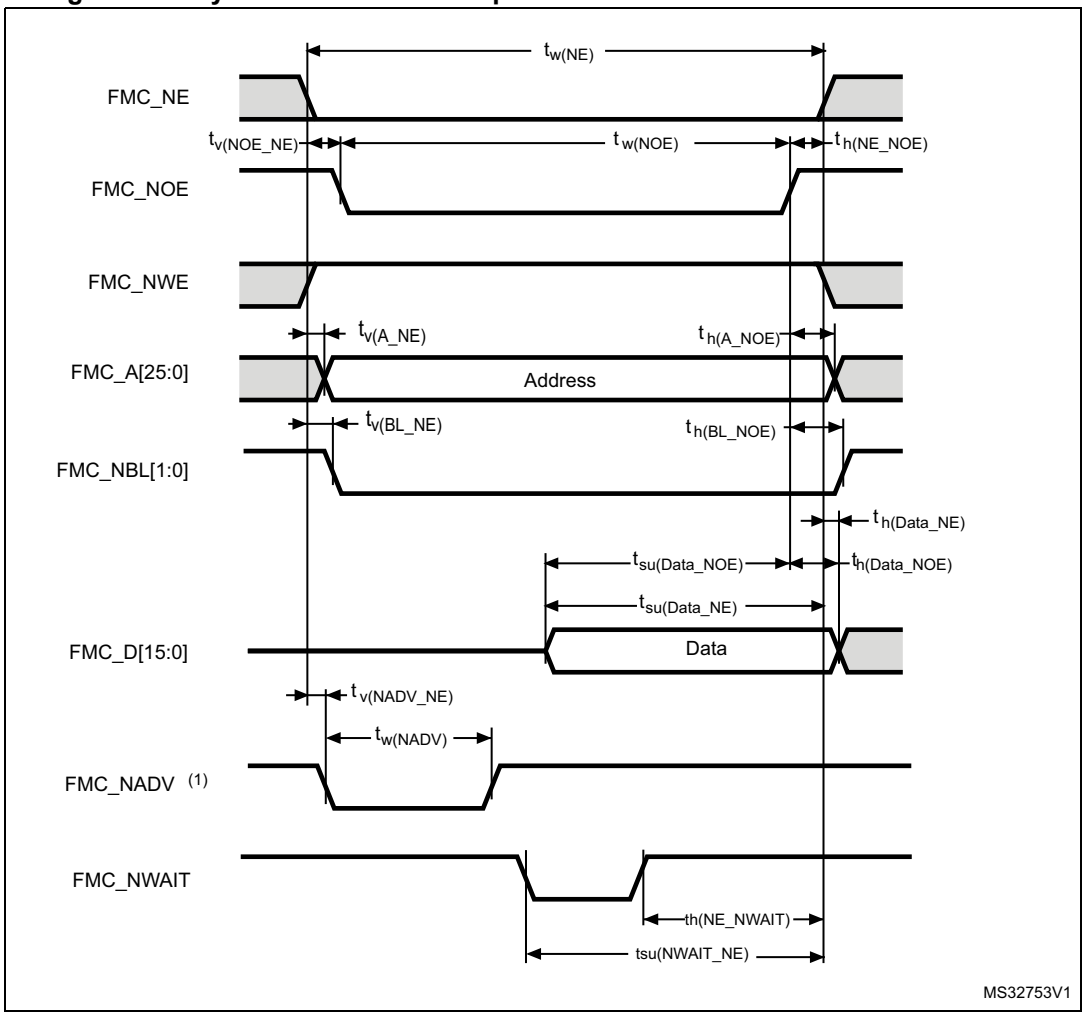
### Asynchronous waveforms and timings

*Figure 29* through *Figure 31* represent asynchronous waveforms and *Table 77* through *Table 84* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- AddressSetupTime = 0x1
- AddressHoldTime = 0x1
- DataSetupTime = 0x1 (except for asynchronous NWAIT mode , DataSetupTime = 0x5)
- BusTurnAroundDuration = 0x0
- Capacitive load $C_L$ = 30 pF

In all timing tables, the $T_{KERCK}$ is the $f_{mc_ker_ck}$ clock period.

**Figure 29. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms**




1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

**Table 77. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $3T_{fmc_ker_ck}-1$ | $3T_{fmc_ker_ck}+1$ | ns |
| $t_{v(NOE_NE)}$ | FMC_NEx low to FMC_NOE low | 0 | 0.5 | |
| $t_{w(NOE)}$ | FMC_NOE low time | $2T_{fmc_ker_ck}-1$ | $2T_{fmc_ker_ck}+1$ | |
| $t_{h(NE_NOE)}$ | FMC_NOE high to FMC_NE high hold time | 0 | - | |
| $t_{v(A_NE)}$ | FMC_NEx low to FMC_A valid | - | 0.5 | |
| $t_{h(A_NOE)}$ | Address hold time after FMC_NOE high | 0 | - | |
| $t_{su(Data_NE)}$ | Data to FMC_NEx high setup time | 11 | - | |
| $t_{su(Data_NOE)}$ | Data to FMC_NOEx high setup time | 11 | - | |
| $t_{h(Data_NOE)}$ | Data hold time after FMC_NOE high | 0 | - | |
| $t_{h(Data_NE)}$ | Data hold time after FMC_NEx high | 0 | - | |
| $t_{v(NADV_NE)}$ | FMC_NEx low to FMC_NADV low | - | 0 | |
| $t_{w(NADV)}$ | FMC_NADV low time | - | $T_{fmc_ker_ck}+1$ | |

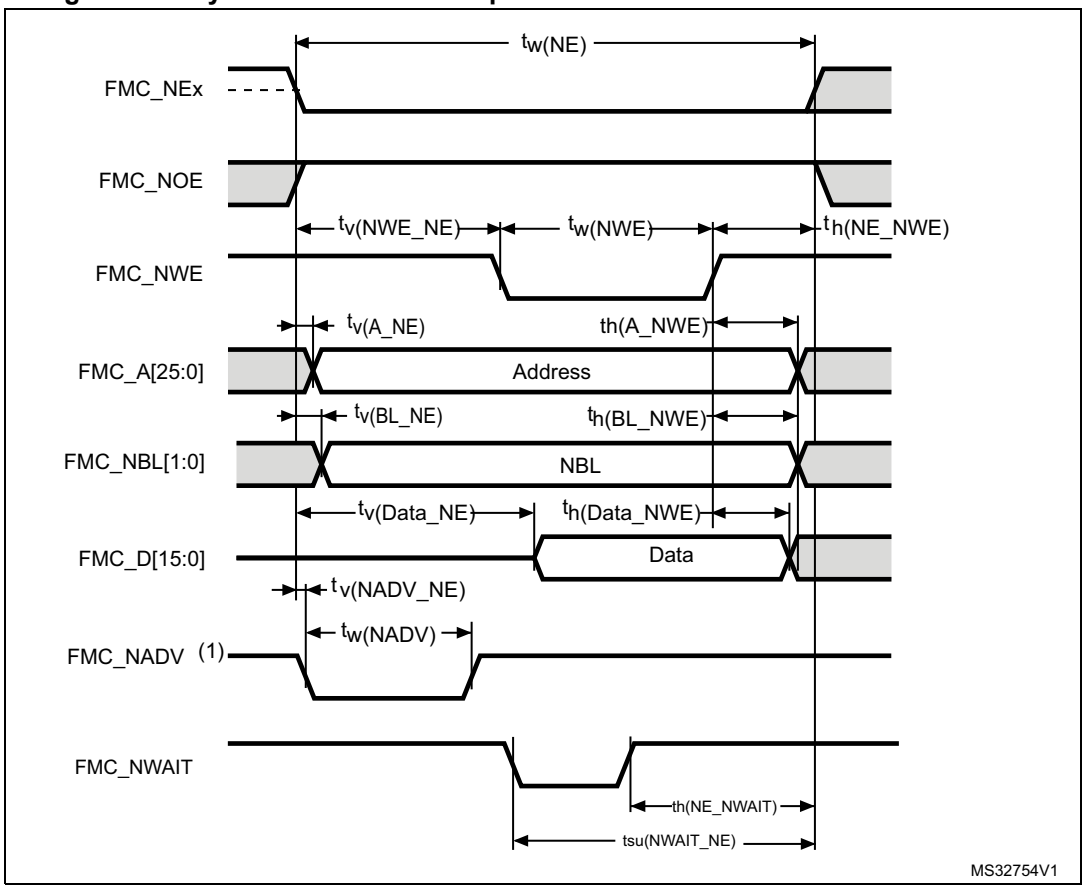
1. Guaranteed by characterization results.

**Table 78. Asynchronous non-multiplexed SRAM/PSRAM/NOR read-NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $7T_{fmc_ker_ck}+1$ | $7T_{fmc_ker_ck}+1$ | ns |
| $t_{w(NOE)}$ | FMC_NOE low time | $5T_{fmc_ker_ck}-1$ | $5T_{fmc_ker_ck}+1$ | |
| $t_{w(NWAIT)}$ | FMC_NWAIT low time | $T_{fmc_ker_ck}-0.5$ | - | |
| $t_{su(NWAIT_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $4T_{fmc_ker_ck}+11$ | - | |
| $t_{h(NE_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $3T_{fmc_ker_ck}+11.5$ | - | |

1. Guaranteed by characterization results.
2. $N_{WAIT}$ pulse width is equal to 1 AHB cycle.

**Figure 30. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms**




1. Mode 2/B, C and D only. In Mode 1, FMC_NADV is not used.

**Table 79. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $3T_{fmc_ker_ck} - 1$ | $3T_{fmc_ker_ck}$ | ns |
| $t_{v(NWE_NE)}$ | FMC_NEx low to FMC_NWE low | $T_{fmc_ker_ck}$ | $T_{fmc_ker_ck}+1$ | |
| $t_{w(NWE)}$ | FMC_NWE low time | $T_{fmc_ker_ck} - 0.5$ | $T_{fmc_ker_ck}+0.5$ | |
| $t_{h(NE_NWE)}$ | FMC_NWE high to FMC_NE high hold time | $T_{fmc_ker_ck}$ | - | |
| $t_{v(A_NE)}$ | FMC_NEx low to FMC_A valid | - | 2 | |
| $t_{h(A_NWE)}$ | Address hold time after FMC_NWE high | $T_{fmc_ker_ck} - 0.5$ | - | |
| $t_{v(BL_NE)}$ | FMC_NEx low to FMC_BL valid | - | 0.5 | |
| $t_{h(BL_NWE)}$ | FMC_BL hold time after FMC_NWE high | $T_{fmc_ker_ck} - 0.5$ | - | |
| $t_{v(Data_NE)}$ | Data to FMC_NEx low to Data valid | - | $T_{fmc_ker_ck}+ 2.5$ | |
| $t_{h(Data_NWE)}$ | Data hold time after FMC_NWE high | $T_{fmc_ker_ck}+0.5$ | - | |
| $t_{v(NADV_NE)}$ | FMC_NEx low to FMC_NADV low | - | 0 | |
| $t_{w(NADV)}$ | FMC_NADV low time | - | $T_{fmc_ker_ck}+ 1$ | |

1. Guaranteed by characterization results.

**Table 80. Asynchronous non-multiplexed SRAM/PSRAM/NOR write-NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $8T_{fmc_ker_ck} - 1$ | $8T_{fmc_ker_ck}+1$ | ns |
| $t_{w(NWE)}$ | FMC_NWE low time | $6T_{fmc_ker_ck} - 1.5$ | $6T_{fmc_ker_ck}+0.5$ | |
| $t_{su(NWAIT_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $5T_{fmc_ker_ck}+13$ | - | |
| $t_{h(NE_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{fmc_ker_ck}+13$ | - | |

1. Guaranteed by characterization results.
2. $N_{WAIT}$ pulse width is equal to 1 AHB cycle.

**Figure 31. Asynchronous multiplexed PSRAM/NOR read waveforms**

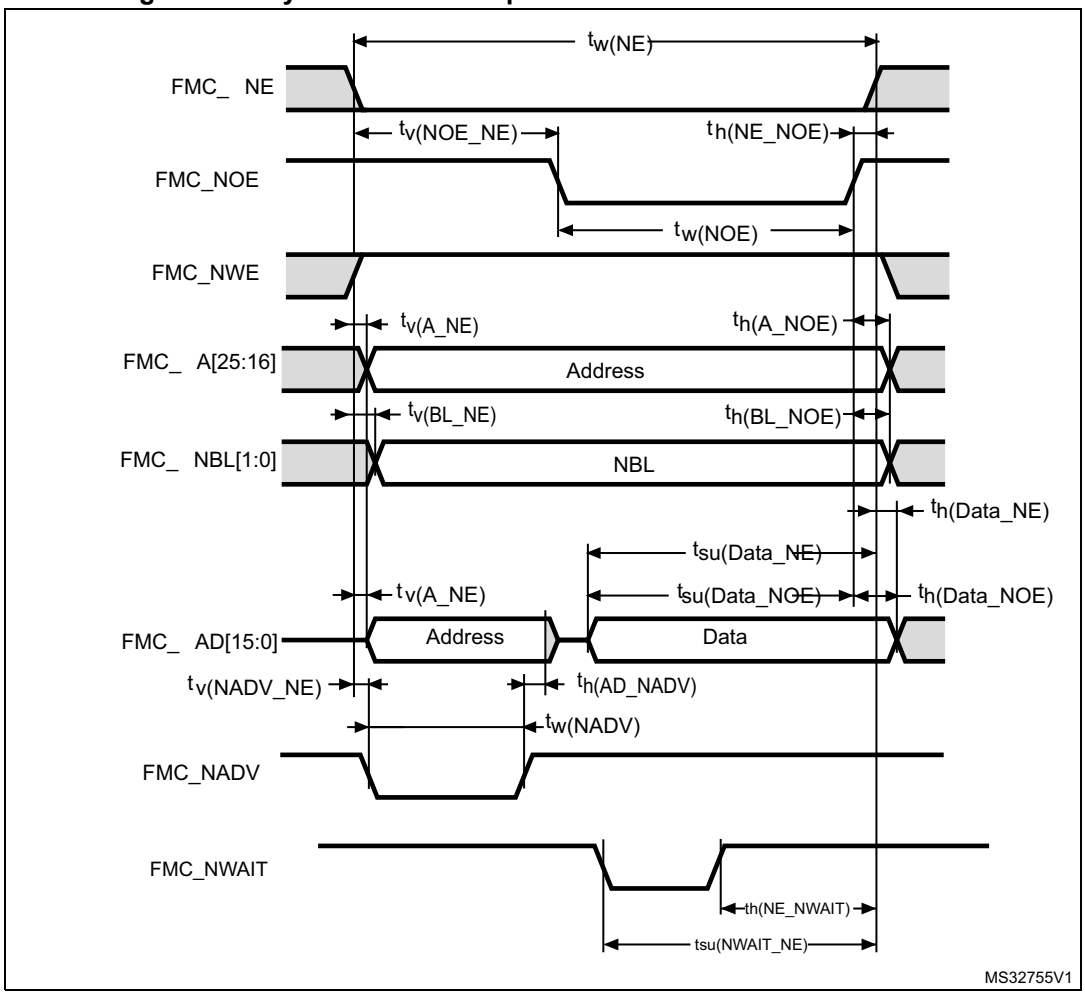


**Table 81. Asynchronous multiplexed PSRAM/NOR read timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $4T_{fmc_ker_ck} - 1$ | $4T_{fmc_ker_ck} + 1$ | ns |
| $t_{v(NOE_NE)}$ | FMC_NEx low to FMC_NOE low | $2T_{fmc_ker_ck}$ | $2T_{fmc_ker_ck} + 0.5$ | |
| $t_{tw(NOE)}$ | FMC_NOE low time | $T_{fmc_ker_ck} - 1$ | $T_{fmc_ker_ck} + 1$ | |
| $t_{h(NE_NOE)}$ | FMC_NOE high to FMC_NE high hold time | 0 | - | |
| $t_{v(A_NE)}$ | FMC_NEx low to FMC_A valid | - | 0.5 | |
| $t_{v(NADV_NE)}$ | FMC_NEx low to FMC_NADV low | 0 | 0.5 | |
| $t_{w(NADV)}$ | FMC_NADV low time | $T_{fmc_ker_ck} - 0.5$ | $T_{fmc_ker_ck} + 1$ | |
| $t_{h(AD_NADV)}$ | FMC_AD(address) valid hold time after FMC_NADV high) | $T_{fmc_ker_ck} + 0.5$ | - | |
| $t_{h(A_NOE)}$ | Address hold time after FMC_NOE high | $T_{fmc_ker_ck} - 0.5$ | - | |
| $t_{su(Data_NE)}$ | Data to FMC_NEx high setup time | 11 | - | |
| $t_{su(Data_NOE)}$ | Data to FMC_NOE high setup time | 11 | - | |
| $t_{h(Data_NE)}$ | Data hold time after FMC_NEx high | 0 | - | |
| $t_{h(Data_NOE)}$ | Data hold time after FMC_NOE high | 0 | - | |

1. Guaranteed by characterization results.

**Table 82. Asynchronous multiplexed PSRAM/NOR read-NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $8T_{fmc_ker_ck} - 1$ | $8T_{fmc_ker_ck}$ | ns |
| $t_{w(NOE)}$ | FMC_NWE low time | $5T_{fmc_ker_ck} - 1.5$ | $5T_{fmc_ker_ck} + 0.5$ | |
| $t_{su(NWAIT_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $4T_{fmc_ker_ck} + 11$ | - | |
| $t_{h(NE_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $3T_{fmc_ker_ck} + 11.5$ | - | |

1. Guaranteed by characterization results.
2. $N_{WAIT}$ pulse width is equal to 1 AHB cycle.

**Table 83. Asynchronous multiplexed PSRAM/NOR write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $4T_{fmc_ker_ck} - 1$ | $4T_{fmc_ker_ck}$ | ns |
| $t_{v(NWE_NE)}$ | FMC_NEx low to FMC_NWE low | $T_{fmc_ker_ck} - 1$ | $T_{fmc_ker_ck} + 0.5$ | |
| $t_{w(NWE)}$ | FMC_NWE low time | $2T_{fmc_ker_ck} - 0.5$ | $2T_{fmc_ker_ck} + 0.5$ | |
| $t_{h(NE_NWE)}$ | FMC_NWE high to FMC_NE high hold time | $T_{fmc_ker_ck} - 0.5$ | - | |
| $t_{v(A_NE)}$ | FMC_NEx low to FMC_A valid | - | 0 | |
| $t_{v(NADV_NE)}$ | FMC_NEx low to FMC_NADV low | 0 | 0.5 | |
| $t_{w(NADV)}$ | FMC_NADV low time | $T_{fmc_ker_ck}$ | $T_{fmc_ker_ck} + 1$ | |
| $t_{h(AD_NADV)}$ | FMC_AD(adress) valid hold time after FMC_NADV high) | $T_{fmc_ker_ck} + 0.5$ | - | |
| $t_{h(A_NWE)}$ | Address hold time after FMC_NWE high | $T_{fmc_ker_ck} + 0.5$ | - | |
| $t_{h(BL_NWE)}$ | FMC_BL hold time after FMC_NWE high | $T_{fmc_ker_ck} - 0.5$ | - | |
| $t_{v(BL_NE)}$ | FMC_NEx low to FMC_BL valid | - | 0.5 | |
| $t_{v(Data_NADV)}$ | FMC_NADV high to Data valid | - | $T_{fmc_ker_ck} + 2$ | |
| $t_{h(Data_NWE)}$ | Data hold time after FMC_NWE high | $T_{fmc_ker_ck} + 0.5$ | - | |

1. Guaranteed by characterization results.

**Table 84. Asynchronous multiplexed PSRAM/NOR write-NWAIT timings(1)(2)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FMC_NE low time | $9T_{fmc_ker_ck} - 1$ | $9T_{fmc_ker_ck}$ | ns |
| $t_{w(NWE)}$ | FMC_NWE low time | $7T_{fmc_ker_ck} - 0.5$ | $7T_{fmc_ker_ck} + 0.5$ | |
| $t_{su(NWAIT_NE)}$ | FMC_NWAIT valid before FMC_NEx high | $5T_{fmc_ker_ck} + 11$ | - | |
| $t_{h(NE_NWAIT)}$ | FMC_NEx hold time after FMC_NWAIT invalid | $4T_{fmc_ker_ck} + 11.5$ | - | |

1. Guaranteed by characterization results.
2. $N_{WAIT}$ pulse width is equal to 1 AHB cycle.

## Synchronous waveforms and timings

*Figure 32* through *Figure 35* represent synchronous waveforms and *Table 85* through *Table 88* provide the corresponding timings. The results shown in these tables are obtained with the following FMC configuration:

- BurstAccessMode = FMC_BurstAccessMode_Enable
- MemoryType = FMC_MemoryType_CRAM
- WriteBurst = FMC_WriteBurst_Enable
- CLKDivision = 1
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

In all the timing tables, the $T_{fmc_ker_ck}$ is the $f_{mc_ker_ck}$ clock period, with the following FMC_CLK maximum values:

- For 2.7 V<$V_{DD}$<3.6 V, FMC_CLK = 125 MHz at 20 pF
- For 1.8 V<$V_{DD}$<1.9 V, FMC_CLK = 100 MHz at 20 pF
- For 1.62 V<$V_{DD}$<1.8 V, FMC_CLK = 100 MHz at 15 pF

**Figure 32. Synchronous multiplexed NOR/PSRAM read timings**

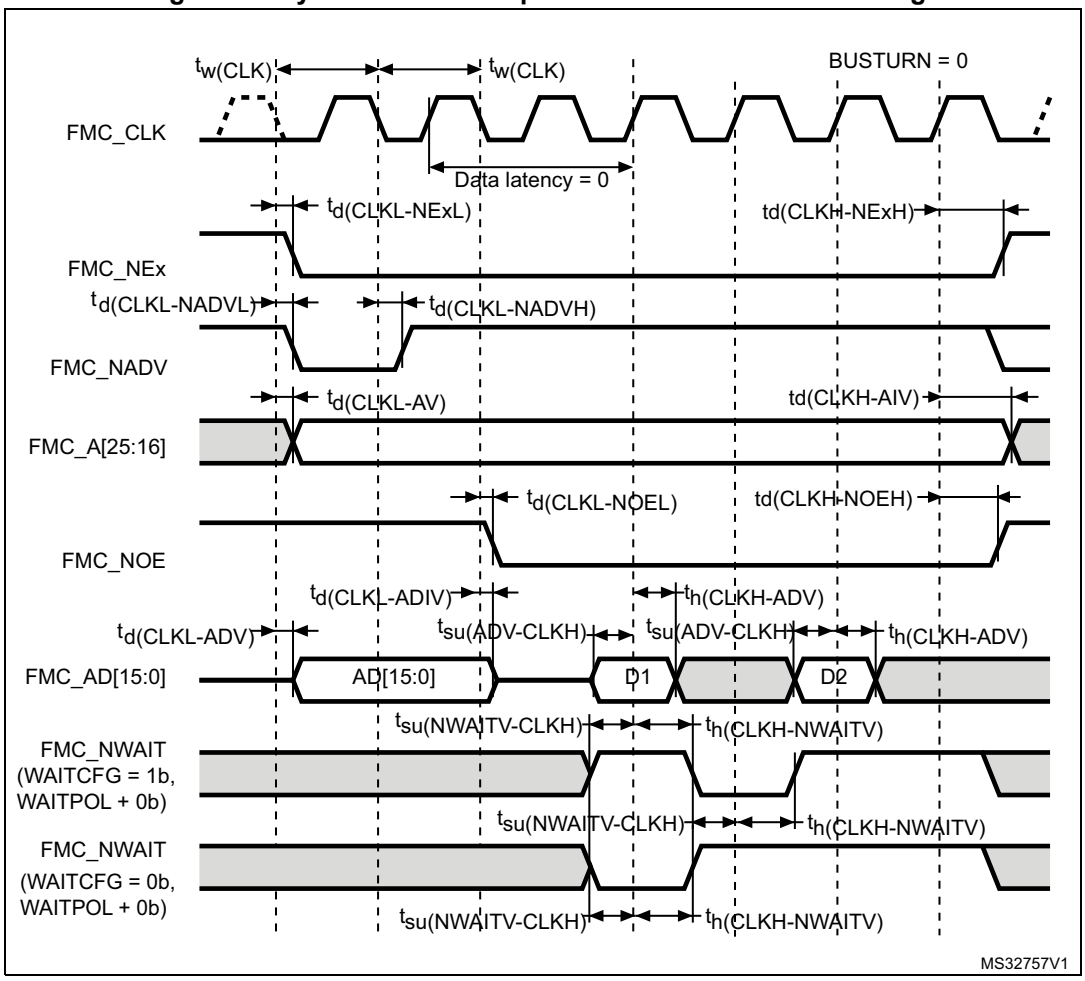


**Table 85. Synchronous multiplexed NOR/PSRAM read timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FMC_CLK period | $2T_{fmc_ker_ck}-1$ | - | ns |
| $t_{d(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 1 | |
| $t_{d(CLKH_NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | $T_{fmc_ker_ck}+0.5$ | - | |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 1 | |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 2.5 | |
| $t_{d(CLKH-AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | $T_{fmc_ker_ck}$ | - | |
| $t_{d(CLKL-NOEL)}$ | FMC_CLK low to FMC_NOE low | - | 1.5 | |
| $t_{d(CLKH-NOEH)}$ | FMC_CLK high to FMC_NOE high | $T_{fmc_ker_ck}-0.5$ | - | |
| $t_{d(CLKL-ADV)}$ | FMC_CLK low to FMC_AD[15:0] valid | - | 3 | |
| $t_{d(CLKL-ADIV)}$ | FMC_CLK low to FMC_AD[15:0] invalid | 0 | - | |
| $t_{su(ADV-CLKH)}$ | FMC_A/D[15:0] valid data before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-ADV)}$ | FMC_A/D[15:0] valid data after FMC_CLK high | 1 | - | |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 2 | - | |

1. Guaranteed by characterization results.

**Figure 33. Synchronous multiplexed PSRAM write timings**

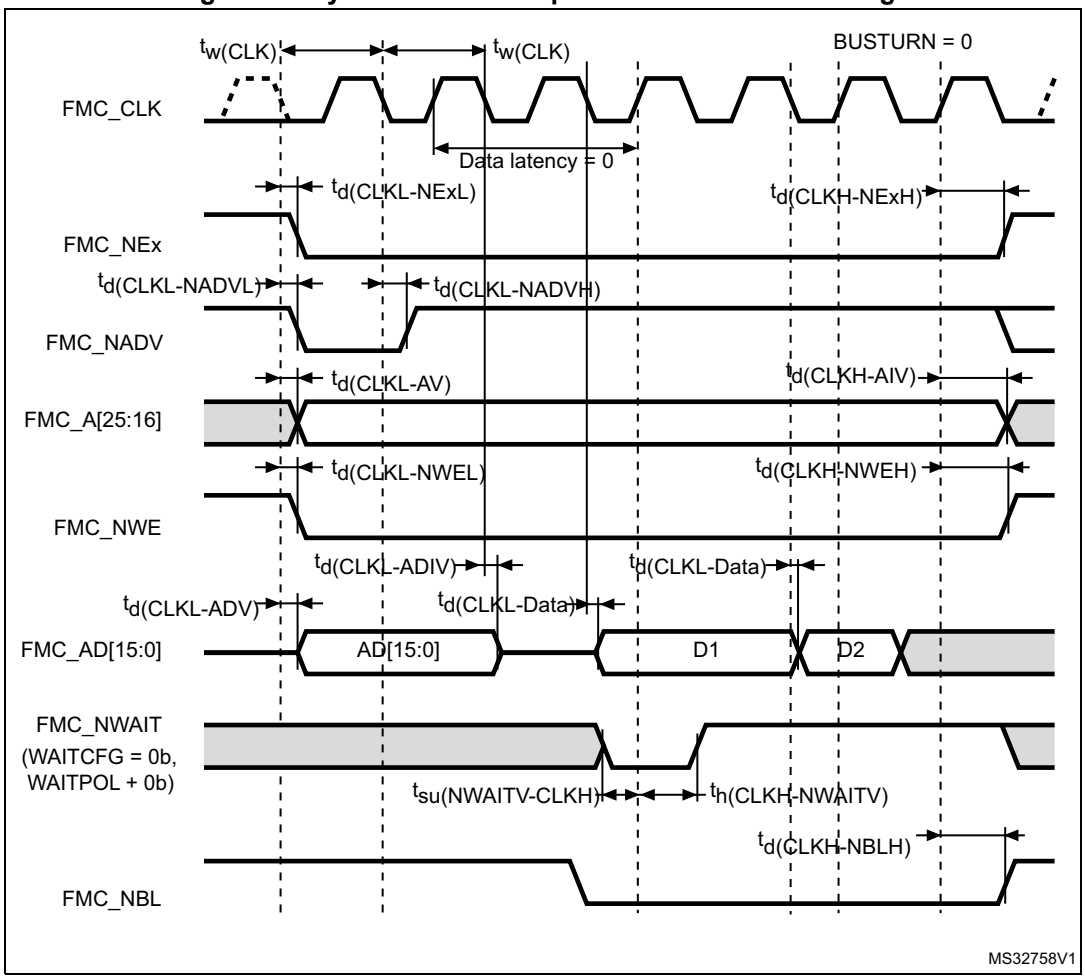


**Table 86. Synchronous multiplexed PSRAM write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FMC_CLK period, $V_{DD}$ = 2.7 to 3.6 V | $2T_{fmc_ker_ck} - 1$ 1 | - | Ns |
| $t_{d(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x =0..2) | - | 1 | |
| $t_{d(CLKH-NExH)}$ | FMC_CLK high to FMC_NEx high (x = 0…2) | $T_{fmc_ker_ck}$ +0.5 | - | |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 1.5 | |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x =16…25) | - | 2 | |
| $t_{d(CLKH-AIV)}$ | FMC_CLK high to FMC_Ax invalid (x =16…25) | $T_{fmc_ker_ck}$ | - | |
| $t_{d(CLKL-NWEL)}$ | FMC_CLK low to FMC_NWE low | - | 1.5 | |
| $t_{(CLKH-NWEH)}$ | FMC_CLK high to FMC_NWE high | $T_{fmc_ker_ck}$ +0.5 | - | |
| $t_{d(CLKL-ADV)}$ | FMC_CLK low to to FMC_AD[15:0] valid | - | 2.5 | |
| $t_{d(CLKL-ADIV)}$ | FMC_CLK low to FMC_AD[15:0] invalid | 0 | - | |
| $t_{d(CLKL-DATA)}$ | FMC_A/D[15:0] valid data after FMC_CLK low | - | 2.5 | |
| $t_{d(CLKL-NBLL)}$ | FMC_CLK low to FMC_NBL low | - | 2 | |
| $t_{d(CLKH-NBLH)}$ | FMC_CLK high to FMC_NBL high | $T_{fmc_ker_ck}$ +0.5 | - | |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 2 | - | |

1. Guaranteed by characterization results.

**Figure 34. Synchronous non-multiplexed NOR/PSRAM read timings**

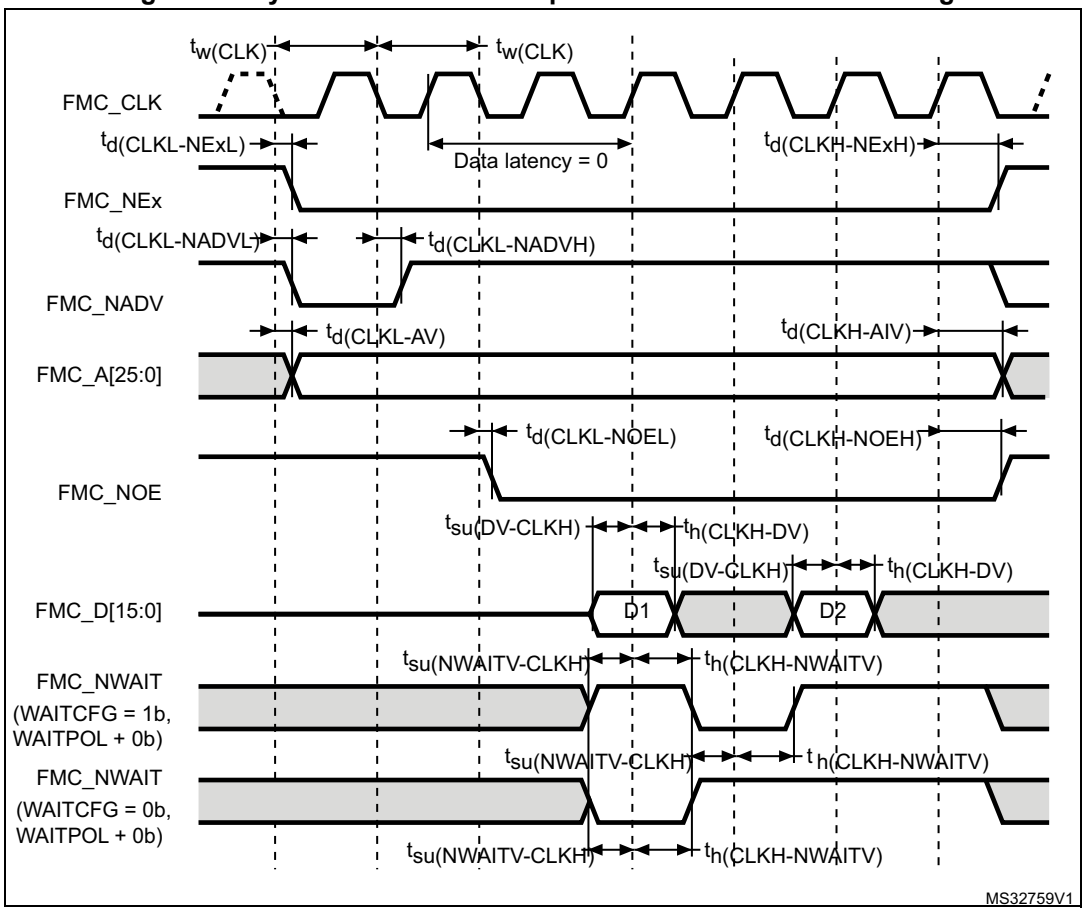


**Table 87. Synchronous non-multiplexed NOR/PSRAM read timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FMC_CLK period | $2T_{fmc_ker_ck}-1$ | - | ns |
| $t_{(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 1 | |
| $t_{d(CLKH-NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | $2T_{fmc_ker_ck}+0.5$ | - | |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 0.5 | |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | 0 | - | |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 2 | |
| $t_{d(CLKH-AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | $2T_{fmc_ker_ck}$ | - | |
| $t_{d(CLKL-NOEL)}$ | FMC_CLK low to FMC_NOE low | - | 1.5 | |
| $t_{d(CLKH-NOEH)}$ | FMC_CLK high to FMC_NOE high | $2T_{fmc_ker_ck}-0.5$ | - | |
| $t_{su(DV-CLKH)}$ | FMC_D[15:0] valid data before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-DV)}$ | FMC_D[15:0] valid data after FMC_CLK high | 1 | - | |
| $t_{(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 2 | - | |

1. Guaranteed by characterization results.

**Figure 35. Synchronous non-multiplexed PSRAM write timings**

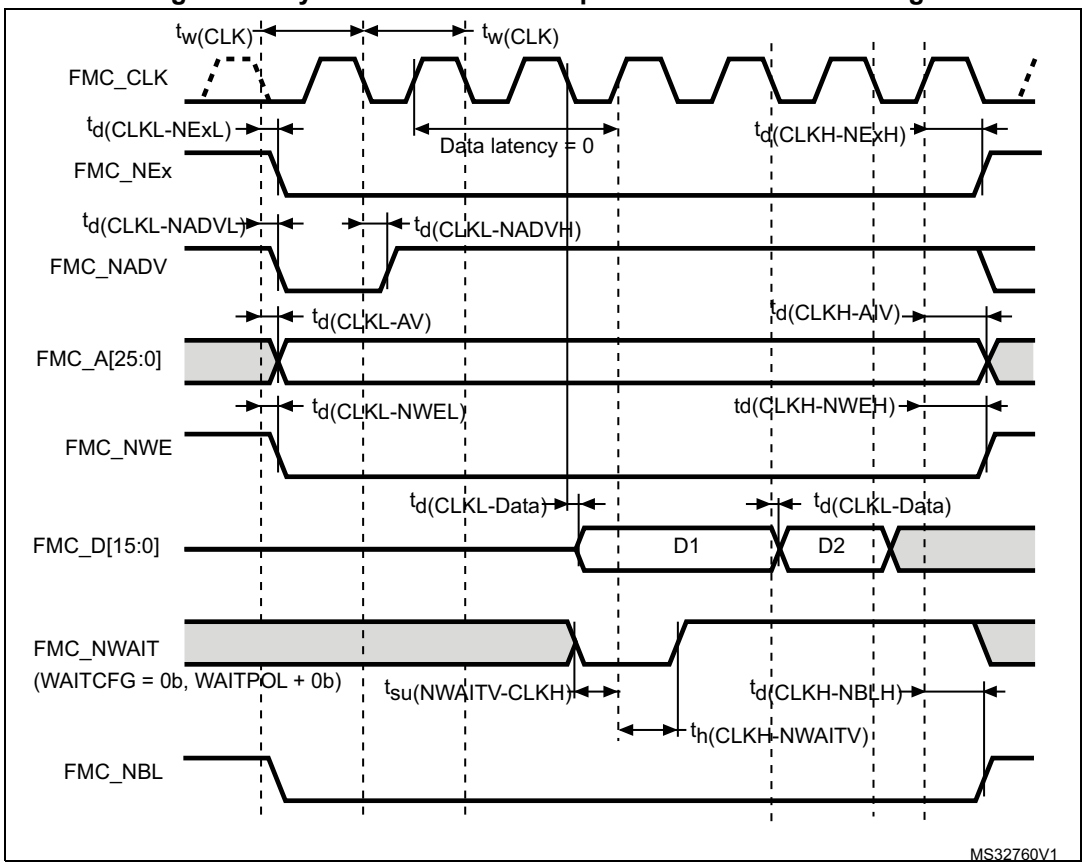


**Table 88. Synchronous non-multiplexed PSRAM write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{(CLK)}$ | FMC_CLK period | $2T_{fmc_ker_ck} - 1$ | - | ns |
| $t_{d(CLKL-NExL)}$ | FMC_CLK low to FMC_NEx low (x=0..2) | - | 2 | |
| $t_{(CLKH-NExH)}$ | FMC_CLK high to FMC_NEx high (x= 0…2) | $T_{fmc_ker_ck}$**+0.5** | - | |
| $t_{d(CLKL-NADVL)}$ | FMC_CLK low to FMC_NADV low | - | 0.5 | |
| $t_{d(CLKL-NADVH)}$ | FMC_CLK low to FMC_NADV high | **0** | - | |
| $t_{d(CLKL-AV)}$ | FMC_CLK low to FMC_Ax valid (x=16…25) | - | 2. | |
| $t_{d(CLKH-AIV)}$ | FMC_CLK high to FMC_Ax invalid (x=16…25) | $T_{fmc_ker_ck}$ | - | |
| $t_{d(CLKL-NWEL)}$ | FMC_CLK low to FMC_NWE low | - | 1.5 | |
| $t_{d(CLKH-NWEH)}$ | FMC_CLK high to FMC_NWE high | $T_{fmc_ker_ck}+1$ | - | |
| $t_{d(CLKL-Data)}$ | FMC_D[15:0] valid data after FMC_CLK low | - | 3.5 | |
| $t_{d(CLKL-NBLL)}$ | FMC_CLK low to FMC_NBL low | - | 2 | |
| $t_{d(CLKH-NBLH)}$ | FMC_CLK high to FMC_NBL high | $T_{fmc_ker_ck}+1$ | - | |
| $t_{su(NWAIT-CLKH)}$ | FMC_NWAIT valid before FMC_CLK high | 2 | - | |
| $t_{h(CLKH-NWAIT)}$ | FMC_NWAIT valid after FMC_CLK high | 2 | - | |

1. Guaranteed by characterization results.

### NAND controller waveforms and timings

*Figure 36* through *Figure 39* represent synchronous waveforms, and *Table 89* and *Table 90* provide the corresponding timings. The results shown in this table are obtained with the following FMC configuration:

- COM.FMC_SetupTime = 0x01
- COM.FMC_WaitSetupTime = 0x03
- COM.FMC_HoldSetupTime = 0x02
- COM.FMC_HiZSetupTime = 0x01
- ATT.FMC_SetupTime = 0x01
- ATT.FMC_WaitSetupTime = 0x03
- ATT.FMC_HoldSetupTime = 0x02
- ATT.FMC_HiZSetupTime = 0x01
- Bank = FMC_Bank_NAND
- MemoryDataWidth = FMC_MemoryDataWidth_16b
- ECC = FMC_ECC_Enable
- ECCPageSize = FMC_ECCPageSize_512Bytes
- TCLRSetupTime = 0
- TARSetupTime = 0
- Capacitive load $C_L$ = 30 pF

In all timing tables, the $T_{fmc_ker_ck}$ is the fmc_ker_ck clock period.

**Figure 36. NAND controller waveforms for read access**

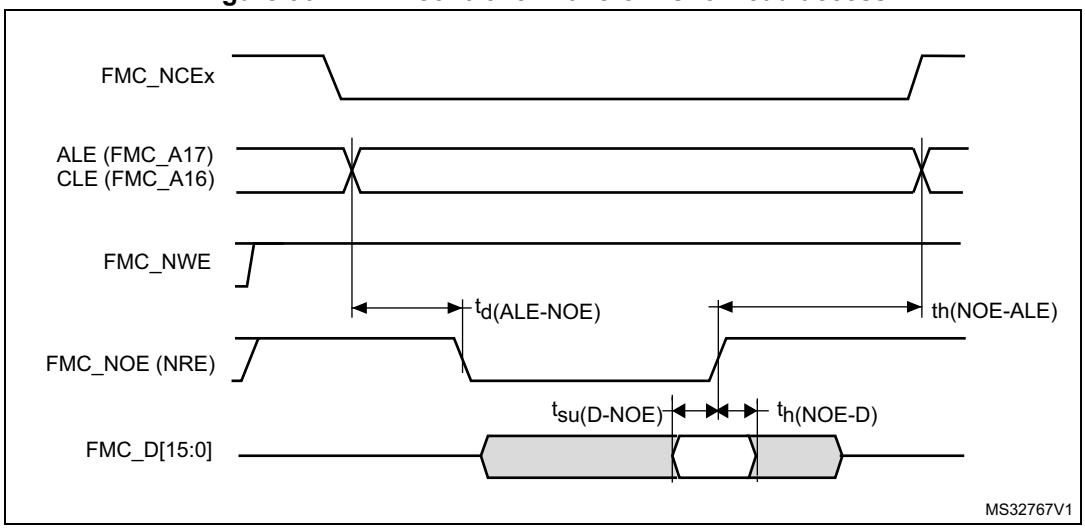


**Figure 37. NAND controller waveforms for write access**

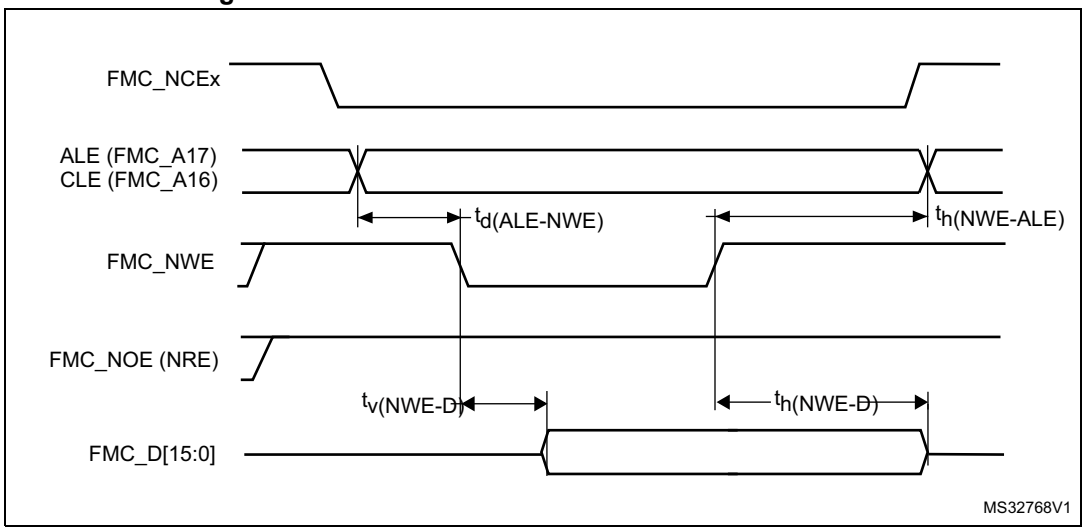



**Figure 38. NAND controller waveforms for common memory read access**

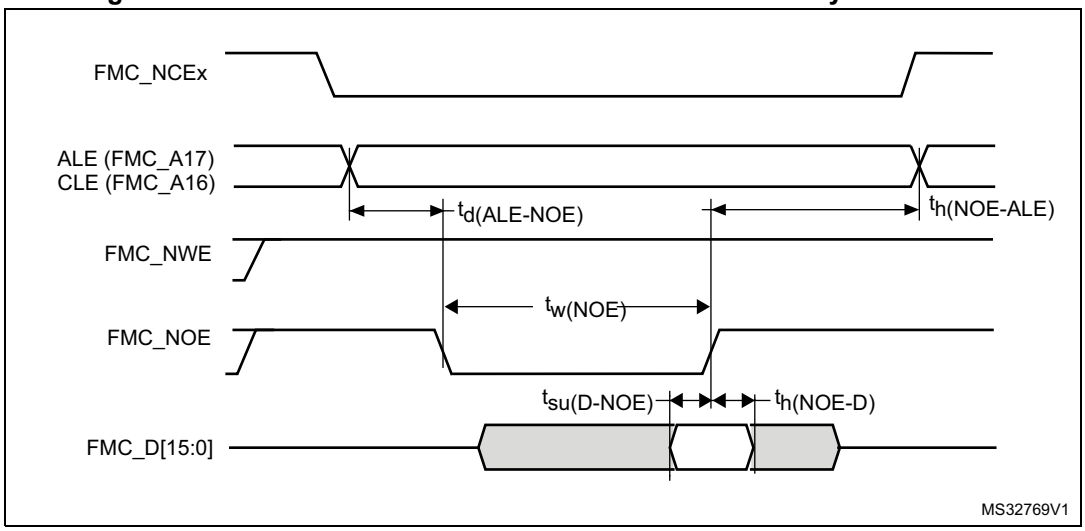


**Figure 39. NAND controller waveforms for common memory write access**

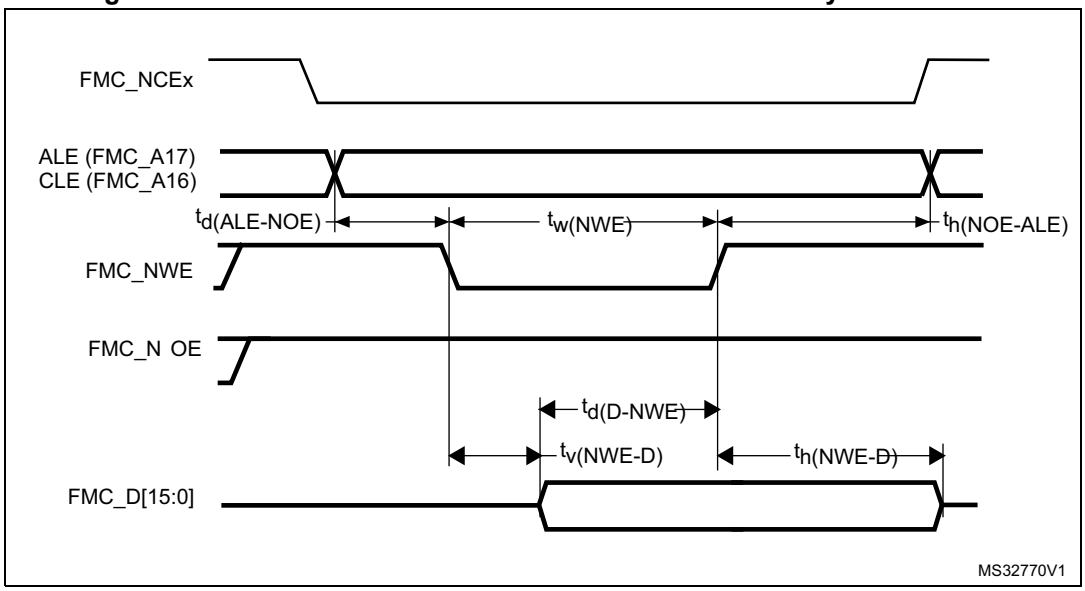



**Table 89. Switching characteristics for NAND Flash read cycles(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(N0E)}$ | FMC_NOE low width | $4T_{fmc_ker_ck} - 0.5$ | $4T_{fmc_ker_ck} + 0.5$ | ns |
| $t_{su(D-NOE)}$ | FMC_D[15-0] valid data before FMC_NOE high | 8 | - | |
| $t_{h(NOE-D)}$ | FMC_D[15-0] valid data after FMC_NOE high | 0 | - | |
| $t_{d(ALE-NOE)}$ | FMC_ALE valid before FMC_NOE low | - | $3T_{fmc_ker_ck} + 1$ | |
| $t_{h(NOE-ALE)}$ | FMC_NWE high to FMC_ALE invalid | $4T_{fmc_ker_ck} - 2$ | - | |

1. Guaranteed by characterization results.

**Table 90. Switching characteristics for NAND Flash write cycles(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NWE)}$ | FMC_NWE low width | $4T_{fmc_ker_ck} - 0.5$ | $4T_{fmc_ker_ck} + 0.5$ | ns |
| $t_{v(NWE-D)}$ | FMC_NWE low to FMC_D[15-0] valid | 0 | - | |
| $t_{h(NWE-D)}$ | FMC_NWE high to FMC_D[15-0] invalid | $2T_{fmc_ker_ck} - 0.5$ | - | |
| $t_{d(D-NWE)}$ | FMC_D[15-0] valid before FMC_NWE high | $5T_{fmc_ker_ck} - 1$ | - | |
| $t_{d(ALE-NWE)}$ | FMC_ALE valid before FMC_NWE low | - | $3T_{fmc_ker_ck} + 0.5$ | |
| $t_{h(NWE-ALE)}$ | FMC_NWE high to FMC_ALE invalid | $2T_{fmc_ker_ck} - 1$ | - | |

1. Guaranteed by characterization results.

### SDRAM waveforms and timings

In all timing tables, the TKERCK is the fmc_ker_ck clock period, with the following FMC_SDCLK maximum values:

- For 2.7 V<$V_{DD}$<3.6 V: FMC_CLK =110 MHz at 20 pF
- For 1.8 V<$V_{DD}$<1.9 V: FMC_CLK =100 MHz at 20 pF
- For 1.62 V<$_{DD}$<1.8 V, FMC_CLK =100 MHz at 15 pF

**Figure 40. SDRAM read access waveforms (CL = 1)**

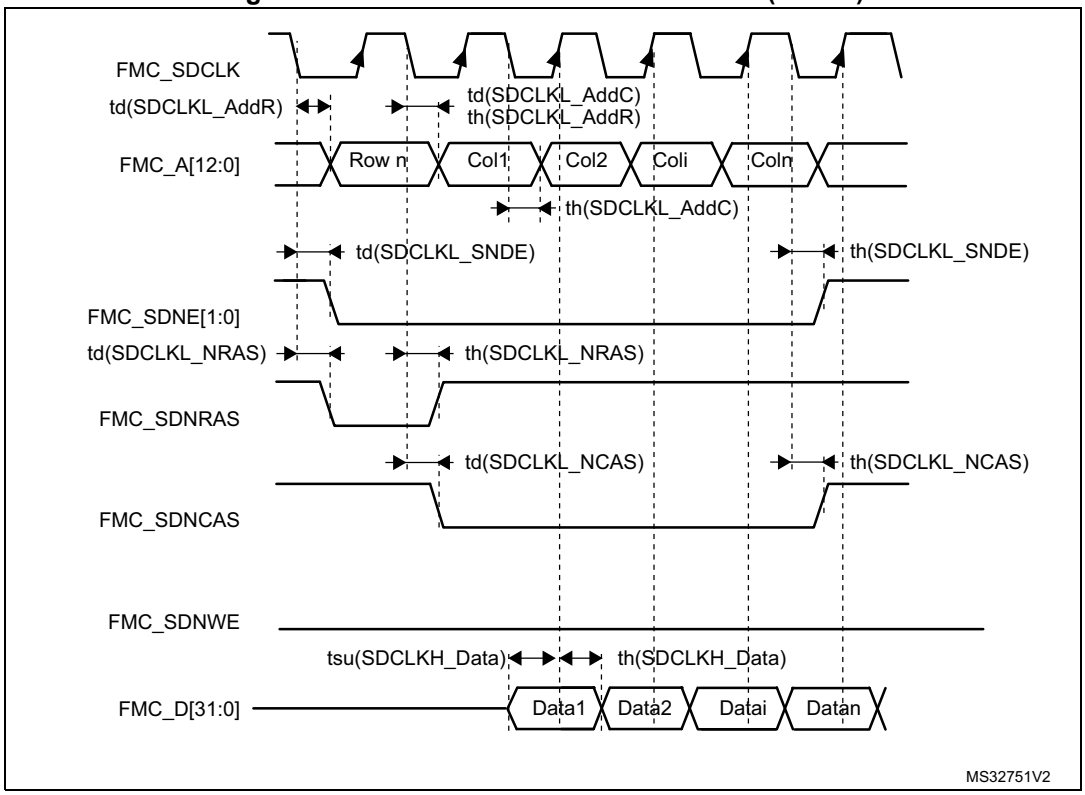


**Table 91. SDRAM read timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{fmc_ker_ck} - 1$ | $2T_{fmc_ker_ck}$ +0.5 | ns |
| $t_{su(SDCLKH_Data)}$ | Data input setup time | 2 | - | |
| $t_{h(SDCLKH_Data)}$ | Data input hold time | 1 | - | |
| $t_{d(SDCLKL_Add)}$ | Address valid time | - | 1.5 | |
| $t_{d(SDCLKL-SDNE)}$ | Chip select valid time | - | 1.5 | |
| $t_{h(SDCLKL_SDNE)}$ | Chip select hold time | 0.5 | - | |
| $t_{d(SDCLKL_SDNRAS)}$ | SDNRAS valid time | - | 1 | |
| $t_{h(SDCLKL_SDNRAS)}$ | SDNRAS hold time | 0.5 | - | |
| $t_{d(SDCLKL_SDNCAS)}$ | SDNCAS valid time | - | 0.5 | |
| $t_{h(SDCLKL_SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

**Table 92. LPSDR SDRAM read timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{W(SDCLK)}$ | FMC_SDCLK period | $2T_{fmc_ker_ck} - 1$ | $2T_{fmc_ker_ck}$+0.5 | ns |
| $t_{su(SDCLKH_Data)}$ | Data input setup time | 2 | - | |
| $t_{h(SDCLKH_Data)}$ | Data input hold time | 1.5 | - | |
| $t_{d(SDCLKL_Add)}$ | Address valid time | - | 2.5 | |
| $t_{d(SDCLKL_SDNE)}$ | Chip select valid time | - | 2.5 | |
| $t_{h(SDCLKL_SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL_SDNRAS}$ | SDNRAS valid time | - | 0.5 | |
| $t_{h(SDCLKL_SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL_SDNCAS)}$ | SDNCAS valid time | - | 1.5 | |
| $t_{h(SDCLKL_SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

**Figure 41. SDRAM write access waveforms**

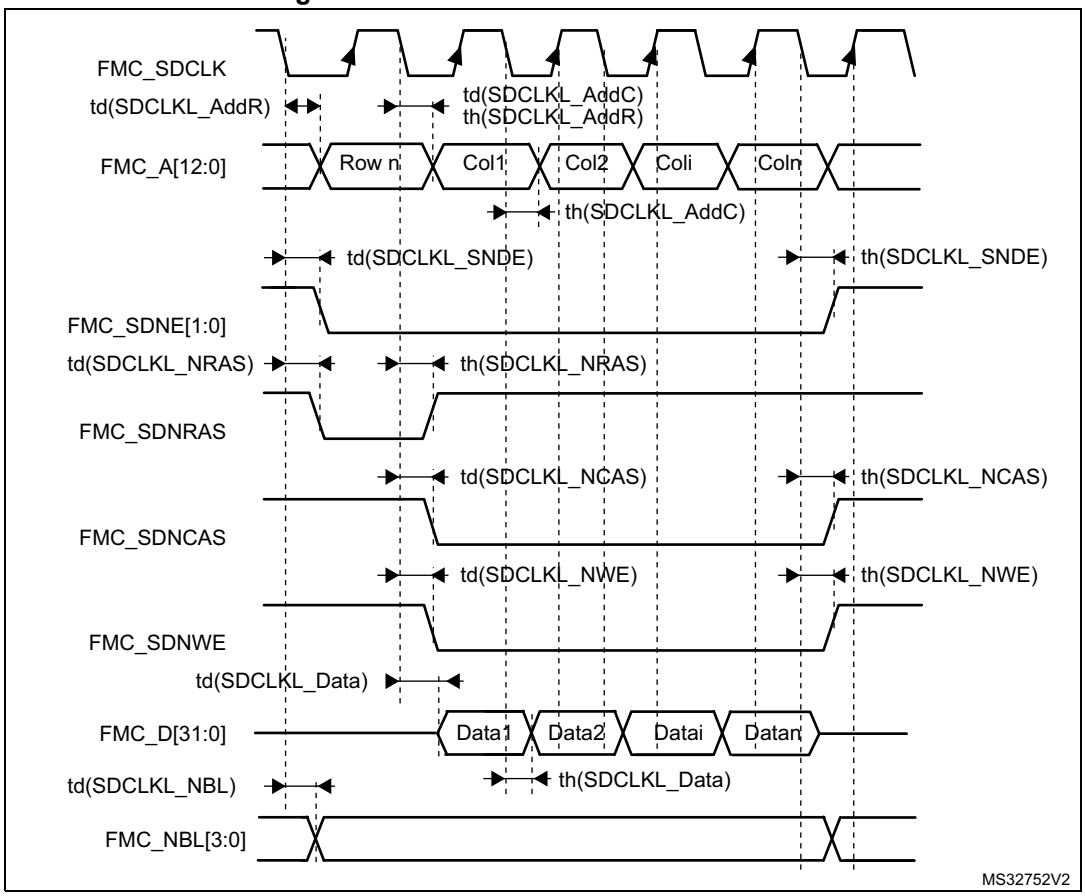



**Table 93. SDRAM Write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{fmc_ker_ck} - 1$ | $2T_{fmc_ker_ck}+0.5$ | ns |
| $t_{d(SDCLKL_Data)}$ | Data output valid time | - | 1 | |
| $t_{h(SDCLKL_Data)}$ | Data output hold time | 0 | - | |
| $t_{d(SDCLKL_Add)}$ | Address valid time | - | 1.5 | |
| $t_{d(SDCLKL_SDNWE)}$ | SDNWE valid time | - | 1.5 | |
| $t_{h(SDCLKL_SDNWE)}$ | SDNWE hold time | 0.5 | - | |
| $t_{d(SDCLKL_SDNE)}$ | Chip select valid time | - | 1.5 | |
| $t_{h(SDCLKL-_SDNE)}$ | Chip select hold time | 0.5 | - | |
| $t_{d(SDCLKL_SDNRAS)}$ | SDNRAS valid time | - | 1 | |
| $t_{h(SDCLKL_SDNRAS)}$ | SDNRAS hold time | 0.5 | - | |
| $t_{d(SDCLKL_SDNCAS)}$ | SDNCAS valid time | - | 1 | |
| $t_{d(SDCLKL_SDNCAS)}$ | SDNCAS hold time | 0.5 | - | |

1. Guaranteed by characterization results.

**Table 94. LPSDR SDRAM Write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(SDCLK)}$ | FMC_SDCLK period | $2T_{fmc_ker_ck} - 1$ | $2T_{fmc_ker_ck}+0.5$ | ns |
| $t_{d(SDCLKL_Data)}$ | Data output valid time | - | 2.5 | |
| $t_{h(SDCLKL_Data)}$ | Data output hold time | 0 | - | |
| $t_{d(SDCLKL_Add)}$ | Address valid time | - | 2.5 | |
| $t_{d(SDCLKL-SDNWE)}$ | SDNWE valid time | - | 2.5 | |
| $t_{h(SDCLKL-SDNWE)}$ | SDNWE hold time | 0 | - | |
| $t_{d(SDCLKL- SDNE)}$ | Chip select valid time | - | 3 | |
| $t_{h(SDCLKL- SDNE)}$ | Chip select hold time | 0 | - | |
| $t_{d(SDCLKL-SDNRAS)}$ | SDNRAS valid time | - | 1.5 | |
| $t_{h(SDCLKL-SDNRAS)}$ | SDNRAS hold time | 0 | - | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS valid time | - | 1.5 | |
| $t_{d(SDCLKL-SDNCAS)}$ | SDNCAS hold time | 0 | - | |

1. Guaranteed by characterization results.

## 6.3.21 Quad-SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 95* and *Table 96* for QUADSPI are derived from tests performed under the ambient temperature, $f_{AHB}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1

Refer to *Section 6.3.18: I/O port characteristics* for more details on the input/output alternate function characteristics.

The following table summarizes the parameters measured in SDR mode.

**Table 95. QUADSPI characteristics in SDR mode(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{ck1}1/T_{CK}$ | QUADSPI clock frequency | $2.7<V_{DD}<3.6$ V<br>CL = 20 pF | - | - | 133 | MHz |
| | | $1.62<V_{DD}<3.6$ V<br>CL = 15 pF | - | - | 100 | |

**Table 95. QUADSPI characteristics in SDR mode(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{w(CKH)}$ | QUADSPI clock high and low time Even division | PRESCALER[7:0] = n = 0,1,3,5... | $T_{CK}/2–0.5$ | - | $T_{CK}/2$ | ns |
| $t_{w(CKL)}$ | | | $T_{CK}/2$ | - | $T_{CK}/2+0.5$ | |
| $t_{w(CKH)}$ | QUADSPI clock high and low time Odd division | PRESCALER[7:0] = n = 2,4,6,8... | $(n/2)*T_{CK}/(n+1)-0.5$ | - | $(n/2)*T_{CK}/ (n+1)$ | |
| $t_{w(CKL)}$ | | | $(n/2+1)*T_{CK}/(n+1)$ | - | $(n/2+1)*T_{CK}/ (n+1)+0.5$ | |
| $t_{s(IN)}$ | Data input setup time | - | 1 | - | - | |
| $t_{h(IN)}$ | Data input hold time | | 3.5 | - | - | |
| $t_{v(OUT)}$ | Data output valid time | - | - | 1 | 2 | |
| $t_{h(OUT)}$ | Data output hold time | - | 0 | - | - | |

1. Guaranteed by characterization results.

The following table summarizes the parameters measured in DDR mode.

**Table 96. QUADSPI characteristics in DDR mode(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{ck1}1/T_{CK}$ | QUADSPI clock frequency | $2.7<V_{DD}<3.6$ V CL = 20 pF | - | - | 100 | MHz |
| | | $1.62<V_{DD}<3.6$ V CL = 15 pF | - | - | 100 | |
| $t_{w(CKH)}$ | QUADSPI clock high and low time Even division | PRESCALER[7:0] = n = 0,1,3,5... | $T_{CK}/2–0.5$ | - | $T_{CK}/2$ | ns |
| $t_{w(CKL)}$ | | | $T_{CK}/2$ | - | $T_{CK}/2+0.5$ | |
| $t_{w(CKH)}$ | QUADSPI clock high and low time Odd division | PRESCALER[7:0] = n = 2,4,6,8... | $(n/2)*T_{CK}/(n+1)-0.5$ | - | $(n/2)*T_{CK}/(n+1)$ | |
| $t_{w(CKL)}$ | | | $(n/2+1)*T_{CK}/(n+1)$ | - | $(n/2+1)*T_{CK}/(n+1)+0.5$ | |
| $t_{sr(IN)}$, $t_{sf(IN)}$ | Data input setup time | - | 1.5 | - | - | |
| $t_{hr(IN)}$,$t_{hf(IN)}$ | Data input hold time | - | 3.5 | - | - | |
| $t_{vr(OUT)}$, $t_{vf(OUT)}$ | Data output valid time | DHHC=0 | - | 5 | 6 | |
| | | DHHC=1 PRESCALER[7:0] = 1,2… | - | $T_{CK}/4+1$ | $T_{CK}/4+2$ | |
| $t_{hr(OUT)}$, $t_{hf(OUT)}$ | Data output hold time | DHHC=0 | 3 | - | - | |
| | | DHHC=1 PRESCALER[7:0]=1,2… | $T_{CK}/4$ | - | - | |

1. Guaranteed by characterization results.

**Figure 42. Quad-SPI timing diagram - SDR mode**

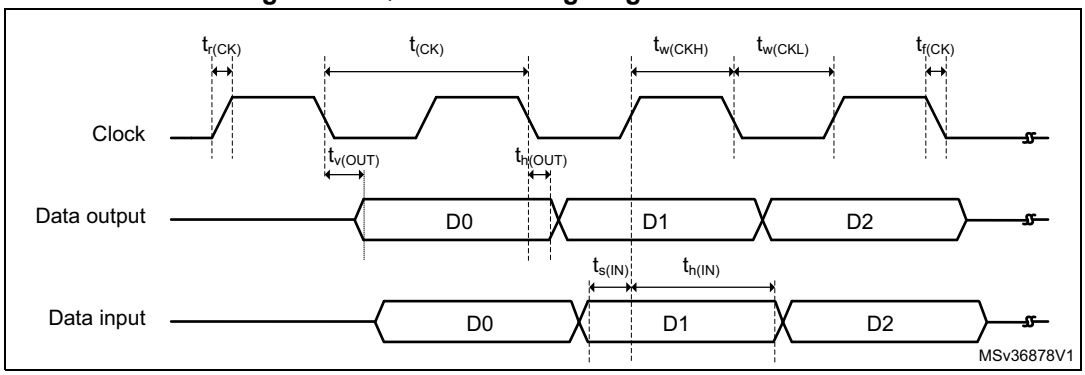
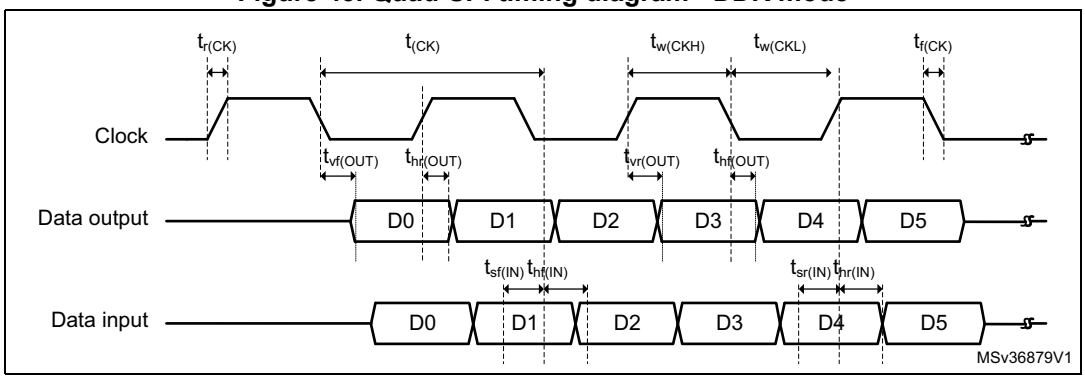



**Figure 43. Quad-SPI timing diagram - DDR mode**




## 6.3.22 Delay block (DLYB) characteristics

Unless otherwise specified, the parameters given in *Table 97* for Delay Block are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and VDD supply voltage summarized in *Table 22: General operating conditions*, with the following configuration:

**Table 97. Delay Block characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{init}$ | Initial delay | - | 1400 | 2200 | 2400 | ps |
| $t_{\Delta}$ | Unit Delay | - | 35 | 40 | 45 | - |

### 6.3.23 16-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 98* are derived from tests performed under the ambient temperature, $f_{PCLK2}$ frequency and $V_{DDA}$ supply voltage conditions summarized in *Table 22: General operating conditions*.

**Table 98. ADC characteristics(1)(2)**

| Symbol | Parameter | Conditions | | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage for ADC ON | - | | | | 1.62 | - | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | - | | | | 1.62 | - | $V_{DDA}$ | V |
| $V_{REF-}$ | Negative reference voltage | - | | | | $V_{SSA}$ | | | V |
| $f_{ADC}$ | ADC clock frequency | 1.62 V ≤ VDDA ≤ 3.6 V | | | BOOST = 11 | 0.12 | - | 50 | MHz |
| | | | | | BOOST = 10 | 0.12 | - | 25 | |
| | | | | | BOOST = 01 | 0.12 | - | 12.5 | |
| | | | | | BOOST = 00 | - | - | 6.25 | |
| $f_s$(3) | Sampling rate for Direct channels(4) | Resolution = 16 bits, $V_{DDA}$ >2.5 V | $T_J$ = 90 °C | $f_{ADC}$=36 MHz | SMP = 1.5 | - | - | 3.60 | MSps |
| | | Resolution = 16 bits | | $f_{ADC}$=37 MHz | SMP = 2.5 | - | - | 3.35 | |
| | | Resolution = 14 bits | $T_J$ = 125 °C | $f_{ADC}$ = 50 MHz | SMP = 2.5 | - | - | 5.00 | |
| | | Resolution = 12 bits | | $f_{ADC}$ = 50 MHz | SMP = 2.5 | - | - | 5.50 | |
| | | Resolution = 10 bits | | $f_{ADC}$ = 50 MHz | SMP = 1.5 | - | - | 7.10 | |
| | | Resolution = 8 bits | | $f_{ADC}$ = 50 MHz | SMP = 1.5 | - | - | 8.30 | |
| | Sampling rate for Fast channels | Resolution = 16 bits, $V_{DDA}$ >2.5 V | $T_J$ = 90 °C | $f_{ADC}$=32 MHz | SMP = 2.5 | - | - | 2.90 | |
| | | Resolution = 16 bits | | $f_{ADC}$=31 MHz | SMP = 2.5 | - | - | 2.80 | |
| | | Resolution = 14 bits | $T_J$ = 125 °C | $f_{ADC}$ = 33 MHz | SMP = 2.5 | - | - | 3.30 | |
| | | Resolution = 12 bits | | $f_{ADC}$ = 39 MHz | SMP = 2.5 | - | - | 4.30 | |
| | | Resolution = 10 bits | | $f_{ADC}$ = 48 MHz | SMP = 2.5 | - | - | 6.00 | |
| | | Resolution = 8 bits | | $f_{ADC}$ = 50 MHz | SMP = 2.5 | - | - | 7.10 | |
| | Sampling rate for Slow channels | Resolution = 16 bits | $T_J$ = 90 °C | $f_{ADC}$ = 10 MHz | SMP = 1.5 | - | - | 1.00 | |
| | | resolution = 14 bits | $T_J$ = 125 °C | | | - | - | | |
| | | resolution = 12 bits | | | | - | - | | |
| | | resolution = 10 bits | | | | - | - | | |
| | | resolution = 8 bits | | | | - | - | | |
| $t_{TRIG}$ | External trigger period | Resolution = 16 bits | | | | - | - | 10 | 1/ $f_{ADC}$ |
| $V_{AIN}$(5) | Conversion voltage range | - | | | | 0 | - | $V_{REF+}$ | V |
| $V_{CMIV}$ | Common mode input voltage | - | | | | $V_{REF}$/2 − 10% | $V_{REF}$/ 2 | $V_{REF}$/2 + 10% | V |

**Table 98. ADC characteristics(1)(2) (continued)**

| Symbol | Parameter | Conditions | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $R_{AIN}$(6) | External input impedance | Resolution = 16 bits, $T_J$ = 125 °C | - | - | - | - | 170 | Ω |
| | | Resolution = 14 bits, $T_J$ = 125 °C | - | - | - | - | 435 | |
| | | Resolution = 12 bits, $T_J$ =125 °C | - | - | - | - | 1150 | |
| | | Resolution = 10 bits, $T_J$ = 125 °C | - | - | - | - | 5650 | |
| | | Resolution = 8 bits, $T_J$ = 125 °C | - | - | - | - | 26500 | |
| $C_{ADC}$ | Internal sample and hold capacitor | - | | | - | 4 | - | pF |
| $t_{ADCVREG_STUP}$ | ADC LDO startup time | - | | | - | 5 | 10 | us |
| $t_{STAB}$ | ADC Power-up time | LDO already started | | | 1 | - | - | conversion cycle |
| $t_{CAL}$ | Offset and linearity calibration time | - | | | 165010 | - | - | $1/f_{ADC}$ |
| $t_{OFF_CAL}$ | Offset calibration time | - | | | 1280 | - | - | $1/f_{ADC}$ |
| $t_{LATR}$ | Trigger conversion latency regular and injected channels without conversion abort | CKMODE = 00 | | | 1.5 | 2 | 2.5 | $1/f_{ADC}$ |
| | | CKMODE = 01 | | | - | - | 2.5 | |
| | | CKMODE = 10 | | | - | - | 2.5 | |
| | | CKMODE = 11 | | | - | - | 2.25 | |
| $t_{LATRINJ}$ | Trigger conversion latency regular injected channels aborting a regular conversion | CKMODE = 00 | | | 2.5 | 3 | 3.5 | $1/f_{ADC}$ |
| | | CKMODE = 01 | | | - | - | 3.5 | |
| | | CKMODE = 10 | | | - | - | 3.5 | |
| | | CKMODE = 11 | | | - | - | 3.25 | |
| $t_S$ | Sampling time | - | | | 1.5 | - | 810.5 | $1/f_{ADC}$ |
| $t_{CONV}$ | Total conversion time (including sampling time) | Resolution = N bits | | | ts + 0.5 + N/2 | - | - | $1/f_{ADC}$ |

**Table 98. ADC characteristics(1)(2) (continued)**

| Symbol | Parameter | Conditions | | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $I_{DDA_D}$ (ADC) | ADC consumption on $V_{DDA}$, BOOST=11, Differential mode | Resolution = 16 bits, $f_{ADC}$=25 MHz | - | - | - | 1440 | - | µA |
| | | Resolution = 14 bits, $f_{ADC}$=30 MHz | - | - | - | 1350 | - | |
| | | Resolution = 12 bits, $f_{ADC}$=40 MHz | - | - | - | 990 | - | |
| | ADC consumption on $V_{DDA}$ BOOST=10, Differential mode $f_{ADC}$=25 MHz | Resolution = 16 bits | - | - | - | 1080 | - | |
| | | Resolution = 14 bits | - | - | - | 810 | - | |
| | | Resolution = 12 bits | - | - | - | 585 | - | |
| | ADC consumption on $V_{DDA}$ BOOST=01, Differential mode $f_{ADC}$=12.5 MHz | Resolution = 16 bits | - | - | - | 630 | - | |
| | | Resolution = 14 bits | - | - | - | 432 | - | |
| | | Resolution = 12 bits | - | - | - | 315 | - | |
| | ADC consumption on $V_{DDA}$ BOOST=00, Differential mode $f_{ADC}$=6.25 MHz | Resolution = 16 bits | - | - | - | 360 | - | |
| | | Resolution = 14 bits | - | - | - | 270 | - | |
| | | Resolution = 12 bits | - | - | - | 225 | - | |
| $I_{DDA_SE}$( ADC) | ADC consumption on $V_{DDA}$ BOOST=11, Single-ended mode | Resolution = 16 bits, $f_{ADC}$=25 MHz | - | - | - | 720 | - | |
| | | Resolution = 14 bits, $f_{ADC}$=30 MHz | - | - | - | 675 | - | |
| | | Resolution = 12 bits, $f_{ADC}$=40 MHz | - | - | - | 495 | - | |
| | ADC consumption on $V_{DDA}$ BOOST=10, Singl-ended mode $f_{ADC}$=25 MHz | Resolution = 16 bits | - | - | - | 540 | - | |
| | | Resolution = 14 bits | - | - | - | 405 | - | |
| | | Resolution = 12 bits | - | - | - | 292.5 | - | |
| | ADC consumption on $V_{DDA}$ BOOST=01, Single-ended mode $f_{ADC}$=12.5 MHz | Resolution = 16 bits | - | - | - | 315 | - | |
| | | Resolution = 14 bits | - | - | - | 216 | - | |
| | | Resolution = 12 bits | - | - | - | 157.5 | - | |
| | ADC consumption on $V_{DDA}$ BOOST=00, Single-ended mode $f_{ADC}$=6.25 MHz | Resolution = 16 bits | - | - | - | 180 | - | |
| | | Resolution = 14 bits | - | - | - | 135 | - | |
| | | Resolution = 12 bits | - | - | - | 112.5 | - | |
| $I_{DD}$ (ADC) | ADC consumption on $V_{DD}$ | $f_{ADC}$=50 MHz | - | - | - | 400 | - | |
| | | $f_{ADC}$=25 MHz | - | - | - | 220 | - | |
| | | $f_{ADC}$=12.5 MHz | - | - | - | 180 | - | |
| | | $f_{ADC}$=6.25 MHz | - | - | - | 120 | - | |
| | | $f_{ADC}$=3.125 MHz | - | - | - | 80 | - | |

1. Guaranteed by design.
2. The voltage booster on ADC switches must be used for VDDA < 2.4 V (embedded I/O switches).
3. These values are valid for UFBGA169 and one ADC. The values for other packages and multiple ADCs may be different.
4. Direct channels are connected to analog I/Os (PA0_C, PA1_C, PC2_C and PC3_C) to optimize ADC performance.
5. Depending on the package, $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ to $V_{SSA}$.
6. The tolerance is 10 LSBs for 16-bit resolution, 4 LSBs for 14-bit resolution, and 2 LSBs for 12-bit, 10-bit and 8-bit resolutions.

**Table 99. Minimum sampling time vs $R_{AIN}$(1)(2)**

| Resolution | RAIN (Ω) | Minimum sampling time (s) | | |
|---|---|---|---|---|
| | | Direct channels(3) | Fast channels(4) | Slow channels(5) |
| 16 bits | 47 | 7.37E-08 | 1.14E-07 | 1.72E-07 |
| 14 bits | 47 | 6.29E-08 | 9.74E-08 | 1.55E-07 |
| | 68 | 6.84E-08 | 1.02E-07 | 1.58E-07 |
| | 100 | 7.80E-08 | 1.12E-07 | 1.62E-07 |
| | 150 | 9.86E-08 | 1.32E-07 | 1.80E-07 |
| | 220 | 1.32E-07 | 1.61E-07 | 2.01E-07 |
| 12 bits | 47 | 5.32E-08 | 8.00E-08 | 1.29E-07 |
| | 68 | 5.74E-08 | 8.50E-08 | 1.32E-07 |
| | 100 | 6.58E-08 | 9.31E-08 | 1.40E-07 |
| | 150 | 8.37E-08 | 1.10E-07 | 1.51E-07 |
| | 220 | 1.11E-07 | 1.34E-07 | 1.73E-07 |
| | 330 | 1.56E-07 | 1.78E-07 | 2.14E-07 |
| | 470 | 2.16E-07 | 2.39E-07 | 2.68E-07 |
| | 680 | 3.01E-07 | 3.29E-07 | 3.54E-07 |
| 10 bits | 47 | 4.34E-08 | 6.51E-08 | 1.08E-07 |
| | 68 | 4.68E-08 | 6.89E-08 | 1.11E-07 |
| | 100 | 5.35E-08 | 7.55E-08 | 1.16E-07 |
| | 150 | 6.68E-08 | 8.77E-08 | 1.26E-07 |
| | 220 | 8.80E-08 | 1.08E-07 | 1.40E-07 |
| | 330 | 1.24E-07 | 1.43E-07 | 1.71E-07 |
| | 470 | 1.69E-07 | 1.89E-07 | 2.13E-07 |
| | 680 | 2.38E-07 | 2.60E-07 | 2.80E-07 |
| | 1000 | 3.45E-07 | 3.66E-07 | 3.84E-07 |
| | 1500 | 5.15E-07 | 5.35E-07 | 5.48E-07 |
| | 2200 | 7.42E-07 | 7.75E-07 | 7.78E-07 |
| | 3300 | 1.10E-06 | 1.14E-06 | 1.14E-06 |

**Table 99. Minimum sampling time vs $R_{AIN}$ (1)(2) (continued)**

| Resolution | RAIN (Ω) | Minimum sampling time (s) | | |
|---|---|---|---|---|
| | | Direct channels(3) | Fast channels(4) | Slow channels(5) |
| 8 bits | 47 | 3.32E-08 | 5.10E-08 | 8.61E-08 |
| | 68 | 3.59E-08 | 5.35E-08 | 8.83E-08 |
| | 100 | 4.10E-08 | 5.83E-08 | 9.22E-08 |
| | 150 | 5.06E-08 | 6.76E-08 | 9.95E-08 |
| | 220 | 6.61E-08 | 8.22E-08 | 1.11E-07 |
| | 330 | 9.17E-08 | 1.08E-07 | 1.32E-07 |
| | 470 | 1.24E-07 | 1.40E-07 | 1.63E-07 |
| | 680 | 1.74E-07 | 1.91E-07 | 2.12E-07 |
| | 1000 | 2.53E-07 | 2.70E-07 | 2.85E-07 |
| | 1500 | 3.73E-07 | 3.93E-07 | 4.05E-07 |
| | 2200 | 5.39E-07 | 5.67E-07 | 5.75E-07 |
| | 3300 | 8.02E-07 | 8.36E-07 | 8.38E-07 |
| | 4700 | 1.13E-06 | 1.18E-06 | 1.18E-06 |
| | 6800 | 1.62E-06 | 1.69E-06 | 1.68E-06 |
| | 10000 | 2.36E-06 | 2.47E-06 | 2.45E-06 |
| | 15000 | 3.50E-06 | 3.69E-06 | 3.65E-06 |

1. Guaranteed by design.
2. Data valid at up to 125 °C, with a 47 pF PCB capacitor, and $V_{DDA}$=1.6 V.
3. Direct channels are connected to analog I/Os (PA0_C, PA1_C, PC2_C and PC3_C) to optimize ADC performance.
4. Fast channels correspond to PF3, PF5, PF7, PF9, PA6, PC4, PB1, PF11 and PF13.
5. Slow channels correspond to all ADC inputs except for the Direct and Fast channels.

**Table 100. ADC accuracy(1)(2)**

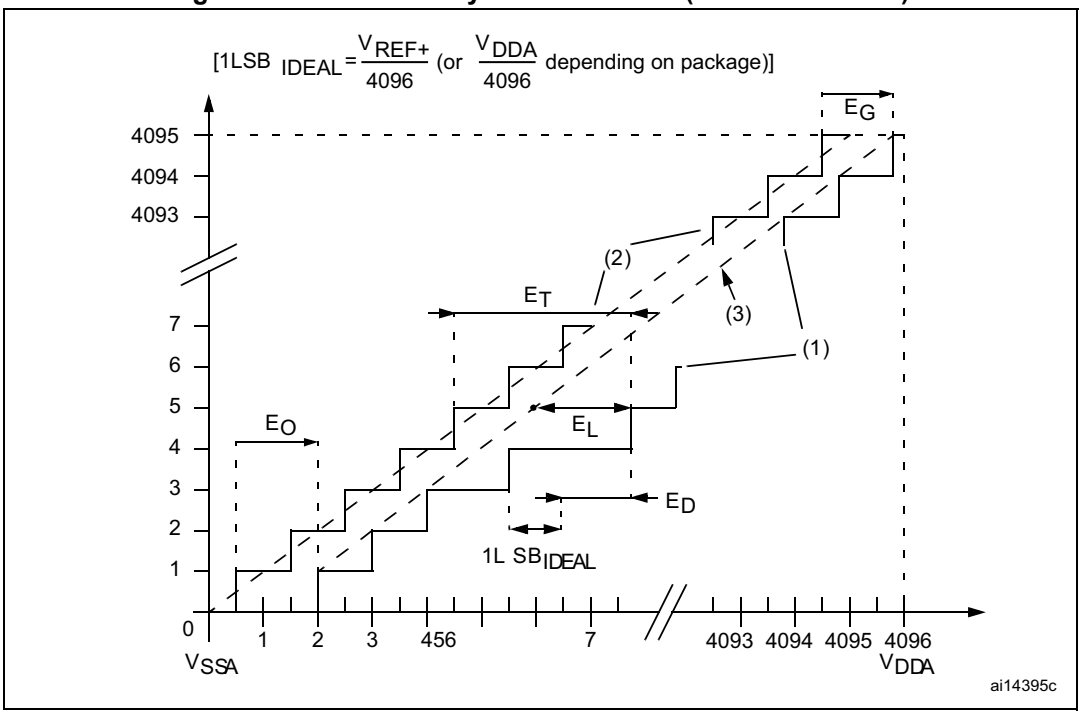
| Symbol | Parameter | Conditions(3) | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| ET | Total undadjusted error | Direct channel | Single ended | - | +10/–20 | - | LSB |
| | | | Differential | - | ±15 | - | |
| | | Fast channel | Single ended | - | +10/–20 | - | |
| | | | Differential | - | ±15 | - | |
| | | Slow channel | Single ended | - | ±10 | - | |
| | | | Differential | | ±10 | - | |
| EO | Offset error | - | | - | ±10 | - | |
| EG | Gain error | - | | - | ±15 | - | |
| ED | Differential linearity error | Single ended | | - | +3/–1 | - | |
| | | Differential | | - | +4.5/–1 | - | |
| EL | Integral linearity error | Direct channel | Single ended | - | ±11 | - | |
| | | | Differential | - | ±7 | - | |
| | | Fast channel | Single ended | - | ±13 | - | |
| | | | Differential | - | ±7 | - | |
| | | Slow channel | Single ended | - | ±10 | - | |
| | | | Differential | - | ±6 | - | |
| ENOB | Effective number of bits | Single ended | | - | 12.2 | - | Bits |
| | | Differential | | - | 13.2 | - | |
| SINAD | Signal-to-noise and distortion ratio | Single ended | | - | 75.2 | - | dB |
| | | Differential | | - | 81.2 | - | |
| SNR | Signal-to-noise ratio | Single ended | | - | 77.0 | - | |
| | | Differential | | - | 81.0 | - | |
| THD | Total harmonic distortion | Single ended | | - | 87 | - | |
| | | Differential | | - | 90 | - | |

1. Data guaranteed by characterization for BGA packages. The values for LQFP packages might differ.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC clock frequency = 25 MHz, ADC resolution = 16 bits, $V_{DDA}$=$V_{REF+}$=3.3 V and BOOST=11.

Note: ADC accuracy vs. negative injection current: injecting a negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative currents.

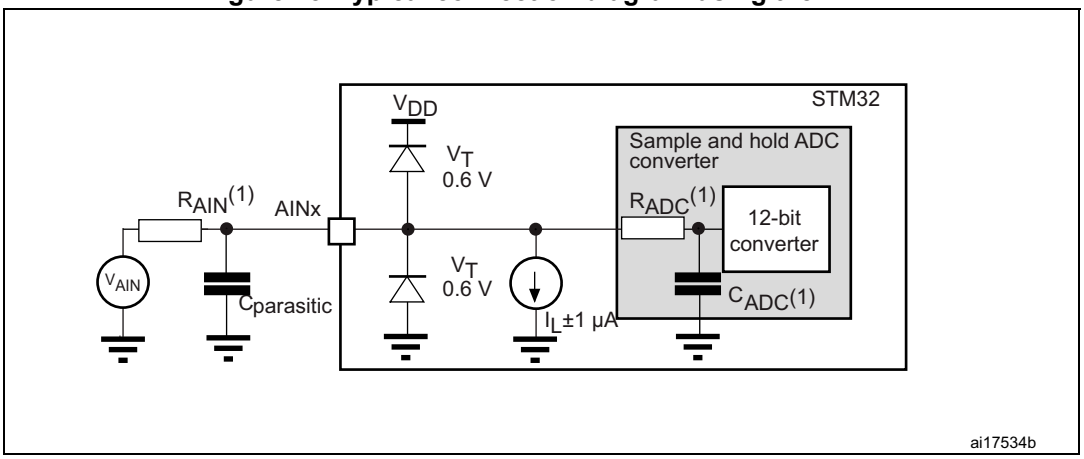
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.17* does not affect the ADC accuracy.

**Figure 44. ADC accuracy characteristics (12-bit resolution)**




1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. $E_T$ = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

**Figure 45. Typical connection diagram using the ADC**

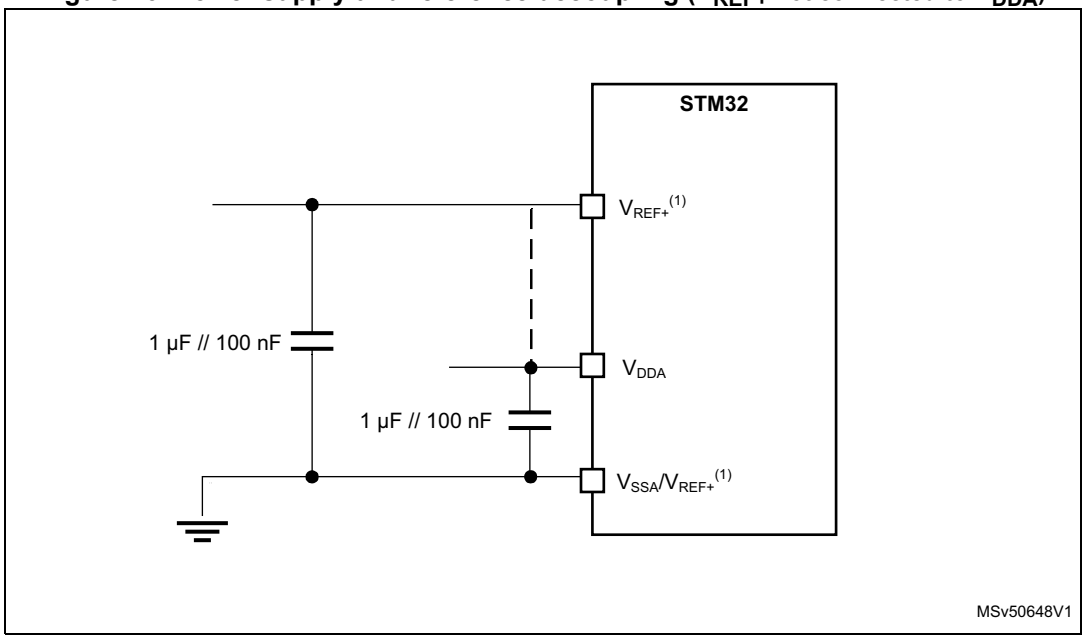



1. Refer to *Table 98* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

### General PCB design guidelines

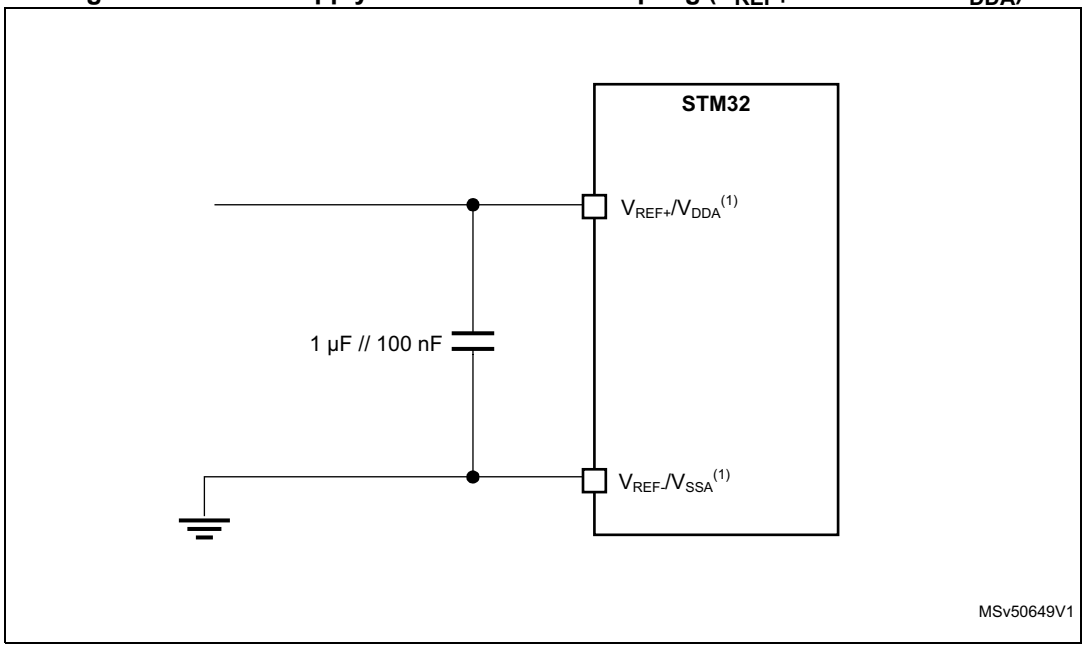
Power supply decoupling should be performed as shown in *Figure 46* or *Figure 47*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 46. Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)**




1. $V_{REF+}$ input is available on all package whereas the $V_{REF-}$ s available only on UFBGA176+25 and TFBGA240+25. When $V_{REF-}$ is not available, it is internally connected to $V_{DDA}$ and $V_{SSA}$.

**Figure 47. Power supply and reference decoupling ($V_{REF+}$ connected to $V_{DDA}$)**




1. $V_{REF+}$ input is available on all package whereas the $V_{REF-}$ s available only on UFBGA176+25 and TFBGA240+25. When $V_{REF-}$ is not available, it is internally connected to $V_{DDA}$ and $V_{SSA}$.

### 6.3.24 DAC characteristics

**Table 101. DAC characteristics(1)(2)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | 1.8 | 3.3 | 3.6 | V |
| $V_{REF+}$ | Positive reference voltage | - | | 1.80 | - | $V_{DDA}$ | |
| $V_{REF-}$ | Negative reference voltage | - | | - | $V_{SSA}$ | - | |
| $R_L$ | Resistive Load | DAC output buffer ON | connected to $V_{SSA}$ | 5 | - | - | kΩ |
| | | | connected to $V_{DDA}$ | 25 | - | - | |
| $R_O$ | Output Impedance | DAC output buffer OFF | | 10.3 | 13 | 16 | |
| $R_{BON}$ | Output impedance sample and hold mode, output buffer ON | DAC output buffer ON | $V_{DD}$ = 2.7 V | - | - | 1.6 | kΩ |
| | | | $V_{DD}$ = 2.0 V | - | - | 2.6 | |
| $R_{BOFF}$ | Output impedance sample and hold mode, output buffer OFF | DAC output buffer OFF | $V_{DD}$ = 2.7 V | - | - | 17.8 | kΩ |
| | | | $V_{DD}$ = 2.0 V | - | - | 18.7 | |
| $C_L$ | Capacitive Load | DAC output buffer OFF | | - | - | 50 | pF |
| $C_{SH}$ | | Sample and Hold mode | | - | 0.1 | 1 | µF |
| $V_{DAC_OUT}$ | Voltage on DAC_OUT output | DAC output buffer ON | | 0.2 | - | $V_{DDA}$ −0.2 | V |
| | | DAC output buffer OFF | | 0 | - | $V_{REF+}$ | |
| $t_{SETTLING}$ | Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches the final value of ±0.5LSB, ±1LSB, ±2LSB, ±4LSB, ±8LSB) | Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ | ±0.5 LSB | - | 2.05 | - | µs |
| | | | ±1 LSB | - | 1.97 | - | |
| | | | ±2 LSB | - | 1.67 | - | |
| | | | ±4 LSB | - | 1.66 | - | |
| | | | ±8 LSB | - | 1.65 | - | |
| | | Normal mode, DAC output buffer OFF, ±1LSB $C_L$=10 pF | | - | 1.7 | 2 | |
| $t_{WAKEUP}$(3) | Wakeup time from off state (setting the ENx bit in the DAC Control register) until the final value of ±1LSB is reached | Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L = 5$ kΩ | | - | 5 | 7.5 | µs |
| | | Normal mode, DAC output buffer OFF, $C_L \leq 10$ pF | | | 2 | 5 | |
| PSRR | DC $V_{DDA}$ supply rejection ratio | Normal mode, DAC output buffer ON, $C_L \leq 50$ pF, $R_L = 5$ kΩ | | - | −80 | −28 | dB |

**Table 101. DAC characteristics(1)(2) (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{SAMP}$ | Sampling time in Sample and Hold mode $C_L$=100 nF (code transition between the lowest input code and the highest input code when DAC_OUT reaches the ±1LSB final value) | MODE<2:0>_V12=100/101 (BUFFER ON) | | - | 0.7 | 2.6 | ms |
| | | MODE<2:0>_V12=110 (BUFFER OFF) | | - | 11.5 | 18.7 | |
| | | MODE<2:0>_V12=111 (INTERNAL BUFFER OFF) | | - | 0.3 | 0.6 | µs |
| $C_{lint}$ | Internal sample and hold capacitor | - | | 1.8 | 2.2 | 2.6 | pF |
| $t_{TRIM}$ | Middle code offset trim time | Minimum time to verify the each code | | 50 | - | - | µs |
| $V_{offset}$ | Middle code offset for 1 trim code step | $V_{REF+}$ = 3.6 V | | - | 850 | - | µV |
| | | $V_{REF+}$ = 1.8 V | | - | 425 | - | |
| $I_{DDA(DAC)}$ | DAC quiescent consumption from $V_{DDA}$ | DAC output buffer ON | No load, middle code (0x800) | - | 360 | - | µA |
| | | | No load, worst code (0xF1C) | - | 490 | - | |
| | | DAC output buffer OFF | No load, middle/worst code (0x800) | - | 20 | - | |
| | | Sample and Hold mode, $C_{SH}$=100 nF | | - | $360*T_{ON}/(T_{ON}+T_{OFF})$ (4) | - | |
| $I_{DDV}$(DAC) | DAC consumption from $V_{REF+}$ | DAC output buffer ON | No load, middle code (0x800) | - | 170 | - | |
| | | | No load, worst code (0xF1C) | - | 170 | - | |
| | | DAC output buffer OFF | No load, middle/worst code (0x800) | - | 160 | - | |
| | | Sample and Hold mode, Buffer ON, $C_{SH}$=100 nF (worst code) | | - | $170*T_{ON}/(T_{ON}+T_{OFF})$ (4) | - | |
| | | Sample and Hold mode, Buffer OFF, $C_{SH}$=100 nF (worst code) | | - | $160*T_{ON}/(T_{ON}+T_{OFF})$ (4) | - | |

1. Guaranteed by design unless otherwise specified.

2. TBD stands for “to be defined”.
3. In buffered mode, the output can overshoot above the final value for low input code (starting from the minimum value).
4. $T_{ON}$ is the refresh phase duration, while $T_{OFF}$ is the hold phase duration. Refer to the product reference manual for more details.

**Table 102. DAC accuracy(1)**

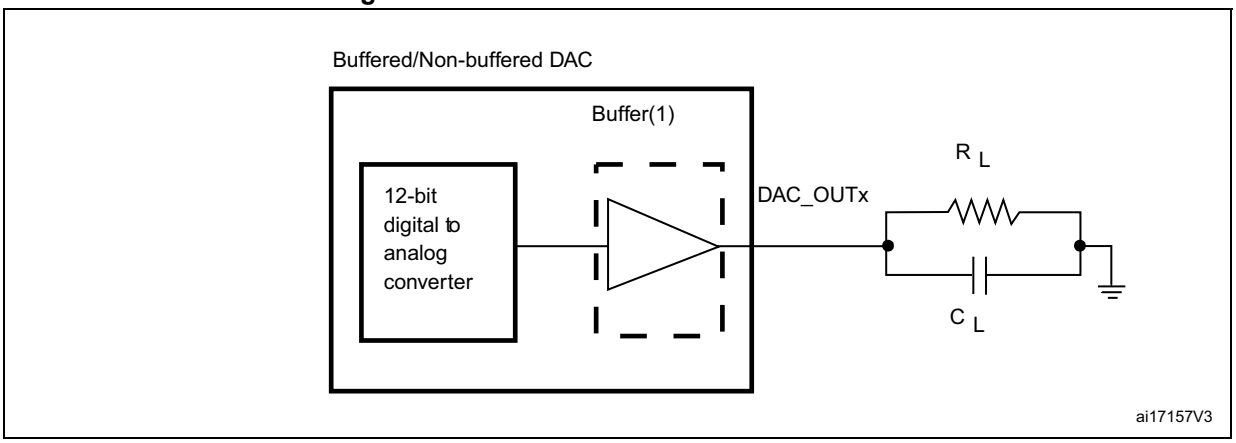
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| DNL | Differential non linearity(2) | DAC output buffer ON | | −2 | - | 2 | LSB |
| | | DAC output buffer OFF | | −2 | - | 2 | |
| - | Monotonicity | 10 bits | | - | - | - | - |
| INL | Integral non linearity(3) | DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ | | −4 | - | 4 | LSB |
| | | DAC output buffer OFF, $C_L \le 50$ pF, no $R_L$ | | −4 | - | 4 | |
| Offset | Offset error at code 0x800 (3) | DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ | $V_{REF+} = 3.6$ V | - | - | ±15 | LSB |
| | | | $V_{REF+} = 1.8$ V | - | - | ±30 | |
| | | DAC output buffer OFF, $C_L \le 50$ pF, no $R_L$ | | - | - | ±8 | |
| Offset1 | Offset error at code 0x001(4) | DAC output buffer OFF, $C_L \le 50$ pF, no $R_L$ | | - | - | ±5 | LSB |
| OffsetCal | Offset error at code 0x800 after factory calibration | DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ | $V_{REF+} = 3.6$ V | - | - | ±6 | LSB |
| | | | $V_{REF+} = 1.8$ V | - | - | ±7 | |
| Gain | Gain error(5) | DAC output buffer ON,$C_L \le 50$ pF, $R_L \ge 5$ kΩ | | - | - | ±1 | % |
| | | DAC output buffer OFF, $C_L \le 50$ pF, no $R_L$ | | - | - | ±1 | |
| SNR | Signal-to-noise ratio(6) | DAC output buffer ON,$C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1 kHz, BW = 500 KHz | | - | 67.8 | - | dB |
| | | DAC output buffer OFF, $C_L \le 50$ pF, no $R_L$,1 kHz, BW = 500 KHz | | - | 67.8 | - | |
| THD | Total harmonic distortion(6) | DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1 kHz | | - | −78.6 | - | dB |
| | | DAC output buffer OFF, $C_L \le 50$ pF, no $R_L$, 1 kHz | | - | −78.6 | - | |
| SINAD | Signal-to-noise and distortion ratio(6) | DAC output buffer ON, $C_L \le 50$ pF, $R_L \ge 5$ kΩ , 1 kHz | | - | 67.5 | - | dB |
| | | DAC output buffer OFF, $C_L \le 50$ pF, no $R_L$, 1 kHz | | - | 67.5 | - | |

**Table 102. DAC accuracy(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ENOB | Effective number of bits | DAC output buffer ON, $C_L \leq 50$ pF, $R_L \geq 5$ kΩ , 1 kHz | - | 10.9 | - | bits |
| | | DAC output buffer OFF, $C_L \leq 50$ pF, no $R_L$, 1 kHz | - | 10.9 | - | |

1. Guaranteed by characterization.
2. Difference between two consecutive codes minus 1 LSB.
3. Difference between the value measured at Code i and the value measured at Code i on a line drawn between Code 0 and last Code 4095.
4. Difference between the value measured at Code (0x001) and the ideal value.
5. Difference between the ideal slope of the transfer function and the measured slope computed from code 0x000 and 0xFFF when the buffer is OFF, and from code giving 0.2 V and ($V_{REF+}$ - 0.2 V) when the buffer is ON.
6. Signal is −0.5dBFS with $F_{sampling}$=1 MHz.

**Figure 48. 12-bit buffered /non-buffered DAC**




1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

### 6.3.25 Voltage reference buffer characteristics

**Table 103. VREFBUF characteristics(1)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | Normal mode | VSCALE = 000 | 2.8 | 3.3 | 3.6 | V |
| | | | VSCALE = 001 | 2.4 | - | 3.6 | |
| | | | VSCALE = 010 | 2.1 | - | 3.6 | |
| | | | VSCALE = 011 | 1.8 | - | 3.6 | |
| | | Degraded mode | VSCALE = 000 | 1.62 | - | 2.80 | |
| | | | VSCALE = 001 | 1.62 | - | 2.40 | |
| | | | VSCALE = 010 | 1.62 | - | 2.10 | |
| | | | VSCALE = 011 | 1.62 | - | 1.80 | |
| $V_{REFBUF_OUT}$ | Voltage Reference Buffer Output, at 30 °C, $I_{load}$= 100 µA | Normal mode | VSCALE = 000 | 2.498 | 2.5 | 2.5035 | |
| | | | VSCALE = 001 | 2.046 | 2.049 | 2.052 | |
| | | | VSCALE = 010 | 1.801 | 1.804 | 1.806 | |
| | | | VSCALE = 011 | 1.4995 | 1.5015 | 1.504 | |
| | | Degraded mode(2) | VSCALE = 000 | $V_{DDA}$– 150 mV | - | $V_{DDA}$ | |
| | | | VSCALE = 001 | $V_{DDA}$– 150 mV | - | $V_{DDA}$ | |
| | | | VSCALE = 010 | $V_{DDA}$– 150 mV | - | $V_{DDA}$ | |
| | | | VSCALE = 011 | $V_{DDA}$– 150 mV | - | $V_{DDA}$ | |
| TRIM | Trim step resolution | - | - | - | ±0.05 | ±0.1 | % |
| $C_L$ | Load capacitor | - | - | 0.5 | 1 | 1.50 | uF |
| esr | Equivalent Serial Resistor of $C_L$ | - | - | - | - | 2 | Ω |
| $I_{load}$ | Static load current | - | - | - | - | 4 | mA |
| $I_{line_reg}$ | Line regulation | 2.8 V ≤ $V_{DDA}$ ≤ 3.6 V | $I_{load}$ = 500 µA | - | 200 | - | ppm/V |
| | | | $I_{load}$ = 4 mA | - | 100 | - | |
| $I_{load_reg}$ | Load regulation | 500 µA ≤ $I_{LOAD}$ ≤ 4 mA | Normal Mode | - | 50 | - | ppm/ mA |
| $T_{coeff}$ | Temperature coefficient | −40 °C < $T_J$ < +125 °C | | - | - | $T_{coeff}$ $V_{REFINT}$ + 100 | ppm/ °C |
| PSRR | Power supply rejection | DC | - | - | 60 | - | dB |
| | | 100KHz | - | - | 40 | - | |

**Table 103. VREFBUF characteristics(1) (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{START}$ | Start-up time | $C_L$=0.5 µF | - | - | 300 | - | µs |
| | | $C_L$=1 µF | - | - | 500 | - | |
| | | $C_L$=1.5 µF | - | - | 650 | - | |
| $I_{INRUSH}$ | Control of maximum DC current drive on $V_{REFBUF_OUT}$ during startup phase(3) | - | | - | 8 | - | mA |
| $I_{DDA(VREFBUF)}$ | VREFBUF consumption from $V_{DDA}$ | $I_{LOAD}$ = 0 µA | - | - | 15 | 25 | µA |
| | | $I_{LOAD}$ = 500 µA | - | - | 16 | 30 | |
| | | $I_{LOAD}$ = 4 mA | - | - | 32 | 50 | |

1. Guaranteed by design.
2. In degraded mode, the voltage reference buffer cannot accurately maintain the output voltage ($V_{DDA}$−drop voltage).
3. To properly control VREFBUF $I_{INRUSH}$ current during the startup phase and the change of scaling, $V_{DDA}$ voltage should be in the range of 1.8 V-3.6 V, 2.1 V-3.6 V, 2.4 V-3.6 V and 2.8 V-3.6 V for VSCALE = 011, 010, 001 and 000, respectively.

## 6.3.26 Temperature sensor characteristics

**Table 104. Temperature sensor characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_L$(1) | $V_{SENSE}$ linearity with temperature | - | - | 3 | °C |
| Avg_Slope(2) | Average slope | - | 2 | - | mV/°C |
| $V_{30}$(3) | Voltage at 30°C ± 5 °C | - | 0.62 | - | V |
| $t_{start_run}$ | Startup time in Run mode (buffer startup) | - | - | 25.2 | µs |
| $t_{S_temp}$(1) | ADC sampling time when reading the temperature | 9 | - | - | |
| $I_{sens}$(1) | Sensor consumption | - | 0.18 | 0.31 | µA |
| $I_{sensbuf}$(1) | Sensor buffer consumption | - | 3.8 | 6.5 | |

1. Guaranteed by design.
2. Guaranteed by characterization.
3. Measured at $V_{DDA}$ = 3.3 V ± 10 mV. The $V_{30}$ ADC conversion result is stored in the TS_CAL1 byte.

**Table 105. Temperature sensor calibration values**

| Symbol | Parameter | Memory address |
|---|---|---|
| TS_CAL1 | Temperature sensor raw data acquired value at 30 °C, $V_{DDA}$=3.3 V | 0x1FF1 E820 -0x1FF1 E821 |
| TS_CAL2 | Temperature sensor raw data acquired value at 110 °C, $V_{DDA}$=3.3 V | 0x1FF1 E840 - 0x1FF1 E841 |

### 6.3.27 Temperature and $V_{BAT}$ monitoring

**Table 106. $V_{BAT}$ monitoring characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| R | Resistor bridge for $V_{BAT}$ | - | 26 | - | KΩ |
| Q | Ratio on $V_{BAT}$ measurement | - | 4 | - | - |
| Er(1) | Error on Q | –10 | - | +10 | % |
| $t_{S_vbat}$(1) | ADC sampling time when reading $V_{BAT}$ input | 9 | - | - | µs |
| $V_{BAThigh}$ | High supply monitoring | - | 3.55 | - | V |
| $V_{BATlow}$ | Low supply monitoring | - | 1.36 | - | |

1. Guaranteed by design.

**Table 107. $V_{BAT}$ charging characteristics**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $R_{BC}$ | Battery charging resistor | VBRS in PWR_CR3= 0 | - | 5 | - | KΩ |
| | | VBRS in PWR_CR3= 1 | | 1.5 | - | |

**Table 108. Temperature monitoring characteristics**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $TEMP_{high}$ | High temperature monitoring | - | 117 | - | °C |
| $TEMP_{low}$ | Low temperature monitoring | - | –25 | - | |

### 6.3.28 Voltage booster for analog switch

**Table 109. Voltage booster for analog switch characteristics(1)**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | - | 1.62 | 2.6 | 3.6 | V |
| $t_{SU(BOOST)}$ | Booster startup time | - | - | - | 50 | µs |
| $I_{DD(BOOST)}$ | Booster consumption | 1.62 V ≤ $V_{DD}$ ≤ 2.7 V | - | - | 125 | µA |
| | | 2.7 V < $V_{DD}$ < 3.6 V | - | - | 250 | |

1. Guaranteed by characterization results.

## 6.3.29 Comparator characteristics

**Table 110. COMP characteristics(1)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage | - | | 1.62 | 3.3 | 3.6 | V |
| $V_{IN}$ | Comparator input voltage range | - | | 0 | - | $V_{DDA}$ | |
| $V_{BG}$ | Scaler input voltage | - | | (2) | | | |
| $V_{SC}$ | Scaler offset voltage | - | | - | ±5 | ±10 | mV |
| $I_{DDA(SCALER)}$ | Scaler static consumption from $V_{DDA}$ | BRG_EN=0 (bridge disable) | | - | 0.2 | 0.3 | µA |
| | | BRG_EN=1 (bridge enable) | | - | 0.8 | 1 | |
| $t_{START_SCALER}$ | Scaler startup time | - | | - | 140 | 250 | µs |
| $t_{START}$ | Comparator startup time to reach propagation delay specification | High-speed mode | | - | 2 | 5 | µs |
| | | Medium mode | | - | 5 | 20 | |
| | | Ultra-low-power mode | | - | 15 | 80 | |
| $t_D$(3) | Propagation delay for 200 mV step with 100 mV overdrive | High-speed mode | | - | 50 | 80 | ns |
| | | Medium mode | | - | 0.5 | 1.2 | µs |
| | | Ultra-low-power mode | | - | 2.5 | 7 | |
| | Propagation delay for step > 200 mV with 100 mV overdrive only on positive inputs | High-speed mode | | - | 50 | 120 | ns |
| | | Medium mode | | - | 0.5 | 1.2 | µs |
| | | Ultra-low-power mode | | - | 2.5 | 7 | |
| $V_{offset}$ | Comparator offset error | Full common mode range | | - | ±5 | ±20 | mV |
| $V_{hys}$ | Comparator hysteresis | No hysteresis | | - | 0 | - | mV |
| | | Low hysteresis | | 5 | 10 | 22 | |
| | | Medium hysteresis | | 8 | 20 | 37 | |
| | | High hysteresis | | 16 | 30 | 52 | |
| $I_{DDA(COMP)}$ | Comparator consumption from $V_{DDA}$ | Ultra-low-power mode | Static | - | 400 | 600 | nA |
| | | | With 50 kHz ±100 mV overdrive square signal | - | 800 | - | |
| | | Medium mode | Static | - | 5 | 7 | µA |
| | | | With 50 kHz ±100 mV overdrive square signal | - | 6 | - | |
| | | High-speed mode | Static | - | 70 | 100 | |
| | | | With 50 kHz ±100 mV overdrive square signal | - | 75 | - | |

1. Guaranteed by design, unless otherwise specified.
2. Refer to *Table 29: Embedded reference voltage*.

3. Guaranteed by characterization results.

## 6.3.30 Operational amplifier characteristics

**Table 111. Operational amplifier characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage Range | - | 2 | 3.3 | 3.6 | V |
| CMIR | Common Mode Input Range | - | 0 | - | $V_{DDA}$ | |
| $VI_{OFFSET}$ | Input offset voltage | 25°C, no load on output | - | - | ±1.5 | mV |
| | | All voltages and temperature, no load | - | - | ±2.5 | |
| $\Delta VI_{OFFSET}$ | Input offset voltage drift | - | - | ±3.0 | - | µV/°C |
| TRIMOFFSETP TRIMLPOFFSETP | Offset trim step at low common input voltage ($0.1*V_{DDA}$) | - | - | 1.1 | 1.5 | mV |
| TRIMOFFSETN TRIMLPOFFSETN | Offset trim step at high common input voltage ($0.9*V_{DDA}$) | - | - | 1.1 | 1.5 | |
| $I_{LOAD}$ | Drive current | - | - | - | 500 | µA |
| $I_{LOAD_PGA}$ | Drive current in PGA mode | - | - | - | 270 | |
| $C_{LOAD}$ | Capacitive load | - | - | - | 50 | pF |
| CMRR | Common mode rejection ratio | - | - | 80 | - | dB |
| PSRR | Power supply rejection ratio | $C_{LOAD} \le 50pf$ / $R_{LOAD} \ge 4\ k\Omega$ (1) at 1 kHz, $V_{com}=V_{DDA}/2$ | 50 | 66 | - | dB |
| GBW | Gain bandwidth for high supply range | 200 mV ≤ Output dynamic range ≤ $V_{DDA}$ - 200 mV | 4 | 7.3 | 12.3 | MHz |
| SR | Slew rate (from 10% and 90% of output voltage) | Normal mode | - | 3 | - | V/µs |
| | | High-speed mode | - | 30 | - | |
| AO | Open loop gain | 200 mV ≤ Output dynamic range ≤ $V_{DDA}$ - 200 mV | 59 | 90 | 129 | dB |
| φm | Phase margin | - | - | 55 | - | ° |
| GM | Gain margin | - | - | 12 | - | dB |
| $V_{OHSAT}$ | High saturation voltage | $I_{load}$=max or $R_{LOAD}$=min, Input at $V_{DDA}$ | $V_{DDA}$ −100 mV | - | - | mV |
| $V_{OLSAT}$ | Low saturation voltage | $I_{load}$=max or $R_{LOAD}$=min, Input at 0 V | - | - | 100 | |

**Table 111. Operational amplifier characteristics (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{WAKEUP}$ | Wake up time from OFF state | Normal mode | $C_{LOAD}$ ≤ 50pf, $R_{LOAD}$ ≥ 4 kΩ, follower configuration | - | 0.8 | 3.2 | µs |
| | | High speed mode | $C_{LOAD}$ ≤ 50pf, $R_{LOAD}$ ≥ 4 kΩ, follower configuration | - | 0.9 | 2.8 | |
| PGA gain | Non inverting gain error value | PGA gain = 2 | | −1 | - | 1 | % |
| | | PGA gain = 4 | | −2 | - | 2 | |
| | | PGA gain = 8 | | −2.5 | - | 2.5 | |
| | | PGA gain = 16 | | −3 | - | 3 | |
| | Inverting gain error value | PGA gain = 2 | | −1 | - | 1 | |
| | | PGA gain = 4 | | −1 | - | 1 | |
| | | PGA gain = 8 | | −2 | - | 2 | |
| | | PGA gain = 16 | | −3 | - | 3 | |
| | External non-inverting gain error value | PGA gain = 2 | | −1 | - | 1 | |
| | | PGA gain = 4 | | −3 | - | 3 | |
| | | PGA gain = 8 | | −3.5 | - | 3.5 | |
| | | PGA gain = 16 | | −4 | - | 4 | |
| $R_{network}$ | R2/R1 internal resistance values in non-inverting PGA mode(2) | PGA Gain=2 | | - | 10/10 | - | kΩ/ kΩ |
| | | PGA Gain=4 | | - | 30/10 | - | |
| | | PGA Gain=8 | | - | 70/10 | - | |
| | | PGA Gain=16 | | - | 150/10 | - | |
| | R2/R1 internal resistance values in inverting PGA mode(2) | PGA Gain = -1 | | - | 10/10 | - | |
| | | PGA Gain = -3 | | - | 30/10 | - | |
| | | PGA Gain = -7 | | - | 70/10 | - | |
| | | PGA Gain = -15 | | - | 150/10 | - | |
| Delta R | Resistance variation (R1 or R2) | - | | −15 | - | 15 | % |

**Table 111. Operational amplifier characteristics (continued)**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| PGA BW | PGA bandwidth for different non inverting gain | Gain=2 | | - | GBW/2 | - | MHz |
| | | Gain=4 | | - | GBW/4 | - | |
| | | Gain=8 | | - | GBW/8 | - | |
| | | Gain=16 | | - | GBW/16 | - | |
| | PGA bandwidth for different inverting gain | Gain = -1 | | - | 5.00 | - | MHz |
| | | Gain = -3 | | - | 3.00 | - | |
| | | Gain = -7 | | - | 1.50 | - | |
| | | Gain = -15 | | - | 0.80 | - | |
| en | Voltage noise density | at 1 KHz | output loaded with 4 kΩ | - | 140 | - | nV/√Hz |
| | | at 10 KHz | | - | 55 | - | |
| $I_{DDA(OPAMP)}$ | OPAMP consumption from $V_{DDA}$ | Normal mode | no Load, quiescent mode, follower | - | 570 | 1000 | µA |
| | | High-speed mode | | - | 610 | 1200 | |

1. $R_{LOAD}$ is the resistive load connected to VSSA or to VDDA.
2. R2 is the internal resistance between the OPAMP output and th OPAMP inverting input. R1 is the internal resistance between the OPAMP inverting input and ground. PGA gain = 1 + R2/R1.

### 6.3.31 Digital filter for Sigma-Delta Modulators (DFSDM) characteristics

Unless otherwise specified, the parameters given in *Table 112* for DFSDM are derived from tests performed under the ambient temperature, fPCLKx frequency and supply voltage conditions summarized in *Table 22: General operating conditions*.

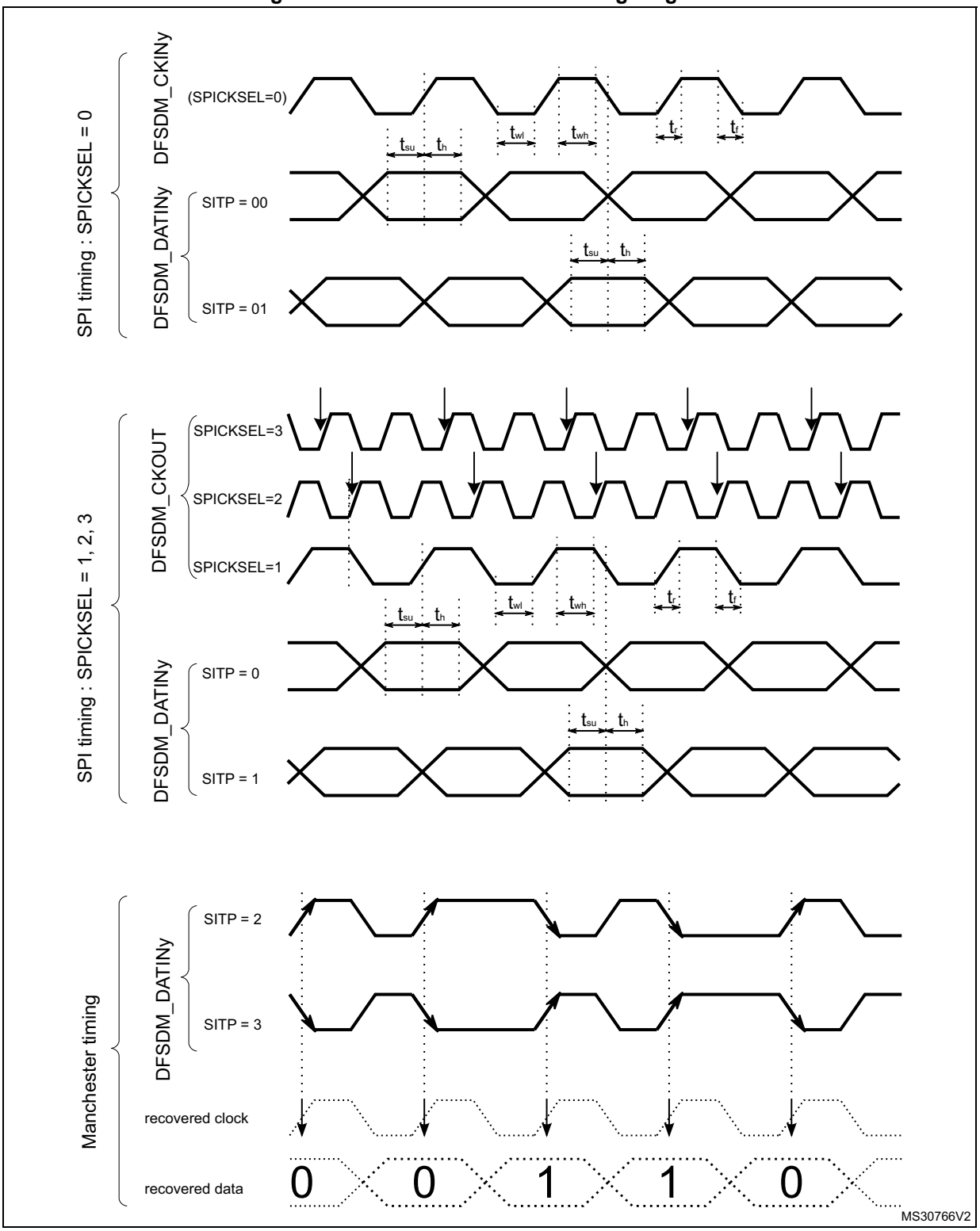
- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load $C_L$ = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS1

Refer to *Section 6.3.18: I/O port characteristics* for more details on the input/output alternate function characteristics (DiFSDM_CKINx, DFSDM_DATINx, DFSDM_CKOUT for DFSDM).

**Table 112. DFSDM measured timing 1.62-3.6 V**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{DFSDMCLK}$ | DFSDM clock | 1.62 < $V_{DD}$ < 3.6 V | - | - | 133 | MHz |
| $f_{CKIN}$ ($1/T_{CKIN}$) | Input clock frequency | SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < $V_{DD}$ < 3.6 V | - | - | 20 | |
| | | SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 2.7 < $V_{DD}$ < 3.6 V | - | - | 20 | |
| | | SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]¹0), 1.62 < $V_{DD}$ < 3.6 V | - | - | 20 | |
| | | SPI mode (SITP[1:0]=0,1), Internal clock mode (SPICKSEL[1:0]¹0), 2.7 < $V_{DD}$ < 3.6 V | - | - | 20 | |
| $f_{CKOUT}$ | Output clock frequency | 1.62 < $V_{DD}$ < 3.6 V | - | - | 20 | |
| $DuCy_{CKOUT}$ | Output clock frequency duty cycle | 1.62 < $V_{DD}$ < 3.6 V | 45 | 50 | 55 | % |
| $t_{wh(CKIN)}$ $t_{wl(CKIN)}$ | Input clock high and low time | SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < $V_{DD}$ < 3.6 V | $T_{CKIN}$/2-0.5 | $T_{CKIN}$/2 | - | ns |
| $t_{su}$ | Data input setup time | SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < $V_{DD}$ < 3.6 V | 1.5 | - | - | |
| $t_h$ | Data input hold time | SPI mode (SITP[1:0]=0,1), External clock mode (SPICKSEL[1:0]=0), 1.62 < $V_{DD}$ < 3.6 V | 0.5 | - | - | |
| $T_{Manchester}$ | Manchester data period (recovered clock period) | Manchester mode (SITP[1:0]=2,3), Internal clock mode (SPICKSEL[1:0]¹0), 1.62 < $V_{DD}$ < 3.6 V | (CKOUTDIV+1) * $T_{DFSDMCLK}$ | - | (2*CKOUTDIV) * $T_{DFSDMCLK}$ | |

**Figure 49. Channel transceiver timing diagrams**



### 6.3.32 Camera interface (DCMI) timing specifications

Unless otherwise specified, the parameters given in *Table 113* for DCMI are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and VDD supply voltage summarized in *Table 22: General operating conditions*, with the following configuration:

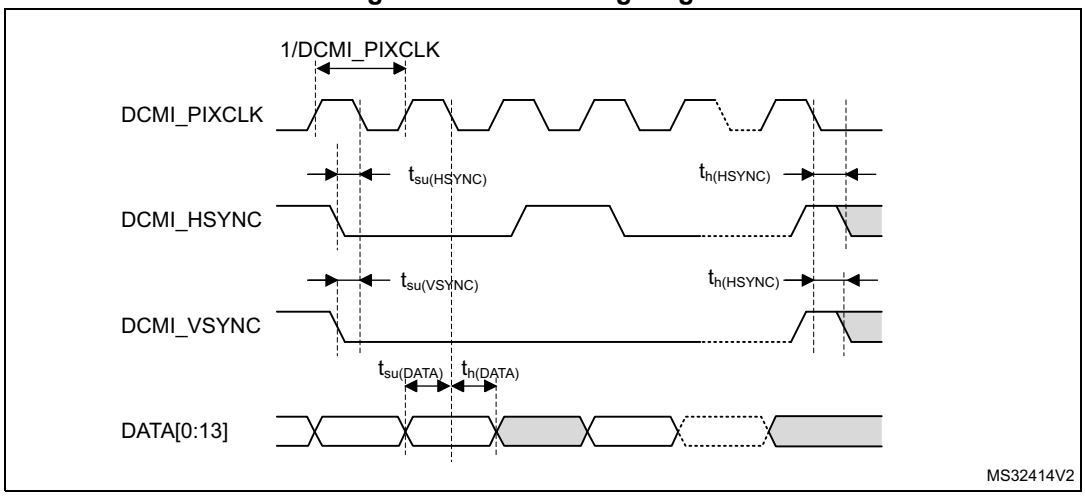
- DCMI_PIXCLK polarity: falling
- DCMI_VSYNC and DCMI_HSYNC polarity: high
- Data formats: 14 bits
- Capacitive load $C_L$=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS1

**Table 113. DCMI characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| - | Frequency ratio DCMI_PIXCLK/$f_{HCLK}$ | - | 0.4 | - |
| DCMI_PIXCLK | Pixel Clock input | - | 80 | MHz |
| $D_{pixel}$ | Pixel Clock input duty cycle | 30 | 70 | % |
| $t_{su(}$DATA) | Data input setup time | 3 | - | - |
| $t_h$(DATA) | Data hold time | 1 | - | |
| tsu(HSYNC), tsu(VSYNC) | DCMI_HSYNC/ DCMI_VSYNC input setup time | 2 | - | ns |
| th(HSYNC), th(VSYNC) | DCMI_HSYNC/ DCMI_VSYNC input hold time | 1 | - | - |

1. Guaranteed by characterization results.

**Figure 50. DCMI timing diagram**



### 6.3.33 LCD-TFT controller (LTDC) characteristics

Unless otherwise specified, the parameters given in *Table 114* for LCD-TFT are derived from tests performed under the ambient temperature, $f_{HCLK}$ frequency and VDD supply voltage summarized in *Table 22: General operating conditions*, with the following configuration:

- LCD_CLK polarity: high
- LCD_DE polarity: low
- LCD_VSYNC and LCD_HSYNC polarity: high
- Pixel formats: 24 bits
- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load $C_L$=30 pF
- Measurement points are done at CMOS levels: 0.5VDD
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1

**Table 114. LTDC characteristics(1)**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{CLK}$ | LTDC clock output frequency | 2.7<$V_{DD}$<3.6 V 20pF | - | 150 | MHz |
| | | 2.7<$V_{DD}$<3.6 V | | 133 | |
| | | 1.62<$V_{DD}$<3.6 V | | 90 | |
| $D_{CLK}$ | LTDC clock output duty cycle | | 45 | 55 | % |
| $t_{w(CLKH)}$, $t_{w(CLKL)}$ | Clock High time, low time | | $t_{w(CLK)}$//2-0.5 | $t_{w(CLK)}$//2+0.5 | - |
| $t_{v(DATA)}$ | Data output valid time | 2.7<$V_{DD}$<3.6 V | - | 0.5 | |
| $t_{h(DATA)}$ | | 1.62<$V_{DD}$<3.6 V | | 5 | |
| $t_{v(DATA)}$ | Data output hold time | | 0 | - | |
| $t_{v(HSYNC)}$, $t_{v(VSYNC)}$, $t_{v(DE)}$ | HSYNC/VSYNC/DE output valid time | 2.7<$V_{DD}$<3.6 V | - | 0.5 | |
| | | 1.62<$V_{DD}$<3.6 V | - | 5 | |
| $t_{h(HSYNC)}$, $t_{h(VSYNC)}$, $t_{h(DE)}$ | HSYNC/VSYNC/DE output hold time | | 0 | - | |

1. Guaranteed by characterization results.

**Figure 51. LCD-TFT horizontal timing diagram**

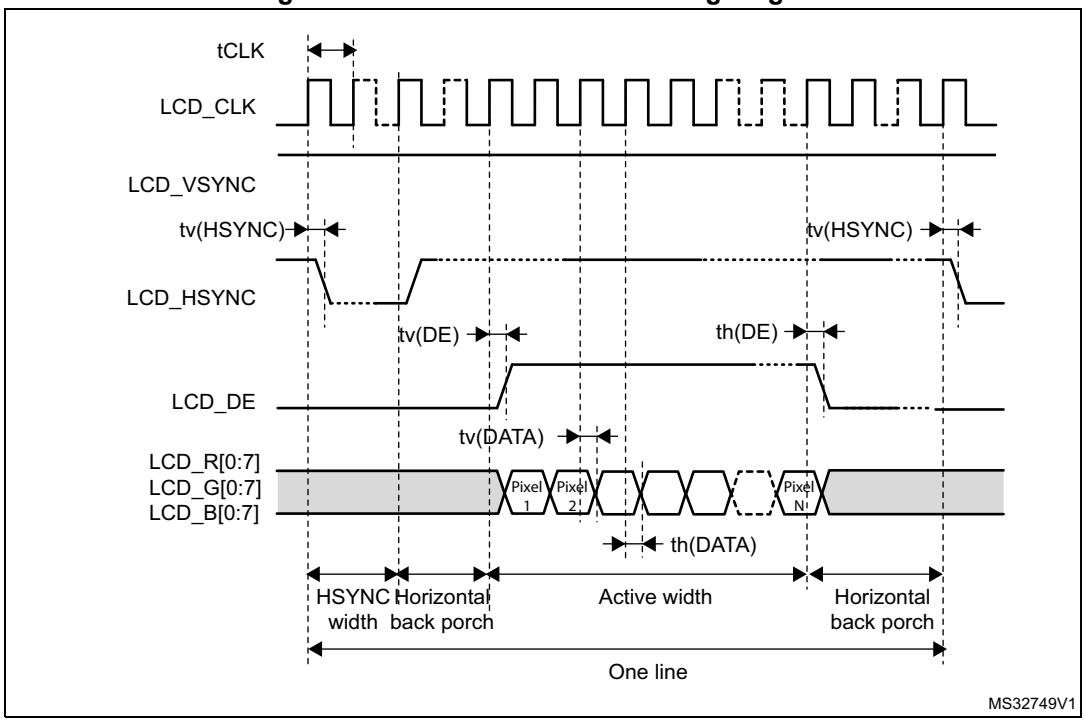
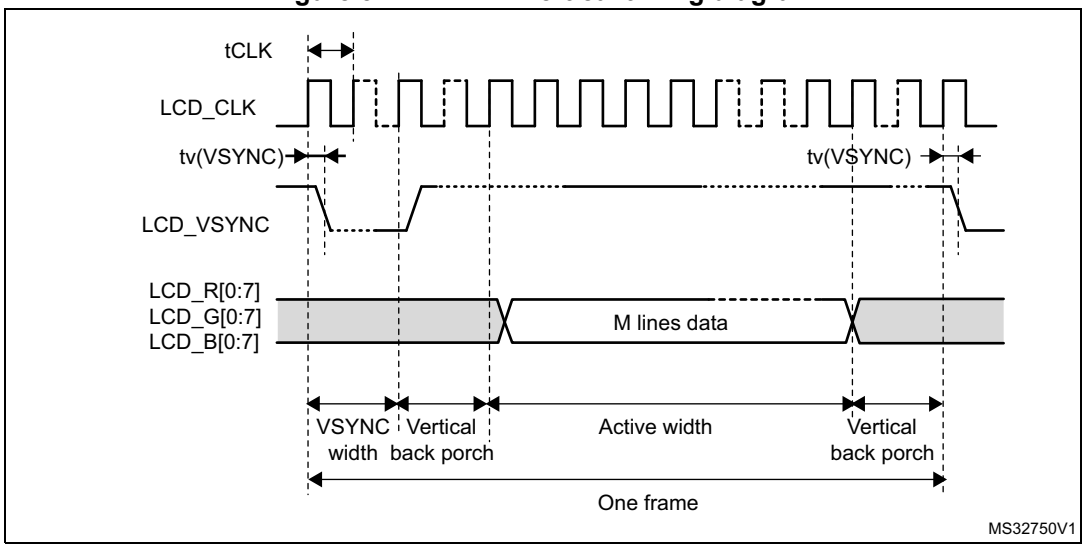



**Figure 52. LCD-TFT vertical timing diagram**



### 6.3.34 Timer characteristics

The parameters given in *Table 115* are guaranteed by design.

Refer to *Section 6.3.18: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

**Table 115. TIMx characteristics(1)(2)**

| Symbol | Parameter | Conditions(3) | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer resolution time | AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 240 MHz | 1 | - | $t_{TIMxCLK}$ |
| | | AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 120 MHz | 1 | - | $t_{TIMxCLK}$ |
| $f_{EXT}$ | Timer external clock frequency on CH1 to CH4 | $f_{TIMxCLK}$ = 240 MHz | 0 | $f_{TIMxCLK}/2$ | MHz |
| $Res_{TIM}$ | Timer resolution | | - | 16/32 | bit |
| $t_{MAX_COUNT}$ | Maximum possible count with 32-bit counter | - | - | 65536 × 65536 | $t_{TIMxCLK}$ |

1. TIMx is used as a general term to refer to the TIM1 to TIM17 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 or APB2 is up to 240 MHz, by setting the TIMPRE bit in the RCC_CFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = rcc_hclk1, otherwise TIMxCLK = 4x $F_{rcc_pclkx_d2}$.

### 6.3.35 Communication interfaces

#### I²C interface characteristics

The I²C interface meets the timings requirements of the I2C-bus specification and user manual revision 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I²C timings requirements are guaranteed by design when the I²C peripheral is properly configured (refer to RM0399 reference manual) and when the i2c_ker_ck frequency is greater than the minimum shown in the table below:

**Table 116. Minimum i2c_ker_ck frequency in all I²C modes**

| Symbol | Parameter | Condition | | Min | Unit |
|---|---|---|---|---|---|
| f(I2CCLK) | I2CCLK frequency | Standard-mode | - | 2 | MHz |
| | | Fast-mode | Analog Filtre ON DNF=0 | 8 | |
| | | | Analog Filtre OFF DNF=1 | 9 | |
| | | Fast-mode Plus | Analog Filtre ON DNF=0 | 17 | |
| | | | Analog Filtre OFF DNF=1 | 16 | - |

The SDA and SCL I/O requirements are met with the following restrictions:

- The SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DDIOx}$ is disabled, but still present.
- The 20 mA output drive requirement in Fast-mode Plus is not supported. This limits the maximum load $C_{Load}$ supported in Fm+, which is given by these formulas:

  $t_{r(SDA/SCL)}=0.8473xR_PxC_{Load}$

  $R_{P(min)}= (V_{DD}-V_{OL(max)})/I_{OL(max)}$

  Where $R_P$ is the I2C lines pull-up. Refer to *Section 6.3.18: I/O port characteristics* for the I²C I/Os characteristics.

All I²C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

**Table 117. I²C analog filter characteristics(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{AF}$ | Maximum pulse width of spikes that are suppressed by analog filter | 50(2) | 80(3) | ns |

1. Guaranteed by characterization results.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered.

### USART interface characteristics

Unless otherwise specified, the parameters given in *Table 118* for USART are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load $C_L$ = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- VOS level set to VOS1

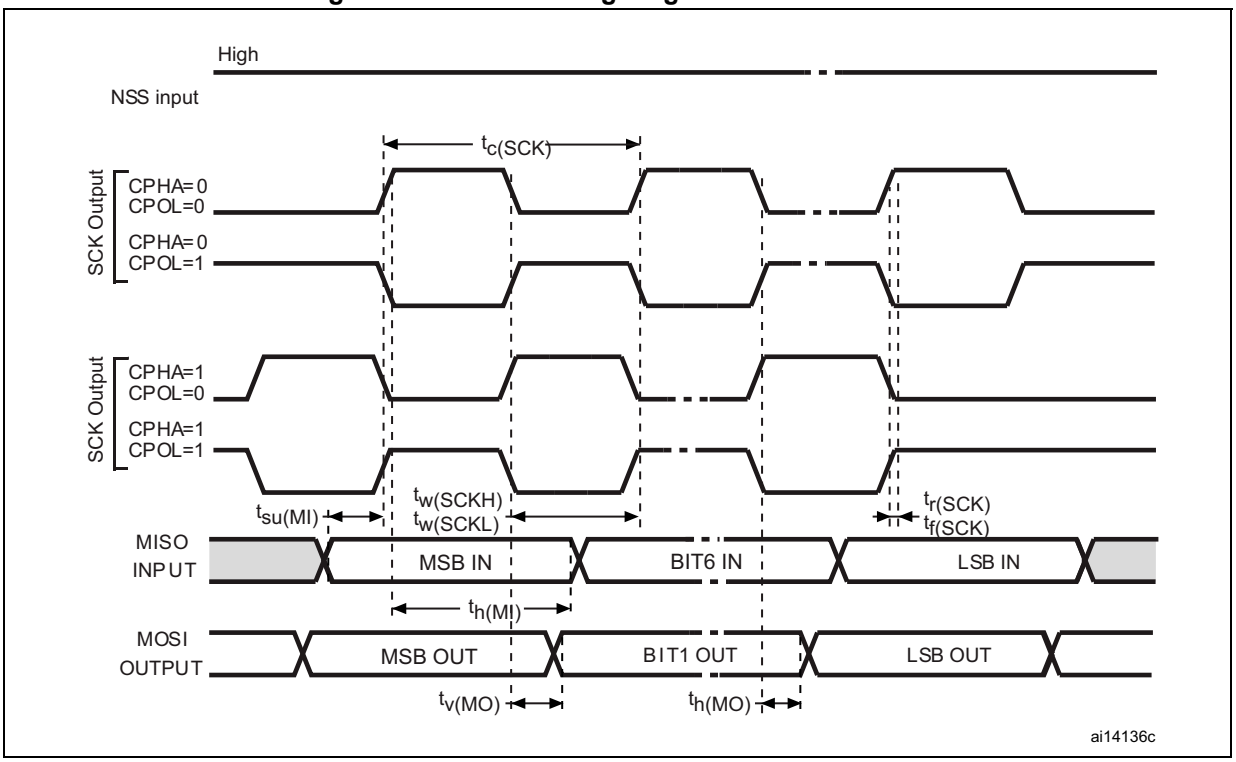
Refer to *Section 6.3.18: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, CK, TX, RX for USART).

**Table 118. USART characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{CK}$ | USART clock frequency | Master mode | - | - | 12.5 | MHz |
| | | Slave mode | | | 25 | |
| $t_{su(NSS)}$ | NSS setup time | Slave mode | $t_{ker}$+1 | - | - | - |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | 2 | - | - | |
| $t_{w(SCKH)}$, $t_{w(SCKL)}$ | CK high and low time | Master mode | $1/f_{CK}/2-2$ | $1/f_{CK}/2$ | $1/f_{CK}/2+2$ | |
| $t_{su(RX)}$ | Data input setup time | Master mode | $t_{ker}$+6 | - | - | ns |
| | | Slave mode | 1.5 | - | - | |
| $t_{h(RX)}$ | Data input hold time | Master mode | 0 | - | - | |
| | | Slave mode | 1.5 | - | - | |
| $t_{v(TX)}$ | Data output valid time | Slave mode | - | 12 | 20 | |
| | | Master mode | - | 0.5 | 1 | |
| $t_{h(TX)}$ | Data output hold time | Slave mode | 9 | - | - | |
| | | Master mode | 0 | - | - | |

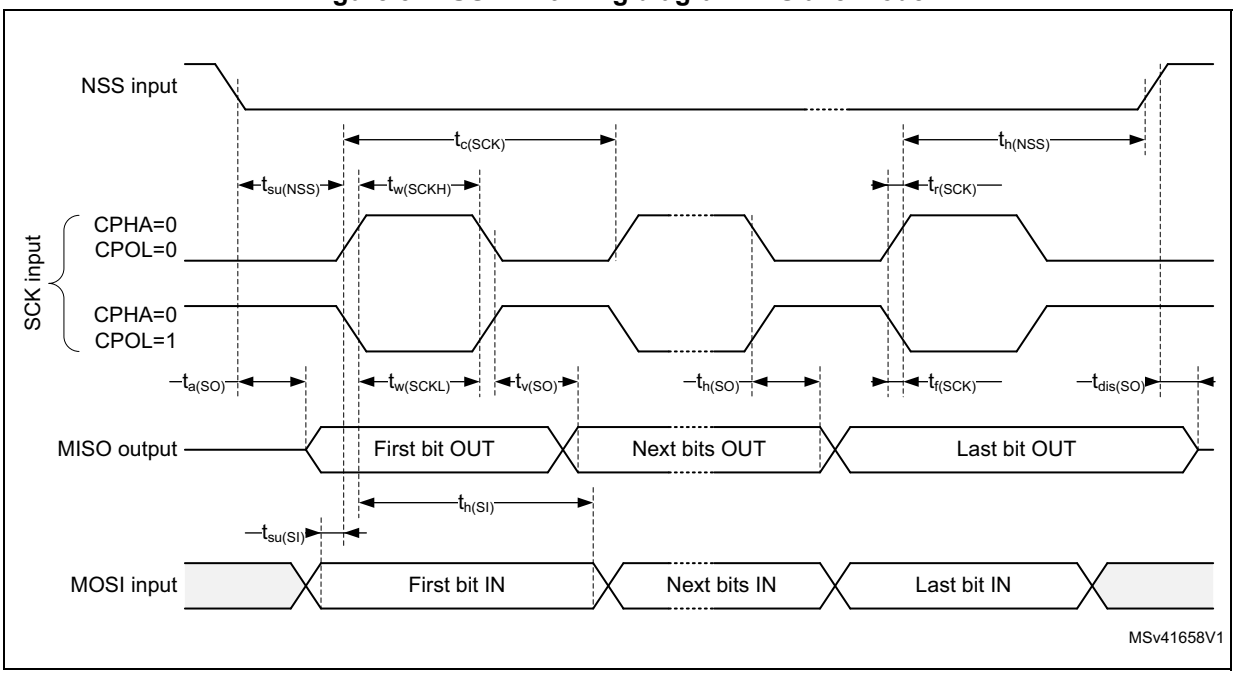
1. Guaranteed by characterization results.

**Figure 53. USART timing diagram in Master mode**




1. Measurement points are done at $0.5V_{DD}$ and with external $C_L$ = 30 pF.

**Figure 54. USART timing diagram in Slave mode**



### SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 119* for SPI are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load $C_L$ = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS1

Refer to *Section 6.3.18: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

**Table 119. SPI characteristics(1)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{SCK}$ | SPI clock frequency | Master mode<br>1.62<$V_{DD}$<3.6 V<br>SPI1, 2, 3 | - | - | 80 | MHz |
| | | Master mode<br>2.7<$V_{DD}$<3.6 V<br>SPI1, 2, 3 | | | 100 | |
| | | Master mode<br>1.62<$V_{DD}$<3.6 V<br>SPI4, 5, 6 | | | 50 | |
| | | Slave receiver mode<br>1.62<$V_{DD}$<3.6 V | | | 100 | |
| | | Slave mode transmitter/full duplex<br>2.7<$V_{DD}$<3.6 V | | | 31 | |
| | | Slave mode transmitter/full duplex<br>1.62 <$V_{DD}$<3.6 V | | | 29 | |
| $t_{su(NSS)}$ | NSS setup time | Slave mode | 2 | - | - | - |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | 1 | - | - | |
| $t_{w(SCKH)}$, $t_{w(SCKL)}$ | SCK high and low time | Master mode | $T_{PCLK}$-2 | $T_{PCLK}$ | $T_{PCLK}$+2 | |

**Table 119. SPI characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{su(MI)}$ | Data input setup time | Master mode | 1 | - | - | ns |
| $t_{su(SI)}$ | | Slave mode | 1 | - | - | |
| $t_{h(MI)}$ | Data input hold time | Master mode | 4 | - | - | |
| $t_{h(SI)}$ | | Slave mode | 2 | - | - | |
| $t_{a(SO)}$ | Data output access time | Slave mode | 9 | 13 | 27 | |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 0 | 1 | 5 | |
| $t_{v(SO)}$ | Data output valid time | Slave mode $2.7<V_{DD}<3.6$ V | - | 12.5 | 16 | |
| | | Slave mode $1.62<V_{DD}<3.6$ V | - | 12.5 | 17 | |
| $t_{v(MO)}$ | | Master mode | - | 1 | 3 | |
| $t_{h(SO)}$ | Data output hold time | Slave mode $1.62<V_{DD}<3.6$ V | 10 | - | - | |
| $t_{h(MO)}$ | | Master mode | 0 | - | - | |

1. Guaranteed by characterization results.

**Figure 55. SPI timing diagram - slave mode and CPHA = 0**

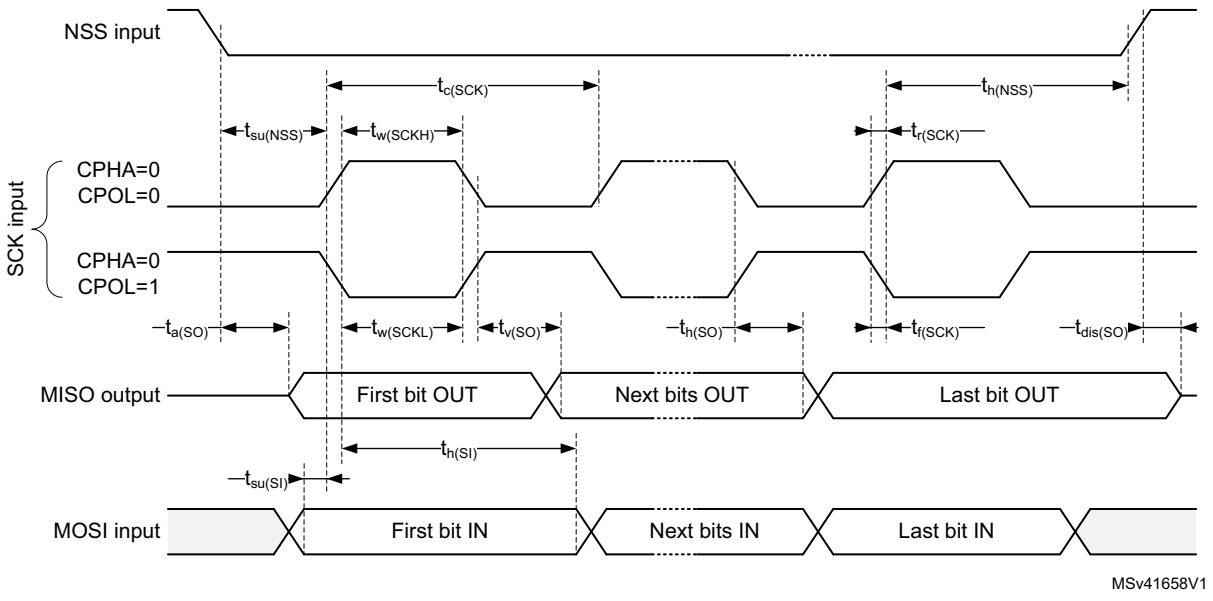
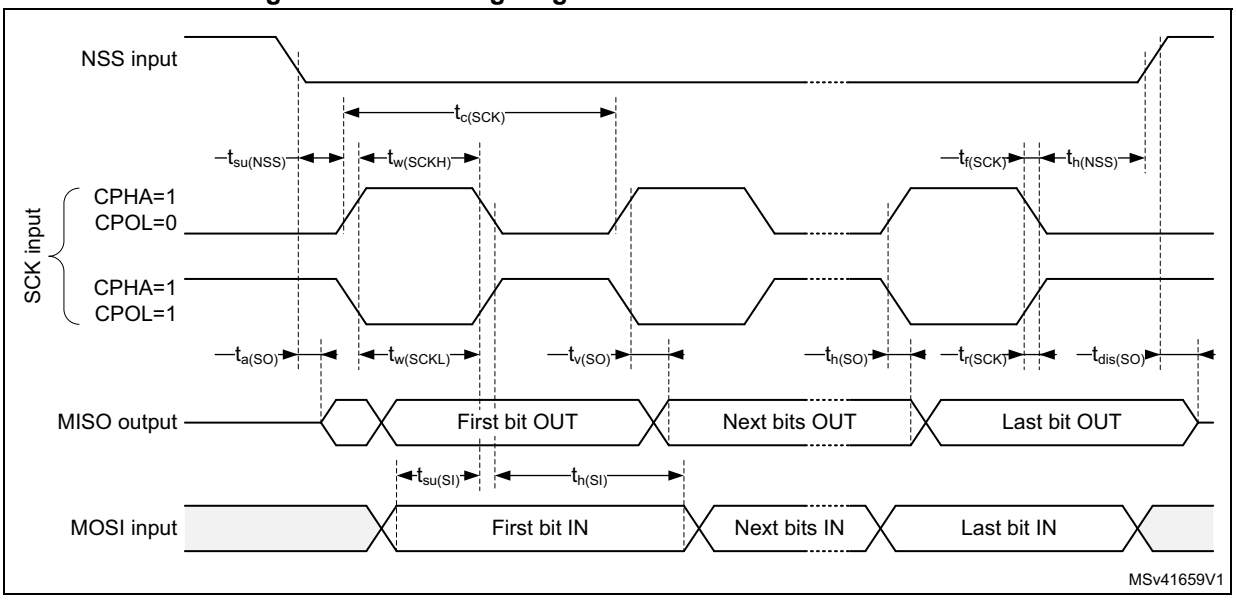
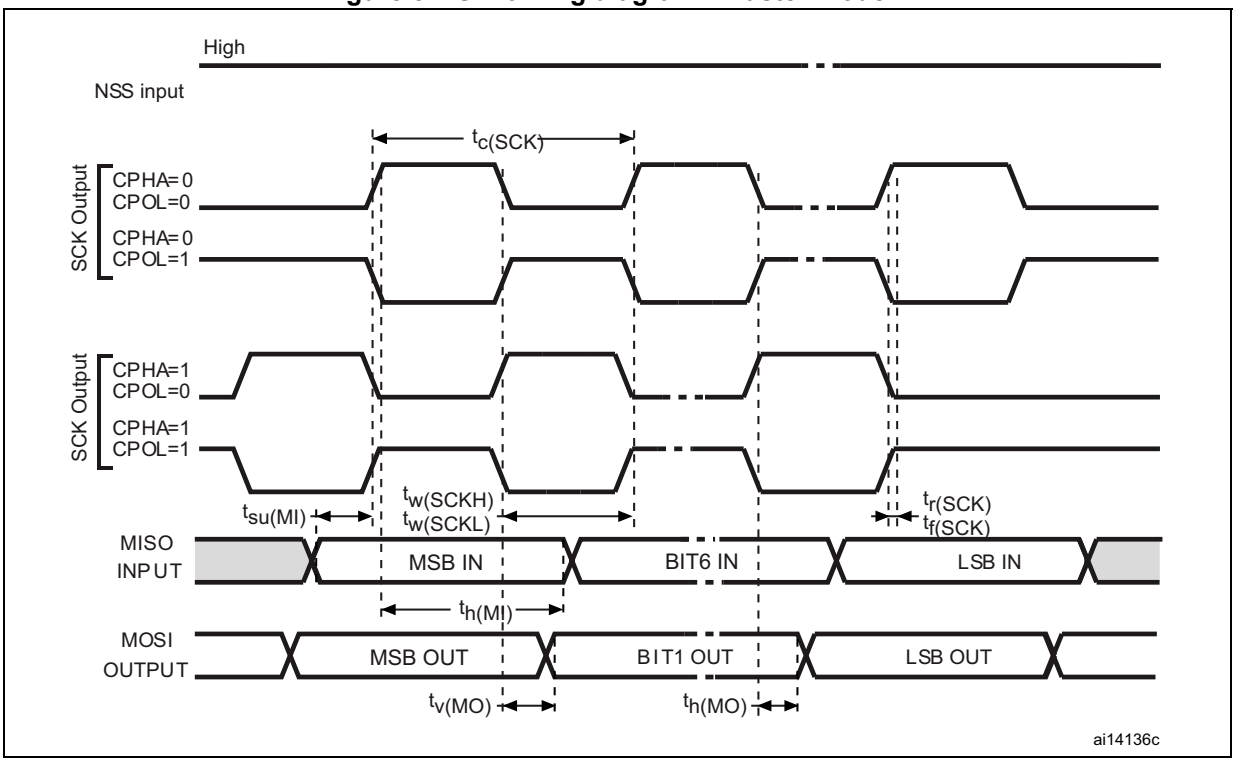


**Figure 56. SPI timing diagram - slave mode and CPHA = 1(1)**




1. Measurement points are done at $0.5V_{DD}$ and with external $C_L$ = 30 pF.

**Figure 57. SPI timing diagram - master mode(1)**




1. Measurement points are done at $0.5V_{DD}$ and with external $C_L$ = 30 pF.

### I²S Interface characteristics

Unless otherwise specified, the parameters given in *Table 120* for I²S are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load $C_L$ = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS1

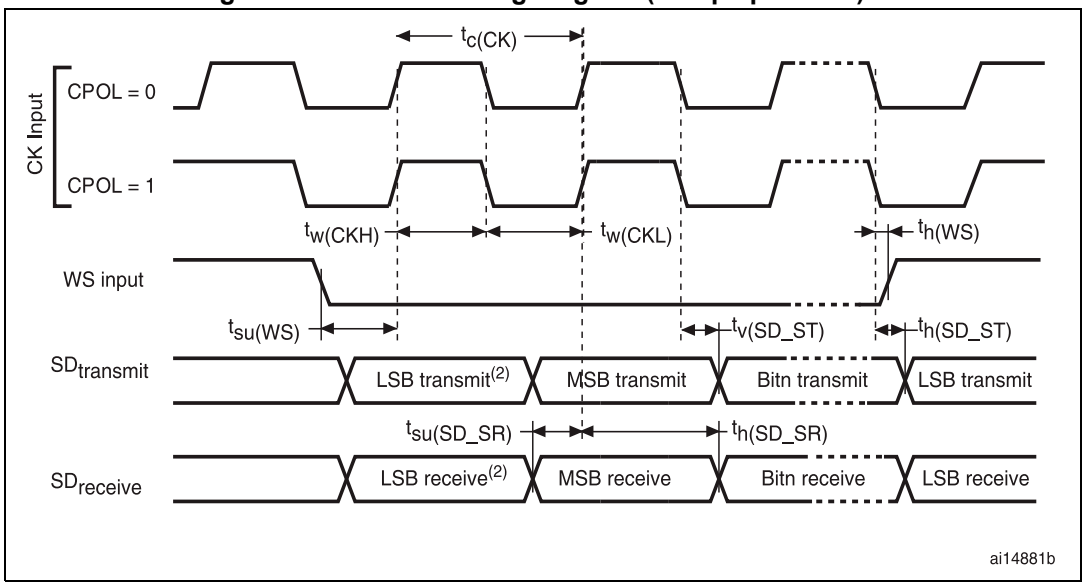
Refer to *Section 6.3.18: I/O port characteristics* for more details on the input/output alternate function characteristics (CK,SD,WS).

**Table 120. I²S dynamic characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCK}$ | I²S main clock output | - | 256x8K | $256F_S$ | MHz |
| $f_{CK}$ | I²S clock frequency | Master data | - | $64F_S$ | MHz |
| | | Slave data | - | $64F_S$ | |
| $t_{v(WS)}$ | WS valid time | Master mode | - | 3 | ns |
| $t_{h(WS)}$ | WS hold time | Master mode | 0 | - | |
| $t_{su(WS)}$ | WS setup time | Slave mode | 1 | - | |
| $t_{h(WS)}$ | WS hold time | Slave mode | 1 | - | |
| $t_{su(SD_MR)}$ | Data input setup time | Master receiver | 1 | - | |
| $t_{su(SD_SR)}$ | | Slave receiver | 1 | - | |
| $t_{h(SD_MR)}$ | Data input hold time | Master receiver | 4 | - | |
| $t_{h(SD_SR)}$ | | Slave receiver | 2 | - | |
| $t_{v(SD_ST)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 17 | |
| $t_{v(SD_MT)}$ | | Master transmitter (after enable edge) | - | 3 | |
| $t_{h(SD_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 9 | - | |
| $t_{h(SD_MT)}$ | | Master transmitter (after enable edge) | 0 | - | |

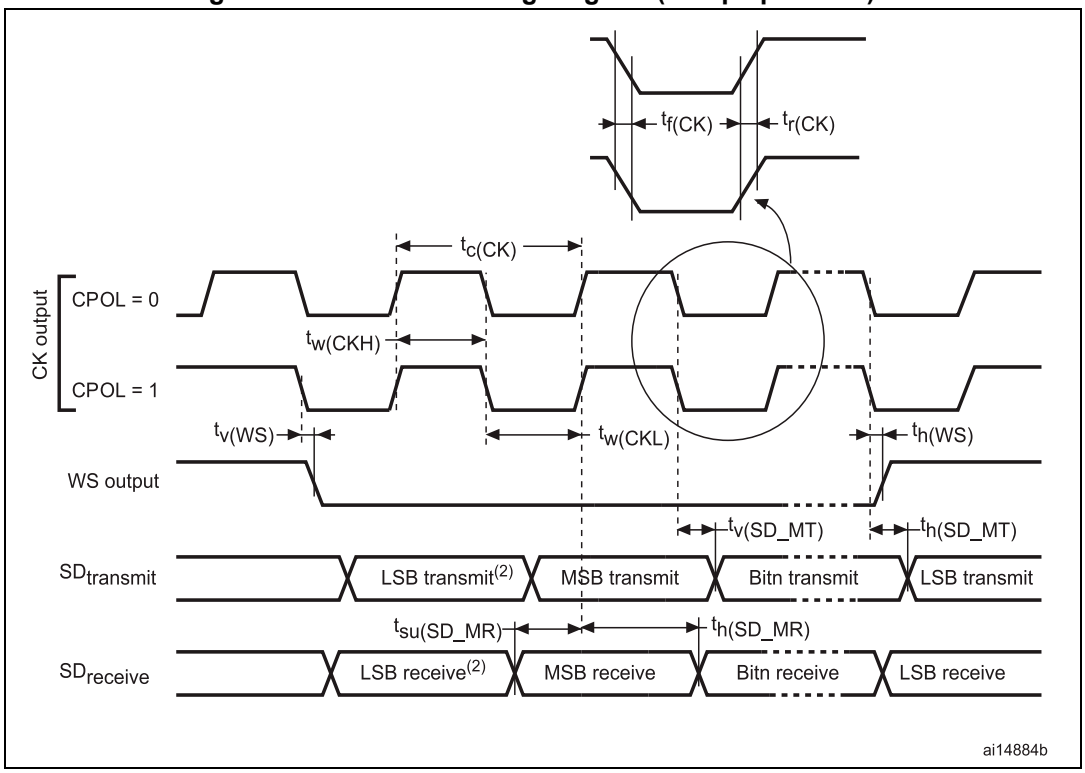
1. Guaranteed by characterization results.

**Figure 58. I²S slave timing diagram (Philips protocol)(1)**




1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 59. I²S master timing diagram (Philips protocol)(1)**




1. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

### SAI characteristics

Unless otherwise specified, the parameters given in *Table 121* for SAI are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and VDD supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load $C_L$ = 30 pF
- IO Compensation cell activated.
- Measurement points are done at CMOS levels: 0.5VDD
- VOS level set to VOS1.

Refer to *Section 6.3.18: I/O port characteristics* for more details on the input/output alternate function characteristics (SCK,SD,WS).

**Table 121. SAI characteristics(1)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{MCK}$ | SAI Main clock output | - | 256x8K | $256xF_S$ | MHz |
| $f_{CK}$ | SAI clock frequency(2) | Master Data: 32 bits | - | $128xF_S$(3) | |
| | | Slave Data: 32 bits | - | $128xF_S$(3) | |

**Table 121. SAI characteristics(1) (continued)**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $t_{v(FS)}$ | $F_S$ valid time | Master mode $2.7 \le V_{DD} \le 3.6$ | - | 13 | ns |
| | | Master mode $1.62 \le V_{DD} \le 3.6$ | - | 20 | |
| $t_{su(FS)}$ | $F_S$ hold time | Master mode | 8 | - | |
| $t_{h(FS)}$ | $F_S$ setup time | Slave mode | 1 | - | |
| | $F_S$ hold time | Slave mode | 1 | - | |
| $t_{su(SD_A_MR)}$ | Data input setup time | Master receiver | 0.5 | - | |
| $t_{su(SD_B_SR)}$ | | Slave receiver | 1 | - | |
| $t_{h(SD_A_MR)}$ | Data input hold time | Master receiver | 3.5 | - | |
| $t_{h(SD_B_SR)}$ | | Slave receiver | 2 | - | |
| $t_{v(SD_B_ST)}$ | Data output valid time | Slave transmitter (after enable edge) $2.7 \le V_{DD} \le 3.6$ | - | 14 | |
| | | Slave transmitter (after enable edge) $1.62 \le V_{DD} \le 3.6$ | - | 20 | |
| $t_{h(SD_B_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 9 | - | |
| $t_{v(SD_A_MT)}$ | Data output valid time | Master transmitter (after enable edge) $2.7 \le V_{DD} \le 3.6$ | - | 12 | |
| | | Master transmitter (after enable edge) $1.62 \le V_{DD} \le 3.6$ | - | 19 | |
| $t_{h(SD_A_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 7.5 | - | |

1. Guaranteed by characterization results.
2. APB clock frequency must be at least twice SAI clock frequency.
3. With $F_S$=192 kHz.

**Figure 60. SAI master timing waveforms**

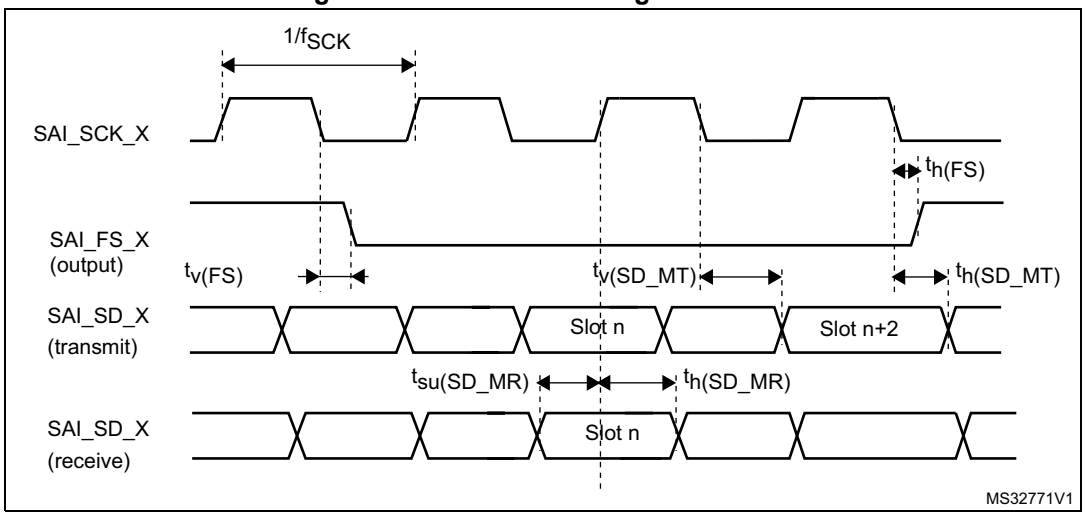
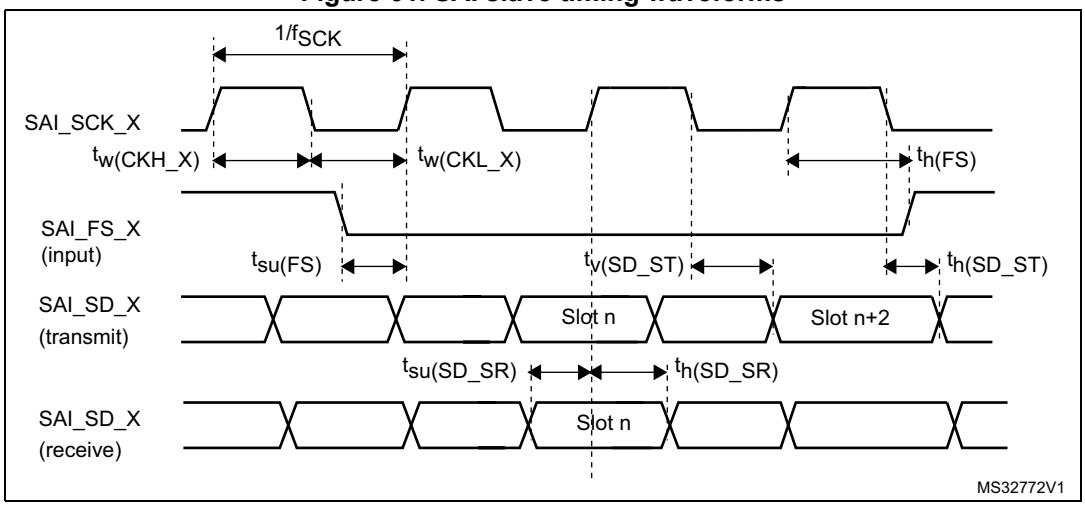



**Figure 61. SAI slave timing waveforms**

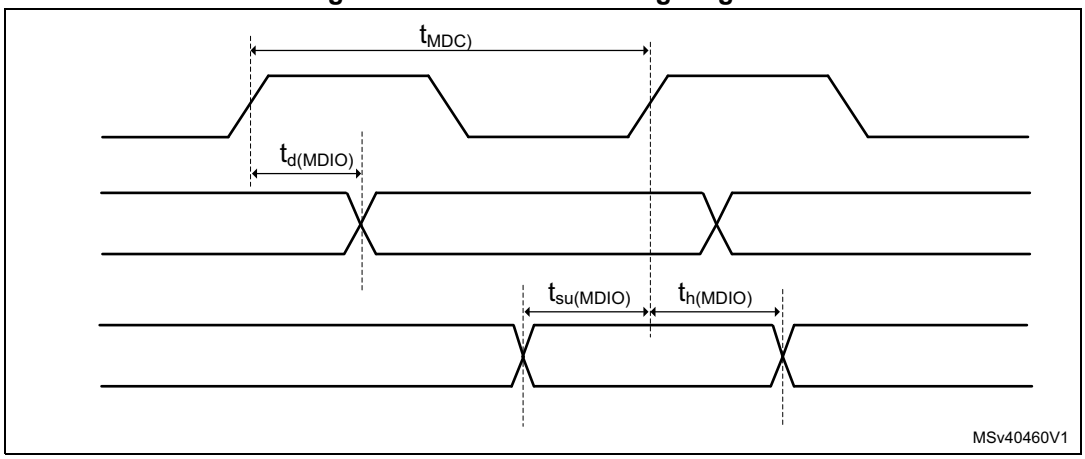



## MDIO characteristics

**Table 122. MDIO Slave timing parameters**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{MDC}$ | Management Data Clock | - | - | 30 | MHz |
| $t_{d(MDIO)}$ | Management Data Iput/output output valid time | 8 | 10 | 19 | ns |
| $t_{su(MDIO)}$ | Management Data Iput/output setup time | 1 | - | - | |
| $t_{h(MDIO)}$ | Management Data Iput/output hold time | 1 | - | - | |

**Figure 62. MDIO Slave timing diagram**




## SD/SDIO MMC card host interface (SDMMC) characteristics

Unless otherwise specified, the parameters given in *Table 123* and *Table 124* for SDIO are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and VDD supply voltage summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x11
- Capacitive load $C_L$=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when $V_{DD} \leq 2.7$ V
- VOS level set to VOS1

Refer to *Section 6.3.18: I/O port characteristics* for more details on the input/output characteristics.

**Table 123. Dynamics characteristics: SD / MMC characteristics, $V_{DD}$=2.7 to 3.6 V(1)(2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PP}$ | Clock frequency in data transfer mode | - | 0 | - | 133 | MHz |
| - | SDIO_CK/fPCLK2 frequency ratio | - | - | - | 8/3 | - |
| $t_{W(CKL)}$ | Clock low time | $f_{PP}$ =52MHz | 8.5 | 9.5 | - | ns |
| $t_{W(CKH)}$ | Clock high time | $f_{PP}$ =52MHz | 8.5 | 9.5 | - | |
| **CMD, D inputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR(3)/DDR(3) mode** | | | | | | |
| $t_{ISU}$ | Input setup time HS | - | 1.5 | - | - | ns |
| $t_{IH}$ | Input hold time HS | - | 1.5 | - | - | |
| $t_{IDW}$(4) | Input valid window (variable window) | - | 3 | - | - | - |
| **CMD, D outputs (referenced to CK) in eMMC legacy/SDR/DDR and SD HS/SDR/DDR(3) mode** | | | | | | |
| $t_{OV}$ | Output valid time HS | - | - | 3.5 | 5 | ns |
| $t_{OH}$ | Output hold time HS | - | 2 | - | - | |

**Table 123. Dynamics characteristics: SD / MMC characteristics, $V_{DD}$=2.7 to 3.6 V(1)(2) (continued)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **CMD, D inputs (referenced to CK) in SD default mode** | | | | | | |
| $t_{ISUD}$ | Input setup time SD | - | 1.5 | | - | ns |
| $t_{IHD}$ | Input hold time SD | - | 1.5 | | - | |
| **CMD, D outputs (referenced to CK) in SD default mode** | | | | | | |
| $t_{OVD}$ | Output valid default time SD | - | - | 0.5 | 2 | ns |
| $t_{OHD}$ | Output hold default time SD | - | 0 | - | - | |

1. Guaranteed by characterization results.
2. Above 100 MHz, $C_L$ = 20 pF.
3. An external voltage converter is required to support SD 1.8 V.
4. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

**Table 124. Dynamics characteristics: eMMC characteristics VDD=1.71V to 1.9V(1)(2)**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{PP}$ | Clock frequency in data transfer mode | - | 0 | - | 120 | MHz |
| - | SDIO_CK/fPCLK2 frequency ratio | - | - | - | 8/3 | - |
| $t_{W(CKL)}$ | Clock low time | $f_{PP}$ =52 MHz | 8.5 | 9.5 | - | ns |
| $t_{W(CKH)}$ | Clock high time | $f_{PP}$ =52 MHz | 8.5 | 9.5 | - | |
| **CMD, D inputs (referenced to CK) in eMMC mode** | | | | | | |
| $t_{ISU}$ | Input setup time HS | - | 1 | - | - | ns |
| $t_{IH}$ | Input hold time HS | - | 2.5 | - | - | |
| $t_{IDW}$(3) | Input valid window (variable window) | - | 3.5 | - | - | |
| **CMD, D outputs (referenced to CK) in eMMC mode** | | | | | | |
| $t_{OVD}$ | Output valid time HS | - | - | 5 | 7 | ns |
| $t_{OHD}$ | Output hold time HS | - | 3 | - | - | |

1. Guaranteed by characterization results.
2. $C_L$ = 20 pF.
3. The minimum window of time where the data needs to be stable for proper sampling in tuning mode.

**Figure 63. SDIO high-speed mode**

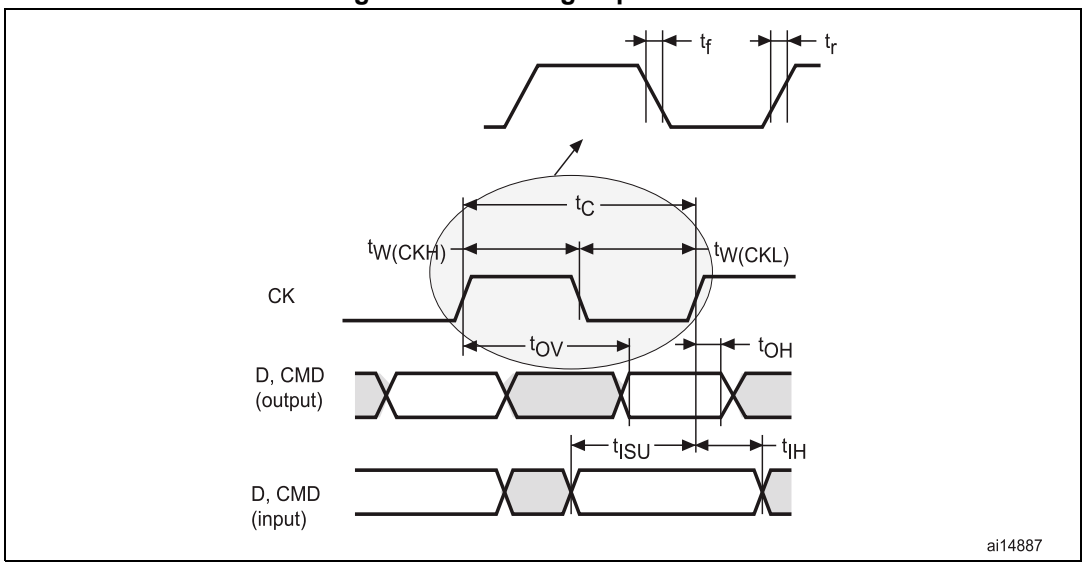



**Figure 64. SD default mode**

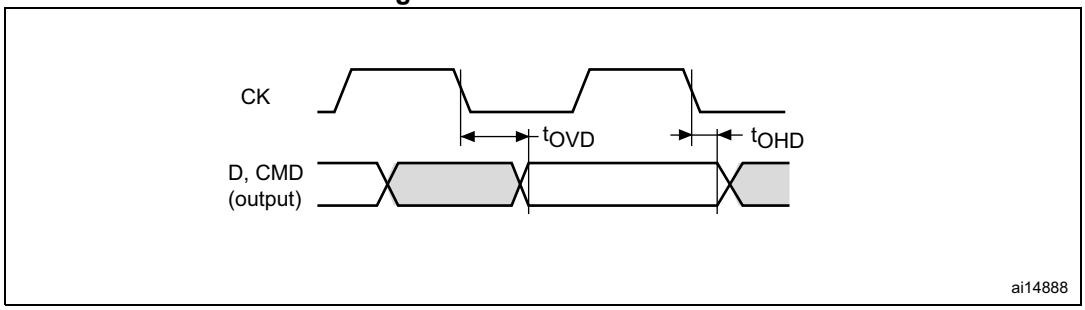
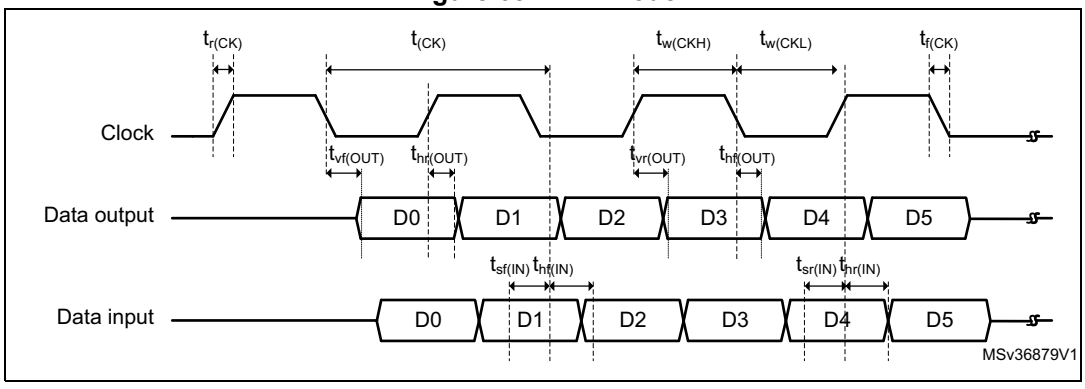



**Figure 65. DDR mode**



### USB OTG_HS characteristics

Unless otherwise specified, the parameters given in *Table 125* for ULPI are derived from tests performed under the ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load $C_L$=20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- VOS level set to VOS1

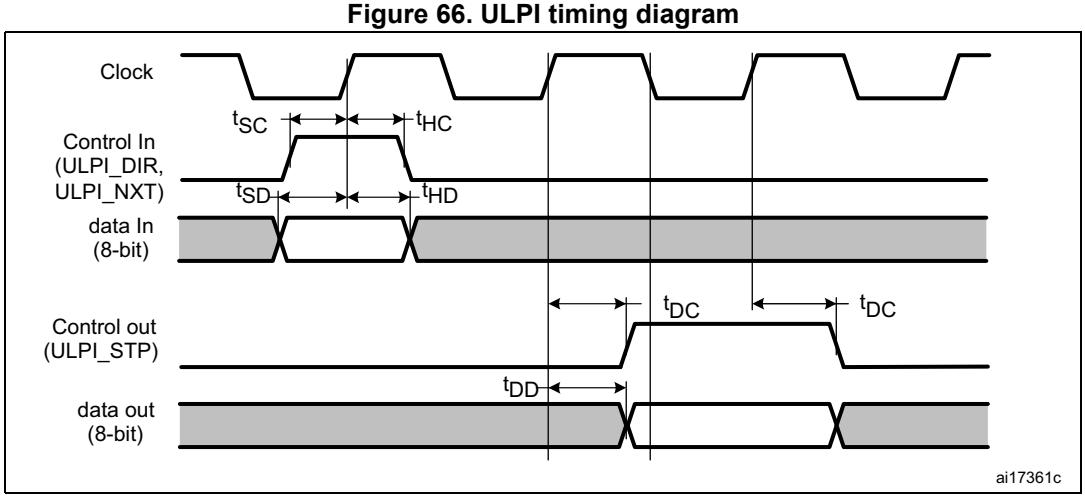
Refer to *Section 6.3.18: I/O port characteristics* for more details on the input/output characteristics.

**Table 125. Dynamics characteristics: USB ULPI(1)**

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{SC}$ | Control in (ULPI_DIR , ULPI_NXT) setup time | - | 2.5 | - | - | ns |
| $t_{HC}$ | Control in (ULPI_DIR, ULPI_NXT) hold time | - | 2 | - | - | |
| $t_{SD}$ | Data in setup time | - | 2.5 | - | - | |
| $t_{HD}$ | Data in hold time | - | 0 | - | - | |
| $t_{DC}/t_{DD}$ | Control/Datal output delay | $2.7<V_{DD}<3.6$ V $C_L$=20 pF | - | 9 | 9.5 | |
| | | $1.71<V_{DD}<3.6$ V $C_L$=15 pF | - | 9 | 14 | |

1. Guaranteed by characterization results.

**Figure 66. ULPI timing diagram**



### Ethernet interface characteristics

Unless otherwise specified, the parameters given in *Table 126*, *Table 127* and *Table 128* for SMI, RMII and MII are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load $C_L$=20 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- IO Compensation cell activated.
- HSLV activated when VDD ≤ 2.7 V
- VOS level set to VOS1

Refer to *Section 6.3.18: I/O port characteristics* for more details on the input/output characteristics:

**Table 126. Dynamics characteristics: Ethernet MAC signals for SMI (1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{MDC}$ | MDC cycle time( 2.5 MHz) | 400 | 400 | 403 | ns |
| $T_{d(MDIO)}$ | Write data valid time | 0.5 | 1.5 | 4 | |
| $t_{su(MDIO)}$ | Read data setup time | 12.5 | - | - | |
| $t_{h(MDIO)}$ | Read data hold time | 0 | - | - | |

1. Guaranteed by characterization results.

**Figure 67. Ethernet SMI timing diagram**

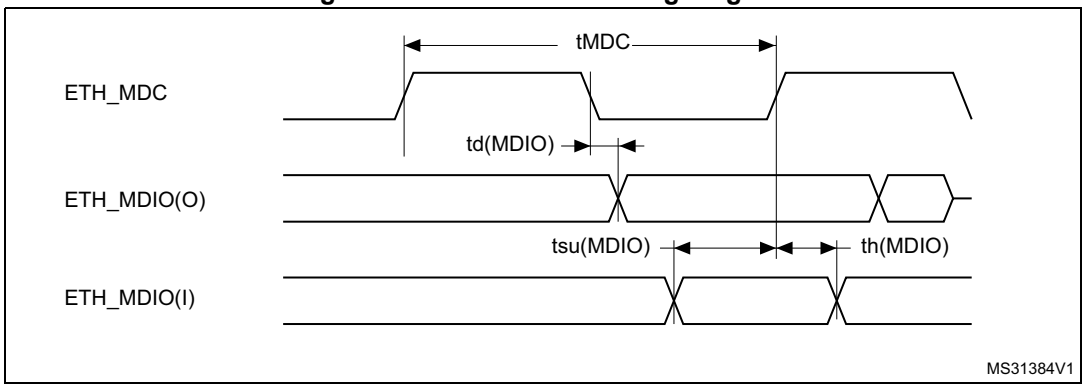


**Table 127. Dynamics characteristics: Ethernet MAC signals for RMII (1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{su(RXD)}$ | Receive data setup time | 2 | - | - | ns |
| $t_{ih(RXD)}$ | Receive data hold time | 2 | - | - | |
| $t_{su(CRS)}$ | Carrier sense setup time | 1.5 | - | - | |
| $t_{ih(CRS)}$ | Carrier sense hold time | 1.5 | - | - | |
| $t_{d(TXEN)}$ | Transmit enable valid delay time | 7 | 8 | 9.5 | |
| $t_{d(TXD)}$ | Transmit data valid delay time | 8 | 9 | 11 | |

1. Guaranteed by characterization results.

**Figure 68. Ethernet RMII timing diagram**

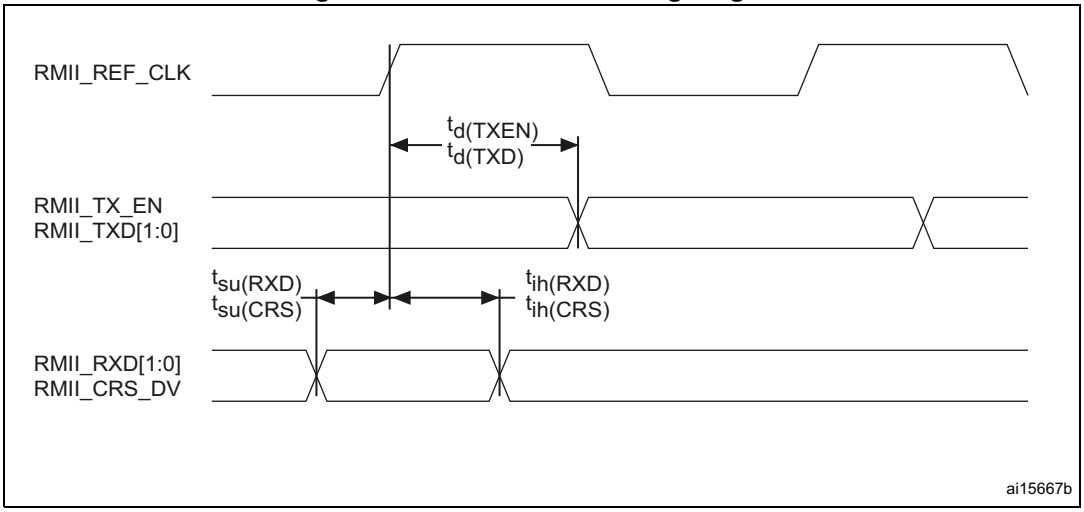
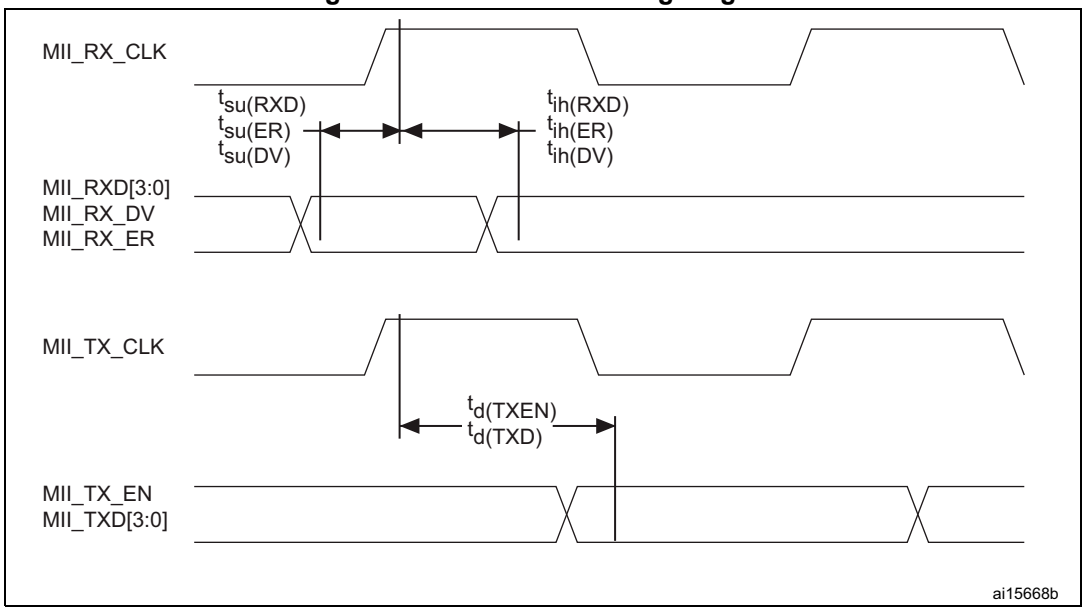



**Table 128. Dynamics characteristics: Ethernet MAC signals for MII (1)**

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{su(RXD)}$ | Receive data setup time | 2 | - | - | ns |
| $t_{ih(RXD)}$ | Receive data hold time | 2 | - | - | |
| $t_{su(DV)}$ | Data valid setup time | 1.5 | - | - | |
| $t_{ih(DV)}$ | Data valid hold time | 1.5 | - | - | |
| $t_{su(ER)}$ | Error setup time | 1.5 | - | - | |
| $t_{ih(ER)}$ | Error hold time | 0.5 | - | - | |
| $t_{d(TXEN)}$ | Transmit enable valid delay time | 9 | 10 | 11 | |
| $t_{d(TXD)}$ | Transmit data valid delay time | 8.5 | 9.5 | 12.5 | |

1. Guaranteed by characterization results.

**Figure 69. Ethernet MII timing diagram**




## JTAG/SWD interface characteristics

Unless otherwise specified, the parameters given in *Table 129* and *Table 130* for JTAG/SWD are derived from tests performed under the ambient temperature, $f_{rcc_c_ck}$ frequency and $V_{DD}$ supply voltage summarized in *Table 22: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 0x10
- Capacitive load $C_L$=30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$
- VOS level set to VOS1

Refer to *Section 6.3.18: I/O port characteristics* for more details on the input/output characteristics:

**Table 129. Dynamics JTAG characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{pp}$ | $T_{CK}$ clock frequency | 2.7V <$V_{DD}$< 3.6 V | - | - | 37 | MHz |
| $1/t_{c(TCK)}$ | | 1.62 <$V_{DD}$< 3.6 V | - | - | 27.5 | |
| $ti_{su(TMS)}$ | TMS input setup time | - | 2.5 | - | - | |
| $ti_{h(TMS)}$ | TMS input hold time | - | 1 | - | - | |
| $ti_{su(TDI)}$ | TDI input setup time | - | 1.5 | - | - | - |
| $ti_{h(TDI)}$ | TDI input hold time | - | 1 | - | - | - |
| $t_{ov(TDO)}$ | TDO output valid time | 2.7V <$V_{DD}$< 3.6 V | - | 8 | 13.5 | - |
| | | 1.62 <$V_{DD}$< 3.6 V | - | 8 | 18 | - |
| $t_{oh(TDO)}$ | TDO output hold time | - | 7 | - | - | - |

**Table 130. Dynamics SWD characteristics:**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{pp}$ | SWCLK clock frequency | 2.7V <$V_{DD}$< 3.6 V | - | - | 71 | MHz |
| $1/t_{c(SWCLK)}$ | | 1.62 <$V_{DD}$< 3.6 V | - | - | 52.5 | |
| $ti_{su(SWDIO)}$ | SWDIO input setup time | - | 2.5 | - | - | - |
| $ti_{h(SWDIO)}$ | SWDIO input hold time | - | 1 | - | - | - |
| $t_{ov(SWDIO)}$ | SWDIO output valid time | 2.7V <$V_{DD}$< 3.6 V | - | 8.5 | 14 | - |
| | | 1.62 <$V_{DD}$< 3.6 V | - | 8.5 | 19 | - |
| $t_{oh(SWDIO)}$ | SWDIO output hold time | - | 8 | - | - | - |

**Figure 70. JTAG timing diagram**

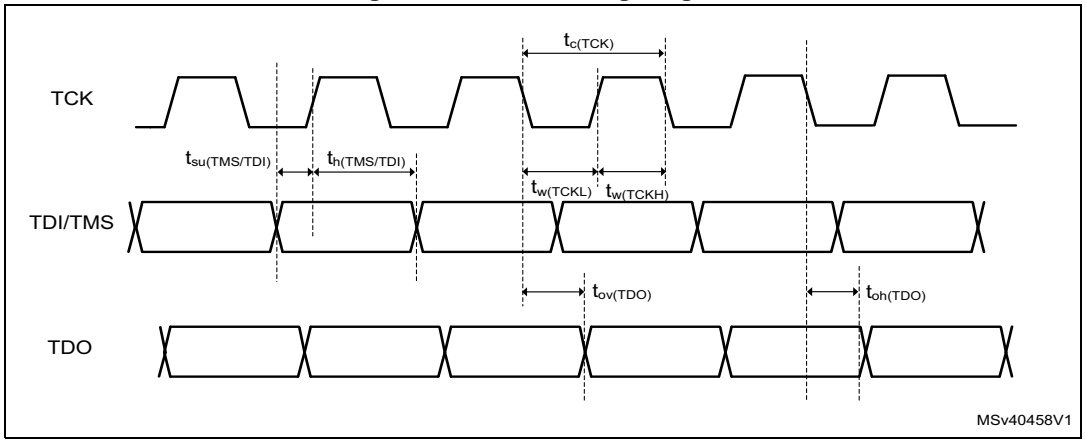
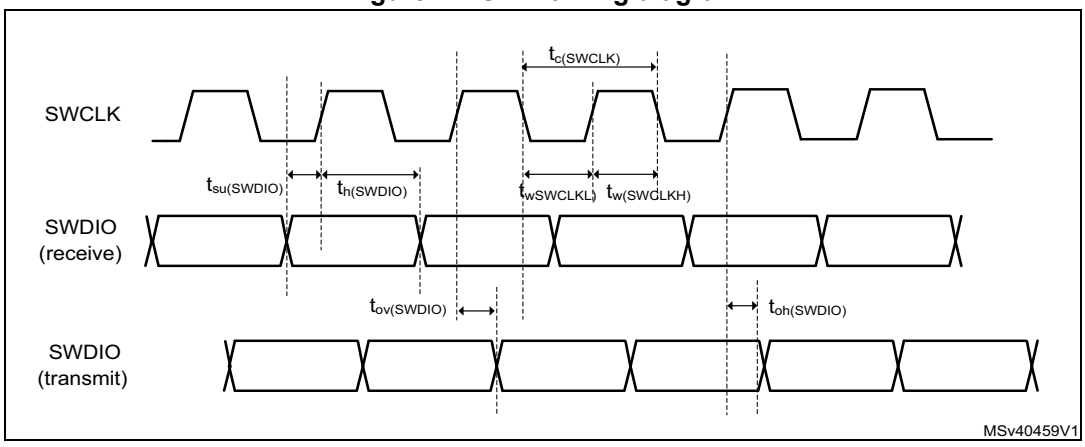



**Figure 71. SWD timing diagram**



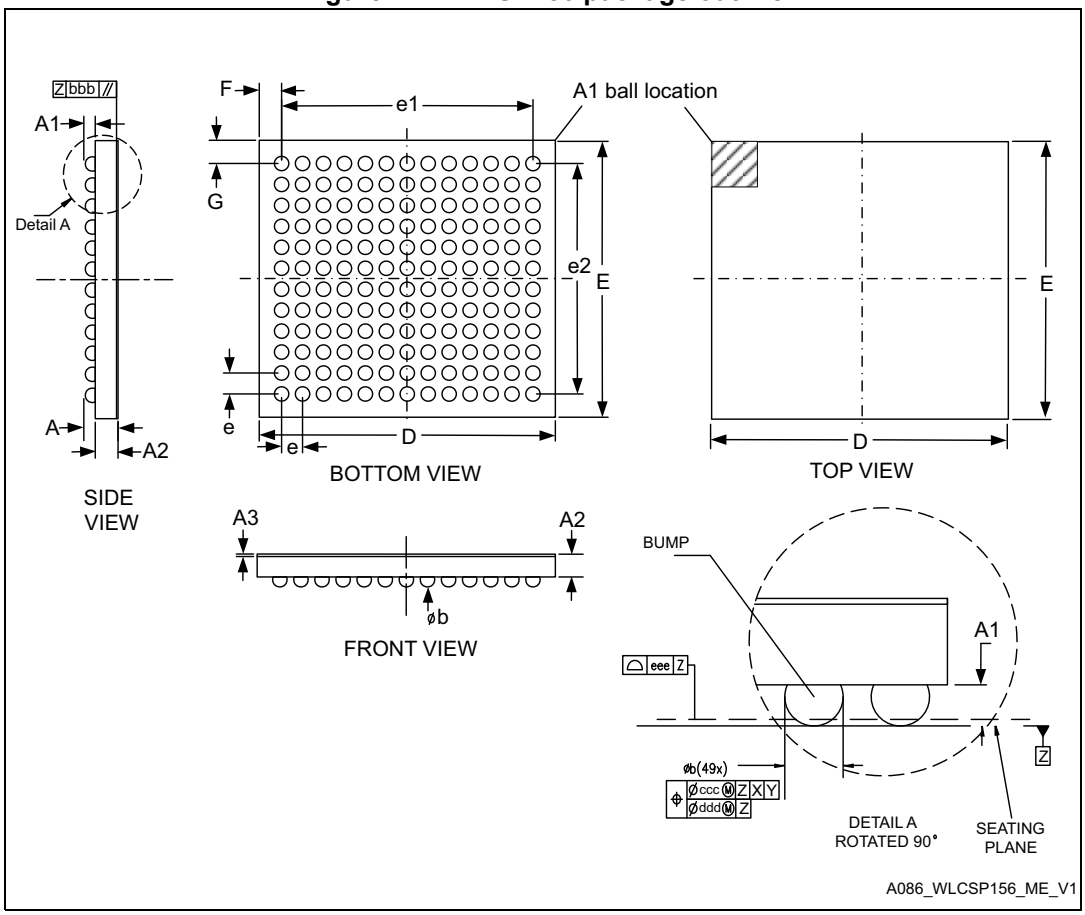
# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status *are available at www.st.com.* ECOPACK® is an ST trademark.

## 7.1 WLCSP156 package information

**WLCSP156 is a 156-bump, 4.96 x 4.64 mm, 0.35 mm pitch, wafer level chip scale package.**

**Figure 72. WLCSP156 package outline**



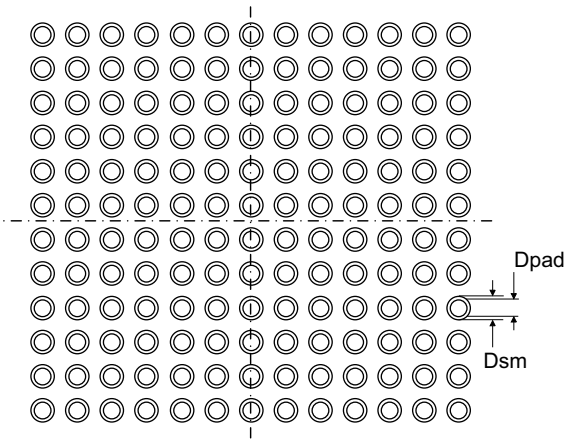

1. Drawing is not to scale.

**Table 131. WLCSP156 package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 0.58 | - | - | 0.023 |
| A1 | - | 0.17 | - | - | 0.006 | - |
| A2 | - | 0.38 | - | - | 0.015 | - |
| A3 | - | 0.025[2] | - | - | 0.001 | - |
| b | 0.21 | 0.24 | 0.27 | 0.008 | 0.009 | 0.011 |
| D | 4.94 | 4.96 | 4.98 | 0.193 | 0.195 | 0.196 |
| E | 4.62 | 4.64 | 4.66 | 0.181 | 0.182 | 0.183 |
| e1 | - | 4.20 | - | - | 0.014 | - |
| e2 | - | 3.85 | - | - | 0.165 | - |
| e | - | 0.35 | - | - | 0.152 | - |
| F | - | 0.380[3] | - | - | 0.015 | - |
| G | - | 0.395[3] | - | - | 0.015 | - |
| aaa | - | - | 0.10 | - | - | 0.004 |
| bbb | - | - | 0.10 | - | - | 0.004 |
| ccc | - | - | 0.10 | - | - | 0.004 |
| ddd | - | - | 0.05 | - | - | 0.002 |
| eee | - | - | 0.05 | - | - | 0.002 |

1. Values in inches are converted from mm and rounded to the 3rd decimal digits.
2. Back side coating. Nominal dimension rounded to the 3rd decimal place resulting from process capability.
3. Calculated dimensions are rounded to 3rd decimal place.

**Figure 73. WLCSP156 bump recommended footprint**




1. Dimensions are expressed in millimeters.

**Table 132. WLCSP156 bump recommended PCB design rules**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.35 mm |
| Dpad | 0.210 mm |
| Dsm | 0.275 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.235 mm |
| Stencil thickness | 0.100 mm |

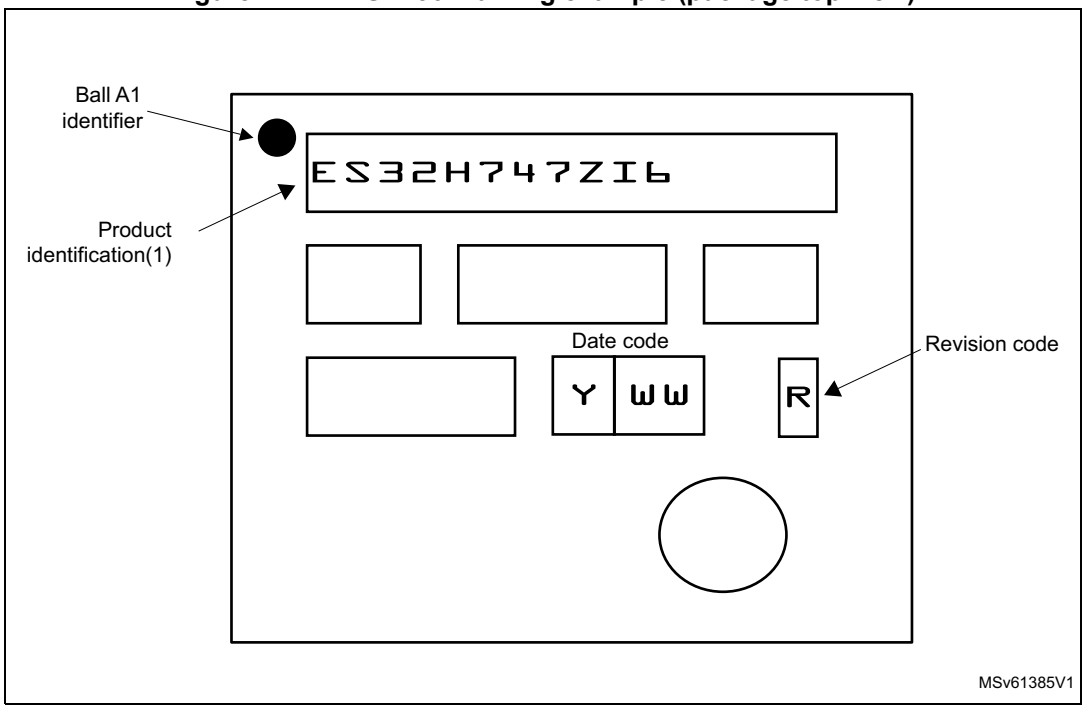
### Device marking for WLSCP156

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 74. WLCSP156 marking example (package top view)**

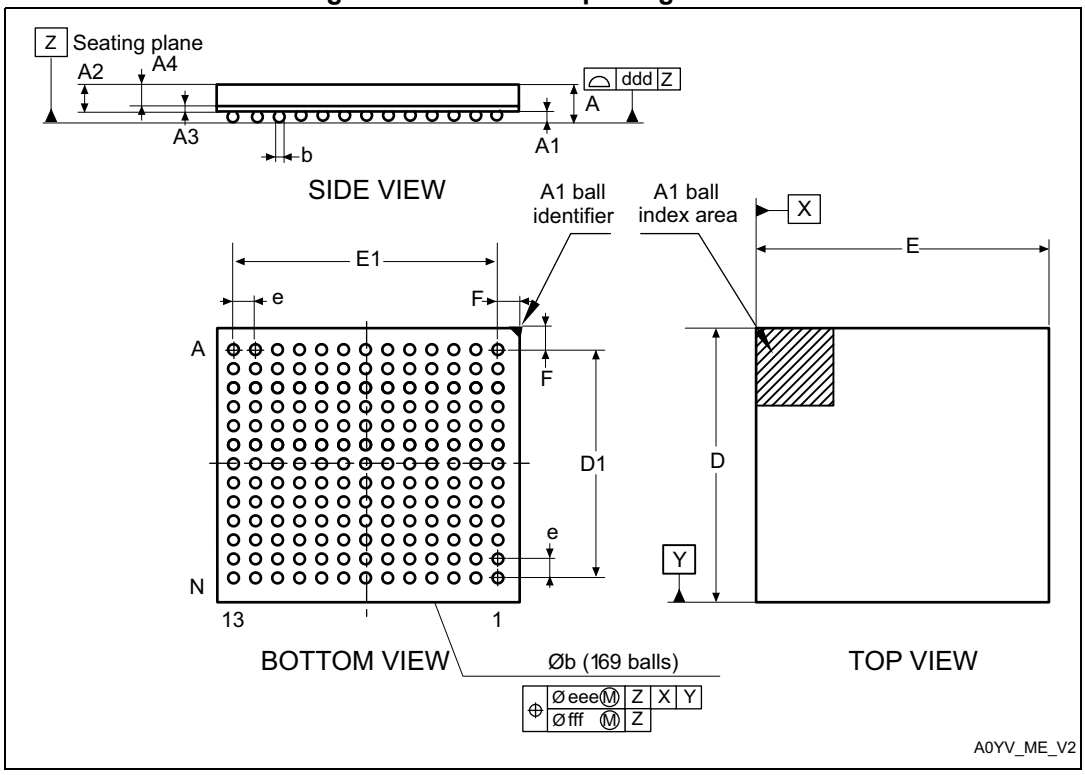



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 7.2 UFBGA169 package information

UFBGA169 is a 169-pin, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package.

**Figure 75. UFBGA169 package outline**




1. Drawing is not in scale.

**Table 133. UFBGA169 package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.0020 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A3 | - | 0.130 | - | - | 0.0051 | - |
| A4 | 0.270 | 0.320 | 0.370 | 0.0106 | 0.0126 | 0.0146 |
| b | 0.230 | 0.280 | 0.330 | 0.0091 | 0.0110 | 0.0130 |
| D | 6.950 | 7.000 | 7.050 | 0.2736 | 0.2756 | 0.2776 |
| D1 | 5.950 | 6.000 | 6.050 | 0.2343 | 0.2362 | 0.2382 |
| E | 6.950 | 7.000 | 7.050 | 0.2736 | 0.2756 | 0.2776 |
| E1 | 5.950 | 6.000 | 6.050 | 0.2343 | 0.2362 | 0.2382 |
| e | - | 0.500 | - | - | 0.0197 | - |
| F | 0.450 | 0.500 | 0.550 | 0.0177 | 0.0197 | 0.0217 |

**Table 133. UFBGA169 package mechanical data (continued)**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| ddd | - | - | 0.100 | - | - | 0.0039 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

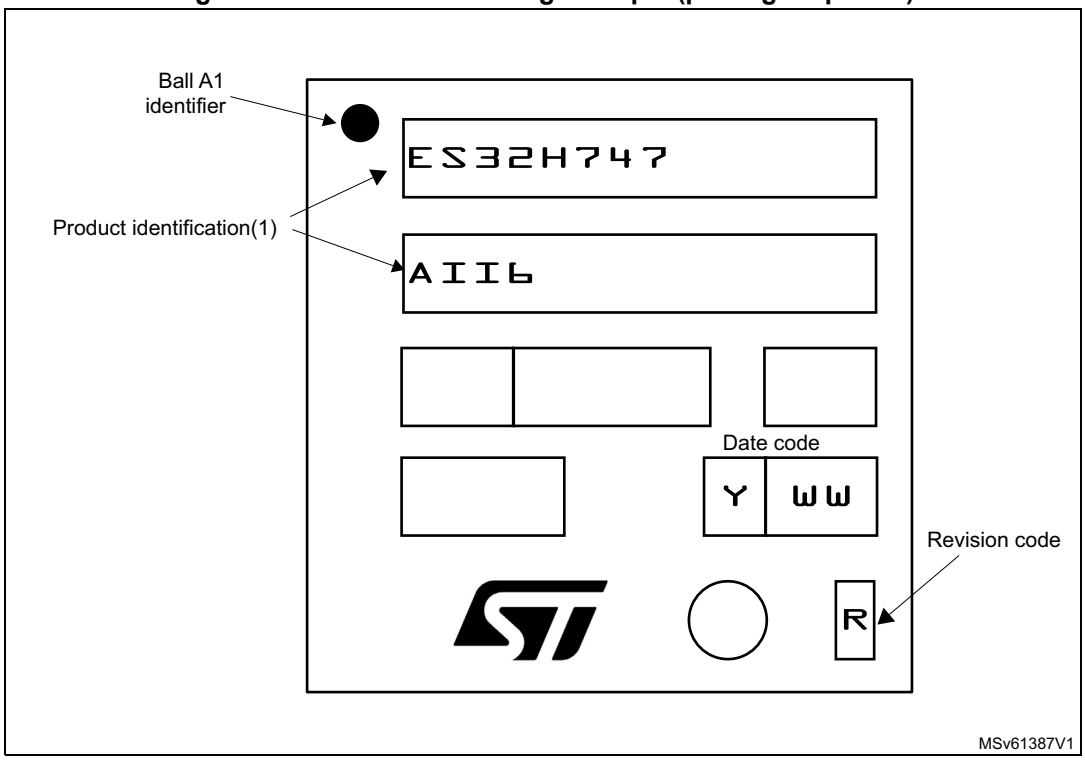
## Device marking for UFBGA169

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 76. UFBGA169 marking example (package top view)**

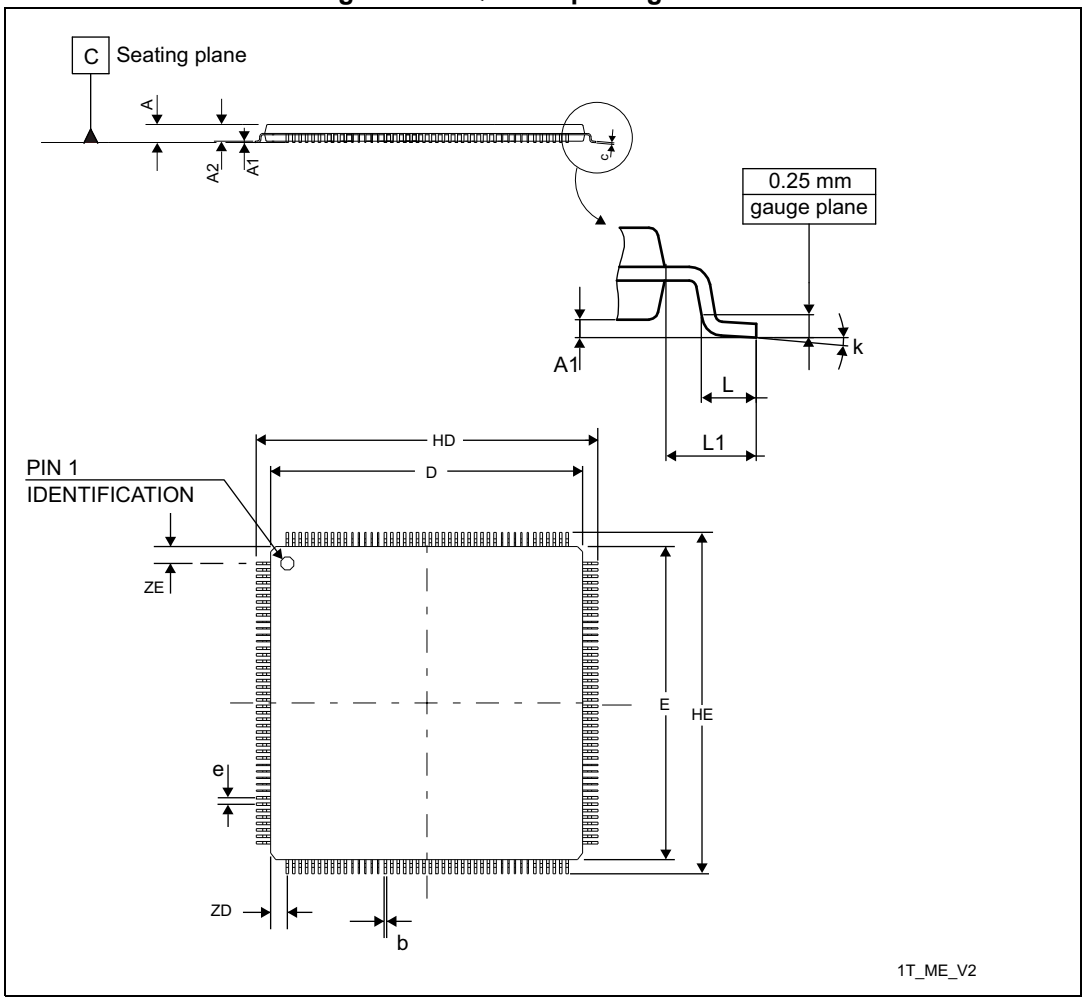



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not approved for use in production. ST is not responsible for any consequences resulting from such use. In no event will ST be liable for the customer using any of these engineering samples in production. ST’s Quality department must be contacted prior to any decision to use these engineering samples to run a qualification activity.

## 7.3 LQFP176 package information

**LQFP176 is a 176-pin, 24 x 24 mm low profile quad flat package.**

**Figure 77. LQFP176 package outline**




1. Drawing is not to scale.

**Table 134. LQFP176 package mechanical data**

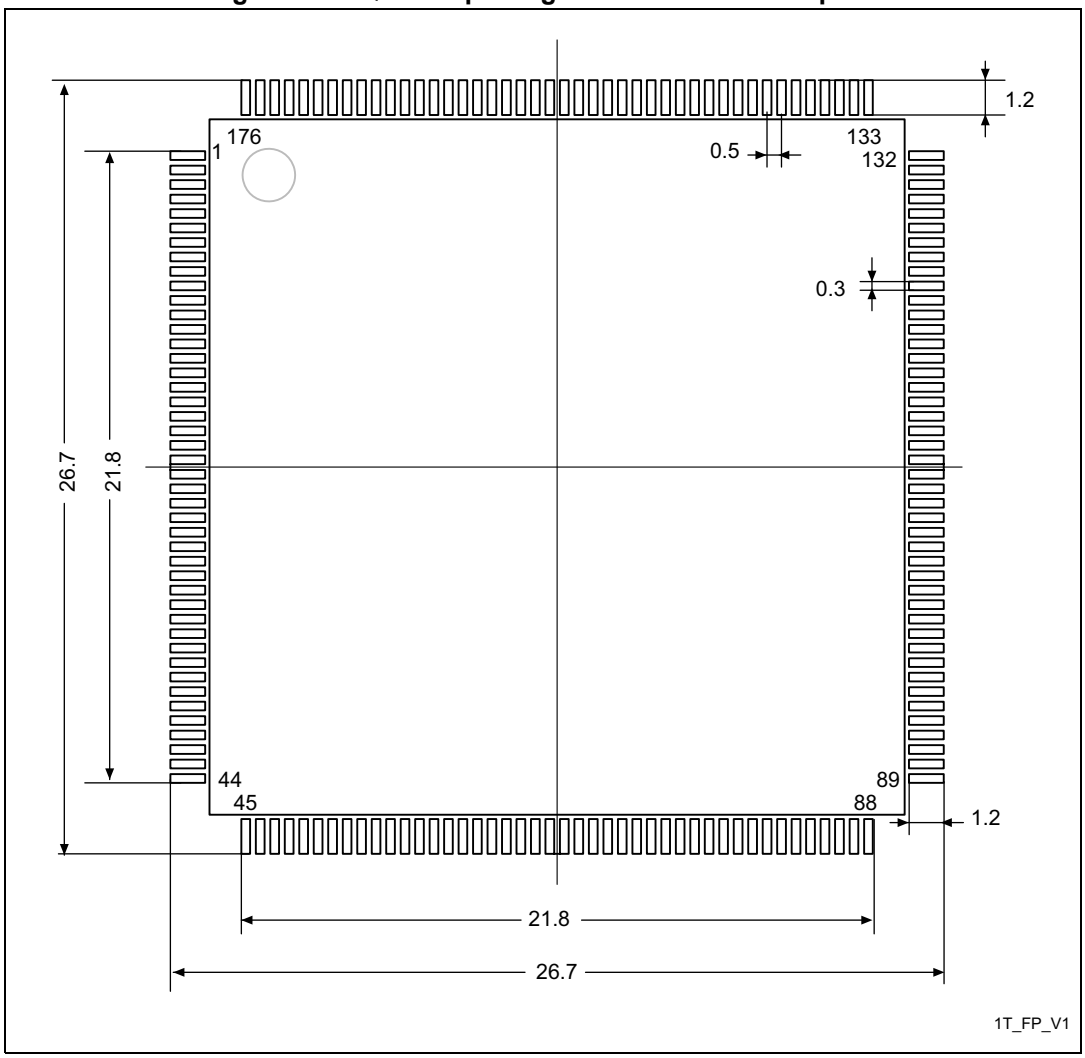
| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches[1] | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | - | 1.450 | 0.0531 | - | 0.0571 |
| b | 0.170 | - | 0.270 | 0.0067 | - | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |

**Table 134. LQFP176 package mechanical data (continued)**

| Ref. | Dimensions | | | | | |
|---|---|---|---|---|---|---|
| | Millimeters | | | Inches[1] | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| D | 23.900 | - | 24.100 | 0.9409 | - | 0.9488 |
| HD | 25.900 | - | 26.100 | 1.0197 | - | 1.0276 |
| ZD | - | 1.250 | - | - | 0.0492 | - |
| E | 23.900 | - | 24.100 | 0.9409 | - | 0.9488 |
| HE | 25.900 | - | 26.100 | 1.0197 | - | 1.0276 |
| ZE | - | 1.250 | - | - | 0.0492 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L[2] | 0.450 | - | 0.750 | 0.0177 | - | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | - | 7° | 0° | - | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. L dimension is measured at gauge plane at 0.25 mm above the seating plane.

**Figure 78. LQFP176 package recommended footprint**




1. Dimensions are expressed in millimeters.

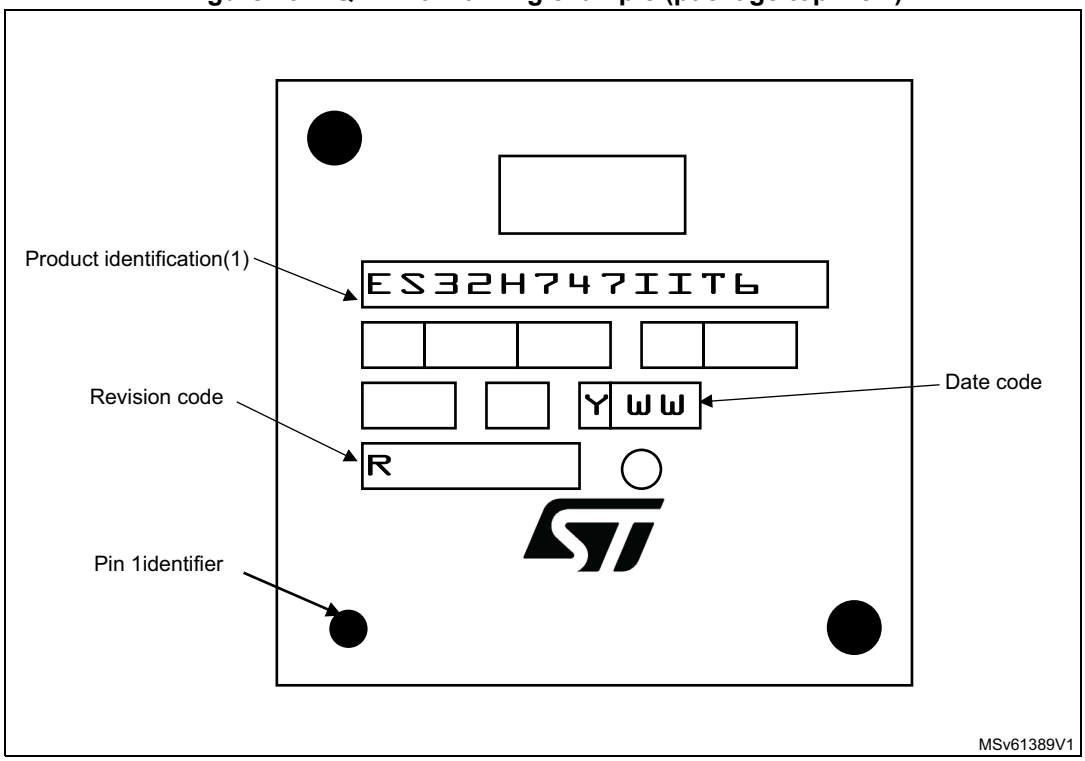
### Device marking for LQFP176

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 79. LQFP176 marking example (package top view)**

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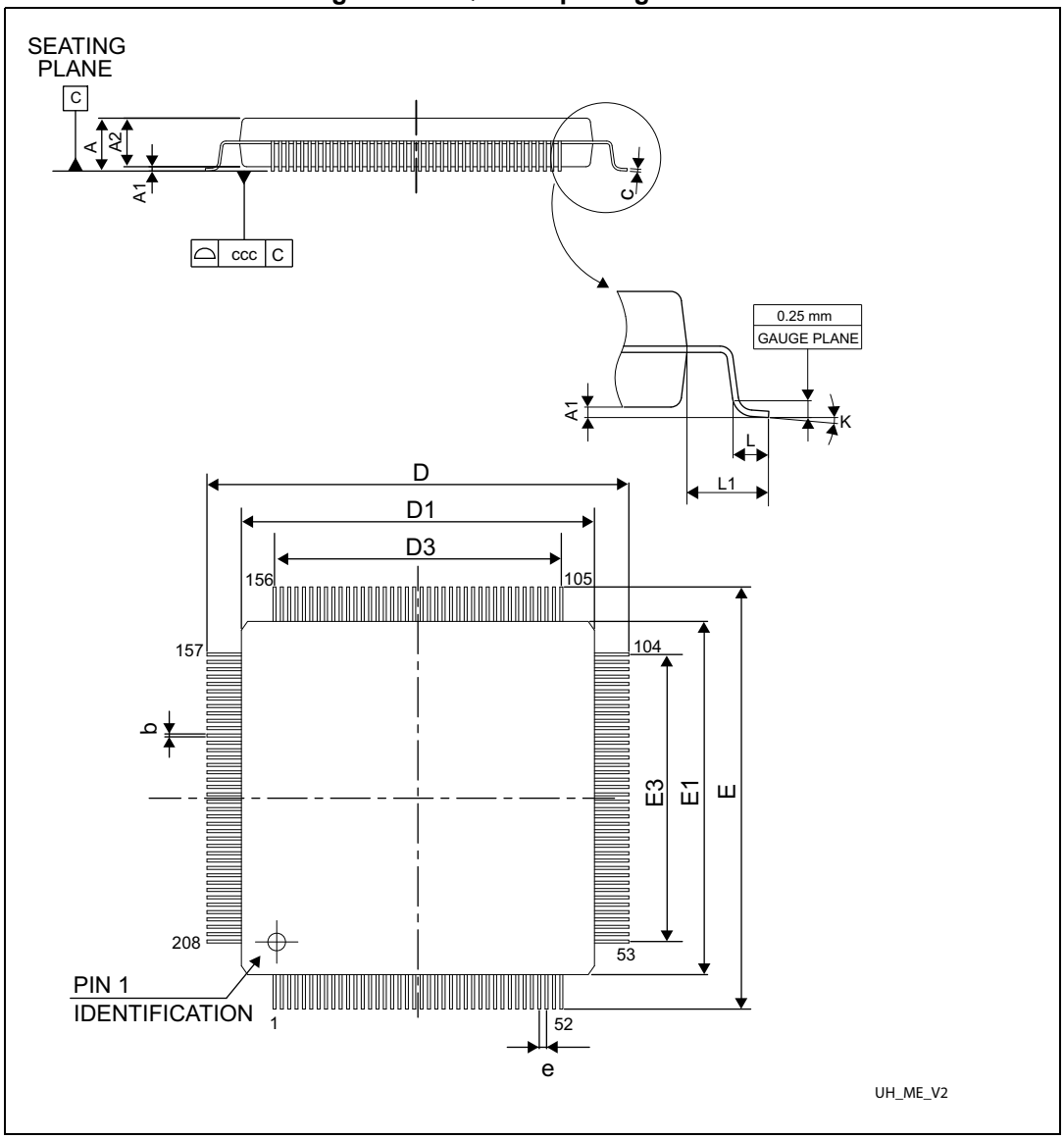
## 7.4 LQFP208 package information

**LQFP208 is a 208-pin, 28 x 28 mm low-profile quad flat package.**

**Figure 80. LQFP208 package outline**



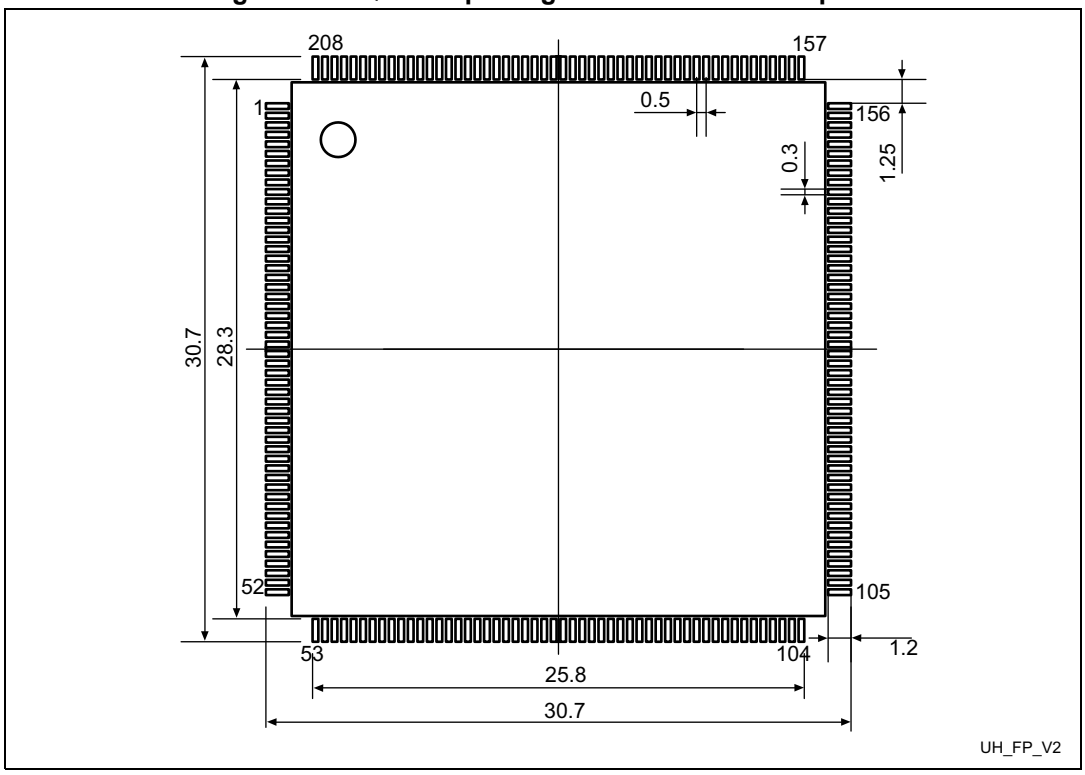

1. Drawing is not to scale.

**Table 135. LQFP208 package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 29.800 | 30.000 | 30.200 | 1.1811 | 1.1732 | 1.1890 |
| D1 | 27.800 | 28.000 | 28.200 | 1.1024 | 1.0945 | 1.1102 |
| D3 | - | 25.500 | - | - | 1.0039 | - |
| E | 29.800 | 30.000 | 30.200 | 1.1811 | 1.1732 | 1.1890 |
| E1 | 27.800 | 28.000 | 28.200 | 1.1024 | 1.0945 | 1.1102 |
| E3 | - | 25.500 | - | - | 1.0039 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 81. LQFP208 package recommended footprint**




1. Dimensions are expressed in millimeters.

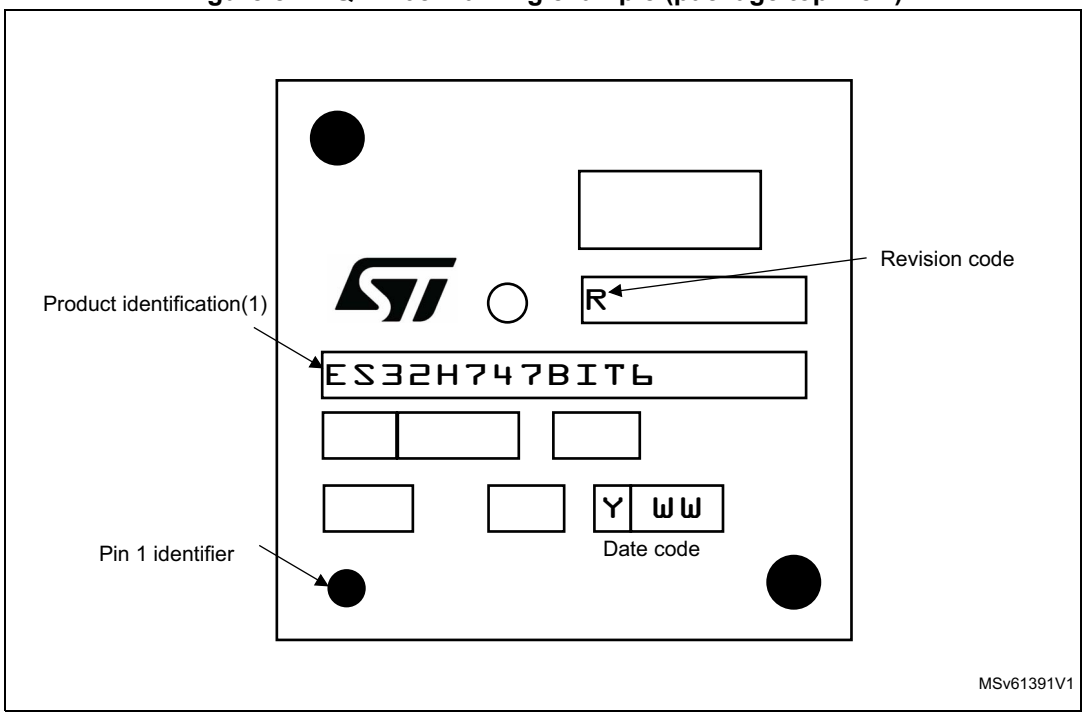
### Device marking for LQFP208

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 82. LQFP208 marking example (package top view)**

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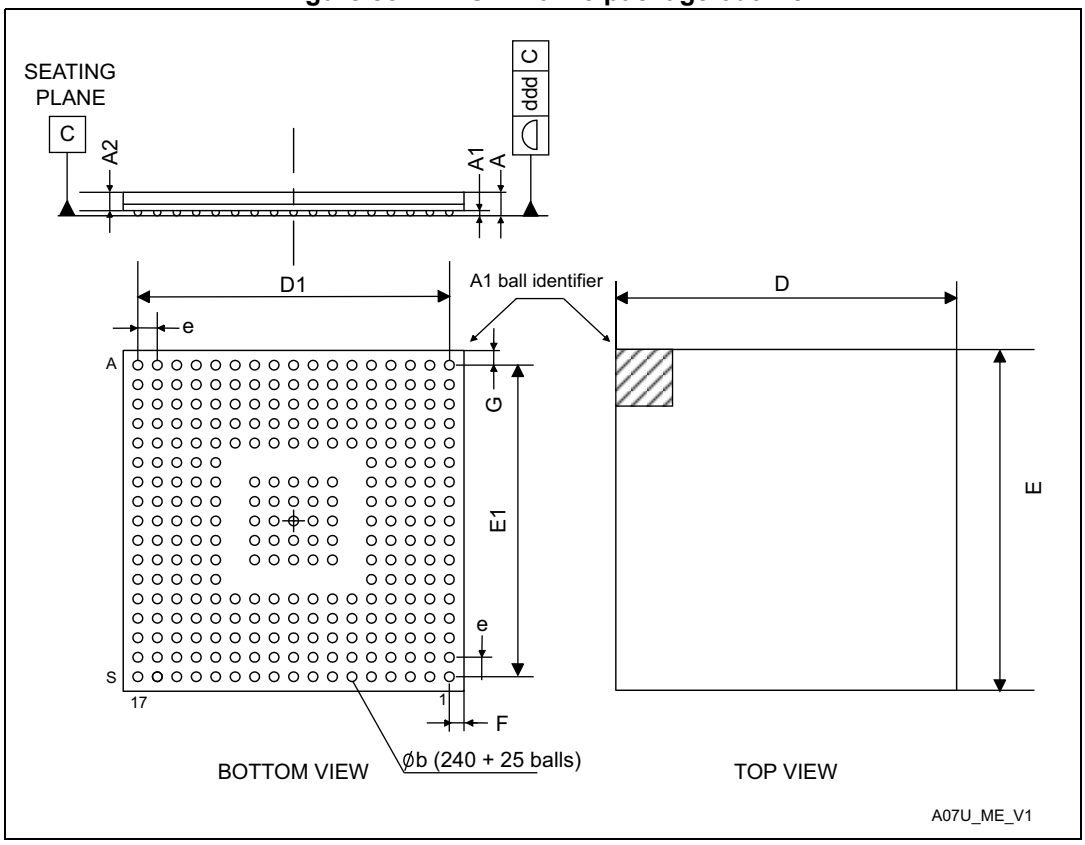
## 7.5 TFBGA240+25 package information

**TFBGA240+25 is a 265 ball, 14x14 mm, 0.8 mm pitch, fine pitch ball grid array package.**

**Figure 83. TFBGA240+25 package outline**



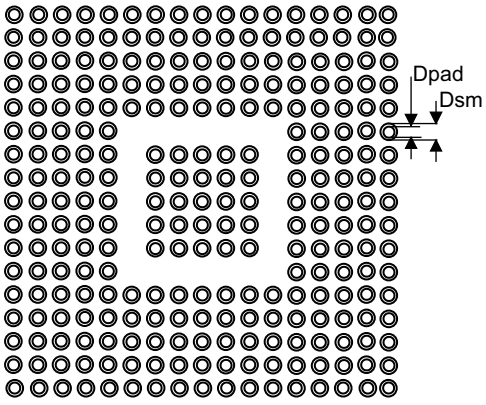

1. Dimensions are expressed in millimeters.

**Table 136. TFBG240+25 ball package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.100 | - | - | 0.0433 |
| A1 | 0.150 | - | - | 0.0059 | - | - |
| A2 | - | 0.760 | - | - | 0.0299 | - |
| b | 0.350 | 0.400 | 0.450 | 0.0138 | 0.0157 | 0.0177 |
| D | 13.850 | 14.000 | 14.150 | 0.5453 | 0.5512 | 0.5571 |
| D1 | - | 12.800 | - | - | 0.5039 | - |
| E | 13.850 | 14.000 | 14.150 | 0.5453 | 0.5512 | 0.5571 |
| E1 | - | 12.800 | - | - | 0.5039 | - |
| e | - | 0.800 | - | - | 0.0315 | - |
| F | - | 0.600 | - | - | 0.0236 | - |
| G | - | 0.600 | - | - | 0.0236 | - |
| ddd | - | - | 0.100 | - | - | 0.0039 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

**Figure 84. TFBGA240+25 package recommended footprint**




1. Dimensions are expressed in millimeters.

**Table 137. TFBGA240+25 recommended PCB design rules (0.8 mm pitch)**

| Dimension | Recommended values |
|---|---|
| Pitch | 0.8 mm |
| Dpad | 0.225 mm |
| Dsm | 0.290 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.250 mm |
| Stencil thickness | 0.100 mm |

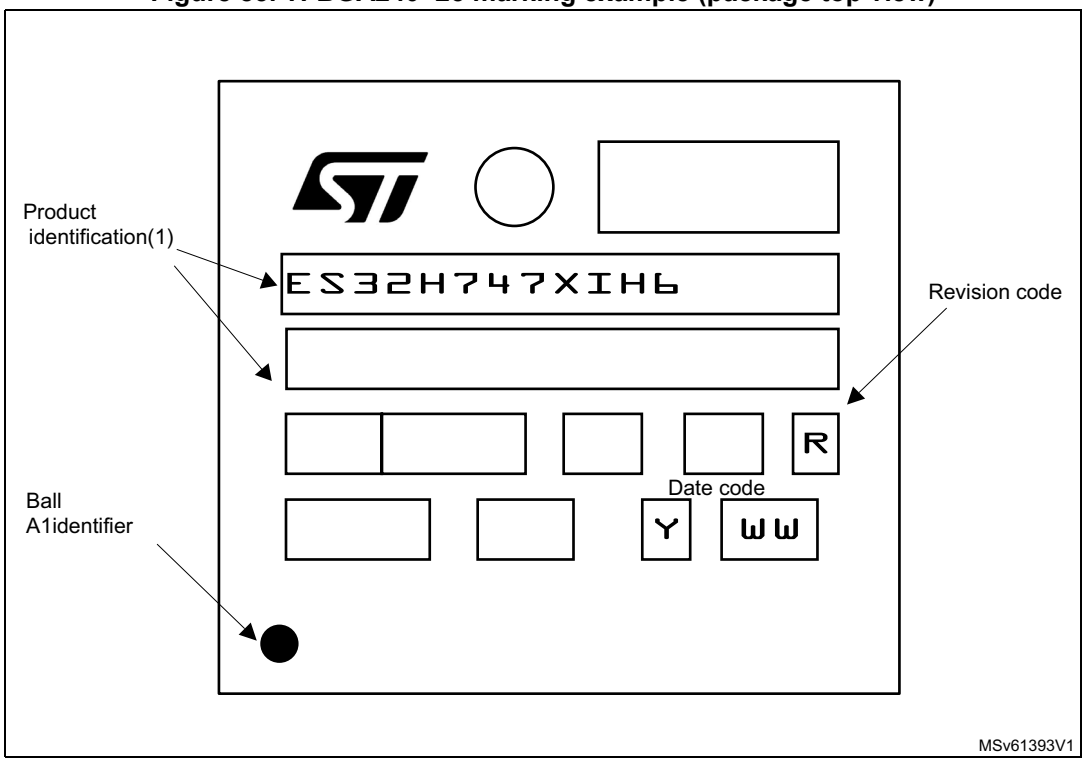
### Device marking for TFBGA240+25

The following figure gives an example of topside marking versus pin 1 position identifier location.

The printed markings may differ depending on the supply chain.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

**Figure 85. TFBGA240+25 marking example (package top view)**

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## 7.6 Thermal characteristics

The maximum chip-junction temperature, $T_J$ max, in degrees Celsius, may be calculated using the following equation:

$T_J$ max = $T_A$ max + ($P_D$ max × $\Theta_{JA}$)

Where:

- $T_A$ max is the maximum ambient temperature in °C,
- $\Theta_{JA}$ is the package junction-to-ambient thermal resistance, in °C/W,
- $P_D$ max is the sum of $P_{INT}$ max and $P_{I/O}$ max ($P_D$ max = $P_{INT}$ max + $P_{I/O}$max),
- $P_{INT}$ max is the product of $I_{DD}$ and $V_{DD}$, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma$ ($V_{OL}$ × $I_{OL}$) + $\Sigma$(($V_{DD}$ – $V_{OH}$) × $I_{OH}$),

taking into account the actual $V_{OL}$ / $I_{OL}$ and $V_{OH}$ / $I_{OH}$ of the I/Os at low and high level in the application.

**Table 138. Thermal characteristics**

| Symbol | Definition | Parameter | Value | Unit |
|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance junction-ambient | **Thermal resistance junction-ambient** WLCSP156 - 4.96 x 4.64 mm /0.35 mm pitch | 35 | °C/W |
| | | **Thermal resistance junction-ambient** UFBGA169 - 7 x 7 mm /0.5 mm pitch | 37.7 | |
| | | **Thermal resistance junction-ambient** LQFP176 - 24 x 24 mm /0.5 mm pitch | 43.0 | |
| | | **Thermal resistance junction-ambient** LQFP208 - 28 x 28 mm /0.5 mm pitch | 42.4 | |
| | | **Thermal resistance junction-ambient** TFBGA240+25 - 14 x 14 mm / 0.8 mm pitch | 36.6 | |
| $\Theta_{JB}$ | Thermal resistance junction-board | **Thermal resistance junction-ambient** WLCSP156 - 4.96 x 4.64 mm /0.35 mm pitch | 18.1 | °C/W |
| | | **Thermal resistance junction-ambient** UFBGA169 - 7 x 7 mm /0.5 mm pitch | 17.3 | |
| | | **Thermal resistance junction-ambient** LQFP176 - 24 x 24 mm /0.5 mm pitch | 39.4 | |
| | | **Thermal resistance junction-ambient** LQFP208 - 28 x 28 mm /0.5 mm pitch | 40.3 | |
| | | **Thermal resistance junction-ambient** TFBGA240+25 - 14 x 14 mm / 0.8 mm pitch | 24.3 | |

Table 138. Thermal characteristics (continued)

| Symbol | Definition | Parameter | Value | Unit |
|---|---|---|---|---|
| $\Theta_{JC}$ | Thermal resistance junction-case | **Thermal resistance junction-ambient** WLCSP156 - 4.96 x 4.64 mm /0.35 mm pitch | 1 | °C/W |
| | | **Thermal resistance junction-ambient** UFBGA169 - 7 x 7 mm /0.5 mm pitch | 11 | |
| | | **Thermal resistance junction-ambient** LQFP176 - 24 x 24 mm /0.5 mm pitch | 11.2 | |
| | | **Thermal resistance junction-ambient** LQFP208 - 28 x 28 mm /0.5 mm pitch | 11.1 | |
| | | **Thermal resistance junction-ambient** TFBGA240+25 - 14 x 14 mm / 0.8 mm pitch | 7.4 | |

### 7.6.1 Reference document

- JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org.
- For information on thermal management, refer to application note “Thermal management guidelines for STM32 32-bit Arm Cortex MCUs applications” (AN5036) available from *www.st.com*.

# 8 Ordering information

Example: STM32 H 747 X I T 6 TR

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

H = High performance

Device subfamily

747 = STM32H7x7 dual core MIPI-DSI line

Pin count

Z = 156 pins

A = 169 pins

I = 176 pins/balls

B = 208 pins

X = 240 balls

Flash memory size

G = 1 Mbytes

I = 2 Mbytes

Package

T = LQFP ECOPACK®2

I = UFBGA pitch 0.5 mm ECOPACK®2

H = TFBGA ECOPACK®2

Y = WLCSP ECOPACK®2

Temperature range

6 = –40 to 85 °C

Packing

TR = tape and reel

No character = tray or tube

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

# 9 Revision history

Table 139. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 16-May-2019 | 1 | Initial release. |

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- *Подбор аналогов.*
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