



0.5 dB LSB GaAs MMIC 6-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, 2.2 - 8.0 GHz

Typical Applications

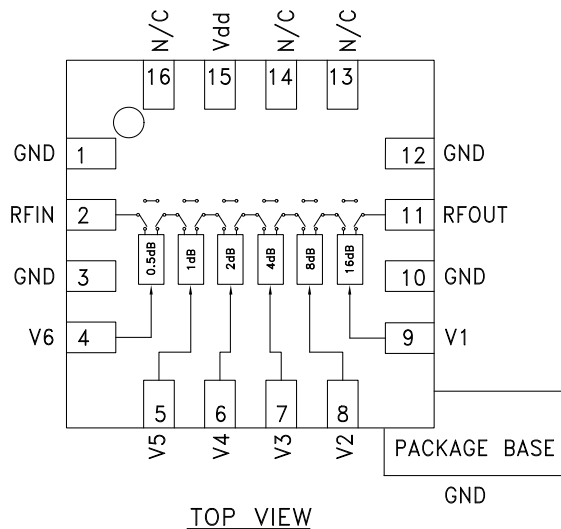
The HMC425LP3 / HMC425LP3E is ideal for:

- WLAN & Point-to-Multi-Point
- Fiber Optics & Broadband Telecom
- Microwave Radio & VSAT
- Military

Features

- 0.5 dB LSB Steps to 31.5 dB
- Single Control Line Per Bit
- ± 0.5 dB Typical Bit Error
- Single +5V Supply
- 3x3 mm SMT Package

Functional Diagram



General Description

The HMC425LP3 & HMC425LP3E are broadband 6-bit GaAs IC digital attenuators in low cost leadless surface mount packages. Covering 2.2 to 8.0 GHz, the insertion loss is less than 3.8 dB typical. The attenuator bit values are 0.5 (LSB), 1, 2, 4, 8, and 16 dB for a total attenuation of 31.5 dB. Attenuation accuracy is excellent at ± 0.5 dB typical step error with an IIP3 of +40 dBm. Six control voltage inputs, toggled between 0 and +3 to +5V, are used to select each attenuation state. A single Vdd bias of +3 to +5V is required.

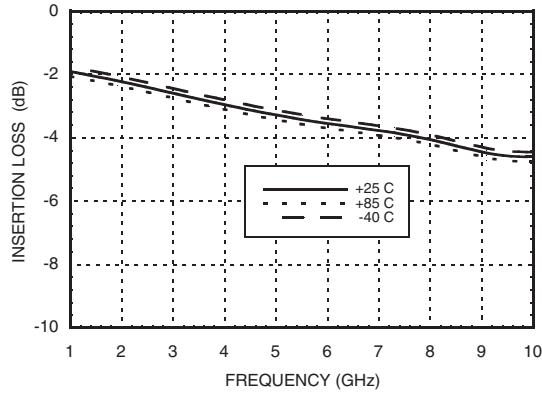
Electrical Specifications,

$T_a = +25^\circ \text{C}$, With $V_{dd} = +5\text{V}$ & $V_{ctl} = 0/+5\text{V}$ (Unless Otherwise Noted)

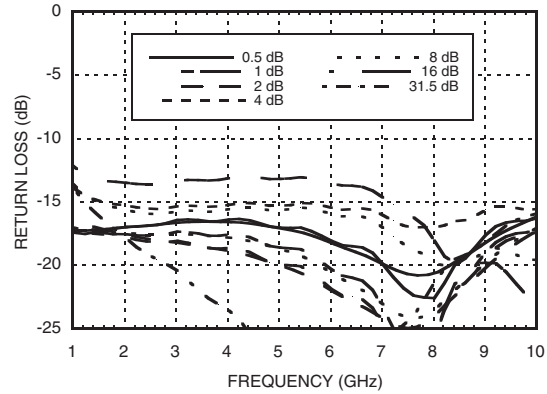
| Parameter | Frequency (GHz) | Min. | Typ. | Max. | Units |
|--|-----------------------------|--|-----------------------|------|-------|
| Insertion Loss | 2.2 - 6.0 GHz | | 3.5 | 3.8 | dB |
| | 6.0 - 8.0 GHz | | 3.8 | 4.3 | dB |
| Attenuation Range | 2.2 - 8.0 GHz | | 31.5 | | dB |
| Return Loss (RF1 & RF2, All Atten. States) | 2.2 - 8.0 GHz | | 15 | | dB |
| Attenuation Accuracy: (Referenced to Insertion Loss) | All States 2.2 - 8.0 GHz | $\pm 0.5 + 5\%$ of Atten. Setting Max. | | | dB |
| Input Power for 0.1 dB Compression | 2.2 - 8.0 GHz | | Vdd = 5V | 22 | dBm |
| | | | Vdd = 3V | 19 | dBm |
| Input Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone) | 2.2 - 8.0 GHz | | REF - 16.0 dB States | 45 | dBm |
| | | | 16.5 - 31.5 dB States | 35 | dBm |
| Switching Characteristics | 2.2 - 8.0 GHz | | | | |
| tRISE, tFALL (10/90% RF) | | | 160 | | ns |
| tON, tOFF (50% CTL to 10/90% RF) | | | 180 | | ns |

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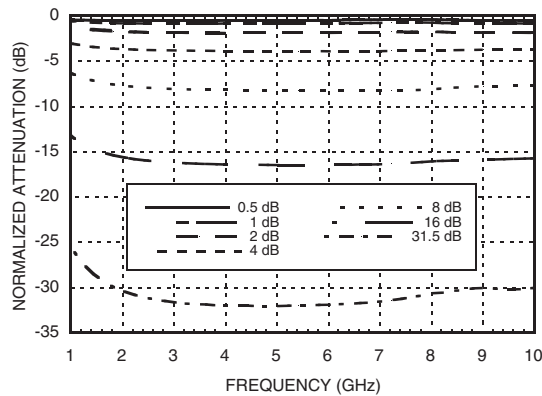
Insertion Loss



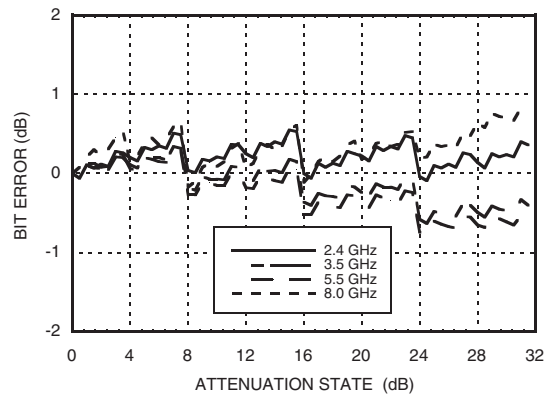
Return Loss RF1, RF2 (Only Major States are Shown)



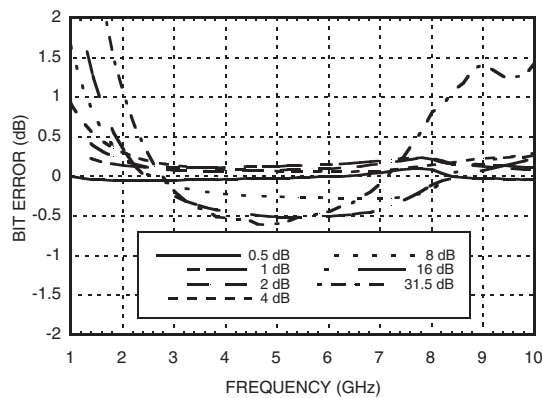
Normalized Attenuation (Only Major States are Shown)



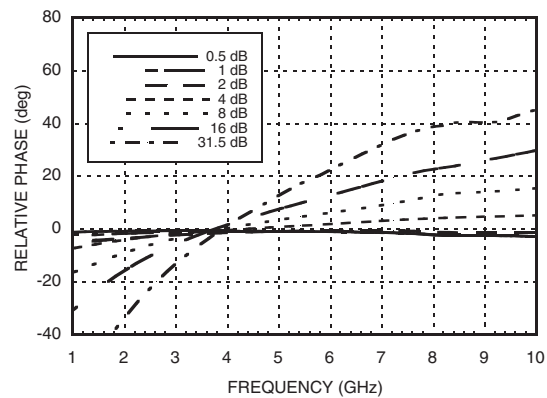
Bit Error vs. Attenuation State



Bit Error vs. Frequency (Only Major States are Shown)



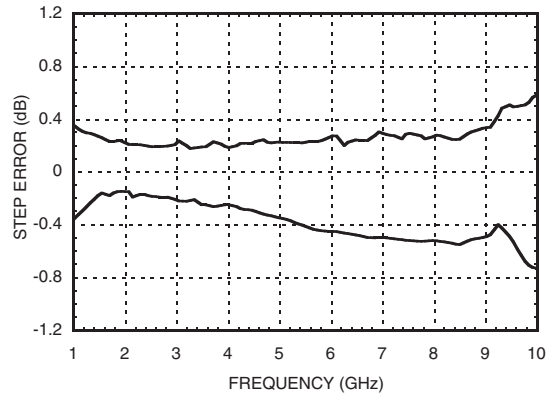
Relative Phase vs. Frequency (Only Major States are Shown)





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Worst Case Step Error Between Successive Attenuation States



Bias Voltage & Current

| Vdd Range = 3.0 to +5.0 Vdc | |
|-----------------------------|-----------------|
| Vdd (VDC) | Idd (Typ.) (µA) |
| +3.0 | 10 |
| +5.0 | 30 |

Control Voltage

| State | Bias Condition |
|-------|------------------------|
| Low | 0 to 0.2V @ 10 uA Typ. |
| High | Vdd ± 0.2V @ 5 uA Typ. |

Note: Vdd = +3V to +5V

Truth Table

| Control Voltage Input | | | | | | Attenuation State RF1 - RF2 |
|-----------------------|------------|------------|------------|------------|--------------|-----------------------------|
| V1 16 dB | V2 8 dB | V3 4 dB | V4 2 dB | V5 1 dB | V6 0.5 dB | |
| High | High | High | High | High | High | Reference I.L. |
| High | High | High | High | High | Low | 0.5 dB |
| High | High | High | High | Low | High | 1 dB |
| High | High | High | Low | High | High | 2 dB |
| High | High | Low | High | High | High | 4 dB |
| High | Low | High | High | High | High | 8 dB |
| Low | High | High | High | High | High | 16 dB |
| Low | Low | Low | Low | Low | Low | 31.5 dB |

Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

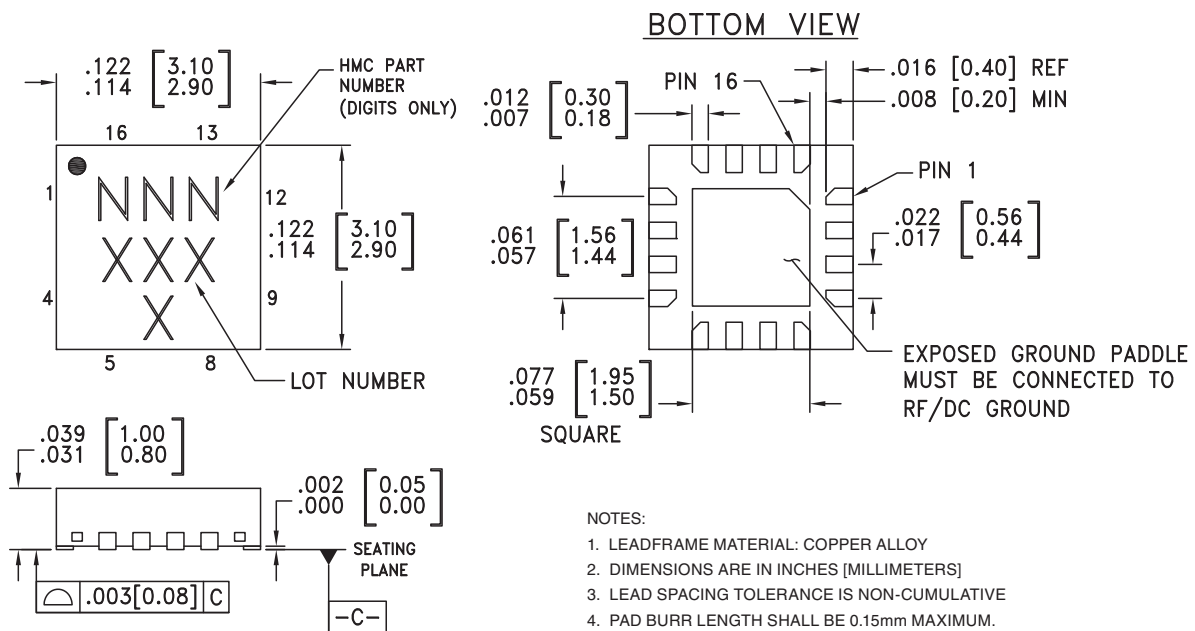
Absolute Maximum Ratings

| | |
|--------------------------------|----------------|
| Control Voltage (V1 to V6) | Vdd +0.5 Vdc |
| Bias Voltage (Vdd) | +7.0 Vdc |
| Storage Temperature | -65 to +150 °C |
| Operating Temperature | -40 to +85 °C |
| RF Input Power (2.4 - 8.0 GHz) | +30 dBm |
| ESD Sensitivity (HBM) | Class 1A |



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

| Part Number | Package Body Material | Lead Finish | MSL Rating | Package Marking ^[3] |
|-------------|--|---------------|---------------------|--------------------------------|
| HMC425LP3 | Low Stress Injection Molded Plastic | Sn/Pb Solder | MSL1 ^[1] | 425 XXXX |
| HMC425LP3E | RoHS-compliant Low Stress Injection Molded Plastic | 100% matte Sn | MSL1 ^[2] | 425 XXXX |

[1] Max peak reflow temperature of 235 °C

[2] Max peak reflow temperature of 260 °C

[3] 4-Digit lot number XXXX


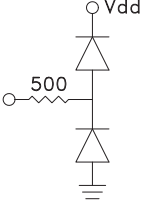


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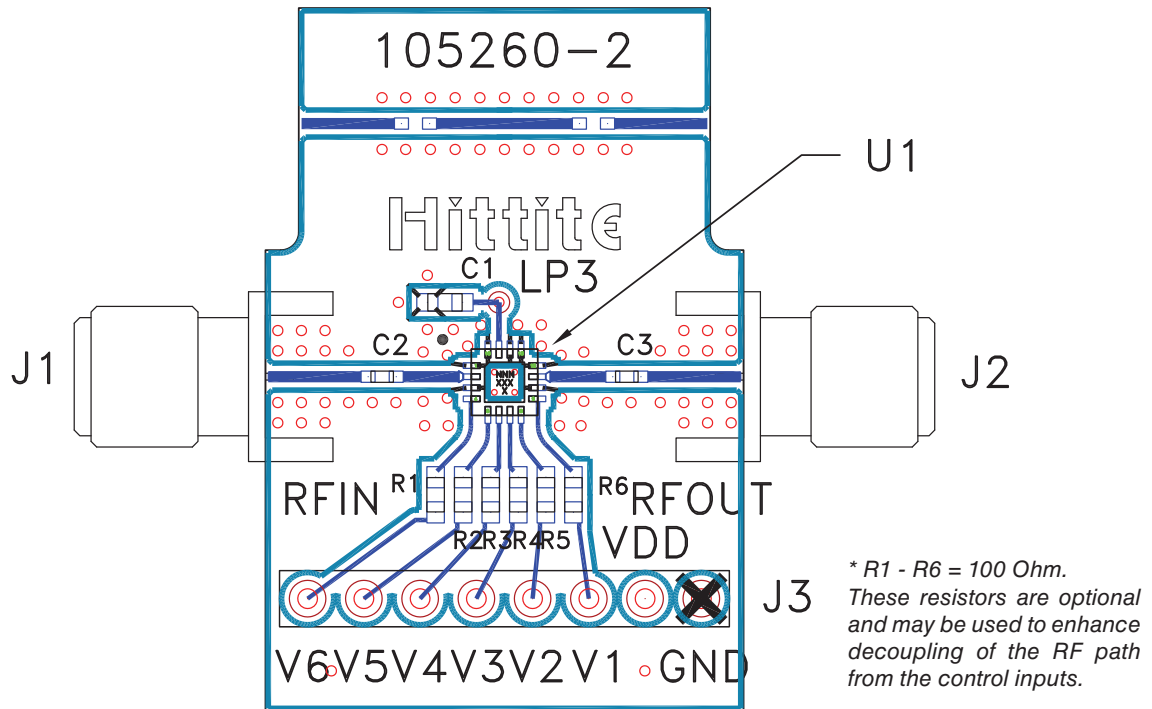
ATTENUATORS - DIGITAL - SMT

Pin Descriptions

| Pin Number | Function | Description | Interface Schematic |
|------------------|-------------|--|---|
| 1, 3, 10, 12 | GND | Package bottom has an exposed metal paddle that must also be connected to RF ground. |  |
| 2, 11 | RFIN, RFOUT | This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required. | |
| 4, 5, 6, 7, 8, 9 | V1 - V6 | See truth table and control voltage table. |  |
| 13, 14, 16 | N/C | This pin should be connected to PCB RF ground to maximize performance. | |
| 15 | Vdd | Supply Voltage. | |



Evaluation PCB



List of Materials for Evaluation PCB 105408 [1]

| Item | Description |
|---------|---|
| J1 - J2 | PCB Mount SMA Connector |
| J3 | 8 Pin DC Connector |
| C1 | 0.01 μ F Capacitor, 0603 Pkg. |
| C2, C3 | 100 pF Capacitor, 0402 Pkg. |
| R1 - R6 | 100 Ohm Resistor, 0603 Pkg. |
| U1 | HMC425LP3 / HMC425LP3E Digital Attenuator |
| PCB [2] | 105260 Evaluation PCB |

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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