High Voltage, Isolated Gate Driver with Internal Miller Clamp, 2 A Output

Data Sheet

ADuM4121/ADuM4121-1

FEATURES

2 A peak output current (<2 Ω R_{DSON})
2.5 V to 6.5 V input
4.5 V to 35 V output
Undervoltage lockout (UVLO) at 2.5 V V_{DD1}
Multiple UVLO options on V_{DD2}
- **Grade A: 4.4 V (typical) UVLO on V_{DD2}**
- **Grade B: 7.3 V (typical) UVLO on V_{DD2}**
- **Grade C: 11.3 V (typical) UVLO on V_{DD2}**

Precise timing characteristics
- **53 ns maximum isolator and driver propagation delay**

CMOS input logic levels
High common-mode transient immunity: >150 kV/µs
High junction temperature operation: 125°C
Default low output
Internal Miller clamp
Safety and regulatory approvals (pending)
- **UL recognition per UL 1577**
  - **5 kV rms for 1-minute withstand**
- **CSA Component Acceptance Notice 5A**
- **VDE certificate of conformity (pending)**
  - **DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12**
  - **V_{IORM} = 849 V peak**

Wide-body, 8-lead SOIC

APPLICATIONS

Switching power supplies
Isolated IGBT/MOSFET gate drives
Industrial inverters
Gallium nitride (GaN)/silicon carbide (SiC) power devices

GENERAL DESCRIPTION

The ADuM4121/ADuM4121-1[1] are 2 A isolated, single-channel drivers that employ Analog Devices, Inc.'s *i*Coupler® technology to provide precision isolation. The ADuM4121/ADuM4121-1 provide 5 kV rms isolation in the wide-body, 8-lead SOIC package. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as the combination of pulse transformers and gate drivers.

The ADuM4121/ADuM4121-1 operate with an input supply ranging from 2.5 V to 6.5 V, providing compatibility with lower voltage systems. In comparison to gate drivers that employ high voltage level translation methodologies, the ADuM4121/ADuM4121-1 offer the benefit of true, galvanic isolation between the input and the output.

The ADuM4121/ADuM4121-1 include an internal Miller clamp that activates at 2 V on the falling edge of the gate drive output, supplying the driven gate with a lower impedance path to reduce the chance of Miller capacitance induced turn on.

Options exists to allow the thermal shutdown to be enabled or disabled. As a result, the ADuM4121/ADuM4121-1 provide reliable control over the switching characteristics of insulated gate bipolar transistor (IGBT)/metal oxide semiconductor field, effect transistor (MOSFET) configurations over a wide range of switching voltages.

FUNCTIONAL BLOCK DIAGRAM

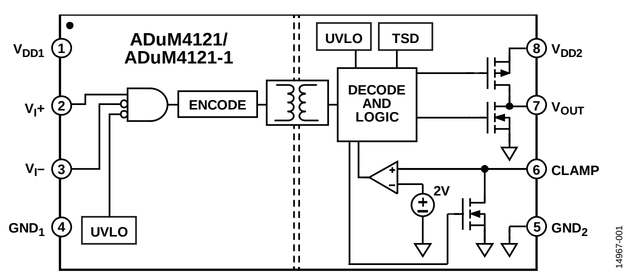

Figure 1.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,239. Other patents pending.

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REVISION HISTORY

10/2016—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Low-side voltages referenced to GND_1. High side voltages referenced to GND_2; 2.5 V ≤ V_{DD1} ≤ 6.5 V; 4.5 V ≤ V_{DD2} ≤ 35 V, T_J = −40°C to +125°C. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_J = 25°C, V_{DD1} = 5.0 V, V_{DD2}= 15 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
High Side Power Supply						
V_{DD2} Input Voltage	V_{DD2}	4.5		35	V	
V_{DD2} Input Current, Quiescent	$I_{DD2(Q)}$		2.3	2.7	mA	
Logic Supply						
V_{DD1} Input Voltage	V_{DD1}	2.5		6.5	V	
Input Current	I_{DD1}		3.6	5	mA	V_I+ = high, V_I− = low
Logic Inputs (V_I+, V_I−)						
Input Current	I_I+, I_I−	−1	0.01	+1	µA	
Input Voltage						
Logic High	V_{IH}	0.7 × V_{DD1}			V	2.5 V ≤ V_{DD1} ≤ 5 V
		3.5			V	V_{DD1} > 5 V
Logic Low	V_{IL}			0.3 × V_{DD1}	V	2.5 V ≤ V_{DD1} ≤ 5 V
				1.5	V	V_{DD1} > 5 V
UVLO						
V_{DD1}						
Positive-Going Threshold	$V_{VDD1UV+}$		2.45	2.5	V	
Negative-Going Threshold	$V_{VDD1UV-}$	2.3	2.35		V	
Hysteresis	$V_{VDD1UVH}$		0.1		V	
V_{DD2}						
Grade A						
Positive Going Threshold	$V_{VDD2UV+}$		4.4	4.5	V	
Negative Going Threshold	$V_{VDD2UV-}$	4.1	4.2		V	
Hysteresis	$V_{VDD2UVH}$		0.2		V	
Grade B						
Positive Going Threshold	$V_{VDD2UV+}$		7.3	7.5	V	
Negative Going Threshold	$V_{VDD2UV-}$	6.9	7.1		V	
Hysteresis	$V_{VDD2UVH}$		0.2		V	
Grade C						
Positive Going Threshold	$V_{VDD2UV+}$		11.3	11.6	V	
Negative Going Threshold	$V_{VDD2UV-}$	10.8	11.1		V	
Hysteresis	$V_{VDD2UVH}$		0.2		V	
Thermal Shutdown (TSD)						The ADuM4121-1 does not have TSD
Positive Edge	T_{TSD_POS}		155		°C	
Hysteresis	T_{TSD_HYST}		30		°C	
Internal NMOS Gate Resistance	R_{DSON_N}		0.6	1.6	Ω	Tested at 250 mA, V_{DD2} = 15 V
			0.6	1.6	Ω	Tested at 1 A, V_{DD2} = 15 V
Internal PMOS Gate Resistance	R_{DSON_P}		0.8	1.8	Ω	Tested at 250 mA, V_{DD2} = 15 V
			0.8	1.8	Ω	Tested at 1 A, V_{DD2} = 15 V
Internal Miller Clamp Resistance	R_{DSON_MILLER}		0.8	2	Ω	Tested at 200 mA, V_{DD2} = 15 V
Miller Clamp Voltage Threshold	V_{CLP_TH}	1.75	2	2.25	V	Referenced to GND_2, V_{DD2} = 15 V
Peak Current	I_{PK}		2.3		A	V_{DD2} = 12 V, 4 Ω gate resistance
SWITCHING SPECIFICATIONS						
Pulse Width	PW	50			ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON}[1] = R_{GOFF}[1] = 5 Ω
Propagation Delay						
Rising Edge[2]	t_{DLH}	22	32	42	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
Falling Edge[2]	t_{DHL}	30	38	53	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Skew[3]	t_{PSK}			22	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
Falling Edge[4]	t_{PSKHL}			12	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
Rising Edge[5]	t_{PSKLH}			15	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
Pulse Width Distortion	t_{PWD}		7	13	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
Output Rise/Fall Time (10% to 90%)	t_R/t_F	11	18	26	ns	C_L = 2 nF, V_{DD2} = 15 V, R_{GON} = R_{GOFF} = 5 Ω
Common-Mode Transient Immunity (CMTI)	|CM|					
Static CMTI[6]		150			kV/µs	V_{CM} = 1500 V
Dynamic CMTI[7]		150			kV/µs	V_{CM} = 1500 V

1 R_{GON} and R_{GOFF} are the external gate resistors in the test.
2 t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% threshold of the V_{OUT} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{Ox} signal. See Figure 24 for waveforms of the propagation delay parameters.
3 t_{PSK} is the magnitude of the worst case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 24 for waveforms of the propagation delay parameters.
4 t_{PSKHL} is the magnitude of the worst case difference in t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 24 for waveforms of the propagation delay parameters.
5 t_{PSKLH} is the magnitude of the worst case difference in t_{DLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 24 for waveforms of the propagation delay parameters.
6 Static common-mode transient immunity (CMTI) is defined as the largest dv/dt between GND_1 and GND_2, with inputs held either high or low, such that the output voltage remains either above 0.8 × V_{DD2} for output high or 0.8 V for output low. Operation with transients above recommended levels can cause momentary data upsets.
7 Dynamic common-mode transient immunity (CMTI) is defined as the largest dv/dt between GND_1 and GND_2 with the switching edge coincident with the transient test pulse. Operation with transients above the recommended levels can cause momentary data upsets.

REGULATORY INFORMATION

The ADuM4121/ADuM4121-1 are pending approval by the organizations listed in Table 2.

Table 2.

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
UL1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Certified under CQC11-471543-2012
Single Protection, 5000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2:	Reinforced insulation, 849 V peak, V_{IOSM} = 10 kV peak	GB4943.1-2011
	Basic insulation at 800 V rms (1131 V peak)	Basic insulation 849 V peak, V_{IOSM} = 16 kV peak	Basic insulation at 800 V rms (1131 V peak)
	Reinforced insulation at 400 V rms (565 V peak)		Reinforced insulation at 400 V rms (565 V peak)
	IEC 60601-1 Edition 3.1:		
	Basic insulation (1 MOPP), 500 V rms (707 V peak)		
	Reinforced insulation (2 MOPP), 250 V rms (1414 V peak)		
	CSA 61010-1-12 and IEC 61010-1 third edition		
	Basic insulation at: 600 V rms mains, 800 V secondary (1089 V peak)		
	Reinforced insulation at: 300 V rms mains, 400 V secondary (565 V peak)		
File E214100	File 205078	File 2471900-4880-0001	File (pending)

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input Side to High-Side Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input Side to High-Side Output)[1]	C_{I-O}		2.0		pF	
Input Capacitance	C_I		4.0		pF	
Junction to Top Characterization Parameter	Ψ_{JT}		7.3		°C/W	4-layer PCB

1 The device is considered a two-terminal device: Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.3 min	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		25.5 min	μm	Minimum distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 3
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits.

Table 5. VDE Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 600 V rms			I to IV	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd (m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd (m)}$	1592	V peak
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd (m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd (m)}$	1274	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd (m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd (m)}$	1019	V peak
Highest Allowable Overvoltage		V_{IOTM}	7000	V peak
Surge Isolation Voltage Basic	VPEAK = 16 kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	16,000	V peak
Surge Isolation Voltage Reinforced	VPEAK = 16 kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	10,000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Safety Total Dissipated Power		P_S	1.2	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

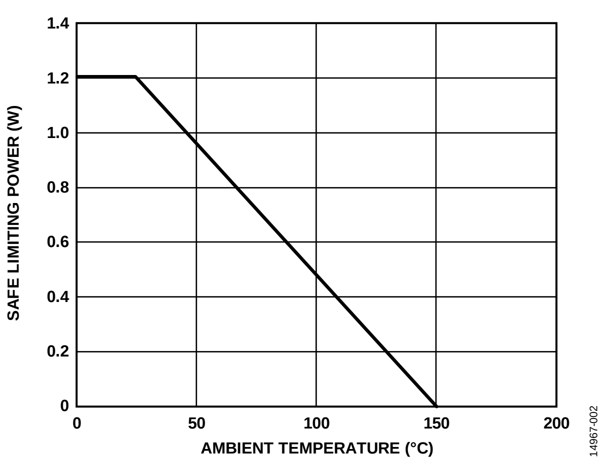

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Value
Operating Temperature Range (T_J)	−40°C to +125°C
Supply Voltages	
V_{DD1} to GND_1	2.5 V to 6.5 V
V_{DD2} to GND_2	4.5 V to 35 V

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
Storage Temperature Range (T_{ST})	−55°C to +150°C
Junction Operating Temperature Range (T_J)	−40°C to +125°C
Supply Voltages	
V_{DD1} to GND_1	−0.3 V to +7 V
V_{DD2} to GND_2	−0.3 V to +40 V
Input Voltages	
V_I+, V_I−[1]	−0.3 V to +7 V
V_{CLAMP}[2]	−0.3 V to V_{DD2} + 0.3 V
Output Voltages	
V_{OUT}[2]	−0.3 V to V_{DD2} + 0.3 V
Common-Mode Transients (|CM|)[3]	−200 kV/μs to +200 kV/μs

[1] Rating assumes V_{DD1} is above 2.5 V. V_I+ and V_I− are rated up to 6.5 V when V_{DD1} is unpowered.
[2] Referenced to GND_2, maximum of 40 V.
[3] |CM| refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the Absolute Maximum Rating can cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is thermal resistance, junction to ambient (°C/W).

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
RI-8-1[1]	104.2	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on a 4-layer PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 9. Maximum Continuous Working Voltage[1]

Parameter	Rating	Unit	Constraint
AC Voltage			
Bipolar Waveform			
Basic Insulation	849	V peak	50-year minimum insulation lifetime
Reinforced Insulation	789	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Unipolar Waveform			
Basic Insulation	1698	V peak	50-year minimum insulation lifetime
Reinforced Insulation	849	V peak	50-year minimum insulation lifetime
DC Voltage			
Basic Insulation	1118	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Reinforced Insulation	558	V peak	Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1

[1] Maximum continuous working voltage refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 10. Truth Table

V_I−	V_I+	V_{DD1} State	V_{DD2} State	V_{OUT} Output
Don't care	Low	Powered	Powered	Low
Low	High	Powered	Powered	High
High	Don't care	Powered	Powered	Low
Don't care	Don't care	Unpowered	Powered	Low
Don't care	Don't care	Powered	Unpowered	Low[1]

[1] The output is low, but not actively driven because the device is not powered.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

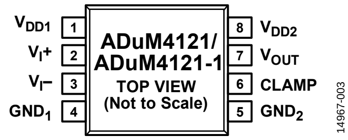

Figure 3. Pin Configuration

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_I+	Noninverting Gate Drive Logic Input.
3	$V_I−$	Inverting Gate Drive Logic Input.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	CLAMP	Miller Clamp and Gate Voltage Sense. Connect this pin directly to the gate being driven.
7	V_{OUT}	Gate Drive Output. Connect this pin to the gate being driven through an external series resistor.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

TYPICAL PERFORMANCE CHARACTERISTICS

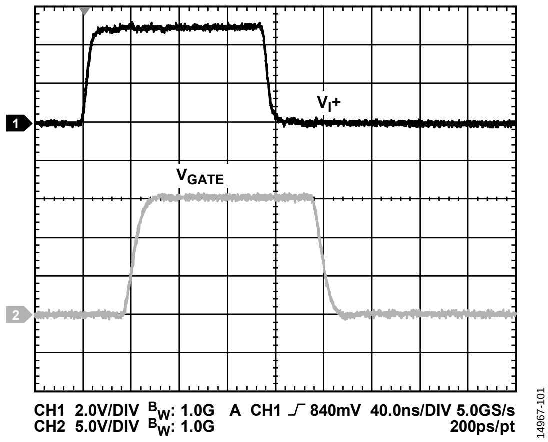

Figure 4. V_I+ to V_{GATE} Waveform for 2 nF Load, 3.9 Ω Series Gate Resistor, V_{DD2} = 15 V (V_{GATE} Is the Voltage After a Gate Resistor)

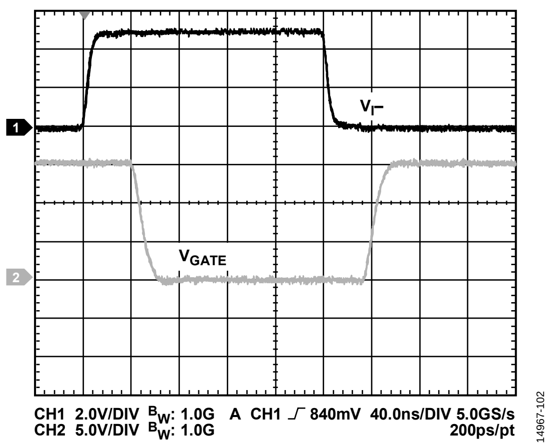

Figure 5. V_I– to V_{GATE} Waveform for 2 nF Load, 3.9 Ω Series Gate Resistor, V_{DD2} = 15 V

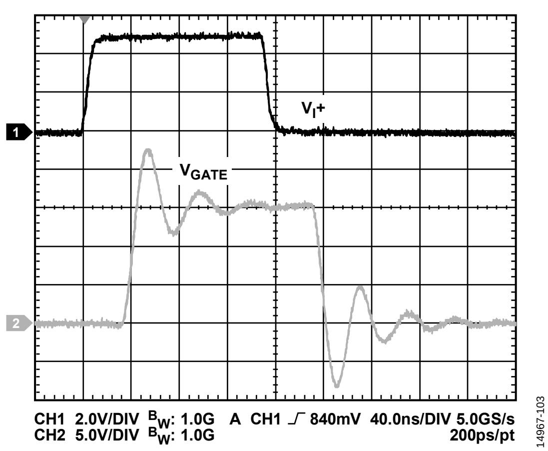

Figure 6. V_I+ to V_{GATE} Waveform for 2 nF Load, 0 Ω Series Gate Resistor, V_{DD2} = 15 V

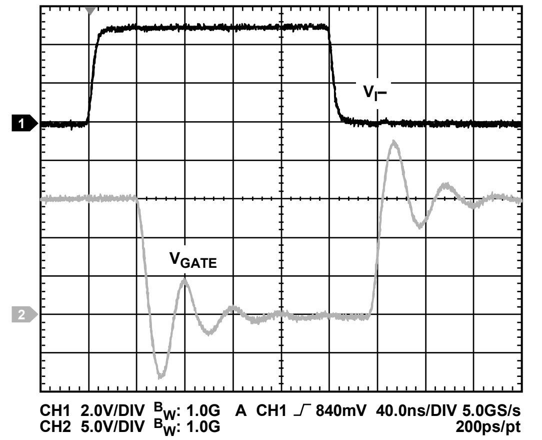

Figure 7. V_I– to V_{GATE} Waveform for 2 nF Load, 0 Ω Series Gate Resistor, V_{DD2} = 15 V

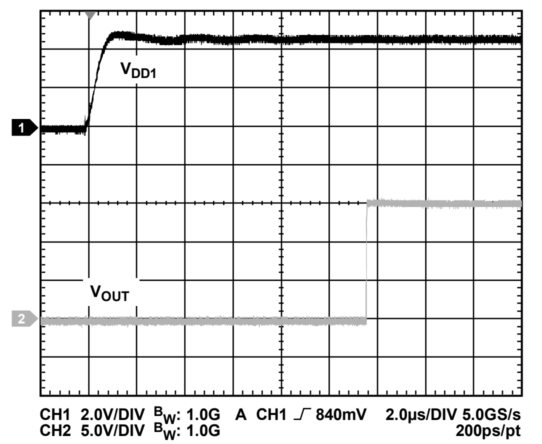

Figure 8. Typical V_{DD1} Delay to Output Waveform, V_I+ = V_{DD1}, V_I– = GND_1

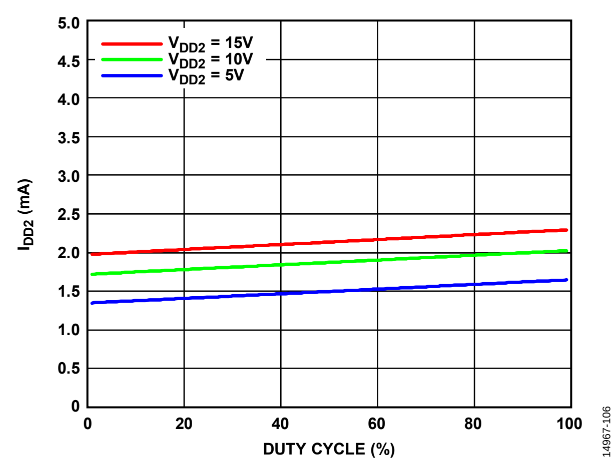

Figure 9. I_{DD2} vs. Duty Cycle, V_{DD1} = 5 V, Switching Frequency (f_{SW}) = 10 kHz, 2 nF Load

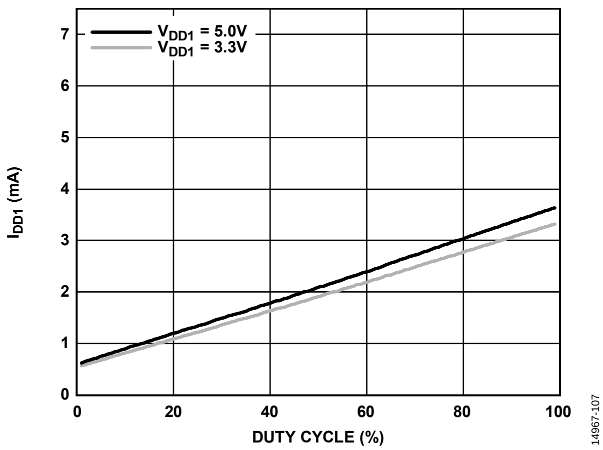

Figure 10. I_{DD1} vs. Duty Cycle, f_{SW} = 10 kHz, 2 nF Load

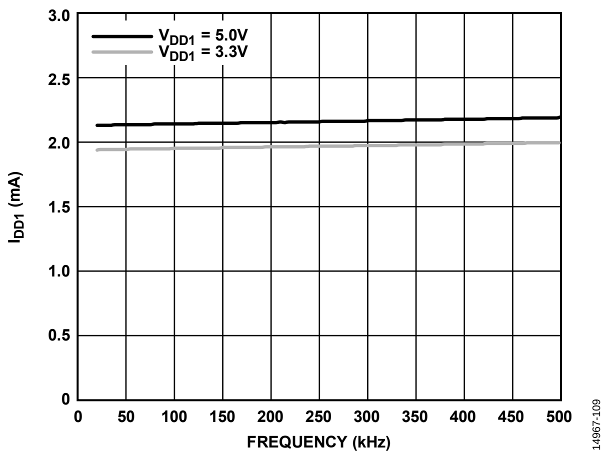

Figure 11. I_{DD1} vs. Frequency

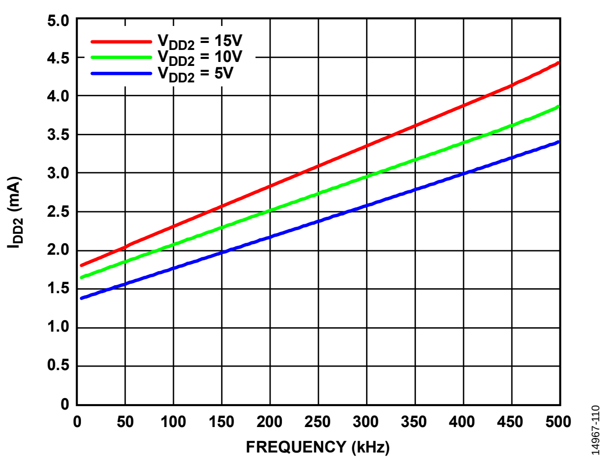

Figure 12. I_{DD2} vs. Frequency with 2 nF Load

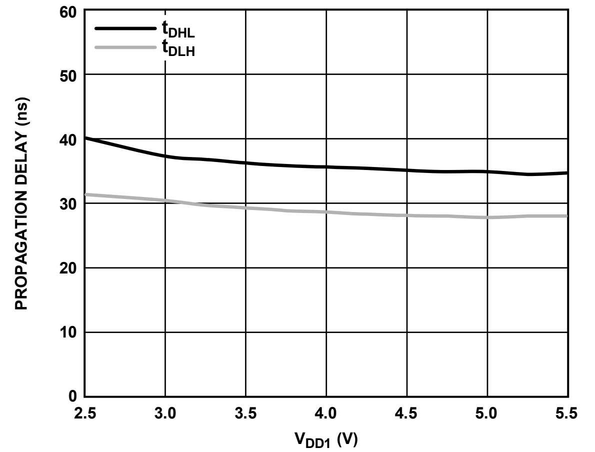

Figure 13. Propagation Delay vs. V_{DD1}, V_{DD2} = 15 V, 2 nF Load, 0 Ω Gate Resistor

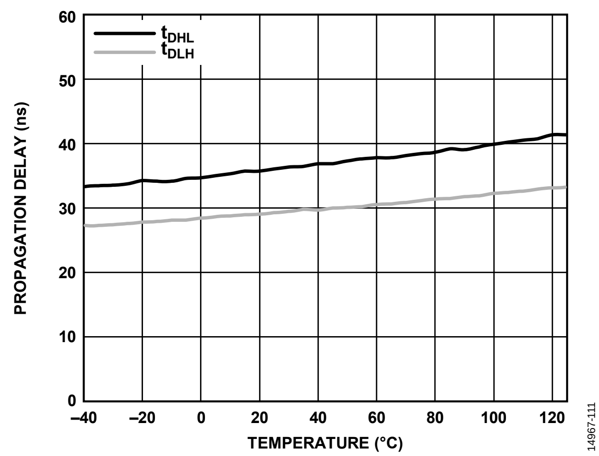

Figure 14. Propagation Delay vs. Temperature, 2 nF Load

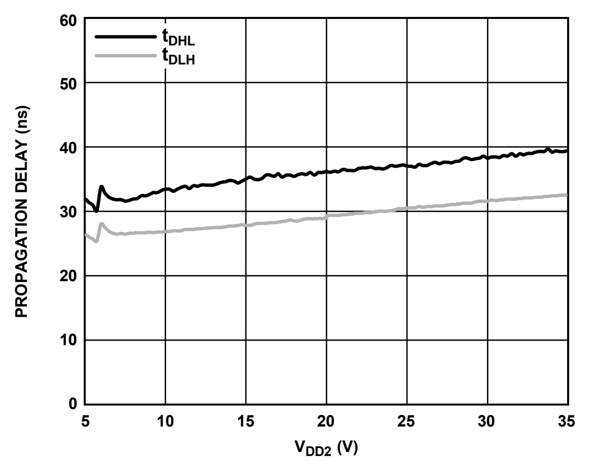

Figure 15. Propagation Delay vs. V_{DD2}, 2 nF Load

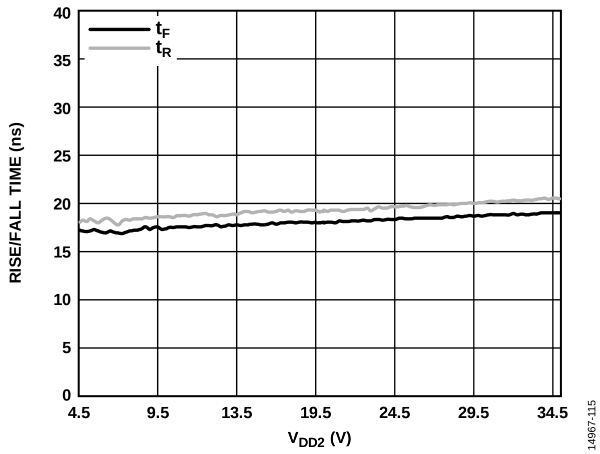

Figure 16. Rise and Fall Time vs. V_{DD2}, 2 nF Load, 3.9 Ω Resistor

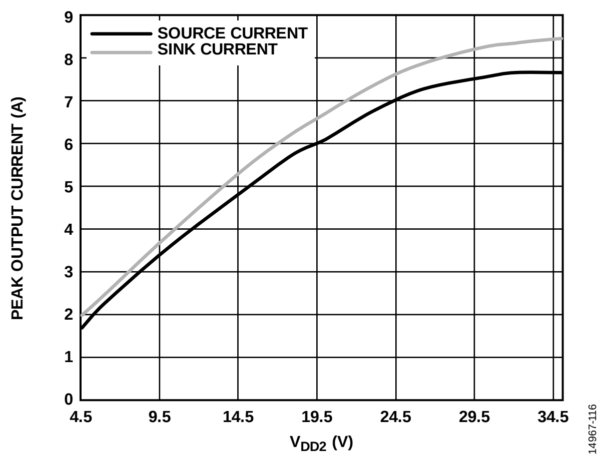

Figure 17. Peak Output Current vs. V_{DD2}, 2 Ω Series Resistance

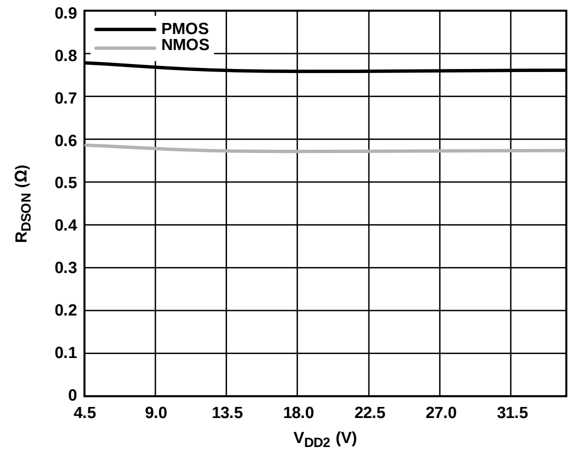

Figure 18. Typical Output Resistance (R_{DSON}) vs. V_{DD2}

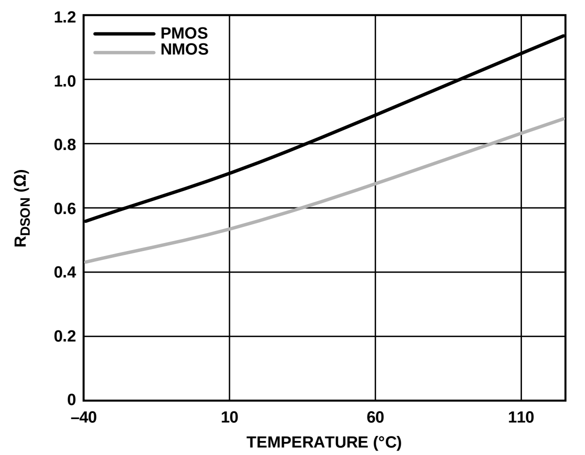

Figure 19. Typical Output Resistance (R_{DSON}) vs. Temperature, V_{DD2} = 15 V

THEORY OF OPERATION

Gate drivers are required in situations where fast rise times of switching device gates are desired. The gate signal for most enhancement type power devices are referenced to a source or emitter node. The gate driver must be able to follow this source or emitter node, necessitating isolation between the controlling signal and the output of the gate driver in topologies where the source or emitter nodes swing, such as a half bridge. Gate switching times are a function of drive strength of the gate driver. Buffer stages before a CMOS output reduce total delay time andincrease the final drive strength of the driver.

The ADuM4121/ADuM4121-1 achieve isolation between the control side and output side of the gate driver by means of a high frequency carrier that transmits data across the isolation barrier using *i*Coupler chip scale transformer coils separated by layers of polyimide isolation. The encoding scheme used by the ADuM4121/ADuM4121-1 is a positive logic on/off keying (OOK), meaning a high signal is transmitted by the presence of the carrier frequency across the *i*Coupler chip scale transformer coils. Positive logic encoding ensures that a low signal is seen on the output when the input side of the gate driver is unpowered. A low state is the most common safe state in enhancement mode power devices, driving in situations where shoot through conditions can exist. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference. Radiated emissions are minimized with a spread spectrum OOK carrier and other techniques such as differential coil layout. Figure 20 illustrates the encoding used by the ADuM4121/ADuM4121-1.

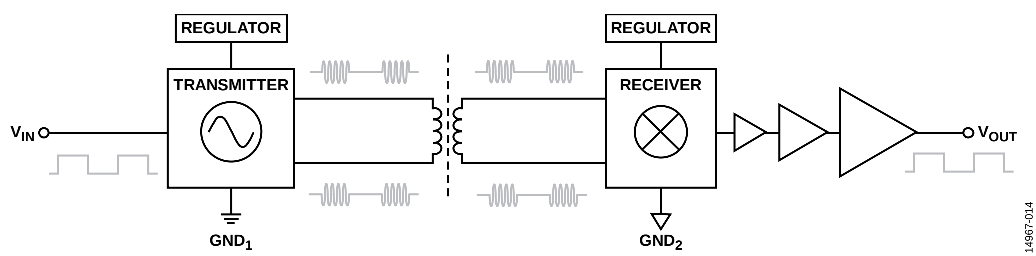

Figure 20. Operational Block Diagram of OOK Encoding

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM4121/ADuM4121-1 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins, as shown in Figure 21. Use a small ceramic capacitor with a value between 0.01 µF and 0.1 µF to provide a good high frequency bypass. On the output power supply pin, V_{DD2}, it is recommended to also add a 10 µF capacitor to provide the charge required to drive the gate capacitance at the ADuM4121/ADuM4121-1 outputs. On the output supply pin, the bypass capacitor use of vias must be avoided or multiple vias must be employed to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin must not exceed 20 mm.

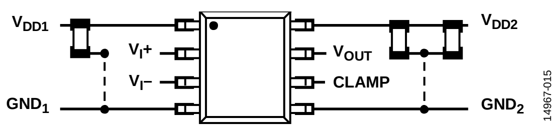

Figure 21. Recommended PCB Layout

V_I+ and V_I– Operation

The ADuM4121/ADuM4121-1 have two drive inputs, V_I+ and V_I–, to control the IGBT gate drive signals, V_{OUT}. Both the V_I+ and V_I– pins use CMOS logic level inputs. Control the input logic of the V_I+ and V_I– pins by either asserting the V_I+ pin high, or the V_I– pin low. With the V_I– pin low, the V_I+ pin accepts positive logic. If V_I+ is held high, the V_I– pin accepts negative logic.

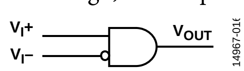

Figure 22. V_I+ and V_I– Block Diagram

See Figure 23 for more details.

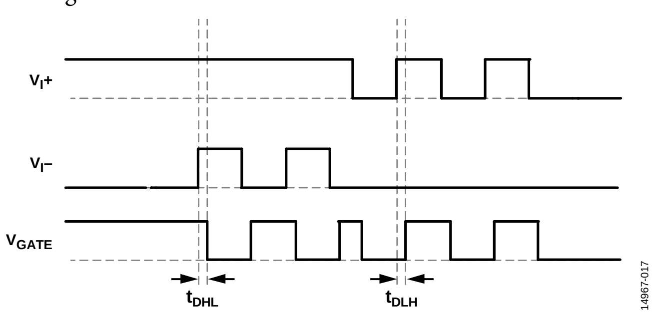

Figure 23. V_I+ and V_I– Timing Diagram

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time a logic signal takes to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output. The ADuM4121/ADuM4121-1 specify t_{DLH} (see Figure 24) as the time between the rising input high logic threshold, V_{IH}, to the output rising 10% threshold. Likewise, the falling propagation delay, t_{DHL}, is defined as the time between the input falling logic low threshold, V_{IL}, and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, as is the industry standard for gate drivers.

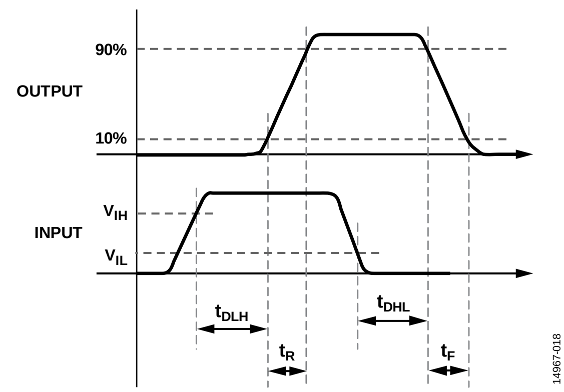

Figure 24. Propagation Delay Parameters

Channel to channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM4121/ADuM4121-1 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM4121/ADuM4121-1 components operating under the same conditions.

UNDERVOLTAGE LOCKOUT (UVLO)

The ADuM4121/ADuM4121-1 have UVLO protections for both the primary and secondary side of the device. If either the primary or secondary side voltages are below the falling edge UVLO, the device outputs a low signal. After the ADuM4121/ADuM4121-1 are powered above the rising edge UVLO threshold, the device outputs the signal found at the input. Hysteresis is built into the UVLO to account for small voltage source ripple. The primary side UVLO thresholds are common among all models. There are three options for the secondary output UVLO thresholds, listed in Table 12.

Table 12. List of Model Options

Model Number	TSD	UVLO (V)
ADuM4121ARIZ	Yes	4.5
ADuM4121BRIZ	Yes	7.5
ADuM4121CRIZ	Yes	11.6
ADuM4121ARIZ-1	No	4.5
ADuM4121BRIZ-1	No	7.5
ADuM4121CRIZ-1	No	11.6

OUTPUT LOAD CHARACTERISTICS

The ADuM4121/ADuM4121-1 output signals depend on the characteristics of the output load, which is typically an N channel MOSFET. Model the driver output response to an N channel MOSFET load with a switch output resistance (R_{SW}), an inductance due to the printed circuit board trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate to source capacitance (C_{GS}), as shown in Figure 25.

R_{SW} is the switch resistance of the internal ADuM4121/ADuM4121-1 driver output, which is about 1.5 Ω. R_{GATE} is the intrinsic gate resistance of the MOSFET or IGBT and any external series resistance. A MOSFET or IGBT that requires a 2 A gate driver has a typical intrinsic gate resistance of about 1 Ω and a gate to source capacitance, C_{GS}, of between 2 nF and 10 nF. L_{TRACE} is the inductance of the printed circuit board trace, typically a value of 5 nH or less for a well designed layout with a very short and wide connection from the ADuM4121/ADuM4121-1 output to the gate of the MOSFET or IGBT.

The following equation defines the quality factor, Q, of the RLC circuit, which indicates how the ADuM4121/ADuM4121-1 output responds to a step change. For a well damped output, Q is less than one. Adding a series gate resistance dampens the output response.

$$Q = \frac{1}{(R_{SW} + R_{GATE})} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}}$$

Output ringing is reduced by adding a series gate resistance to dampen the response. The waveforms shown in Figure 4 show a correctly damped example with a 2 nF load and a 3.9 Ω external series gate resistor. The waveforms shown in Figure 6 show an underdamped example with a 2 nF load and a 0 Ω external series gate resistor.

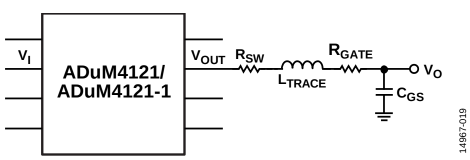

Figure 25. RLC Model of the Gate of an N Channel MOSFET

Miller Clamp

The ADuM4121/ADuM4121-1 have an integrated Miller clamp to reduce voltage spikes on the MOSFET or IGBT gate caused by the Miller capacitance during shutoff of the MOSFET or IGBT. When the input gate signal requests the IGBT to be turned off (driven low), the Miller clamp MOSFET is off initially. After the voltage on the gate sense pin crosses the 2 V internal voltage reference that is referenced to GND_2, the internal Miller clamp latches on for the remainder of the off time of the MOSFET or IGBT, creating a second low impedance current path for the gate current to follow. The Miller clamp switch remains on until the input drive signal changes from low to high. An example waveform of the timings is shown in Figure 26.

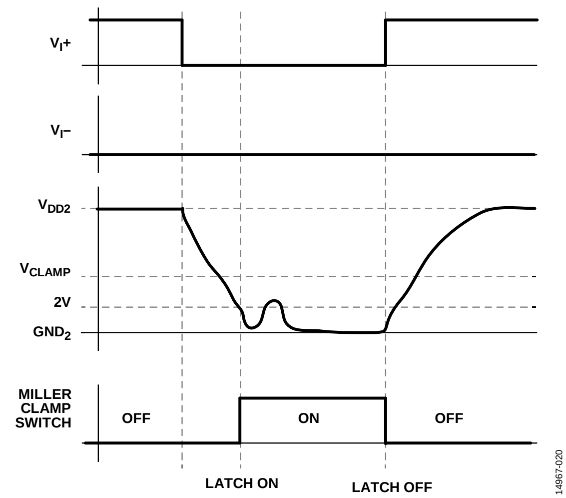

Figure 26. Miller Clamp Example

POWER DISSIPATION

During the driving of a MOSFET or IGBT gate, the driver must dissipate power. This power is not insignificant, and can lead to thermal shutdown (TSD) if considerations are not made. The gate of an IGBT can be approximately simulated as a capacitive load. Due to Miller capacitance and other nonlinearities, it is common practice to take the stated input capacitance of a given MOSFET or IGBT, C_{ISS}, and multiply it by a factor of 3 to 5 to arrive at a conservative estimate of the approximate load being driven. With this value, the estimated total power dissipation in the system due to switching action is given by

$$P_{DISS} = C_{EST} \times (V_{DD2} - GND_2)^2 \times f_{SW}$$

where:

$C_{EST} = C_{ISS} \times 5$.

f_{SW} is the switching frequency of the IGBT.

Alternately, the gate charge can be used as follows:

$$P_{DISS} = Q_G \times (V_{DD2} - GND_2) \times f_{SW}$$

where Q_G is the total gate charge of the device being driven.

This power dissipation is shared between the internal on resistances of the internal gate driver switches, and the external gate resistances, R_{GON} and R_{GOFF}. The ratio of the internal gate resistances to the total series resistance allows the calculation of losses seen within the ADuM4121/ADuM4121-1 devices. The following calculations for the ADuM4121also apply to the ADuM4121-1.

$$P_{DISS\_ADuM4121} = P_{DISS} \times 0.5(R_{DSON\_P}/(R_{GON} + R_{DSON\_P}) + 0.5(R_{DSON\_N}/(R_{GOFF} + R_{DSON\_N}))$$

Taking this power dissipation found inside the chip, and multiplying it by the θ_{JA} gives the rise above ambient temperature that the ADuM4121 experiences.

$$T_{ADuM4121} = \theta_{JA} \times P_{DISS\_ADuM4121} + T_{AMB}$$

For the device to remain within specification, $T_{ADUM4121}$ must not exceed 125°C. If $T_{ADuM4121}$ exceeds the TSD rising edge, the device enters TSD, and the output remains low until the TSD falling edge is crossed. The ADuM4121-1 does not include thermal shutdown.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM4121/ADuM4121-1.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 9 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition, and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM4121/ADuM4121-1 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 27, Figure 28, and Figure 29 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *i*Coupler products and is the 50-year operating lifetime that Analog Devices recommends for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This unipolar ac or dc voltage operation allows operation at higher working voltages while still achieving a 50-year service life. Any cross insulation voltage waveform that does not conform to Figure 28 or Figure 29 must be treated as a bipolar ac waveform, and its peak voltage must be limited to the 50-year lifetime voltage value listed in Table 9.

Note that the voltage presented in Figure 28 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

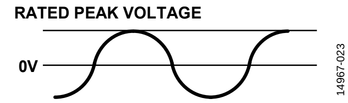

Figure 27. Bipolar AC Waveform

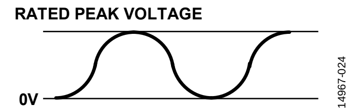

Figure 28. Unipolar AC Waveform

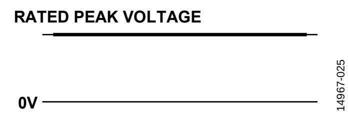

Figure 29. DC Waveform

TYPICAL APPLICATIONS

A typical application of the ADuM4121/ADuM4121-1 is shown in Figure 30. An external gate resistor, R_G, controls the rise and fall times of the gate voltage seen at the device being driven. An optional turn off path is available for further tuning by creating a parallel path through D1. An example bootstrap setup is shown in Figure 31. In both of these examples, the V_I- pins are tied low, creating a positive logic input to the gate drivers. In this manner, the V_I- pins act as a disable pin, bringing the outputs low if the V_I- pins are brought high.

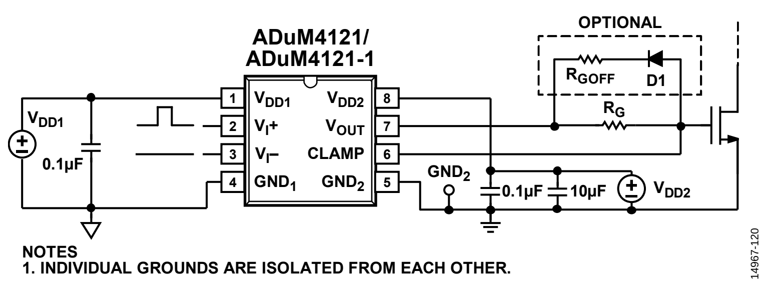

Figure 30. Typical Application Diagram, Single Device

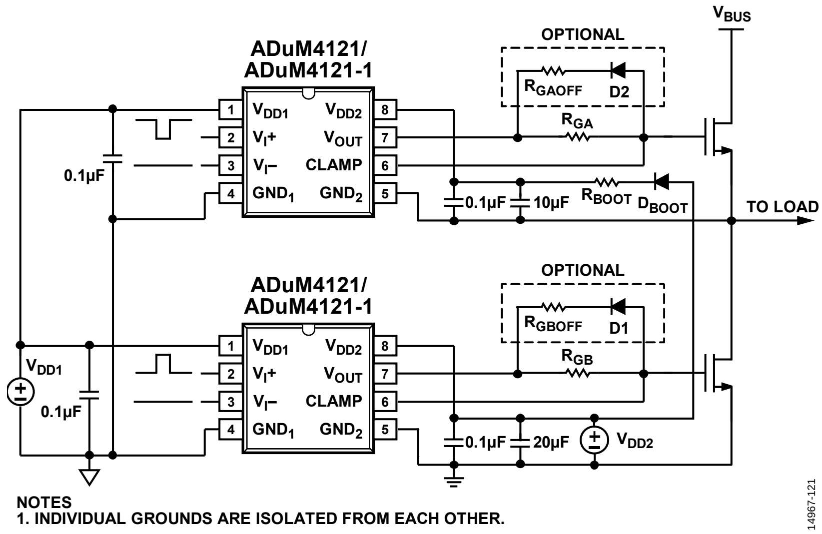

Figure 31. Typical Application Diagram, Bootstrap Setup

OUTLINE DIMENSIONS

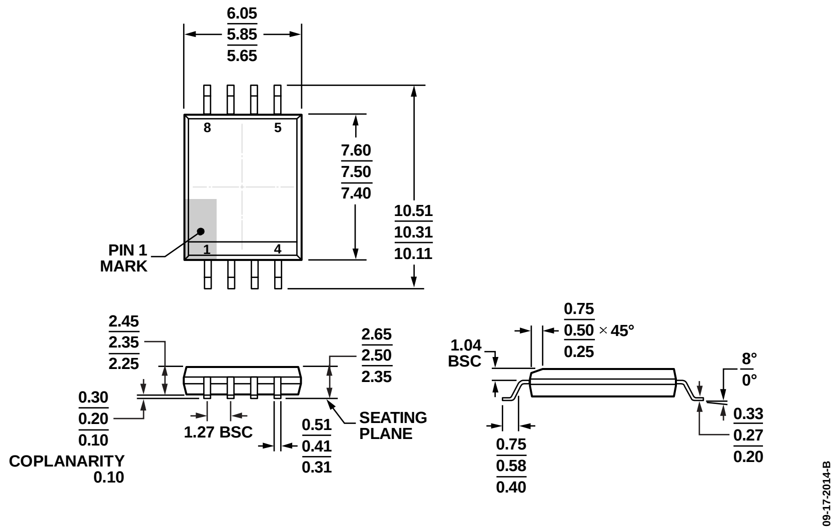

Figure 32. 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	No. of Channels	Output Peak Current (A)	Thermal Shutdown	Minimum Output Voltage (V)	Temperature Range	Package Description	Package Option
ADuM4121ARIZ	1	2	Yes	4.5	−40°C to +125°C	8-Lead SOIC_IC	RI-8-1
ADuM4121ARIZ-RL	1	2	Yes	4.5	−40°C to +125°C	8-Lead SOIC_IC, 13" Tape and Reel	RI-8-1
ADuM4121BRIZ	1	2	Yes	7.5	−40°C to +125°C	8-Lead SOIC_IC	RI-8-1
ADuM4121BRIZ-RL	1	2	Yes	7.5	−40°C to +125°C	8-Lead SOIC_IC, 13" Tape and Reel	RI-8-1
ADuM4121CRIZ	1	2	Yes	11.6	−40°C to +125°C	8-Lead SOIC_IC	RI-8-1
ADuM4121CRIZ-RL	1	2	Yes	11.6	−40°C to +125°C	8-Lead SOIC_IC, 13" Tape and Reel	RI-8-1
ADuM4121-1ARIZ	1	2	No	4.5	−40°C to +125°C	8-Lead SOIC_IC	RI-8-1
ADuM4121-1ARIZ-RL	1	2	No	4.5	−40°C to +125°C	8-Lead SOIC_IC, 13" Tape and Reel	RI-8-1
ADuM4121-1BRIZ	1	2	No	7.5	−40°C to +125°C	8-Lead SOIC_IC	RI-8-1
ADuM4121-1BRIZ-RL	1	2	No	7.5	−40°C to +125°C	8-Lead SOIC_IC, 13" Tape and Reel	RI-8-1
ADuM4121-1CRIZ	1	2	No	11.6	−40°C to +125°C	8-Lead SOIC_IC	RI-8-1
ADuM4121-1CRIZ-RL	1	2	No	11.6	−40°C to +125°C	8-Lead SOIC_IC, 13" Tape and Reel	RI-8-1
EVAL-ADuM4121EBZ	1	2	Yes	4.5	−40°C to +125°C	Evaluation Board	RI-8-1
EVAL-ADuM4121-1EBZ	1	2	No	4.5	−40°C to +125°C	Evaluation Board	RI-8-1

[1] Z = RoHS Compliant Part.

D14967-0-10/16(0)

ООО «ЛайфЭлектроникс» "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

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