ANALOG DEVICES

HMC1034LP6GE

v01.0312

CLOCK GENERATOR WITH FRACTIONAL-N PLL & INTEGRATED VCO, 125 - 3000 MHz

RoHS✓
EARTH FRIENDLY

Typical Applications

• 10G/40G/100G Optical Modules, Transponders, Line Cards

• OTN and SONET/SDH Applications

• 1G/10G Ethernet Line Cards

• High Frequency Processor Clocks

• Low Jitter SAW Oscillator Replacement

• Fiber Channel Interface Clocks

• Cellular/4G Infrastructure

• DDS Replacement

• 10G Optical Modules, Transponders, Line Cards

Features

Frequency Range: 125 - 3000 MHz

78 fs RMS Jitter Generation (Typical)

Exceeds G.8251 & GR-253-CORE Jitter Specifications

-165 dBc/Hz Phase Noise floor

Maximum Phase Detector Rate 100 MHz

Figure of Merit (FOM) -227 dBc/Hz

24-Bit Step Size, Resolution 3 Hz Typical

Exact Frequency Mode

Built-in Digital Self Test

40 Lead 6x6mm SMT Package: 36mm^2

Functional Diagram

HMC1034LP6GE

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General Description

The HMC1034LP6GE is a low-noise, wide-band clock generator IC with a fractional-N Phase Locked Loop (PLL) that features an integrated Voltage Controlled Oscillator (VCO). The device provides differential clock outputs between 125MHz and 3GHz range. The HMC1034LP6GE features low noise Phase Detector (PD) and Delta-Sigma modulator, capable of operating at up to 100MHz, permit wider loop-bandwidths with excellent spectral performance.

The HMC1034LP6GE features industry leading phase noise and jitter performance, across the operating range, that enable it to improve link level jitter performance, Bit-Error-Rates (BER) and eye diagram metrics. The superior noise floor (<-165dBc/Hz) makes the HMC1034LP6GE an ideal source for a variety of applications –such as clock references for high speed data converters, physical layer devices (PHY), serializer/deserializer (SERDES) circuits, FPGAs and processors. The HMC1034LP6GE can also be used as an LO for 10G/40G/100G optical modules and transponders, as well as primary reference clock for 10G/40G/100G line cards, and for jitter attenuation and frequency translation.

The differential output of the HMC1034LP6GE includes a 2-bit output amplitude control which may be set via the SPI serial programming interface, and an output Mute function. The Delta-Sigma Modulator of the HMC1034LP6GE features Hittite's Exact Frequency Mode, which enables users to generate output frequencies with close to 0Hz frequency error.

For theory of operation and register map refer to the "PLLs with Integrated VCOs - RF VCOs Operating Guide". To view the Operating Guide, please visit www.hittite.com and choose HMC1034LP6GE from the "Search by Part Number" pull down menu.

Electrical Specifications, VPPCP, VDDLS, VCC1, VCC2 = 5V; RVDD, AVDD, DVDD3V, VCCPD, VCCHF, VCCPS = 3.3V Min & Max Specified across Temperature -40 °C to 85 °C

Parameter	Condition	Min.	Typ.	Max.	Units
RF Output Characteristics					
Output Frequency		125		3000	MHz
Output Specifications					
Output Voltage	Single-Ended Swing (peak-to-peak), 50 Ohm termination	0.25		1.35	Vpp
Output Amplitude Control	Gain Setting = 00, F=800 MHz		300		mVpp
	Gain Setting = 01, F=800 MHz		450		mVpp
	Gain Setting = 10, F=800 MHz		685		mVpp
	Gain Setting = 11, F=800 MHz		1.1		Vpp
Output Common Mode Voltage		AC Coupling Recommended			
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,...,62	1		62	
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional Nominal Divide Ratio Varies (-3 / +4) Dynamically Max	20		524,283	
REF Input Characteristics					
Max Ref Input Frequency				350	MHz
Ref Input Voltage	AC Coupled [1]	1	2	3.3	Vp-p
Ref Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	

[1] Measured with 100 Ω external termination. See Hittite PLL w/ Integraged VCOs Operating Guide Reference Input Stage section for more details.

[2] Slew rate of greater or equal to 0.5 ns/V is recommended, see PLL with Integrated RF VCOs Operating Guide for more details. Frequency is guaranteed across process voltage and temperature from -40 °C to 85 °C.

[3] This maximum phase detector frequency can only be achieved if the minimum N value is respected. eg. In the case of fractional feedback mode, the maximum PFD rate = fvco/20 or 100 MHz, whichever is less.

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Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
Phase Detector (PD) [2]					
PD Frequency Fractional Mode B	[3]	DC		100	MHz
PD Frequency Fractional Mode A (and Register 6 [17:16] = 11)		DC		80	MHz
PD Frequency Integer Mode		DC		125	MHz
Charge Pump					
Output Current		0.02		2.54	mA
Charge Pump Gain Step Size			20		µA
PD/Charge Pump SSB Phase Noise	50 MHz Ref, Input Referred				
1 kHz			-143		dBc/Hz
10 kHz	Add 1 dB for Fractional		-150		dBc/Hz
100 kHz	Add 3 dB for Fractional		-153		dBc/Hz
Output Rise Time	Measured from 20% to 80% of Output Signal, F=800 MHz Gain Setting = 00			150	ps
	Measured from 20% to 80% of Output Signal, F=800 MHz Gain Setting = 11			250	ps
Output Fall Time	Measured from 80% to 20% of Output Signal, F=800 MHz Gain Setting = 00			150	ps
	Measured from 80% to 20% of Output Signal, F=800MHz Gain Setting = 11			250	ps
Output Duty Cycle	Measured at 50% of Output Signal. F=800 MHz	40		60	%
Logic Inputs					
Vsw	Switching threshold for logic levels	40	50	60	% DVDD
Logic Outputs					
VOH Output High Voltage			DVDD		V
VOL Output Low Voltage			0		V
Output Impedance		100		200	Ω
Maximum Load Current				1.5	mA
Power Supply Voltages					
3.3V Supplies	AVDD, VCCHF, VCCPS, VCCPD, RVDD,DVDD	3.0	3.3	3.5	V
5V Supplies	VPPCP, VDDCP, VCC1, VCC2	4.8	5	5.2	V
Power Supply Currents					
+5V Analog Charge Pump	VPPCP, VDDCP		8		mA
+5V VCO Core & VCO Buffer	fo/1 Mode VCC2		105		mA
	fo/N Mode VCC2		80		mA
+5V VCO Divider & RF/PLL Buffer	fo/1 Mode VCC1		25		mA
	fo/N Mode VCC1	80		100	mA
+3.3V	AVDD, VCCHF, VCCPS, VCCPD, RVDD, DVDD3V		52		mA
Power Down - Crystal Off	Reg 01h=0, Crystal Not Clocked		10		µA
Power Down - Crystal On, 100 MHz	Reg 01h=0, Crystal Clocked 100 MHz		5		mA
Power on Reset					

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Electrical Specifications (Continued)

Parameter	Condition	Min.	Typ.	Max.	Units
Typical Reset Voltage on DVDD			700		mV
Minimum DVDD Voltage for No Reset		1.5			V
Power on Reset Delay			250		µs
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-230		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-227		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz
Phase Jitter RMS	Measured at 622.08 MHz, Integration Bandwidth: 12 kHz to 20 MHz, 50 MHz reference, fractional mode		118		fs
Phase Jitter RMS	Measured at 800 MHz, Integration Bandwidth: 12 kHz to 20 MHz Charge Pump (CP) Current set at 2.54 mA, integer mode, 50 MHz reference		78		fs
Period Jitter RMS	Measured at 2.46 Hz, with digital sampling oscilloscope and precision timebase module. The total measured RMS period jitter of 377 fs includes both the HMC1034 and instrument noise. Further calculations estimate HMC1034 RMS period jitter of <150 fs.		<377		fs

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v01.0312

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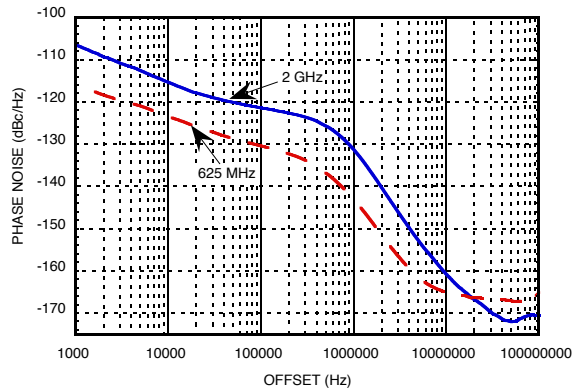### Figure 1. Typical Closed Loop Integer Phase Noise [1]

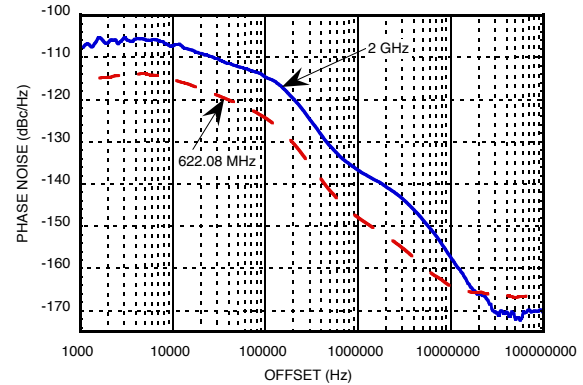### Figure 2. Typical Closed Loop Fractional Phase Noise [2]
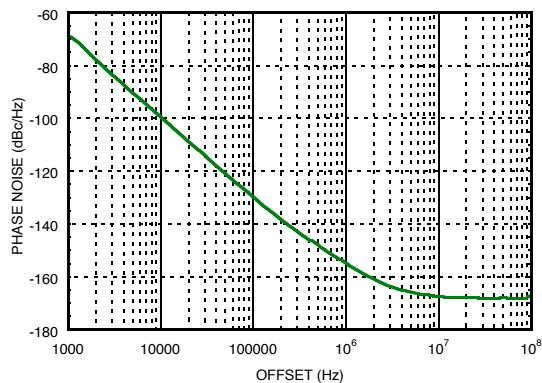

Figure 3. Free Running Phase Noise [3]

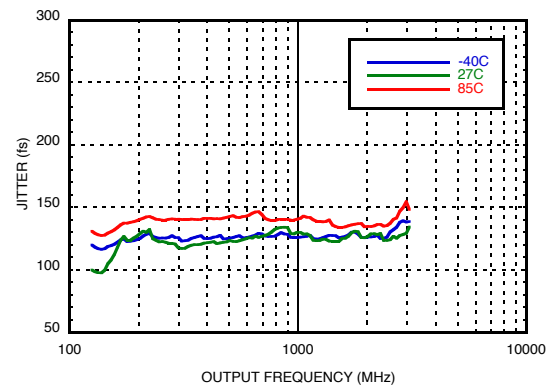### Figure 4. Integrated RMS Jitter [4]
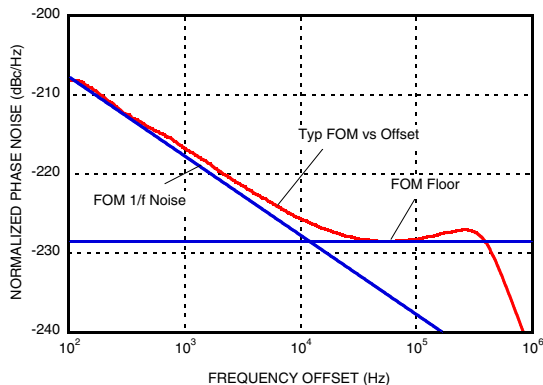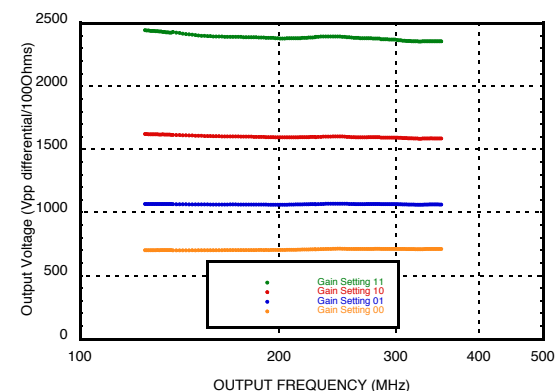

Figure 5. Figure of Merit

Figure 6. Typical Output Voltage

[1] The PN plot is measured with 50 MHz PFD (suntsu), Loop Filter Type 1 Refer to Loop Filter Configuration Table
[2] The PN plot is measured with 50 MHz PFD (suntsu), Loop Filter Type 2 Refer to Loop Filter Configuration Table
[3] Free Running Phase Noise @ fout = 350 MHz
[4] RMS Jitter data is measured in fractional mode with 100 kHz Loop bandwidth using 50 MHz reference frequency from 1 kHz to 20 MHa integration bandwidth.

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v01.0312

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Figure 7. Reference Input Sensitivity, Square Wave [5]
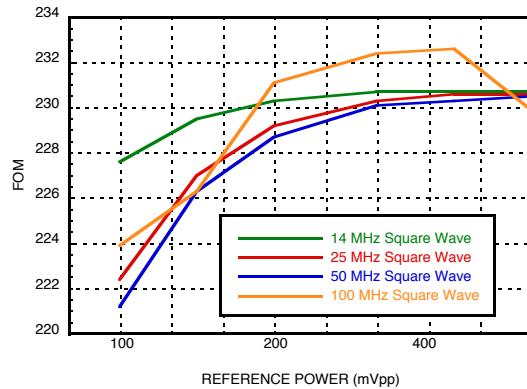

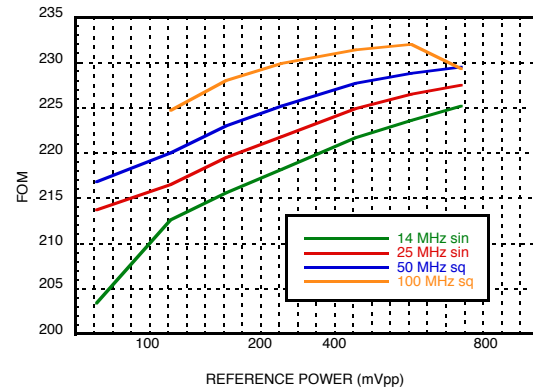### Figure 8. Reference Input Sensitivity Sinusoid Wave [6]

Figure 9. Output Rise Time
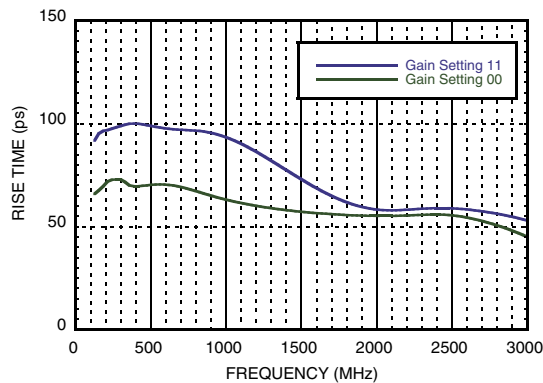
Figure 10. Output Fall Time
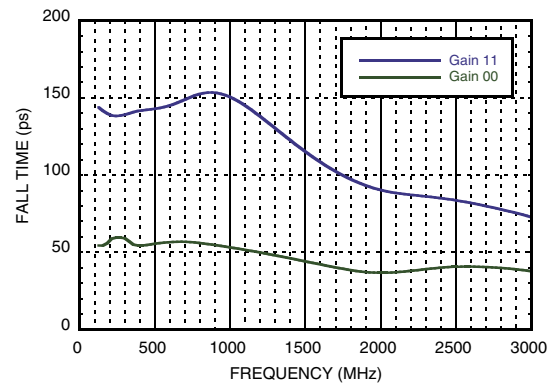
Loop Filter Configuration Table

Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	Loop Filter Design
250	3.9	15	N/A	N/A	2.7	0	0	
135	91	33	91	91	0.82	1	1	
74	150	27	220	220	0.82	1	1	

[5] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

[6] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

v01.0312

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Absolute Maximum Ratings

|	
AVDD, RVDD, DVDD3V, VCCPD, VCCHF, VCCPS	-0.3V to +3.6V
VPPCP, VDDCP, VCC1	-0.3V to +5.5V
VCC2	-0.3V to +5.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to 150°C
Maximum Junction Temperature	125 °C
Thermal Resistance (R_{TH}) (junction to ground paddle)	20 °C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Outline Drawing

NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC1034LP6GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H1034 XXXX

[1] 4-Digit lot number XXXX

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Pin Descriptions

Pin Number	Function	Description
1	AVDD	DC Power Supply for analog circuitry.
2, 5, 6, 8, 9, 11 - 14, 18 - 22, 24, 26, 34, 37, 38	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.
3	VPPCP	Power Supply for charge pump analog section
4	CP	Charge Pump Output
7	VDDLS	Power Supply for the charge pump digital section
10	RVDD	Reference Supply
15	XREFP	Reference Oscillator Input
16	DVDD3V	DC Power Supply for Digital (CMOS) Circuitry
17	CEN	Chip Enable. Connect to logic high for normal operation.
23	VTUNE	VCO Varactor. Tuning Port Input.
25	VCC2	VCO Analog Supply 2
27	VCC1	VCO Analog Supply 1
28	RF_N	Positive Output Signal (Differential)
29	RF_P	Negative Output Signal (Differential)
30	SEN	PLL Serial Port Enable (CMOS) Logic Input
31	SDI	PLL Serial Port Data (CMOS) Logic Input
32	SCK	PLL Serial Port Clock (CMOS) Logic Input
33	LD_SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO)
35	VCCHF	DC Power Supply for Analog Circuitry
36	VCCPS	DC Power Supply for Analog Prescaler
39	VCCPD	DC Power Supply for Phase Detector
40	BIAS	External bypass decoupling for precision bias circuits. Note: 1.920V ±20mV reference voltage (BIAS) is generated internally and cannot drive an external load. Must be measured with 10GΩ meter such as Agilent 34410A, normal 10MΩ DVM will read erroneously.

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Evaluation PCB
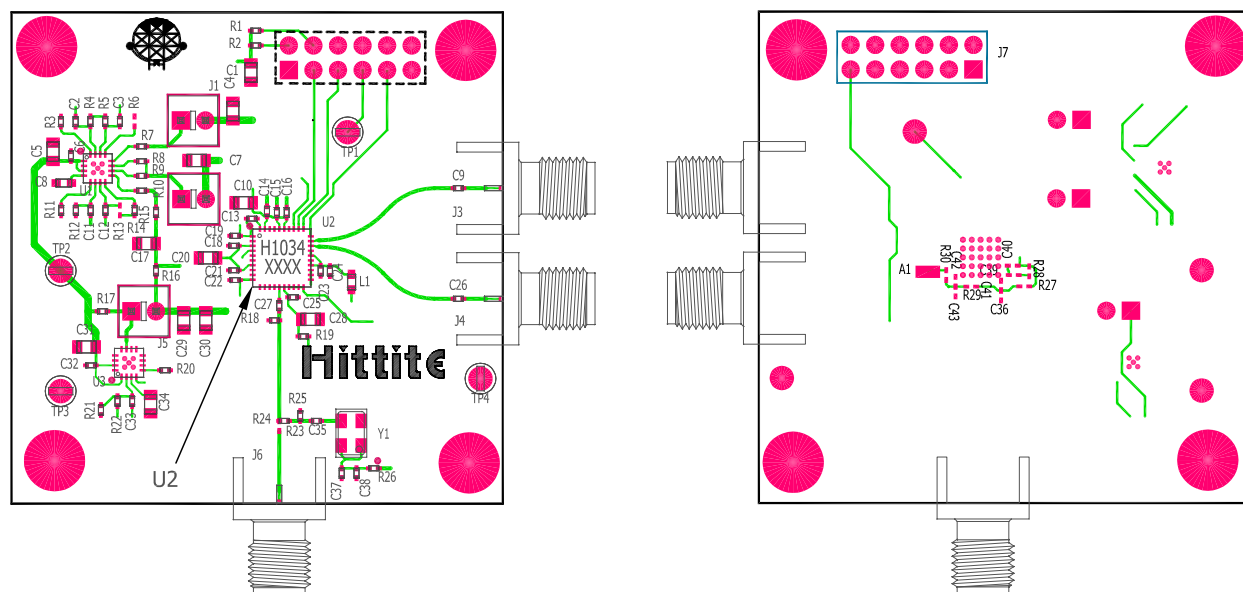
The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC1034LP6GE from the "Search by Part Number" pull down menu to view the product splash page.

Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	HMC1034LP6GE Evaluation PCB	EVAL01-HMC1034LP6GE
Evaluation Kit	HMC1034LP6GE Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC1034LP6GE

v01.0312

HMC1034LP6GE Output Stage

A representative schematic for the HMC1034LP6GE output stage is given in Figure 10 below. The differential output buffer features adjustable amplitudes which can be set by the "Gain Setting" register values. The typical output amplitudes that correspond to each setting are provided in Figure 6.
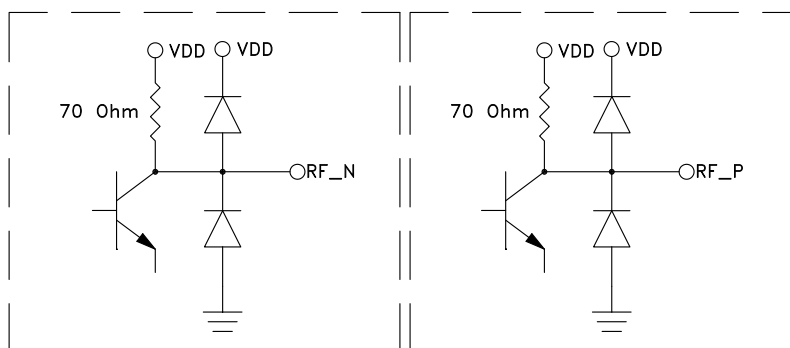
Figure 11. HMC1034LP6GE output stage

HMC1034LP6GE Application Information

The HMC1034LP6GE features a flexible Output Frequency Range (125MHz to 3000MHz), industry leading phase noise and phase jitter performance, excellent noise floor (<-170dBc/Hz), and a high level of integration. HMC1034LP6GE is ideal as a high frequency, low jitter processor clock, a clock source for high-frequency data converters or as a reference oscillator for Physical Layer Devices (PHY).

The HMC1034LP6GE can also be used as an LO for 10G/40G/100G optical modules and transponders, as a reference clock for 10G/40G/100G line cards, and for jitter attenuation and frequency translation. Synchronous Ethernet, SONET/SDH, and OTN applications often require jitter attenuation and frequency translation on the recovered line clock.
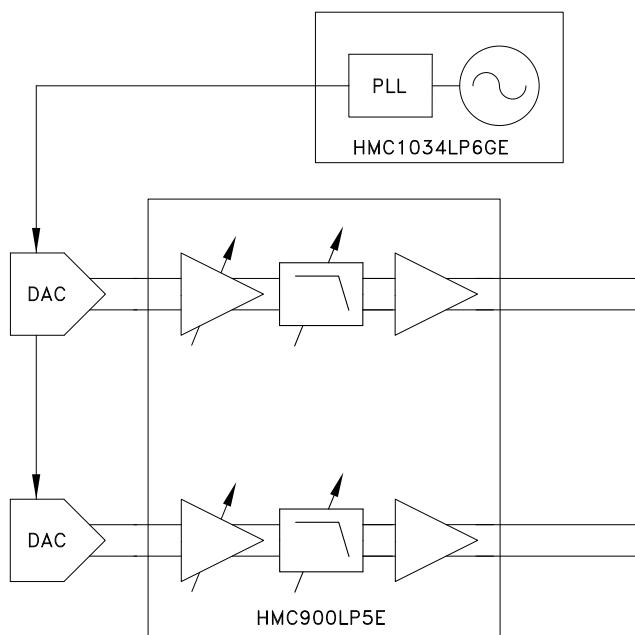
Figure 12. HMC1034LP6GE in a typical transmit chain

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The HMC1034LP6GE can also be used as an LO for 10G optical modules and transponders (Figure 13), as a reference clock for 1G/10G line cards (Figure 14), and for jitter attenuation and frequency translation (Figure 15).

Synchronous Ethernet, SONET/SDH, and OTN applications often require jitter attenuation and frequency translation on the recovered line clock.
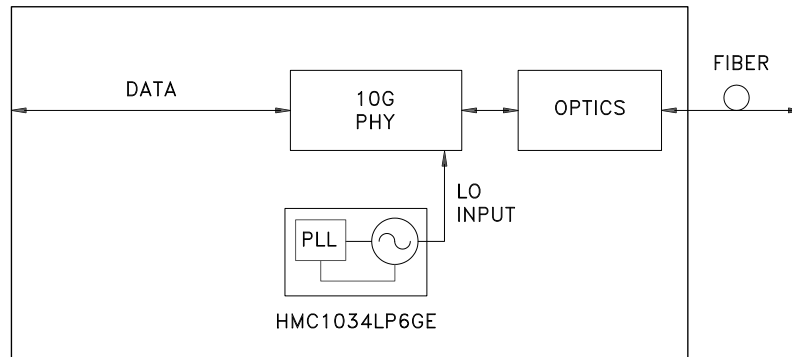

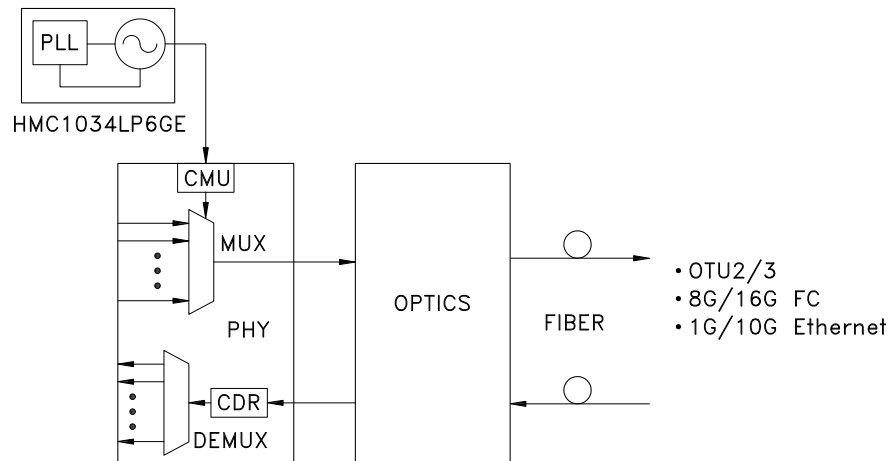*Figure 13. HMC1034LP6GE used as a local oscillator (LO) for 10G modules/transponders*

Figure 14. HMC1034LP6GE used as a reference clock for 1G/10G line cards

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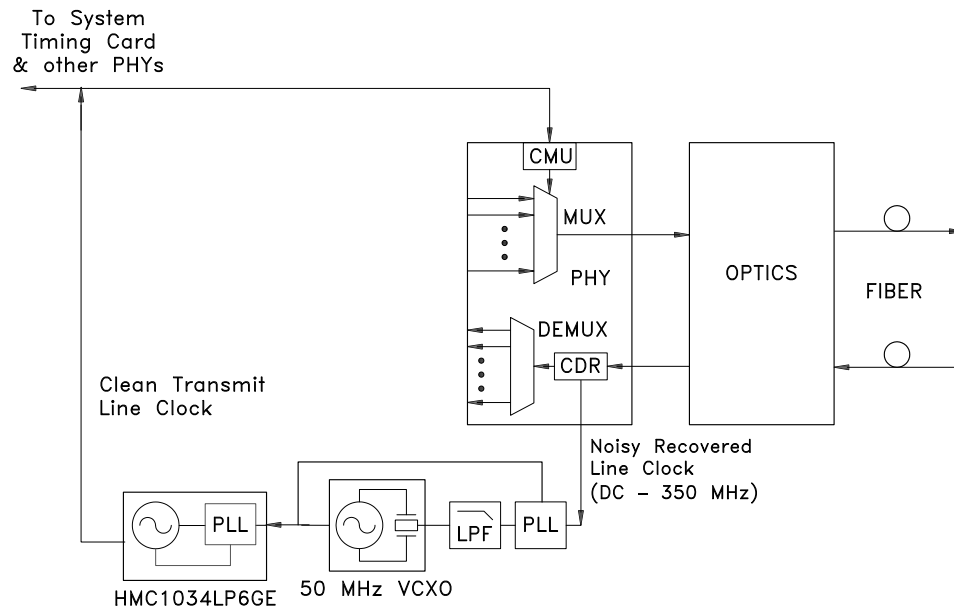
Figure 15. HMC1034LP6GE used in a jitter attenuation application for Synchronous Ethernet & Line Timing

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Line and Reference Clock Rates

OTN	Line Rates (Gbps)	Typical Reference Clock Rates (MHz)	
OTU2	10.709	669.31	167.33
OTU2e	11.095	693.44	173.36
OTU1e	11.049	690.56	172.64
OTU2f	11.317	707.31	176.83
OTU1f	11.27	704.38	176.09
OTU3	43.018	2688.63	672.16
OTU4	111.809		1747.02
OTU4v	127.156		1986.82

SONET/SDH			
STS-192/STM-64	9.95328	622.08	155.52
STS-768/STM-256	39.81312	2488.32	622.08

Ethernet			
10GE LAN	10.3125		156.25
10GE WAN	9.95328	622.08	155.52
XAUI (4 x 3.125G)	3.125		156.25
40GE (4 x 10G)	10.3125		156.25
100GE (4 x 25G)	25.78125	805.66	156.25

Fibre Channel (FC)			
10GFC	10.52		164.38
16GFC	14.025		212.5
32GFC	28.5		425

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Notes:

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