

ASYMMETRICAL BIDIRECTIONAL THYRISTOR SPD

TISP4A265H3BJ LCAS R_{LINE} Protector

RING Line Protection for:

- LCAS (Line Card Access Switch)
- ADSL Interfaces

Voltages Optimized for:

-Battery-Backed Ringing Circuits

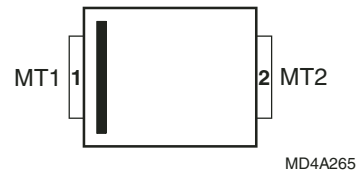
- Maximum Ringing a.c. 90 V rms
- Maximum Battery Voltage -52 V
- ADSL Voltage ±23 V peak
- Minimum Ambient Temperature 0 °C

Device	V _{DRM} V	V _(BO) V
'4A265	+100	+125
	-200	-265

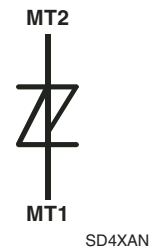
Rated for International Surge Wave Shapes

Wave Shape	Standard	I _{TSP} A
2/10 μs	GR-1089-CORE	500
8/20 μs	IEC 61000-4-5	300
10/160 μs	TIA/EIA-IS-968	250
10/700 μs	ITU-T K.20/45/21	200
10/560 μs	TIA/EIA-IS-968	160
10/1000 μs	GR-1089-CORE	100

SMB Package (Top View)



Device Symbol



..... UL Recognized Component

Description

The TISP4A265H3BJ is an asymmetrical bidirectional overvoltage protector. It is designed to limit the peak voltages on the ring line terminal of the '7581/2/3 LCAS (Line Card Access Switches). The TISP4A265H3BJ must be connected with bar-indexed terminal 1, MT1, to the protective ground and terminal 2, MT2, to the ring conductor.

The TISP4A265H3BJ voltages are chosen to give adequate LCAS ring line terminal protection for all switch conditions. The most potentially stressful condition is low level power cross when the LCAS switches are closed. Under this condition, the TISP4A265H3BJ limits the voltage and corresponding LCAS dissipation until the LCAS thermal trip operates and opens the switches.

Under open-circuit ringing conditions, the line ring conductor will have high peak voltages. For battery backed ringing, the ring conductor will have a larger peak negative voltage than positive, i.e. the peak voltages are asymmetric. The TISP4A265H3BJ has a similar voltage asymmetry and will allow the maximum possible ringing voltage, while giving the most effective protection. On a connected line, the tip conductor will have much smaller voltage levels than the open-circuit ring conductor values. Here a TISP4xxxH3BJ series, symmetrical voltage protector gives adequate protection.

Overvoltages are initially clipped by breakdown clamping. If sufficient current is available from the overvoltage, the breakdown voltage will rise to the breakover level, which causes the device to switch into a low-voltage on-state condition. This switching action removes the high voltage stress from the following circuitry and causes the current resulting from the overvoltage to be safely diverted through the protector. The high holding (switch off) current helps prevent d.c. latchup as the diverted current subsides.

How to Order

Device	Package	Carrier	Order As
TISP4A265H3BJ	BJ (J-Bend DO-214AA/SMB)	R (Embossed Tape Reeled)	TISP4A265H3BJR-S

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex

JANUARY 2002 - REVISED MAY 2007

Specifications are subject to change without notice.

Customers should verify actual device performance in their specific applications.

TISP4A265H3BJ LCAS R_{LINE} Protector

BOURNS®

Description (Continued)

The TISP4A265H3BJ is guaranteed to voltage limit and withstand the listed international lightning surges in both polarities. This high (H) current protection device is in a plastic SMBJ package (JEDEC DO-214AA with J-bend leads) and supplied in embossed carrier reel pack. For alternative voltage and holding current values, consult the factory.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage, (see Note 1)	V _{DRM}	+100 -200	V
Non-repetitive peak on-state pulse current (see Notes 2, 3 and 4) 2/10 μs (GR-1089-CORE, 2/10 μs voltage wave shape) 8/20 μs (IEC 61000-4-5, 1.2/50 μs voltage, 8/20 current combination wave generator) 10/160 μs (TIA/EIA-IS-968 (Replaces FCC Part 68), 10/160 μs voltage wave shape) 5/310 μs (ITU-T K.44, 10/700 μs voltage wave shape used in K.20/45/21) 5/320 μs (TIA/EIA-IS-968 (Replaces FCC Part 68), 9/720 μs voltage wave shape) 10/560 μs (TIA/EIA-IS-968 (Replaces FCC Part 68), 10/560 μs voltage wave shape) 10/1000 μs (GR-1089-CORE, 10/1000 μs voltage wave shape)	I _{TSP}	500 300 250 200 200 160 100	A
Non-repetitive peak on-state current (see Notes 2, 3 and 5) 20 ms (50 Hz) full sine wave 16.7 ms (60 Hz) full sine wave 1000 s 50 Hz/60 Hz a.c.	I _{TSM}	55 60 2.2	A
Initial rate of rise of on-state current, Exponential current ramp, Maximum ramp value < 200 A	di _T /dt	400	A/μs
Junction temperature	T _J	-40 to +150	°C
Storage temperature range	T _{stg}	-65 to +150	°C

- NOTES: 1. See Figure 7 for voltage values at other temperatures.
 2. Initially, the TISP4A265H3BJ must be in thermal equilibrium with T_J = 25 °C.
 3. The surge may be repeated after the TISP4A265H3BJ returns to its initial conditions.
 4. See Figure 8 for current ratings at other temperatures.
 5. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. See Figure 6 for the current ratings at other durations. Derate current values at -0.61 %/°C for ambient temperatures above 25 °C.

Overload Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Maximum overload on-state current without open circuit, 50 Hz/60 Hz a.c. (see Note 6) 0.03 s 0.07 s 1.6 s 5.0 s 1000 s	I _{T(OV)M}	60 40 8 7 2.2	A rms

NOTE 6: Peak overload on-state current during a.c. power cross tests of GR-1089-CORE and UL 1950/60950. These electrical stress levels may damage the TISP4A265H3BJ silicon chip. After test, the pass criterion is either that the device is functional or, if it is faulty, that it has a short circuit fault mode. In the short circuit fault mode, the following equipment is protected as the device is a permanent short across the line. The equipment would be unprotected if an open circuit fault mode developed.

Electrical Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter	Test Conditions	Min	Typ	Max	Unit	
I _{DRM} Repetitive peak off-state current	V _D = +100 V and -200 V T _A = 25 °C T _A = 85 °C			±5 ±10	μA	
V _(BO) Breakover voltage	dv/dt = ±250 V/ms, R _{SOURCE} = 300 Ω			+125 -265	V	
I _(BO) Breakover current	dv/dt = ±250 V/ms, R _{SOURCE} = 300 Ω	±0.15		±0.6	A	
I _H Holding current	I _T = ±5 A, di/dt = +/-30 mA/ms	±0.15		±0.6	A	
dv/dt Critical rate of rise of off-state voltage	Linear voltage ramp, Maximum ramp value < 0.85V _{DRM}	±5			kV/μs	
I _D Off-state current	V _D = ±50 V T _A = 85 °C			±10	μA	
C _{off} Off-state capacitance	f = 1 MHz, V _d = 1 V rms, (see Note 7)		V _D = 98 V	25	30	pF
			V _D = 50 V	30	36	
			V _D = 10 V	45	54	
			V _D = 5 V	52	62	
			V _D = 2 V	60	72	
			V _D = 1 V	65	79	
			V _D = 0	71	86	
			V _D = -1 V	65	79	
			V _D = -2 V	58	69	
			V _D = -5 V	48	57	
V _D = -10 V	40	48				
V _D = -50 V	26	31				
V _D = -100 V	20	24				

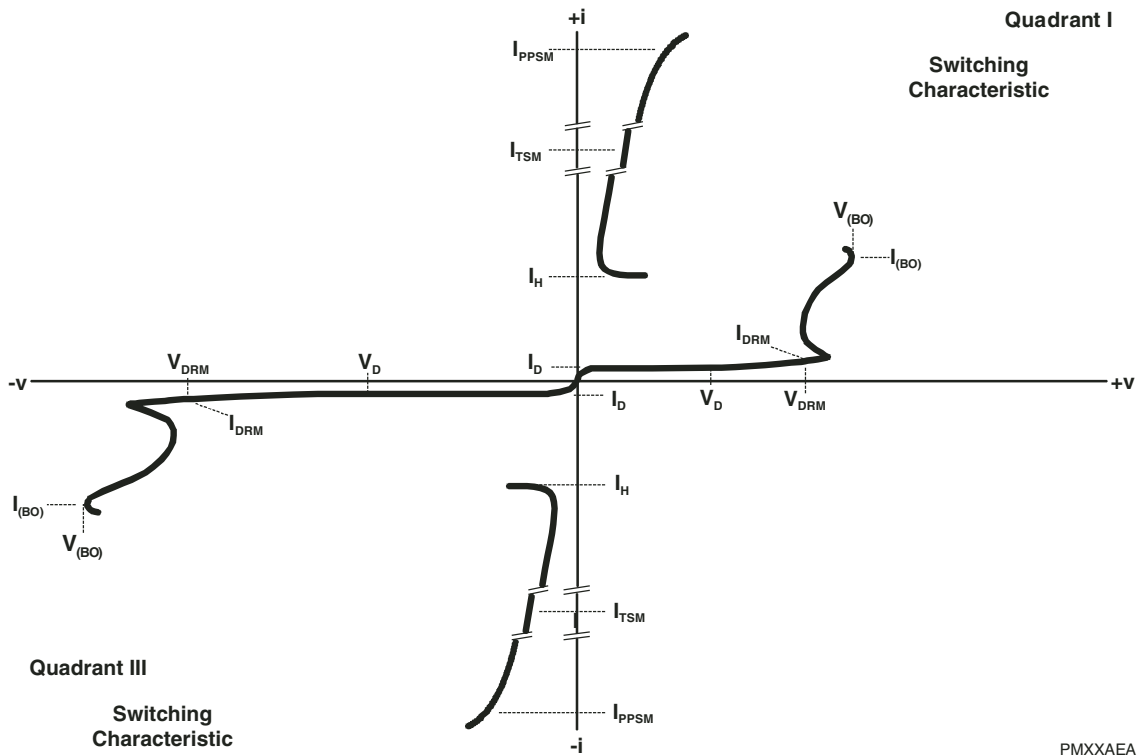
NOTE 7: To avoid possible voltage clipping, the TISP4A265H3BJ is tested with V_D = +98 V in the positive polarity.

Thermal Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
R _{θJA} Junction to free air thermal resistance	EIA/JESD51-3 PCB, I _T = I _{TSM(1000)} , T _A = 25 °C, (see Note 8)			113	°C/W
	265 mm x 210 mm populated line card, 4-layer PCB, I _T = I _{TSM(1000)} , T _A = 25 °C		50		

NOTE 8: EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information



PMXXAEA

Figure 1. Voltage-Current Characteristic for MT1 and MT2 Terminals
All Measurements are Referenced to the MT1 Terminal

Typical Characteristics

**OFF-STATE CURRENT
vs
JUNCTION TEMPERATURE**

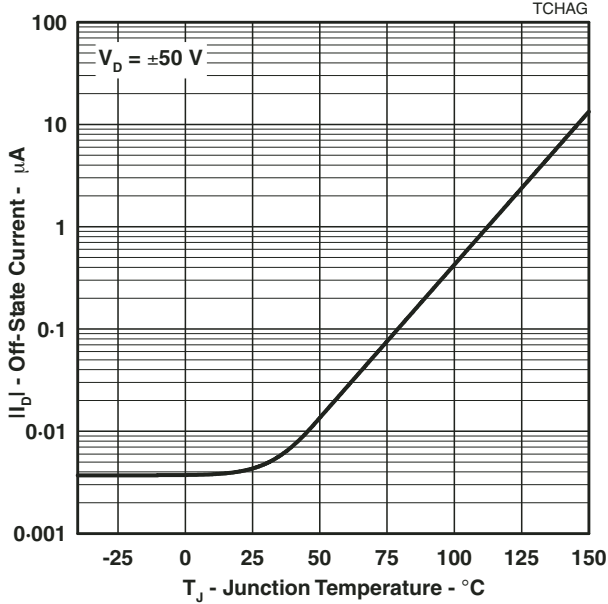


Figure 2.

**NORMALIZED BREAKOVER VOLTAGE
vs
JUNCTION TEMPERATURE**

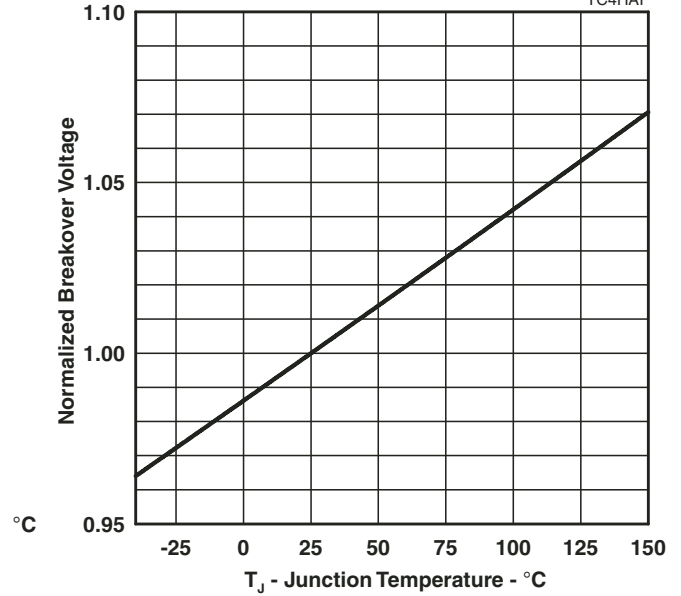


Figure 3.

**ON-STATE CURRENT
vs
ON-STATE VOLTAGE**

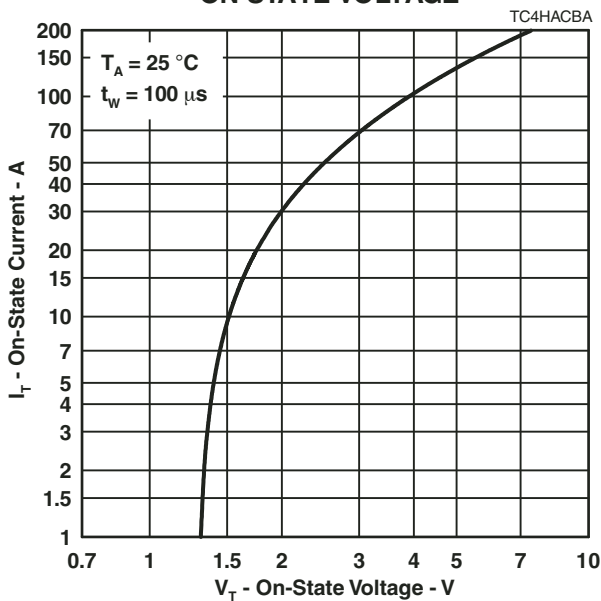


Figure 4.

**NORMALIZED HOLDING CURRENT
vs
JUNCTION TEMPERATURE**

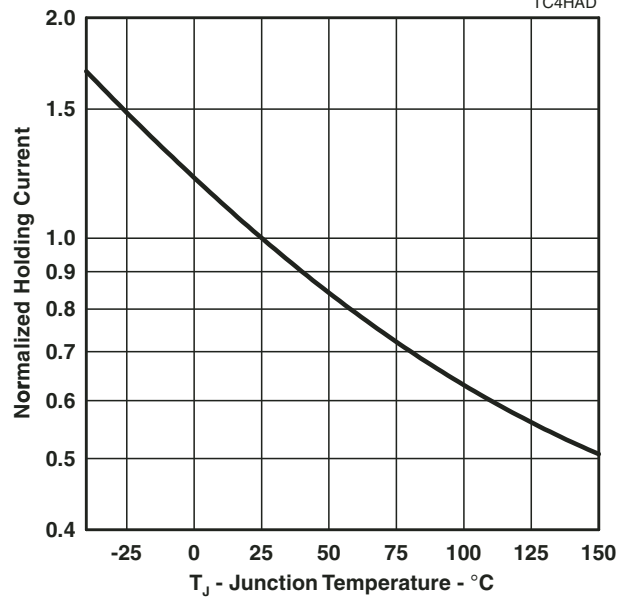


Figure 5.

Rating and Thermal Information

**NON-REPETITIVE PEAK ON-STATE CURRENT
VS
CURRENT DURATION**

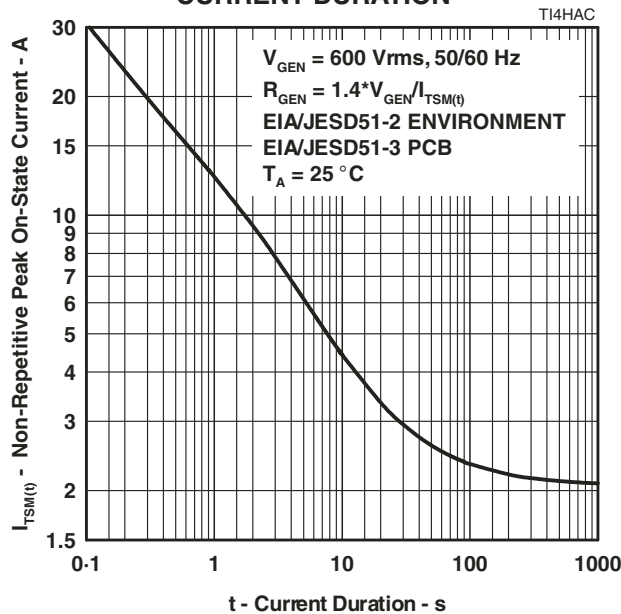


Figure 6.

**V_{DRM} DERATING FACTOR
VS
MINIMUM AMBIENT TEMPERATURE**

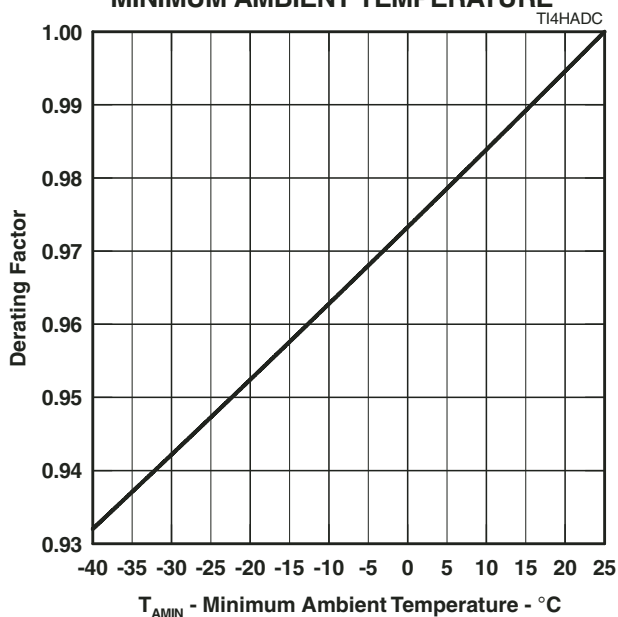


Figure 7.

**IMPULSE RATING
VS
AMBIENT TEMPERATURE**

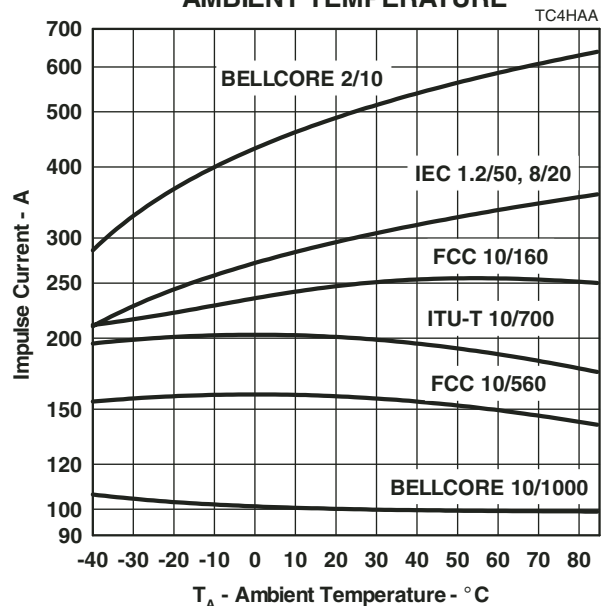
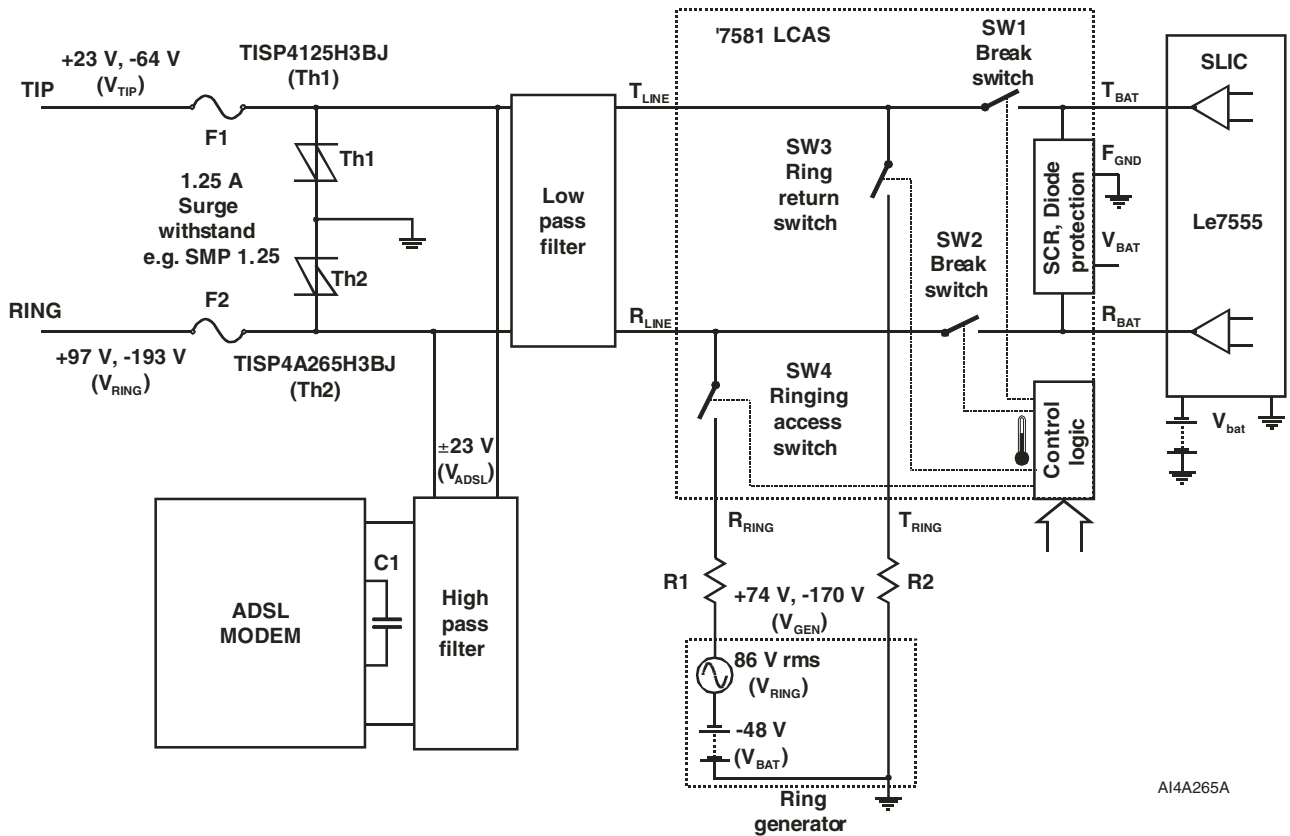


Figure 8.

Typical Circuits

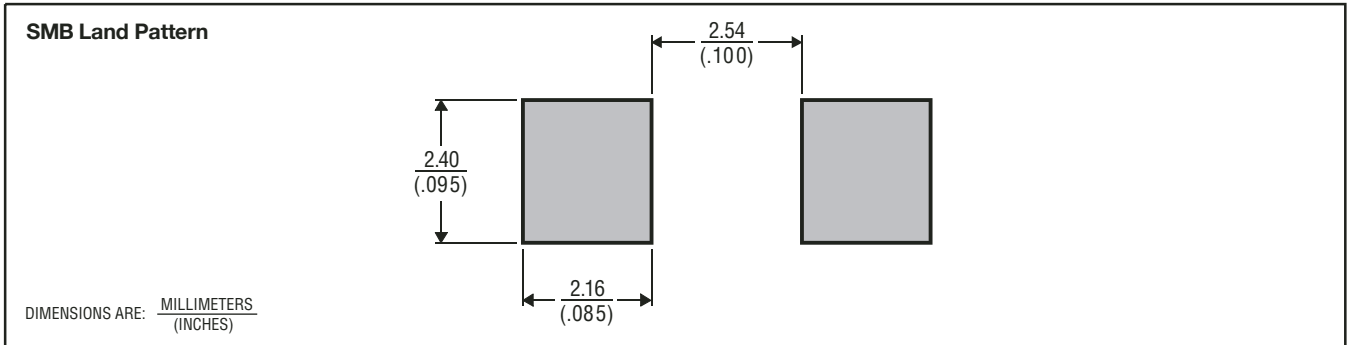


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Figure 9. Integrated Voice Data (IVD) System with Typical Operating Voltage Levels Indicated

MECHANICAL DATA

Recommended Printed Wiring Land Pattern Dimensions



MDXX BID

Device Symbolization Code

Devices will be coded as below. Terminal 1 is indicated by an adjacent bar marked on the package body.

Device	Symbolization Code
TISP4A265H3BJ	4A265H

Carrier Information

For production quantities, the carrier will be embossed tape reel pack. Evaluation quantities may be shipped in bulk pack or embossed tape.

Package	Carrier	Standard Quantity
SMB	Embossed Tape Reel Pack	3000

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