FAIRCHILD™

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

December 2013

FAN3268
2 A Low-Voltage PMOS-NMOS Bridge Driver

Features

- 4.5 V to 18 V Operating Range
- Drives High-Side PMOS and Low-Side NMOS in Motor Control or Buck Step-Down Applications
- Inverting Channel B Biases High-Side PMOS Device Off (with internal 100 kΩ Resistor) when V_{DD} is below UVLO Threshold
- TTL Input Thresholds
- 2.4 A Sink / 1.6 A Source at V_{OUT}=6 V
- Internal Resistors Turn Driver Off If No Inputs
- MillerDrive™ Technology
- 8-Lead SOIC Package
- Rated from −40°C to +125°C Ambient
- Automotive Qualified to AEC-Q100 (F085 Version)

Applications

- Motor Control with PMOS / NMOS Half-Bridge Configuration
- Buck Converters with High-Side PMOS Device; 100% Duty Cycle Operation Possible
- Logic-Controlled Load Circuits with High-Side PMOS Switch
- Automotive-Qualified Systems (F085 version)

Description

The FAN3268 dual 2 A gate driver is optimized to drive a high-side P-channel MOSFET and a low-side N-channel MOSFET in motor control applications operating from a voltage rail up to 18 V. The driver has TTL input thresholds and provides buffer and level translation functions from logic inputs. Internal circuitry provides an under-voltage lockout function that prevents the output switching devices from operating if the V_{DD} supply voltage is below the operating level. Internal 100 kΩ resistors bias the non-inverting output low and the inverting output to V_{DD} to keep the external MOSFETs off during startup intervals when logic control signals may not be present.

The FAN3268 driver incorporates MillerDrive™ architecture for the final output stage. This bipolar-MOSFET combination provides high current during the Miller plateau stage of the MOSFET turn-on / turn-off process to minimize switching loss, while providing rail-to-rail voltage swing and reverse current capability.

The FAN3268 has two independent enable pins that default to on if not connected. If the enable pin for non-inverting channel A is pulled low, OUTA is forced low; if the enable pin for inverting channel B is pulled low, OUTB is forced high. If an input is left unconnected, internal resistors bias the inputs such that the external MOSFETs are off.

Related Resources

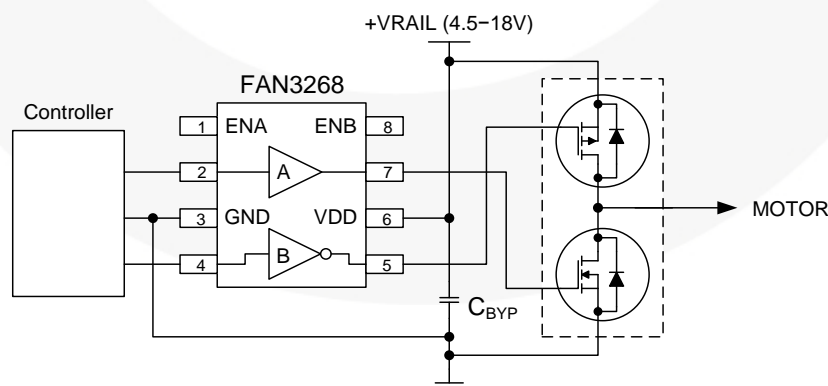*AN-6069 — Application Review and Comparative Evaluation of Low-Side Gate Drivers*

Figure 1.   Typical Motor Drive Application

www.fairchildsemi.com

Ordering Information

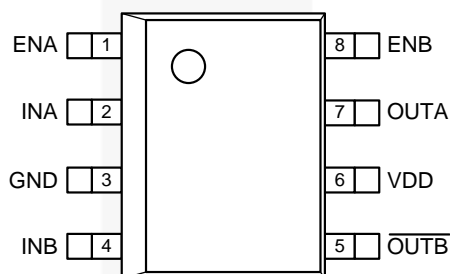| Part Number	Logic	Input Threshold	Packing Method
FAN3268TMX	Non-Inverting Channel and Inverting Channel + Dual Enables	TTL	2,500 Units on Tape & Reel
FAN3268TMX_F085[1]	Non-Inverting Channel and Inverting Channel + Dual Enables	TTL	2,500 Units on Tape & Reel

1. Qualified to AEC-Q100

Package Outline

Figure 2.   Pin Configuration (Top View)

Thermal Characteristics[2]

Package	Θ_{JL}[3]	Θ_{JT}[4]	Θ_{JA}[5]	Ψ_{JB}[6]	Ψ_{JT}[7]	Units
8-Pin Small Outline Integrated Circuit (SOIC)	40	31	89	43	3	°C/W

Notes:
2. Estimates derived from thermal simulation; actual values depend on the application.
3. Theta_JL (Θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
4. Theta_JT (Θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top-side heatsink.
5. Theta_JA (Θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink using a 2S2P board, as specified in JEDEC standards JESD51-2, JESD51-5, and JESD51-7, as appropriate.
6. Psi_JB (Ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 5. For the SOIC-8 package, the board reference is defined as the PCB copper adjacent to pin 6.
7. Psi_JT (Ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 5.

Pin Definitions

Pin#	Name	Description
1	ENA	**Enable Input for Channel A**. Pull pin low to inhibit driver A. ENA has TTL thresholds.
8	ENB	**Enable Input for Channel B**. Pull pin low to inhibit driver B. ENB has TTL thresholds.
3	GND	**Ground**. Common ground reference for input and output circuits.
2	INA	**Input to Channel A**.
4	INB	**Input to Channel B**.
7	OUTA	**Gate Drive Output A**: Held low unless required input(s) are present and V_{DD} is above the UVLO threshold.
5	$\overline{OUTB}$	**Gate Drive Output B** (inverted from the input): Held high unless required input is present and V_{DD} is above UVLO threshold.
6	VDD	**Supply Voltage**. Provides power to the IC.

Output Logic

FAN3268 (Channel A)		
ENA	INA	OUTA
0	0[8]	0
0	1	0
1[8]	0[8]	0
1[8]	1	1

FAN3268 (Channel B)		
ENB	INB	$\overline{OUTB}$
0	0[8]	1
0	1	1
1[8]	0[8]	1
1[8]	1	0

Note:
8. Default input signal if no external connection is made.

Block Diagram

ENA 1

INA 2

GND 3

INB 4

VDD 100kΩ

VDD 100kΩ

V_{DD_OK}

UVLO

8 ENB

7 OUTA 100kΩ
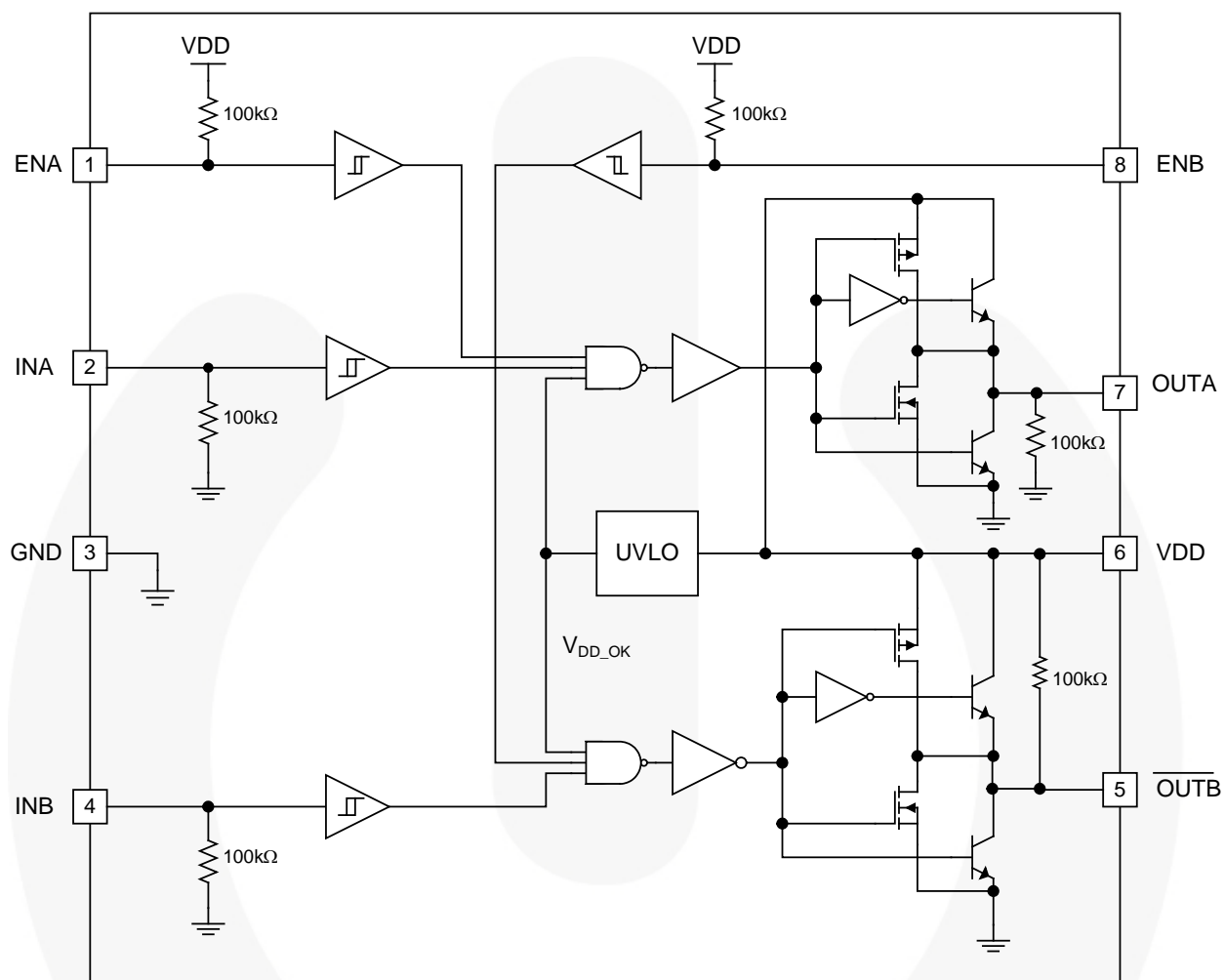
6 VDD 100kΩ

5 $\overline{OUTB}$

Figure 3.   Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	VDD to GND	-0.3	20.0	V
V_{EN}	ENA, ENB to GND	GND - 0.3	V_{DD} + 0.3	V
V_{IN}	INA, INB to GND	GND - 0.3	V_{DD} + 0.3	V
V_{OUT}	OUTA, OUTB to GND	GND - 0.3	V_{DD} + 0.3	V
T_L	Lead Soldering Temperature (10 Seconds)		+260	ºC
T_J	Junction Temperature	-55	+150	ºC
T_{STG}	Storage Temperature	-65	+150	ºC

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage Range	4.5	18.0	V
V_{EN}	Enable Voltage (ENA, ENB)	0	V_{DD}	V
V_{IN}	Input Voltage (INA, INB)	0	V_{DD}	V
T_A	Operating Ambient Temperature	-40	+125	ºC

Electrical Characteristics

Unless otherwise noted, V_{DD}=12 V and T_J=-40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SUPPLY						
V_{DD}	Operating Range		4.5		18.0	V
I_{DD}	Supply Current Inputs / EN Not Connected			0.75	1.20	mA
FAN3268T UVLO						
V_{ON}	Device Turn-On Voltage	INA=ENA=V_{DD}, INB=ENB=0 V	3.5	3.9	4.3	V
V_{OFF}	Device Turn-Off Voltage	INA=ENA=V_{DD}, INB=ENB=0 V	3.3	3.7	4.1	V
FAN3268TMX_F085 UVLO (Automotive-Qualified Versions)						
V_{ON}	Device Turn-On Voltage[12]	INA=ENA=V_{DD}, INB=ENB=0 V	3.3	3.9	4.5	V
V_{OFF}	Device Turn-Off Voltage[12]	INA=ENA=V_{DD}, INB=ENB=0 V	3.1	3.7	4.3	V
INPUT[9]						
FAN3268T						
V_{IL}	INx Logic Low Threshold		0.8	1.2		V
V_{IH}	INx Logic High Threshold			1.6	2.0	V
V_{HYS}	Logic Hysteresis Voltage		0.2	0.4	0.8	V
FAN3268TMX_F085 (Automotive-Qualified Versions)						
V_{IL}	INx Logic Low Threshold[12]		0.8	1.2		V
V_{IH}	INx Logic High Threshold[12]			1.6	2.0	V
V_{HYS}	Logic Hysteresis Voltage[12]		0.1	0.4	0.8	V

Electrical Characteristics (Continued)

Unless otherwise noted, V_{DD}=12 V and T_J=-40°C to +125°C. Currents are defined as positive into the device and negative out of the device.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ENABLE						
V_{ENL}	Enable Logic Low Threshold	EN from 5 V to 0 V	0.8	1.2		V
V_{ENH}	Enable Logic High Threshold	EN from 0 V to 5 V		1.6	2.0	V
V_{HYS}	Logic Hysteresis Voltage[10]			0.4		V
R_{PU}	Enable Pull-up Resistance[10]			100		kΩ
OUTPUT						
I_{SINK}	Out Current, Mid-Voltage, Sinking[10]	Out at V_{DD}/2, C_{LOAD}=0.1 µF, f=1 kHz		2.4		A
I_{SOURCE}	Out Current, Mid-Voltage, Sourcing[10]	Out at V_{DD}/2, C_{LOAD}=0.1 µF, f=1 kHz		-1.6		A
I_{PK_SINK}	Out Current, Peak, Sinking[10]	C_{LOAD}=0.1 µF, f=1 kHz		3		A
I_{PK_SOURCE}	Out Current, Peak, Sourcing[10]	C_{LOAD}=0.1 µF, f=1 kHz		-3		A
t_{RISE}	Output Rise Time[11]	C_{LOAD}=1000 pF		12	22	ns
t_{FALL}	Output Fall Time[11]	C_{LOAD}=1000 pF		9	17	ns
FAN3268T						
t_{D1}	Propagation Delay [11]	0 - 5 V_{IN}, 1 V/ns Slew Rate	7	14	25	ns
t_{D2}	Propagation Delay [11]	0 - 5 V_{IN}, 1 V/ns Slew Rate	10	19	34	ns
FAN3268TMX_F085 (Automotive-Qualified Versions)						
t_{D1}	Propagation Delay [11][12]	0 - 5 V_{IN}, 1 V/ns Slew Rate	7	14	32	ns
t_{D2}	Propagation Delay [11][12]	0 - 5 V_{IN}, 1 V/ns Slew Rate	8	19	34	ns
V_{OH}	High Level Output Voltage[12]	V_{OH}=V_{DD}–V_{OUT}, I_{OUT}=−1 mA		15	40	mV
V_{OL}	Low Level Output Voltage[12]	I_{OUT}=1 mA		10	25	mV

Notes:
9. EN inputs have TTL thresholds; refer to the ENABLE section.
10. Not tested in production.
11. *See the Timing Diagrams of Figure 4 and Figure 5.*
12. Apply only to Automotive Version(FAN3268TMX_F085)

Timing Diagrams
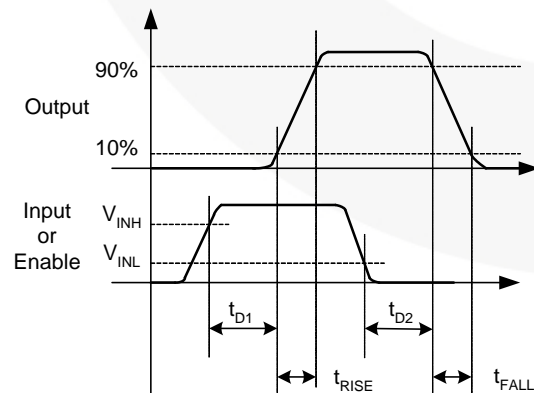
Figure 4. Non-Inverting
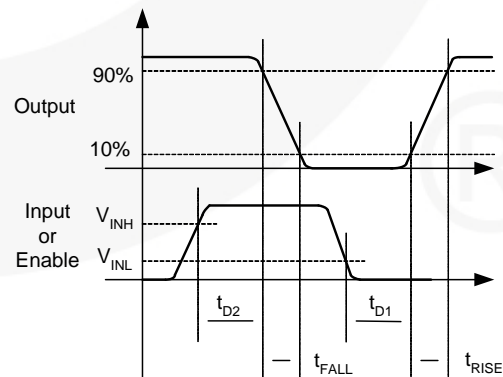
Figure 5. Inverting

Typical Performance Characteristics

Typical characteristics are provided at T_A=25°C and V_{DD}=12 V unless otherwise noted.
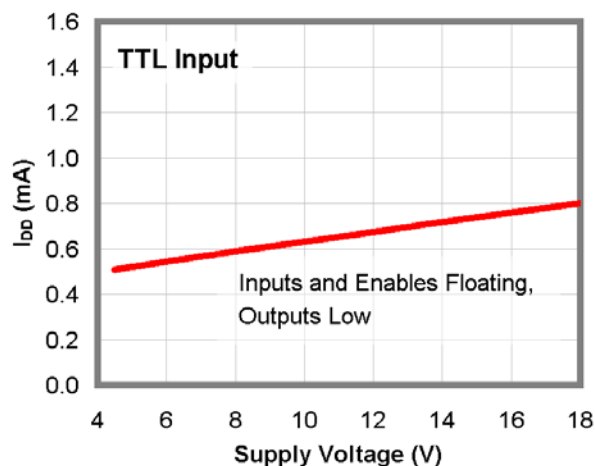

Figure 6. I_{DD} (Static) vs. Supply Voltage[13]
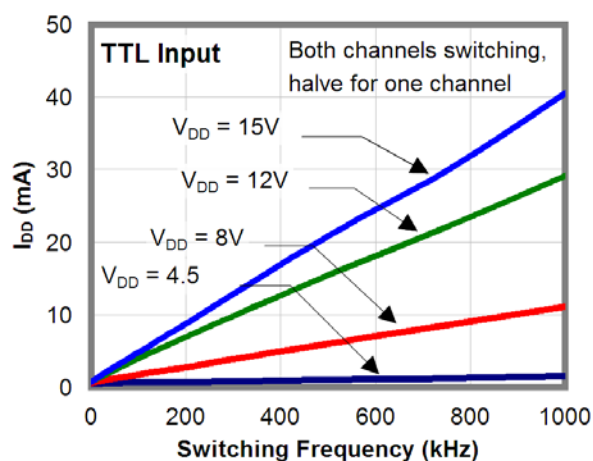

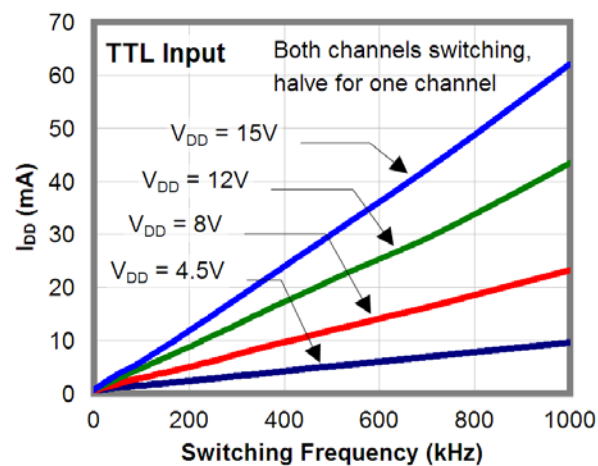Figure 7. I_{DD} (No-Load) vs. Frequency

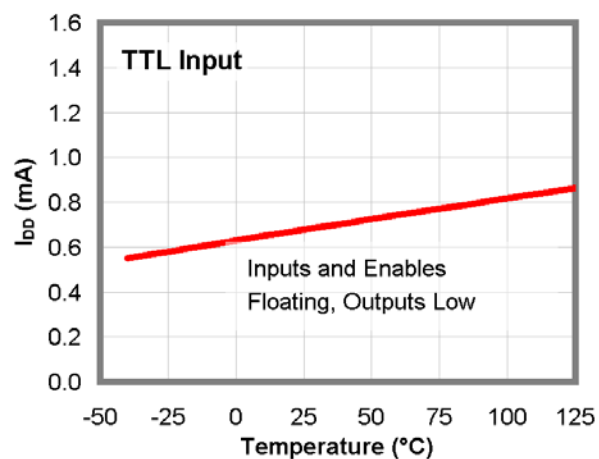Figure 8. I_{DD} (1 nF Load) vs. Frequency

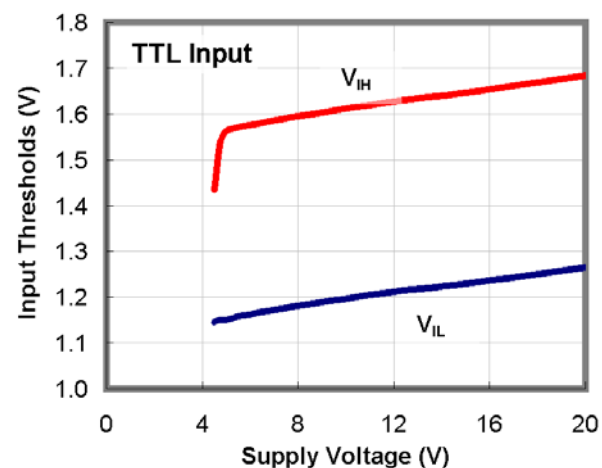Figure 9. I_{DD} (Static) vs. Temperature[13]

Figure 10. Input Thresholds vs. Supply Voltage
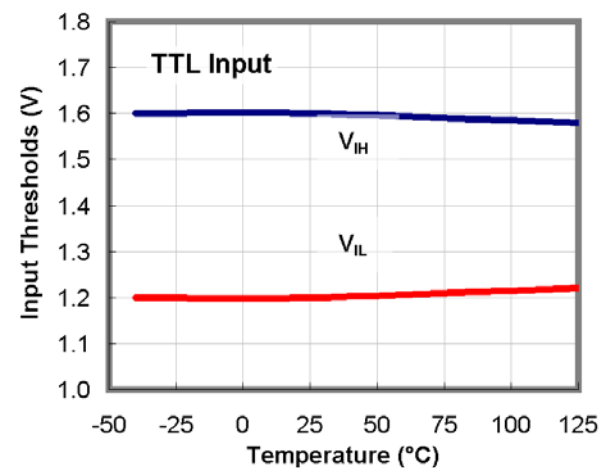

Figure 11. Input Thresholds vs. Temperature

Typical Performance Characteristics

Typical characteristics are provided at T_A=25°C and V_{DD}=12 V unless otherwise noted.
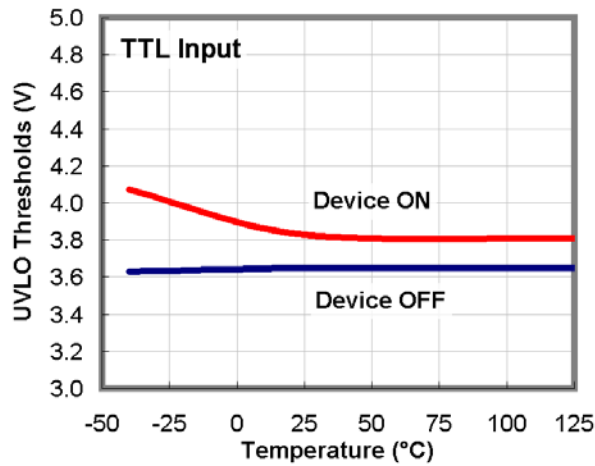

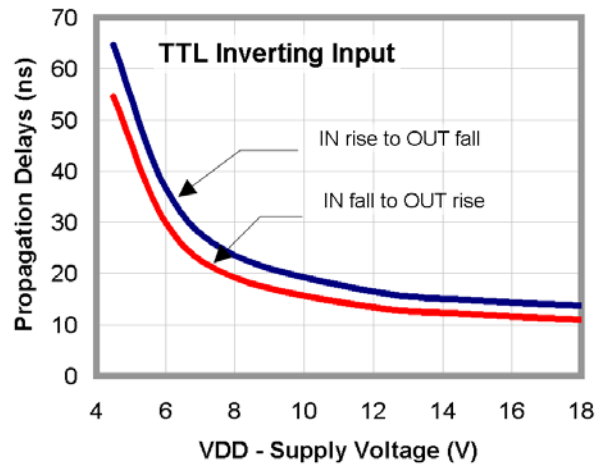**Figure 12. UVLO Threshold vs. Temperature**

Figure 13. Propagation Delays vs. Supply Voltage

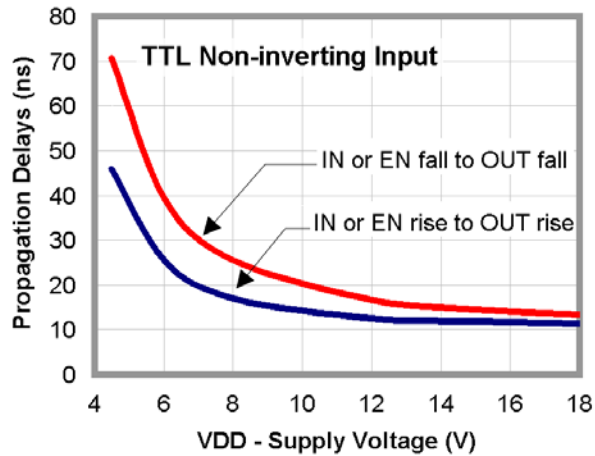**Figure 14. Propagation Delays vs. Supply Voltage**
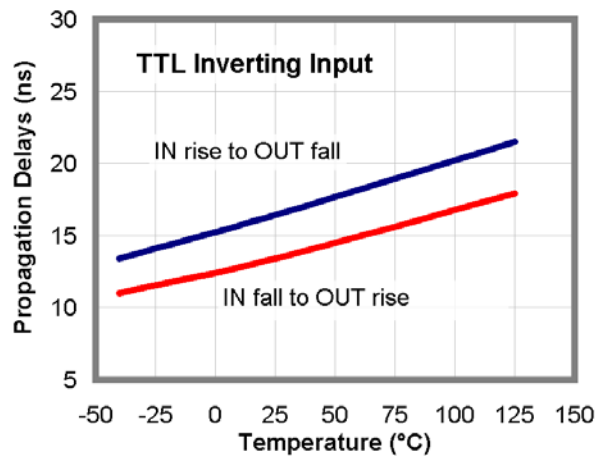
Figure 15. Propagation Delays vs. Temperature
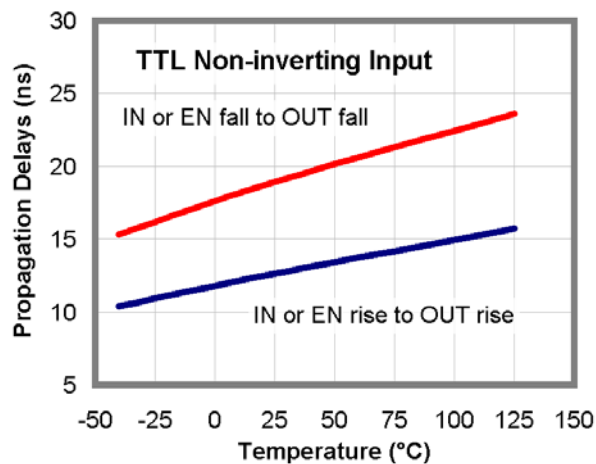
Figure 16. Propagation Delays vs. Temperature

Typical Performance Characteristics

Typical characteristics are provided at T_A=25°C and V_{DD}=12 V unless otherwise noted.

Figure 17. Fall Time vs. Supply Voltage
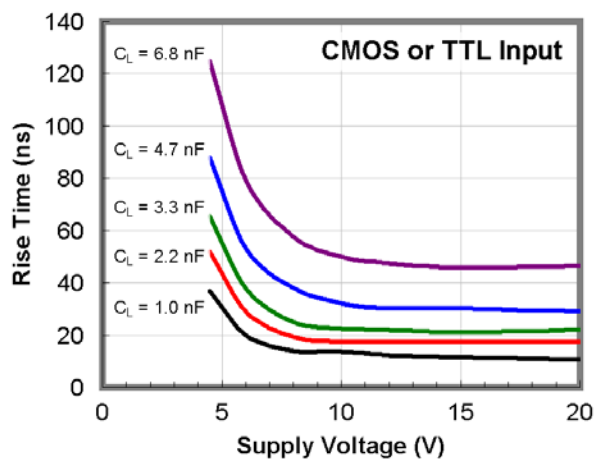
Figure 18.   Rise Time vs. Supply Voltage
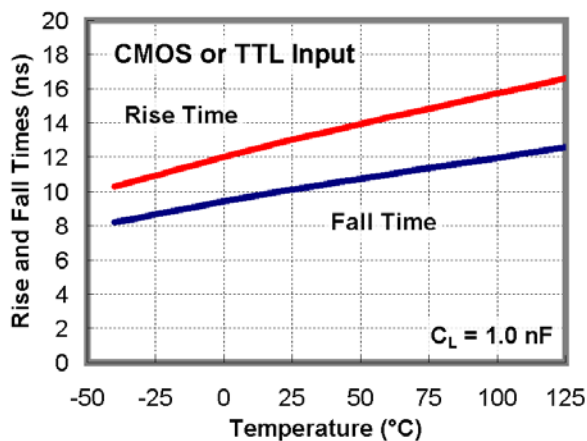
Figure 19. Rise and Fall Times vs. Temperature
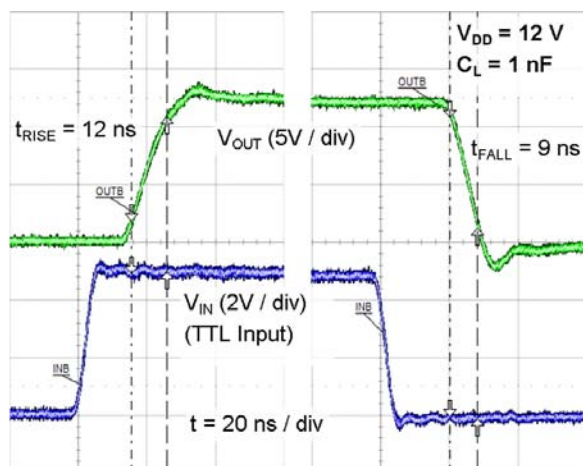
Figure 20. Rise/Fall Waveforms with 1 nF Load
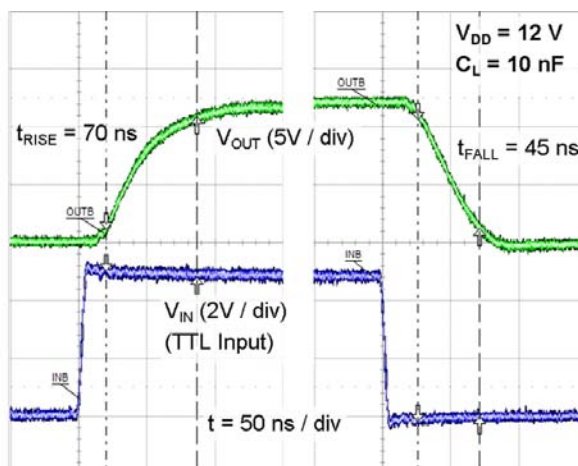
Figure 21. Rise/Fall Waveforms with 10 nF Load

Typical Performance Characteristics

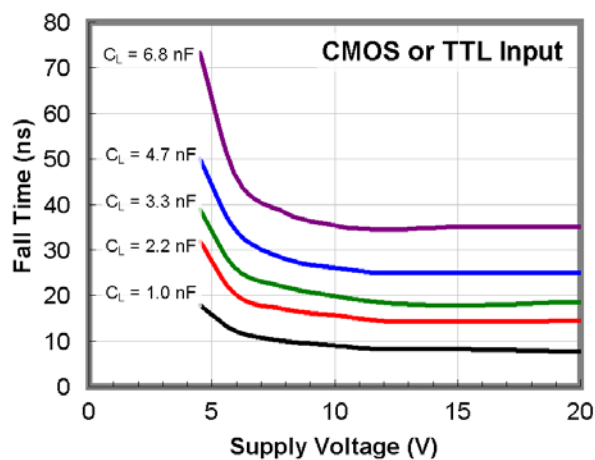Typical characteristics are provided at T_A=25°C and V_{DD}=12 V unless otherwise noted.
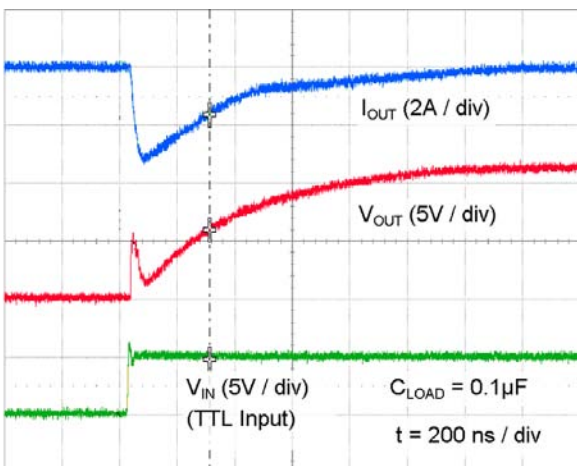
Figure 22. Quasi-Static Source Current with V_{DD}=12 V
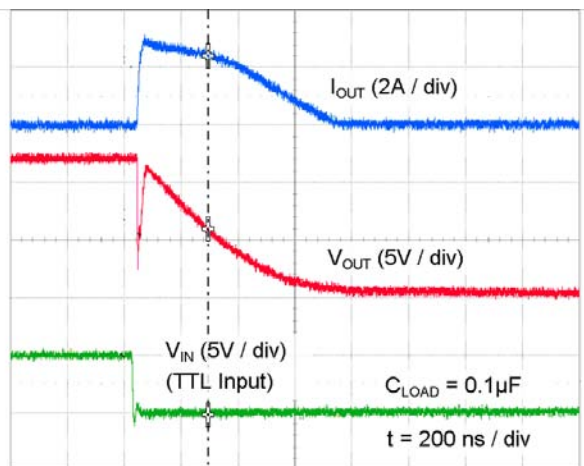
Figure 23. Quasi-Static Sink Current with V_{DD}=12 V
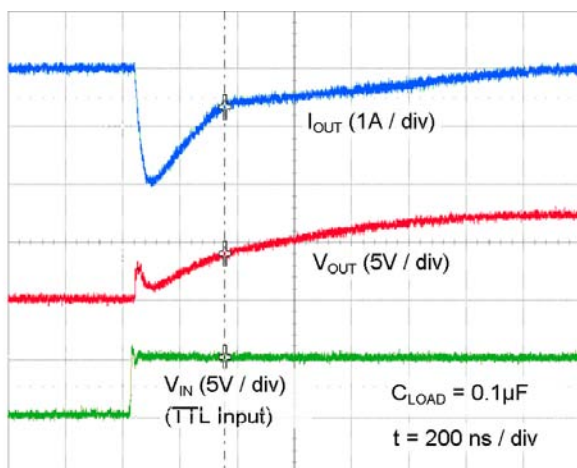
Figure 24. Quasi-Static Source Current with V_{DD}=8 V
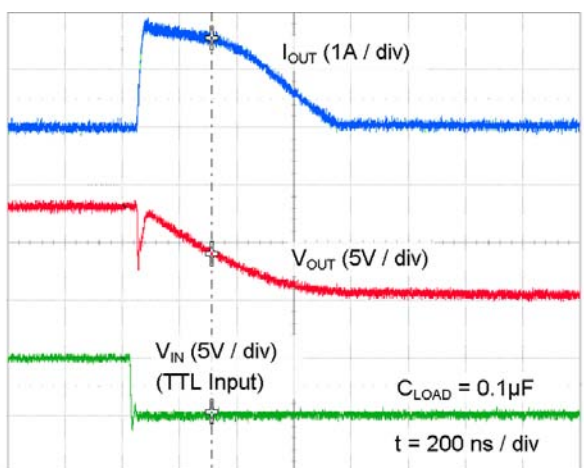
Figure 25. Quasi-Static Sink Current with V_{DD}=8 V

Note:
13. For any inverting inputs pulled low, non-inverting inputs pulled high, or outputs driven high, static I_{DD} increases by the current flowing through the corresponding pull-up/down resistor shown in the block diagram in Figure 3.

Test Circuit
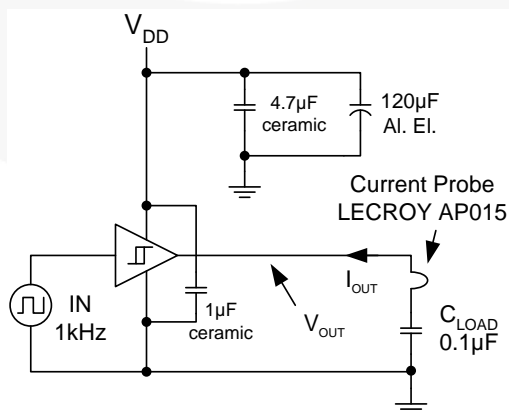
Figure 26. Quasi-Static I_{OUT} / V_{OUT} Test Circuit

Applications Information

Input Thresholds

The FAN3268 driver has TTL input thresholds and provides buffer and level translation functions from logic inputs. The input thresholds meet industry-standard TTL-logic thresholds, independent of the V_{DD} voltage, and there is a hysteresis voltage of approximately 0.4 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic high. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/µs or faster, so a rise time from 0 to 3.3 V should be 550 ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input, causing erratic operation.

Static Supply Current

In the I_{DD} (static) typical performance characteristics *(see Figure 6)*, the curve is produced with all inputs / enables floating (OUT is low) and indicates the lowest static I_{DD} current for the tested configuration. For other states, additional current flows through the 100 kΩ resistors on the inputs and outputs shown in the block diagram *(see Figure 3)*. In these cases, the actual static I_{DD} current is the value obtained from the curves plus this additional current.

MillerDrive™ Gate Drive Technology

FAN3268 gate drivers incorporate the MillerDrive™ architecture shown in Figure 1. For the output stage, a combination of bipolar and MOS devices provide large currents over a wide range of supply voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between one and two thirds V_{DD} and the MOS devices pull the output to the high or low rail.

The purpose of the MillerDrive™ architecture is to speed up switching by providing high current during the Miller plateau region when the gate-drain capacitance of the MOSFET is being charged or discharged as part of the turn-on / turn-off process.

For applications with zero voltage switching during the MOSFET turn-on or turn-off interval, the driver supplies high peak current for fast switching even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched on.

The output pin slew rate is determined by V_{DD} voltage and the load on the output. It is not user adjustable, but a series resistor can be added if a slower rise or fall time at the MOSFET gate is needed.
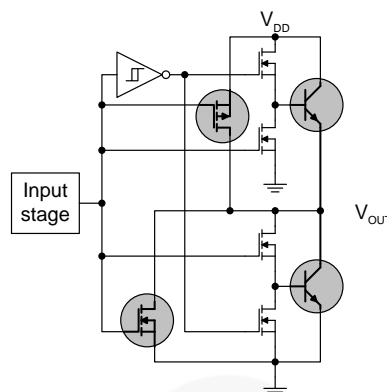

Figure 27. MillerDrive™ Output Architecture

Under-Voltage Lockout

Internal circuitry provides an under-voltage lockout function that prevents the output switching devices from operating if the V_{DD} supply voltage is below the operating level. When V_{DD} is rising, but below the 3.9 V operational level, internal 100 kΩ resistors bias the non-inverting output low and the inverting output to V_{DD} to keep the external MOSFETs off during startup intervals when logic control signals may not be present. After the part is active, the supply voltage must drop 0.2 V before the part shuts down. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power switching.

V_{DD} Bypass Capacitor Guidelines

To enable this IC to turn a device on quickly, a local high-frequency bypass capacitor C_{BYP} with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10 µF to 47 µF commonly found on driver and controller bias circuits.

A typical criterion for choosing the value of C_{BYP} is to keep the ripple voltage on the V_{DD} supply to ≤5%. This is often achieved with a value ≥20 times the equivalent load capacitance C_{EQV}, defined here as Q_{GATE}/V_{DD}. Ceramic capacitors of 0.1 µF to 1 µF or larger are common choices, as are dielectrics, such as X5R and X7R, with good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of C_{BYP} may be increased to 50-100 times the C_{EQV} or C_{BYP} may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1-10 nF mounted closest to the VDD and GND pins to carry the higher frequency components of the current pulses. The bypass capacitor must provide the pulsed current from both of the driver channels and, if the drivers are switching simultaneously, the combined peak current sourced from the C_{BYP} would be twice as large as when a single channel is switching.

Layout and Connection Guidelines

The FAN3268 gate driver incorporates fast-reacting input circuits, short propagation delays, and powerful output stages capable of delivering current peaks over 2 A to facilitate voltage transition times from under 10ns to over 150 ns. The following layout and connection guidelines are strongly recommended:

- Keep high-current output and power ground paths separate from logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds at driver inputs and enable pins.

- Keep the driver as close to the load as possible to minimize the length of high-current traces. This reduces the series inductance to improve high-speed switching, while reducing the loop area that can radiate EMI to the driver inputs and surrounding circuitry.

- If the inputs to a channel are not externally connected, the internal 100 kΩ resistors indicated on block diagrams command a low output (channel A) or a high output (channel B). In noisy environments, it may be necessary to tie inputs or enables of an unused channel to VDD or GND using short traces to prevent noise from causing spurious output switching.

- Many high-speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be obvious if the circuit is tested in breadboard or non-optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.

- The turn-on and turn-off current paths should be minimized.

Operational Waveforms

Figure 28 shows startup waveforms for non-inverting channel A. At power-up, the driver output for channel A remains low until the V_{DD} voltage reaches the UVLO turn-on threshold, then OUTA operates in-phase with INA.
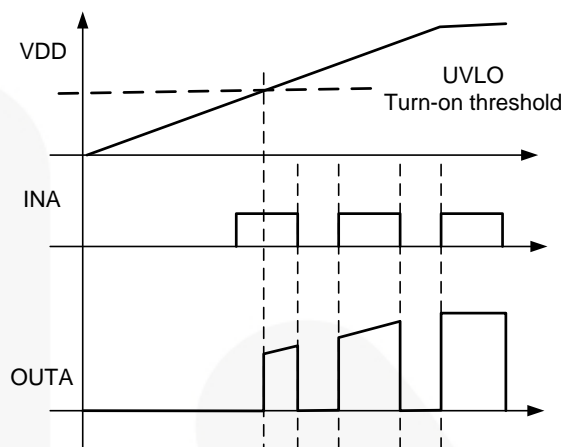

Figure 28. Non-Inverting Startup Waveforms

Figure 29 illustrates startup waveforms for inverting channel B. At power-up, the driver output for channel B is tied to V_{DD} through an internal 100 kΩ resistor until the V_{DD} voltage reaches the UVLO turn-on threshold, then OUTB operates out of phase with INB.
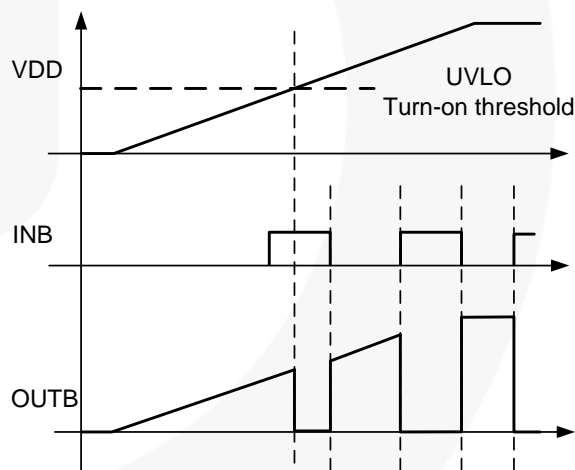

Figure 29. Inverting Startup Waveforms

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components, P_{GATE} and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \qquad (1)$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate-source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE} = Q_G \bullet V_{GS} \bullet f_{SW} \bullet n \qquad (2)$$

where n is the number of driver channels in use (1 or 2).

Dynamic Pre-drive / Shoot-through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull-up / pull-down resistors, can be obtained using the "I_{DD} (No-Load) vs. Frequency" graphs in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \bullet V_{DD} \bullet n \qquad (3)$$

Once the power dissipated in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming ψ_{JB} was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \bullet \psi_{JB} + T_B \qquad (4)$$

where:

T_J = driver junction temperature

ψ_{JB} = (psi) thermal characterization parameter relating temperature rise to total power dissipation

T_B = board temperature in location defined in Note 2 under Thermal Resistance table.

As an example of a power dissipation calculation, consider an application driving two MOSFETs with a gate charge of 60 nC with $V_{GS} = V_{DD} = 7$ V. At a switching frequency of 500 kHz, the total power dissipation is:

$$P_{GATE} = 60nC \bullet 7V \bullet 500kHz \bullet 2 = 0.42W \qquad (5)$$

$$P_{DYNAMIC} = 3mA \bullet 7V \bullet 2 = 0.042W \qquad (6)$$

$$P_{TOTAL} = 0.46W \qquad (7)$$

The SOIC-8 has a junction-to-board thermal characterization parameter of $\psi_{JB} = 43°C/W$. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150°C; with 80% derating, T_J would be limited to 120°C. Rearranging Equation 4 determines the board temperature required to maintain the junction temperature below 120°C:

$$T_B = T_J - P_{TOTAL} \bullet \psi_{JB} \qquad (8)$$

$$T_B = 120°C - 0.46W \bullet 43°C/W = 100°C \qquad (9)$$

Table 1.   Related Products

Part Number	Type	Gate Drive[14] (Sink/Src)	Input Threshold	Logic	Package
FAN3111C	Single 1 A	+1.1 A / -0.9 A	CMOS	Single Channel of Dual-Input/Single-Output	SOT23-5, MLP6
FAN3111E	Single 1 A	+1.1 A / -0.9 A	External[15]	Single Non-Inverting Channel with External Reference	SOT23-5, MLP6
FAN3100C	Single 2 A	+2.5 A / -1.8 A	CMOS	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
FAN3100T	Single 2 A	+2.5 A / -1.8 A	TTL	Single Channel of Two-Input/One-Output	SOT23-5, MLP6
FAN3226C	Dual 2 A	+2.4 A / -1.6 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3226T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227C	Dual 2 A	+2.4 A / -1.6 A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3227T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3228C	Dual 2 A	+2.4 A / -1.6 A	CMOS	Dual Channels of Two-Input/One-Output, Pin Config.1	SOIC8, MLP8
FAN3228T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Channels of Two-Input/One-Output, Pin Config.1	SOIC8, MLP8
FAN3229C	Dual 2 A	+2.4 A / -1.6 A	CMOS	Dual Channels of Two-Input/One-Output, Pin Config.2	SOIC8, MLP8
FAN3229T	Dual 2 A	+2.4 A / -1.6 A	TTL	Dual Channels of Two-Input/One-Output, Pin Config.2	SOIC8, MLP8
FAN3268T	**Dual 2 A**	**+2.4 A / -1.6 A**	**TTL**	**Non-Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables**	**SOIC8**
FAN3223C	Dual 4 A	+4.3 A / -2.8 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3223T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224C	Dual 4 A	+4.3 A / -2.8 A	CMOS	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3224T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Non-Inverting Channels + Dual Enable	SOIC8, MLP8
FAN3225C	Dual 4 A	+4.3 A / -2.8 A	CMOS	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3225T	Dual 4 A	+4.3 A / -2.8 A	TTL	Dual Channels of Two-Input/One-Output	SOIC8, MLP8
FAN3121C	Single 9 A	+9.7 A / -7.1 A	CMOS	Single Inverting Channel + Enable	SOIC8, MLP8
FAN3121T	Single 9 A	+9.7 A / -7.1 A	TTL	Single Inverting Channel + Enable	SOIC8, MLP8
FAN3122T	Single 9 A	+9.7 A / -7.1 A	CMOS	Single Non-Inverting Channel + Enable	SOIC8, MLP8
FAN3122C	Single 9 A	+9.7 A / -7.1 A	TTL	Single Non-Inverting Channel + Enable	SOIC8, MLP8

Notes:
14. Typical currents with OUT at 6 V and V_{DD}=12 V.
15. Thresholds proportional to an externally supplied reference voltage.

Physical Dimensions

4.90±0.10 [A]

(0.635)

8   5

[B]

6.00±0.20

3.90±0.10

PIN ONE
INDICATOR

1   4

1.27

⊕ | 0.25 Ⓜ | C | B | A

0.65

1.75

5.60

1.27

LAND PATTERN RECOMMENDATION

0.175±0.75

1.75 MAX

[C]

0.42±0.09

SEE DETAIL A

0.22±0.30

⌓ | 0.10

OPTION A - BEVEL EDGE

OPTION B - NO BEVEL EDGE

(0.86) x 45°

R0.10

R0.10

GAGE PLANE

0.36

8°
0°

0.65±0.25

SEATING PLANE

(1.04)

DETAIL A
SCALE: 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC
MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD
FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
E) DRAWING FILENAME: M08Arev15
F) FAIRCHILD SEMICONDUCTOR.

Figure 30. 8-Lead Small Outline Integrated Circuit (SOIC)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:
http://www.fairchildsemi.com/packaging/.

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

AccuPower™
AX-CAP®*
BitSiC™
Build it Now™
CorePLUS™
CorePOWER™
CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™

F®
Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™

F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder
    and Better™
MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
mWSaver®
OptoHiT™
OPTOLOGIC®
OPTOPLANAR®

®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™

○™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
Solutions for Your Success™
SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SupreMOS®
SyncFET™

Sync-Lock™

SYSTEM GENERAL®*

TinyBoost®
TinyBuck®
TinyCalc™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
TranSiC™
TriFault Detect™
TRUECURRENT®*
μSerDes™

μSerDes™
UHC®
Ultra FRFET™
UniFET™
VCX™
VisualMax™
VoltagePlus™
XS™

* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I66

PUBLICATION ORDERING INFORMATION

© Semiconductor Components Industries, LLC

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[ON Semiconductor](#):

  [FAN3268TMX](#)

ООО "ЛайфЭлектроникс"   **"LifeElectronics" LLC**

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

* Конкурентоспособные цены и скидки постоянным клиентам.
* Специальные условия для постоянных клиентов.
* Подбор аналогов.
* Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.

* Приемлемые сроки поставки, возможна ускоренная поставка.
* Доставку товара в любую точку России и стран СНГ.
* Комплексную поставку.
* Работу по проектам и поставку образцов.
* Формирование склада под заказчика.

* Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
* Тестирование поставляемой продукции.
* Поставку компонентов, требующих военную и космическую приемку.
* Входной контроль качества.
* Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

* Регистрацию проекта у производителя компонентов.
* Техническую поддержку проекта.
* Защиту от снятия компонента с производства.
* Оценку стоимости проекта по компонентам.
* Изготовление тестовой платы монтаж и пусконаладочные работы.

Тел: +7 (812) 336 43 04 (многоканальный)
Email: org@lifeelectronics.ru

www.lifeelectronics.ru