# 74HC125-Q100; 74HCT125-Q100

Quad buffer/line driver; 3-state

Rev. 2 — 19 January 2015

**Product data sheet** 

### 1. General description

The 74HC125-Q100; 74HCT125-Q100 is a quad buffer/line driver with 3-state outputs controlled by the output enable inputs (n $\overline{\text{OE}}$ ). A HIGH on n $\overline{\text{OE}}$  causes the outputs to assume a high impedance OFF-state. Inputs include clamp diodes which enable the use of current limiting resistors to interface inputs to voltages in excess of V<sub>CC</sub>.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

### 2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - ◆ Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Complies with JEDEC standard no. 7A
- Input levels:
  - ◆ The 74HC125-Q100: CMOS levels
  - ◆ The 74HCT125-Q100: TTL levels
- ESD protection:
  - MIL-STD-883, method 3015 exceeds 2000 V
  - ♦ HBM JESD22-A114F exceeds 2000 V
  - ♦ MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

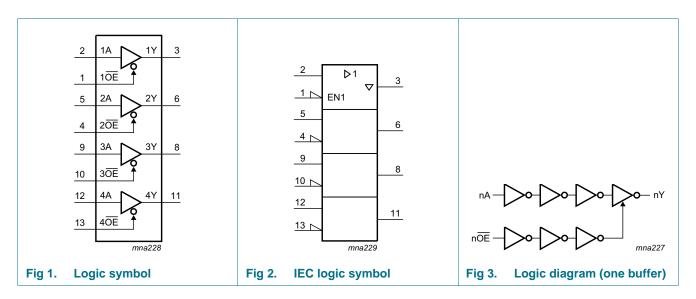
## 3. Ordering information

Table 1. Ordering information

Type number	Package								
	Temperature range Name Description								
74HC125D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width	SOT108-1					
74HCT125D-Q100			3.9 mm						
74HC125PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads;	SOT402-1					
74HCT125PW-Q100			body width 4.4 mm						

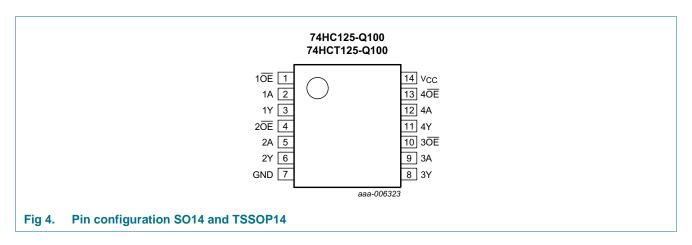


# 4. Functional diagram



## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
10E, 20E, 30E, 40E	1, 4, 10, 13	output enable input (active LOW)
1A, 2A, 3A, 4A	2, 5, 9, 12	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V <sub>CC</sub>	14	supply voltage

### 6. Functional description

#### Table 3. Function table[1]

Control	Input	Output
nOE	nA	nY
L	L	L
	Н	Н
Н	X	Z

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

# 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$		-	±35	mA
I <sub>CC</sub>	supply current			-	+70	mA
I <sub>GND</sub>	ground current			-	-70	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation		[1]	-	500	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

<sup>[2]</sup> For SO14 packages: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C. For TSSOP14 packages: P<sub>tot</sub> derates linearly with 5.5 mW/K above 60 °C.

# 8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74H	IC125-Q	100	74H	CT125-C	100	Unit
			Min	Тур	Max	Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 2.0 \text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5 \text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}$	-	-	83	-	-	-	ns/V

### 9. Static characteristics

#### Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC12	5-Q100							1		
V <sub>IH</sub>	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V <sub>IL</sub>	LOW-level	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_O = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu A; V_{CC} = 6.0 V$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_{O} = -6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_{O} = -7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 V$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 6.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 7.8 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
I <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_O = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.5	-	±5.0	-	±10.0	μΑ

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	–40 °C t	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0 \text{ V}$	-	-	8.0	-	80	-	160	μΑ
C <sub>I</sub>	input capacitance		-	3.5	-					pF
74HCT1	25-Q100									
$V_{IH}$	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	8.0	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	$I_{O} = -20 \mu A$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -6 \text{ mA}$	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub> LOW-level		$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 4.5 \text{ V}$								
	output voltage	I <sub>O</sub> = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		$I_{O} = 6.0 \text{ mA}$	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μΑ
l <sub>OZ</sub>	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$ ; $V_{CC} = 5.5$ V; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10	μΑ
I <sub>CC</sub>	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	8.0	-	80	-	160	μΑ
Δl <sub>CC</sub>	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V; } I_O = 0 \text{ A;}$ other inputs at $V_{CC}$ or GND; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	100	360	-	450	-	490	μА
Cı	input capacitance		-	3.5	-					pF

# 10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see Figure 7.

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C t	o +125 °C	Unit
				Min	Тур	Max	Min	Max	Min	Max	
74HC12	5-Q100										
t <sub>pd</sub>	propagation	nA to nY; see Figure 5	[1]								
	delay	V <sub>CC</sub> = 2.0 V		-	30	100	-	125	-	150	ns
		V <sub>CC</sub> = 4.5 V		-	11	20	-	25	-	30	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	9	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V		-	9	17	-	21	-	26	ns
t <sub>en</sub>	enable time	nOE to nY; see Figure 6	[2]								
		V <sub>CC</sub> = 2.0 V		-	41	125	-	155	-	190	ns
		V <sub>CC</sub> = 4.5 V		-	15	25	-	31	-	38	ns
		V <sub>CC</sub> = 6.0 V		-	12	21	-	26	-	32	ns
t <sub>dis</sub>	disable time	nOE to nY; see Figure 6	[3]								
		V <sub>CC</sub> = 2.0 V		-	41	125	-	155	-	190	ns
		V <sub>CC</sub> = 4.5 V		-	15	25	-	31	-	38	ns
		V <sub>CC</sub> = 6.0 V		-	12	21	-	26	-	32	ns
t <sub>t</sub>	transition	nY; see Figure 5	[4]								
	time	V <sub>CC</sub> = 2.0 V		-	14	60	-	75	-	90	ns
		V <sub>CC</sub> = 4.5 V		-	5	12	-	15	-	18	ns
		V <sub>CC</sub> = 6.0 V		-	4	10	-	13	-	15	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; f = 1 MHz; $V_I$ = GND to $V_{CC}$	<u>[5]</u>	-	22	-	-	-	-	-	pF

Table 7. Dynamic characteristics ... continued

Voltages are referenced to GND (ground = 0 V); C<sub>L</sub> = 50 pF unless otherwise specified; for test circuit see Figure 7.

Symbol	Parameter	Conditions			25 °C		-40 °C	to +85 °C	-40 °C to +125 °C		Unit
				Min	Тур	Max	Min	Max	Min	Max	
74HCT1	25-Q100								1	1	
t <sub>pd</sub>	propagation	nA to nY; see Figure 5	[1]								
	delay	V <sub>CC</sub> = 4.5 V		-	15	25	-	31	-	38	ns
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$		-	12	-	-	-	-	-	ns
t <sub>en</sub>	enable time	nOE to nY; see Figure 6	[2]								
		V <sub>CC</sub> = 4.5 V		-	15	28	-	35	-	42	ns
t <sub>dis</sub>	disable time	nOE to nY; see Figure 6	[3]								
		V <sub>CC</sub> = 4.5 V		-	15	25	-	31	-	38	ns
t <sub>t</sub>	transition time	nY; see <u>Figure 5</u>	[4]	-	5	12	-	15	-	18	ns
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; f = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub> - 1.5 V	<u>[5]</u>	-	24	-	-	-	-	-	pF

- [1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [2]  $t_{en}$  is the same as  $t_{PZH}$  and  $t_{PZL}$ .
- [3]  $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .
- [4]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .
- [5]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

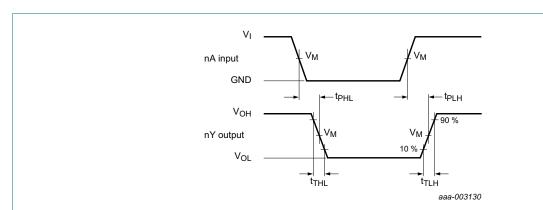
C<sub>L</sub> = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

### 11. Waveforms



Measurement points are given in Table 8.

V<sub>OL</sub> and V<sub>OH</sub> are typical voltage output levels that occur with the output load.

Fig 5. Propagation delay input (nA) to output (nY)

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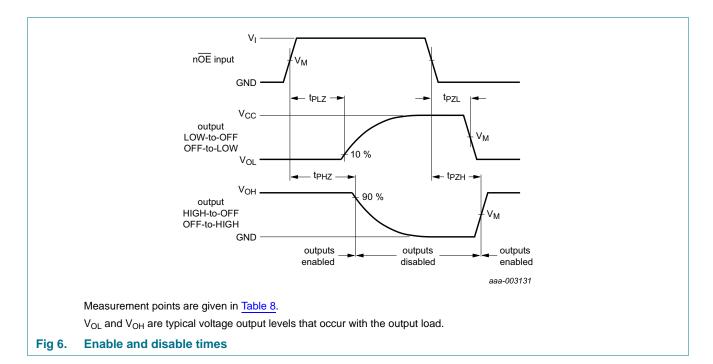
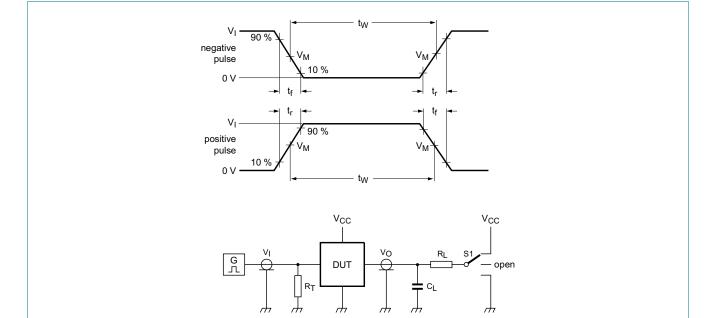


Table 8. Measurement points

Туре	Input	Output		
	V <sub>M</sub>	V <sub>M</sub>		
74HC125-Q100	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>		
74HCT125-Q100	1.3 V	1.3 V		

001aad983

Quad buffer/line driver; 3-state



Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

 $C_L$  = Load capacitance including jig and probe capacitance.

R<sub>L</sub> = Load resistance.

S1 = Test selection switch.

Fig 7. Test circuit for measuring switching times

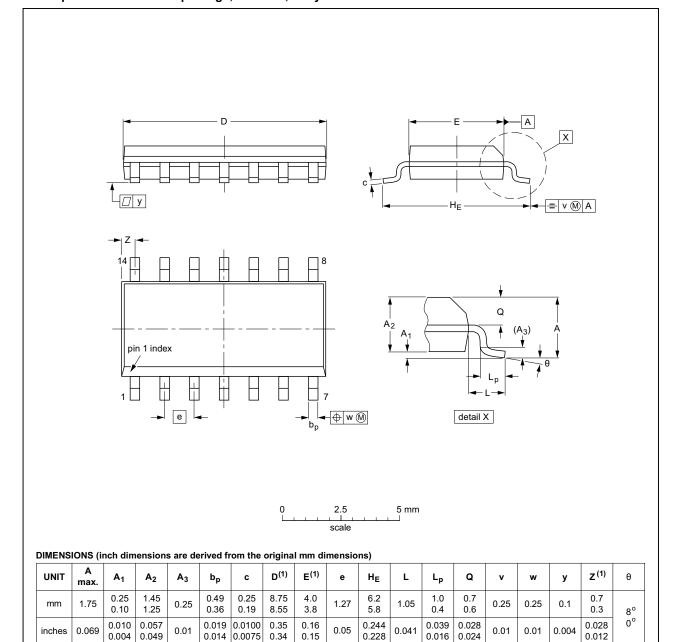
Table 9. Test data

Туре	Input		Load		S1 position			
	VI	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub> R <sub>L</sub>		t <sub>PHL</sub> , t <sub>PLH</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub>	
74HC125-Q100	V <sub>CC</sub>	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>	
74HCT125-Q100	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V <sub>CC</sub>	

### 12. Package outline

### SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



#### Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION		REFER	EUROPEAN	ISSUE DATE		
	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				<del>99-12-27</del> 03-02-19

Fig 8. Package outline SOT108-1 (SO14)

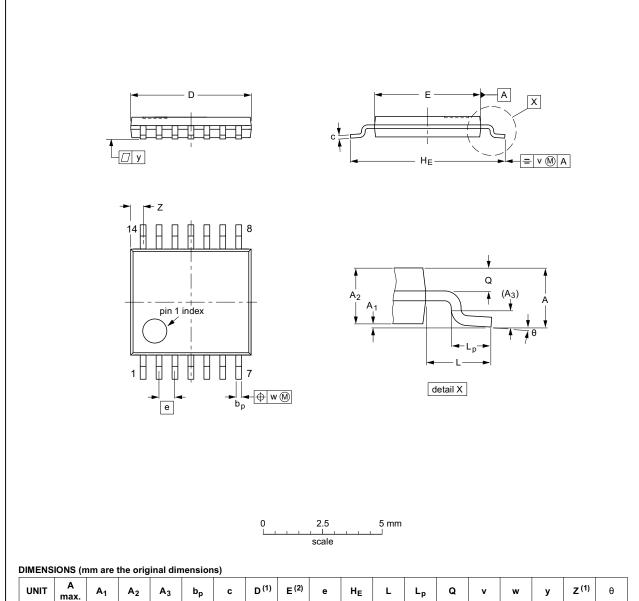
74HC\_HCT125\_Q100

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	bp	С	D <sup>(1)</sup>	E <sup>(2)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

	REFER	EUROPEAN	ISSUE DATE			
IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
	MO-153				<del>99-12-27</del> 03-02-18	
	IEC	IEC JEDEC	IEC JEDEC JEITA	IEC JEDEC JEITA	IEC JEDEC JEITA PROJECTION	

Fig 9. Package outline SOT402-1 (TSSOP14)

74HC\_HCT125\_Q100

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### 13. Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
MIL	Military
TTL	Transistor-Transistor Logic

# 14. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT125_Q100 v.2	20150119	Product data sheet	-	74HC_HCT125_Q100 v.1	
Modifications:	• <u>Table 7</u> : Power	er dissipation capacitance cond	dition for 74HCT125-	Q100 is corrected.	
74HC_HCT125_Q100 v.1	20130226	Product data sheet	-	-	

### 15. Legal information

#### 15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition					
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.					
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.					
Product [short] data sheet	Production	This document contains the product specification.					

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <a href="http://www.nexperia.com">http://www.nexperia.com</a>.

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74HC\_HCT125\_Q100

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### 16. Contact information

For more information, please visit: http://www.nexperia.com

For sales office addresses, please send an email to: salesaddresses@nexperia.com

# 74HC125-Q100; 74HCT125-Q100

### **Nexperia**

Quad buffer/line driver; 3-state

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