

A large, light blue graphic consisting of a thick curved line that forms a partial circle, with a small circle at its top end.

ISOFACE™

ISO1H815G

Galvanic Isolated 8 Channel High-Side Switch

Datasheet

Revision 2.2, 2013-01-31

Power Management & Multimarket

**Edition 2013-01-31**

**Published by  
Infineon Technologies AG  
81726 Munich, Germany**

**© 2013 Infineon Technologies AG  
All Rights Reserved.**

### **Legal Disclaimer**

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

### **Information**

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office ([www.infineon.com](http://www.infineon.com)).

### **Warnings**

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

## Revision History

| Page or Item                    | Subjects (major changes since previous revision)       |
|---------------------------------|--------------------------------------------------------|
| <b>Revision 2.2, 2013-01-31</b> |                                                        |
| Page 12                         | Page 12 table 4.1 Extended operating temperature added |
| <b>Revision 2.1</b>             |                                                        |
| Page 16                         | Page 16 table 4.8 updated                              |
| <b>Revision 2.0</b>             |                                                        |
| all                             | Final Datasheet                                        |

## Trademarks of Infineon Technologies AG

AURIX™, C166™, CanPAK™, CIPOS™, CIPURSE™, EconoPACK™, CoolMOS™, CoolSET™, CORECONTROL™, CROSSAVE™, DAVE™, DI-POL™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPIM™, EconoPACK™, EiceDRIVER™, eupec™, FCOS™, HITFET™, HybridPACK™, I<sup>2</sup>RF™, ISOFACE™, IsoPACK™, MIPAK™, ModSTACK™, my-d™, NovalithIC™, OptiMOS™, ORIGA™, POWERCODE™, PRIMARION™, PrimePACK™, PrimeSTACK™, PRO-SIL™, PROFET™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SIPMOS™, SmartLEWIS™, SOLID FLASH™, TEMPFET™, thinQ!™, TRENCHSTOP™, TriCore™.

## Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, KEIL™, PRIMECELL™, REALVIEW™, THUMB™, µVision™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Satellite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2011-11-11

### Coreless Transformer Isolated Digital Output 8 Channel 0.625 A High-Side Switch

#### Product Highlights

- Coreless transformer isolated data interface
- Galvanic isolation
- 8 High-side output switches 1,2A
- $\mu$ C compatible 8-bit parallel peripheral



#### Features

- Interface 3.3/5V CMOS operation compatible
- Parallel interface
- Direct control mode
- High common mode transient immunity
- Short circuit protection
- Maximum current internally limited
- Overload protection
- Overvoltage protection (including load dump)
- Undervoltage shutdown with autorestart and hysteresis
- Switching inductive loads
- Common output disable pin
- Thermal shutdown with restart
- Thermal independence of separate channels
- Common diagnostic output for overtemperature
- ESD protection
- Loss of GNDbb and loss of  $V_{bb}$  protection
- Reverse Output Voltage protection
- Isolated return path for DIAG signal
- RoHS compliant

#### Typical Application

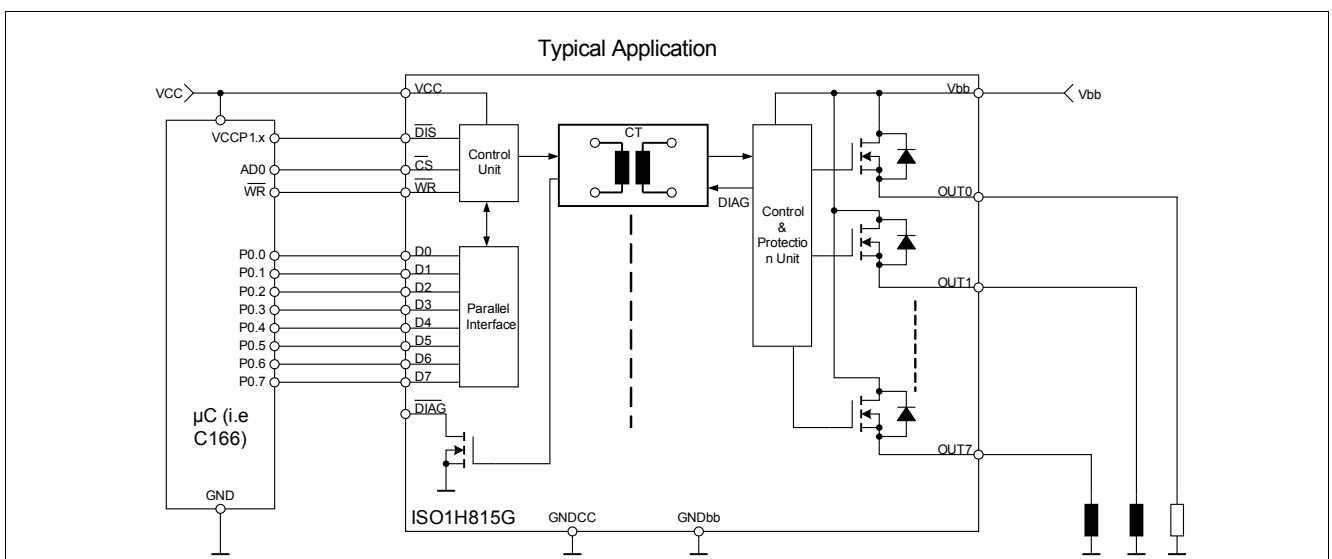
- Isolated switch for industrial applications (PLC)
- All types of resistive, inductive and capacitive loads
- $\mu$ C compatible power switch for 24V DC applications
- Driver for solenoid, relays and resistive loads

#### Description

The ISO1H815G is a galvanically isolated 8 bit data interface in PG-DSO-36 package that provides 8 fully protected high-side power switches that are able to handle currents up to 1.2A.

An 8 bit parallel  $\mu$ C compatible interface allows to connect the IC directly to a  $\mu$ C system. The input interface supports also a direct control mode and is designed to operate with 3.3/5V CMOS compatible levels.

The data transfer from input to output side is realized by

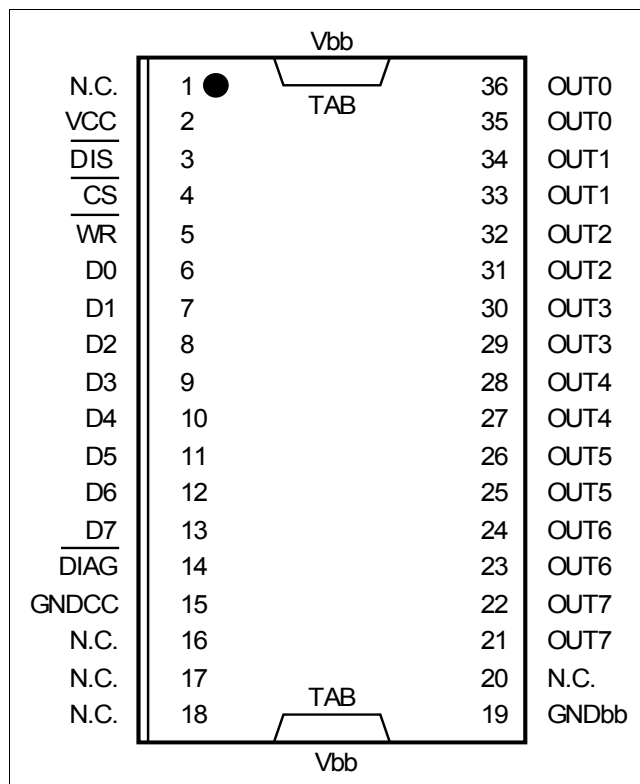


| Type      | On-state Resistance | Package  |
|-----------|---------------------|----------|
| ISO1H815G | 200m $\Omega$       | PG-DSO36 |

# 1 Pin Configuration and Functionality

## 1.1 Pin Configuration

| Pin | Symbol                   | Function                                     |
|-----|--------------------------|----------------------------------------------|
| 1   | N.C.                     | Not connected                                |
| 2   | VCC                      | Positive 3.3/5V logic supply                 |
| 3   | $\overline{\text{DIS}}$  | Output disable                               |
| 4   | $\overline{\text{CS}}$   | Chip select                                  |
| 5   | $\overline{\text{WR}}$   | Parallel write                               |
| 6   | D0                       | Data input bit0                              |
| 7   | D1                       | Data input bit1                              |
| 8   | D2                       | Data input bit2                              |
| 9   | D3                       | Data input bit3                              |
| 10  | D4                       | Data input bit4                              |
| 11  | D5                       | Data input bit5                              |
| 12  | D6                       | Data input bit6                              |
| 13  | D7                       | Data input bit7                              |
| 14  | $\overline{\text{DIAG}}$ | Common diagnostic output for overtemperature |
| 15  | GNDCC                    | Input logic ground                           |
| 16  | N.C.                     | Not connected                                |
| 17  | N.C.                     | Not connected                                |
| 18  | N.C.                     | Not connected                                |
| 19  | GNDbb                    | Output driver ground                         |
| 20  | N.C                      | Not connected                                |
| 21  | OUT7                     | High-side output of channel 7                |
| 22  | OUT7                     | High-side output of channel 7                |
| 23  | OUT6                     | High-side output of channel 6                |
| 24  | OUT6                     | High-side output of channel 6                |
| 25  | OUT5                     | High-side output of channel 5                |
| 26  | OUT5                     | High-side output of channel 5                |
| 27  | OUT4                     | High-side output of channel 4                |
| 28  | OUT4                     | High-side output of channel 4                |
| 29  | OUT3                     | High-side output of channel 3                |
| 30  | OUT3                     | High-side output of channel 3                |
| 31  | OUT2                     | High-side output of channel 2                |
| 32  | OUT2                     | High-side output of channel 2                |
| 33  | OUT1                     | High-side output of channel 1                |
| 34  | OUT1                     | High-side output of channel 1                |
| 35  | OUT0                     | High-side output of channel 0                |
| 36  | OUT0                     | High-side output of channel 0                |
| TAB | Vbb                      | Positive driver power supply voltage         |



**Figure 1 Power SO-36 (430mil)**

## 1.2 Pin Functionality

### VCC (Positive 3.3/5V logic supply)

The VCC supplies the input interface that is galvanically isolated from the output driver stage. The input interface can be supplied with 3.3/5V.

### $\overline{\text{DIS}}$ (Output disable)

The high-side outputs OUT0...OUT7 can be immediately switched off by means of the low active pin  $\overline{\text{DIS}}$  that is an asynchronous signal. The input registers are also reset by the  $\overline{\text{DIS}}$  signal. The Output remains switched off after low-high transition of  $\overline{\text{DIS}}$  signal, till new information is written into the input register. Current Sink to GNDCC.

### $\overline{\text{CS}}$ (Chip select)

The system microcontroller selects the ISO1H815G by means of the low active pin  $\overline{\text{CS}}$  to activate the parallel interface. By connecting the  $\overline{\text{CS}}$  pin and  $\overline{\text{WR}}$  pin to ground the parallel direct control is activated. Current Source to VCC.

### $\overline{\text{WR}}$ (Parallel write)

In parallel mode data at the input pins (D0 ... D7) are latched by means of the rising edge of the low active signal  $\overline{\text{WR}}$  (write). Current Source to VCC.

### D0 ... D7 (Data input bit0 ... bit7)

The present data can be latched on the rising edge of the write signal  $\overline{\text{WR}}$ . D0 ... D7 control the corresponding output channels OUT0 ...OUT7. By connecting CS and  $\overline{\text{WR}}$  to ground, the signals at D0 ... D7 directly control the outputs. Current Sink to GNDCC.

### $\overline{\text{DIAG}}$ (Common diagnostic output for overtemperature)

The low active  $\overline{\text{DIAG}}$  signal contains the OR-wired information of the separated overtemperature detection units for each channel. The output pin  $\overline{\text{DIAG}}$  provides an open drain functionality. A current source is also connected to the pin  $\overline{\text{DIAG}}$ . In normal operation the signal  $\overline{\text{DIAG}}$  is high. When overtemperature or Vbb below ON-Limit is detected the signal  $\overline{\text{DIAG}}$  changes to low.

### GNDCC (Ground for VCC domain)

This pin acts as the ground reference for the input interface that is supplied by VCC.

### GNDbb (Output driver ground domain)

This pin acts as the ground reference for the output

driver that is supplied by Vbb.

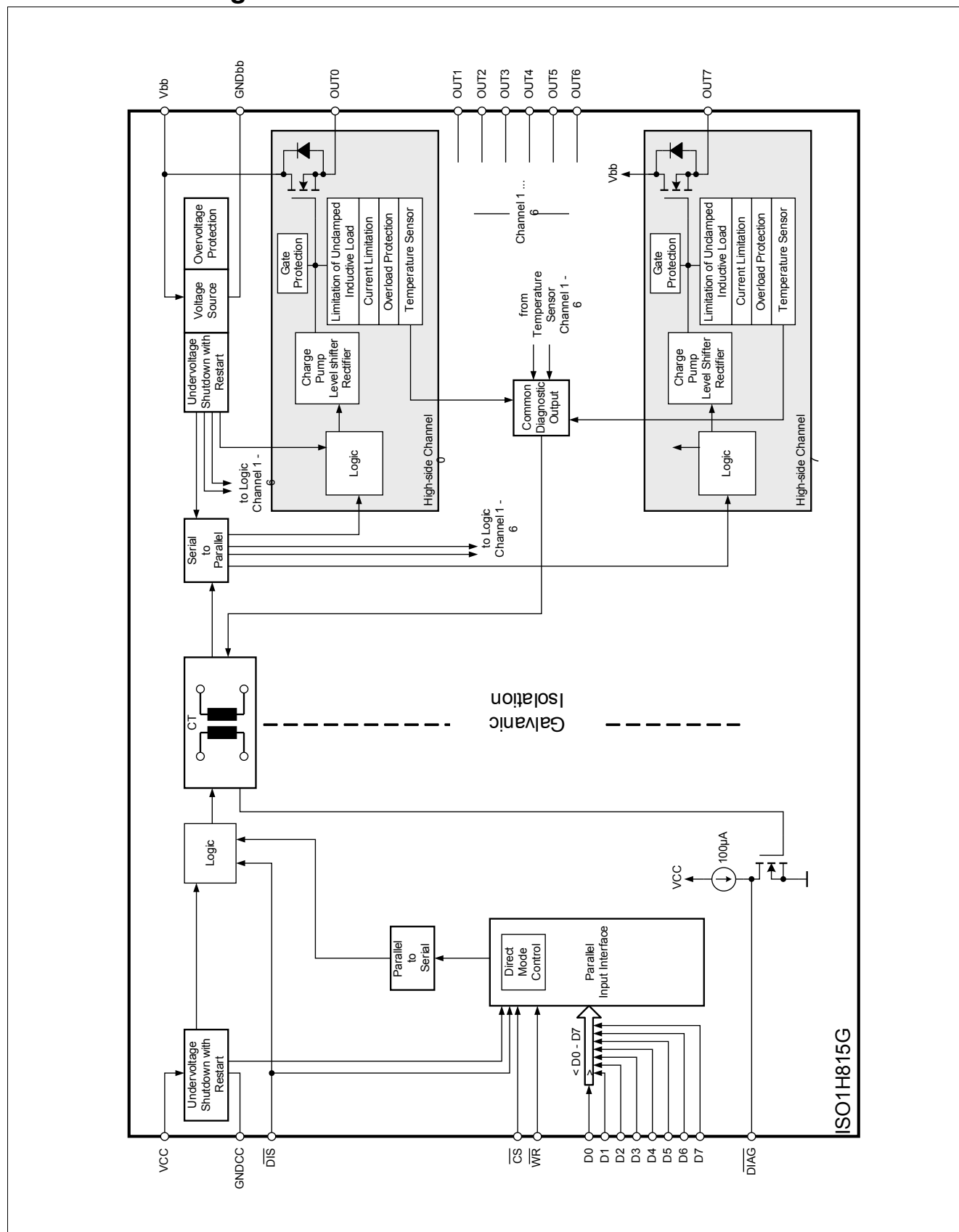
### OUT0 ... OUT7 (High side output channel 0 ... 7)

The output high side channels are internally connected to Vbb and controlled by the corresponding data input pins D0 ... D7 in parallel mode.

### TAB (Vbb, Positive supply for output driver)

The heatslug is connected to the positive supply port of the output interface.

## 2 Blockdiagram



**Figure 2 Blockdiagram**

## 3 Functional Description

### 3.1 Introduction

The ISOFACE ISO1H815G includes 8 high-side power switches that are controlled by means of the integrated parallel interface. The interface is 8bit  $\mu\text{C}$  compatible. Furthermore a direct control mode can be selected that allows the direct control of the outputs OUT0...OUT7 by means of the inputs D0...D7 without any additional logic signal. The IC can replace 8 optocouplers and the 8 high-side switches in conventional I/O-Applications as a galvanic isolation is implemented by means of the integrated coreless transformer technology. The  $\mu\text{C}$  compatible interfaces allow a direct connection to the ports of a microcontroller without the need for other components. Each of the 8 high-side power switches is protected against short to  $V_{bb}$ , overload, overtemperature and against overvoltage by an active zener clamp.

The diagnostic logic on the power chip recognizes the overtemperature information of each power transistor. The information is send via the internal coreless transformer to the pin DIAG at the input interface.

### 3.2 Power Supply

The IC contains 2 galvanic isolated voltage domains that are independent from each other. The input interface is supplied at VCC and the output stage is supplied at  $V_{bb}$ . The different voltage domains can be switched on at different time. The output stage is only enabled once the input stage enters a stable state.

### 3.3 Output Stage

Each channel contains a high-side vertical power FET that is protected by embedded protection functions.

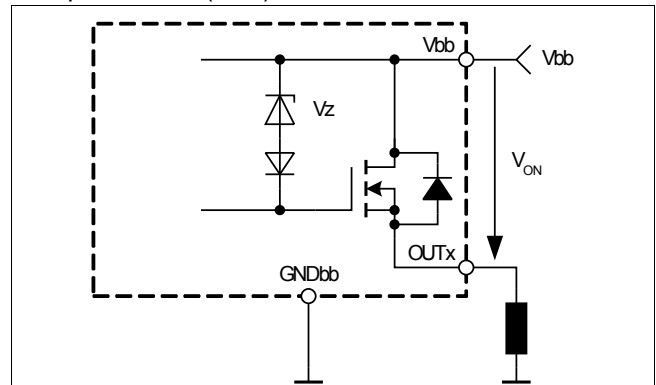
The continuous current for each channel is 1.2A (all channels ON).

#### 3.3.1 Output Stage Control

Each output is independently controlled by an output latch and a common reset line via the pin  $\overline{\text{DIS}}$  that disables all eight outputs and reset the latches. The parallel input data is transferred to the input latches with a high-to-low transition of the signal  $\overline{\text{WR}}$  (write) while the  $\overline{\text{CS}}$  is logic low. A low-to-high transition of  $\overline{\text{CS}}$  transfers then the data of the input latches to the output buffer.

#### 3.3.2 Power Transistor Overvoltage Protection

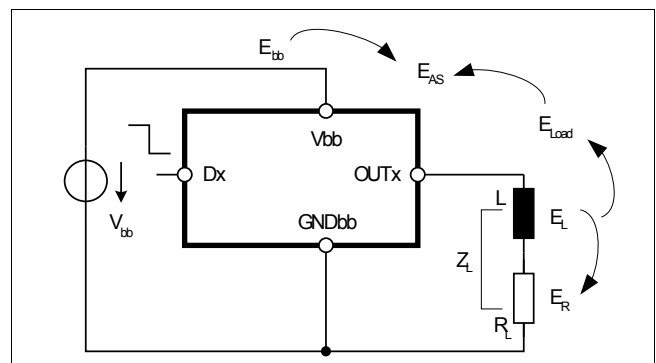
Each of the eight output stages has it own zener clamp that causes a voltage limitation at the power transistor when solenoid loads are switched off.  $V_{ON}$  is then clamped to 47V (min.).



**Figure 3 Inductive and overvoltage output clamp (each channel)**

Energy is stored in the load inductance during an inductive load switch-off.

$$E_L = 1/2 \times L \times I_L^2$$



**Figure 4 Inductive load switch-off energy dissipation (each channel)**

While demagnetizing the load inductance, the energy dissipation in the DMOS is

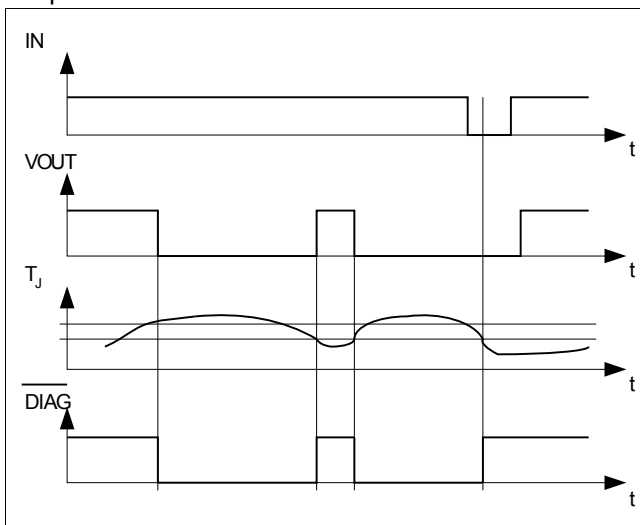
$$E_{AS} = E_{bb} + E_L - E_R = V_{ON(CL)} \times i_L(t) dt$$

with an approximate solution for  $R_L > 0\Omega$ :

$$E_{AS} = \frac{I_L \times L}{2 \times R_L} \times (V_{bb} + |V_{ON(CL)}|) \times \ln\left(1 + \frac{I_L \times R_L}{|V_{ON(CL)}|}\right)$$

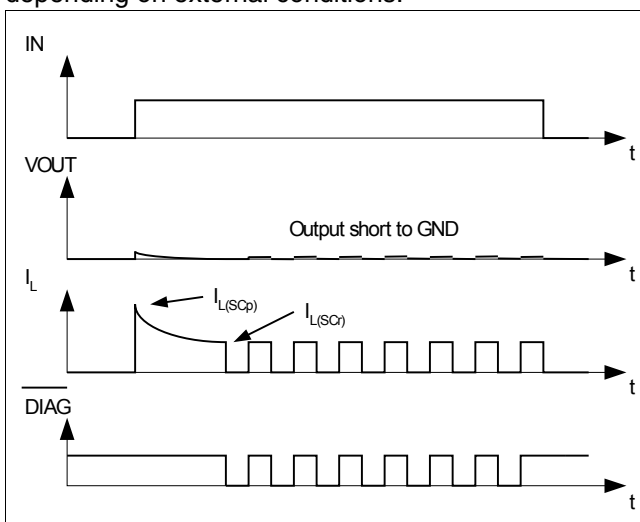
### 3.3.3 Power Transistor Overcurrent Protection

The outputs are provided with a current limitation that enters a repetitive switched mode after an initial peak current has been exceeded. The initial peak short circuit current limit is set to  $I_{L(SCP)}$ . During the repetitive mode short circuit current the limit is set to  $I_{L(SCR)}$ . If this operation leads to an overtemperature condition, a second protection level ( $T_j > 135^\circ\text{C}$ ) will change the output into a low duty cycle PWM (selective thermal shutdown with restart) to prevent critical chip temperatures.

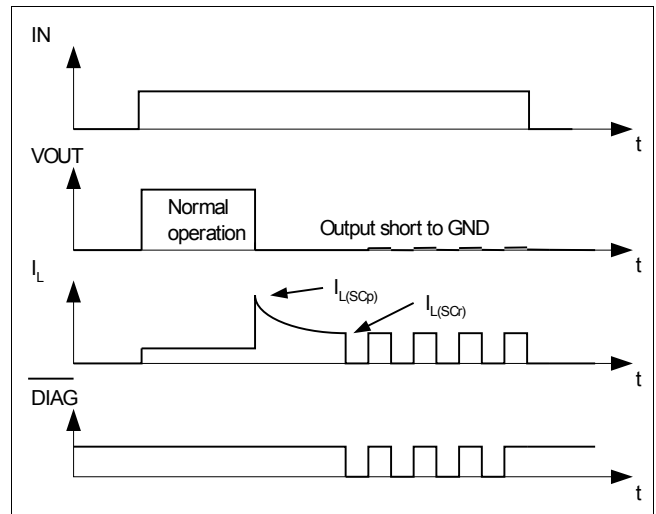


**Figure 5 Overtemperature detection**

The following figures show the timing for a turn on into short circuit and a short circuit in on-state. Heating up of the chip may require several milliseconds, depending on external conditions.



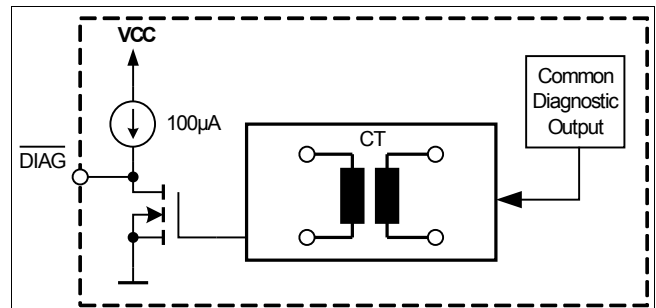
**Figure 6 Turn on into short circuit, shut down by overtemperature, restart by cooling**



**Figure 7 Short circuit in on-state, shut down by overtemperature, restart by cooling**

### 3.4 Common Diagnostic Output

The overtemperature detection information are OR-wired in the common diagnostic output block. The information is send via the integrated coreless transformer to the input interface. The output stage at pin DIAG has an open drain functionality combined with a current source.



**Figure 8 Common diagnostic output**

### 3.5 Parallel Interface

The ISO1H815G contains a parallel interface that can be directly controlled by the microcontroller output ports. The parallel interface can also be switched over to a direct control that allows direct changes of the outputs OUT0 ... OUT7 by means of the corresponding inputs D0 ... D7 without additional logic signals. To activate the parallel direct control mode pin  $\overline{CS}$  and pin  $\overline{WR}$  have to be connected both to ground.

#### 3.5.1 Parallel Interface Signal Description

$\overline{CS}$  - Chip select. The system microcontroller selects the ISO1H815G by means of the  $\overline{CS}$  pin. Whenever the pin is in a logic low state, data can be transferred from the  $\mu C$ .

$\overline{CS}$  High to low transition:



- Parallel input data can be written in from then on

$\overline{CS}$  Low to high transition:



- The data in the input latches is transferred to the output buffer

$\overline{WR}$  - Write. The system controller enables the write procedure in the ISO1H815G by means of the signal  $\overline{WR}$ . A logic low state signal at pin  $\overline{WR}$  writes the input data into the input latches when the  $\overline{CS}$  pin is in a logic low state.

$\overline{WR}$  Logic low level:



- Parallel input data at the pins D0 - D7 is written into the input latches

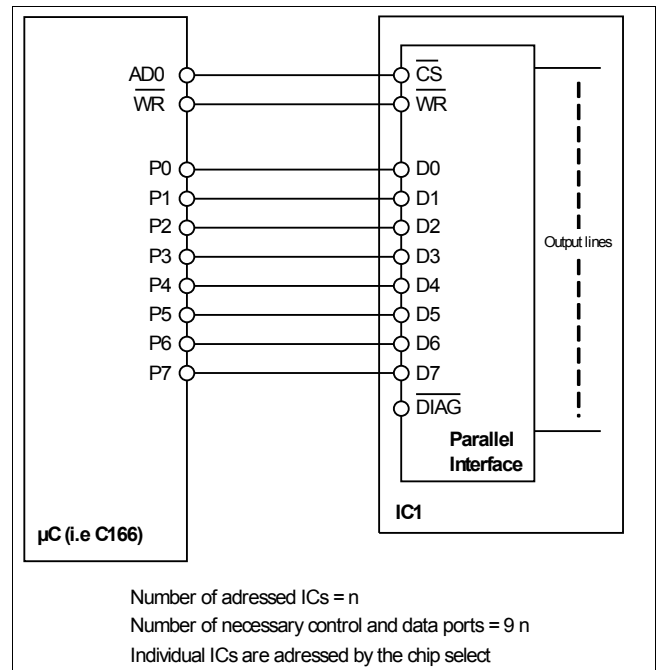
$\overline{WR}$  Logic high level:



- The parallel input data is latched in the input latches. Any changes at the pins D0 - D7 after the low-to-high transition of  $\overline{WR}$  do not affect the input latches.

**D0 ... D7** - Parallel input. Parallel data bits are fed into the pins D0 ... D7. The data is written into the input latches when  $\overline{WR}$  is logic low.

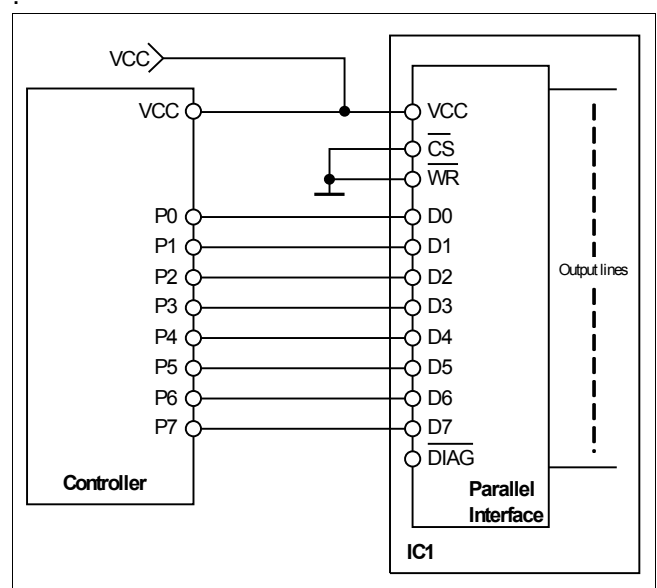
#### 3.5.2 $\mu C$ Control Mode



**Figure 9 Parallel bus configuration**

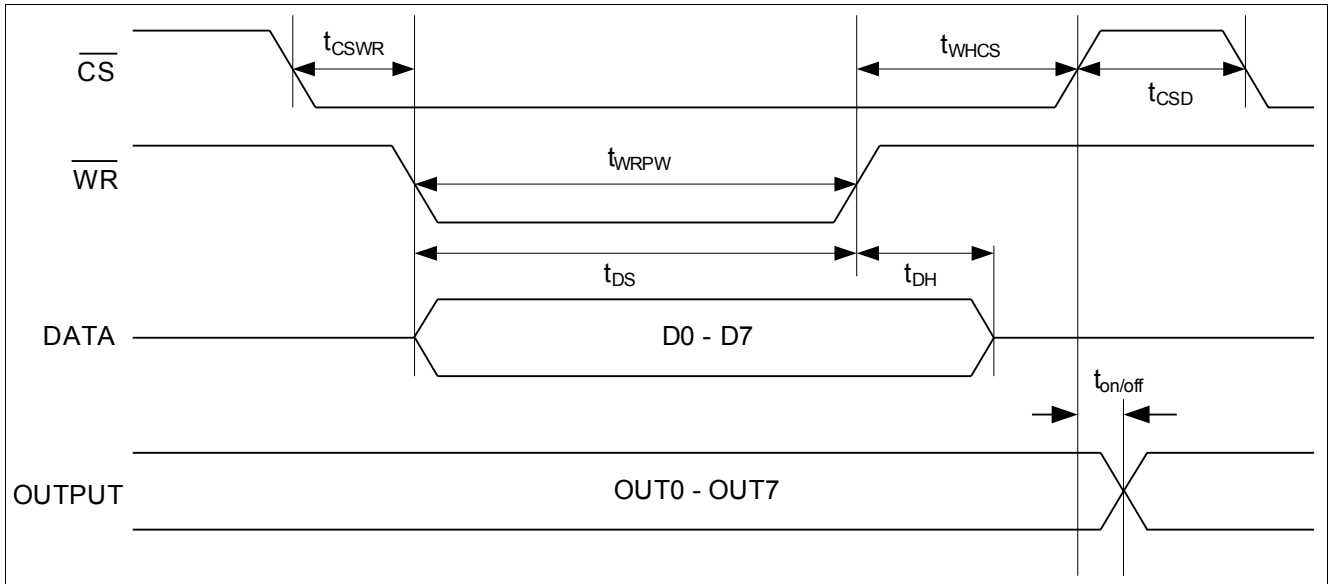
#### 3.5.3 Direct Control Mode

Beside the use of the parallel  $\mu C$  compatible interface a parallel direct control mode can be chosen. In this mode the output OUT0...OUT7 can be directly controlled via the inputs D0...D7 without the need for additional logic signals. To activate this mode pin  $\overline{CS}$  and  $\overline{WR}$  need to be connected to ground.



**Figure 10 Parallel Direct Control**

### 3.6 Parallel Interface Timing



**Figure 11** Parallel input - output timing diagram

### 3.7 Transmission Failure Detection

There is a failure detection unit integrated to ensure also a stable functionality during the integrated coreless transformer transmission. This unit decides whether the transmitted data is valid or not. If four times serial data coming in from the internal registers is not accepted, the output stages are switched off until the next valid data is received.

## 4 Electrical Characteristics

*Note: All voltages at pins 2 to 14 are measured with respect to ground GNDCC (pin 15). All voltages at pin 20 to pin 36 and TAB are measured with respect to ground GNDbb (pin 19). The voltage levels are valid if other ratings are not violated. The two voltage domains  $V_{CC}$  and  $V_{bb}$  are internally galvanic isolated.*

### 4.1 Absolute Maximum Ratings

*Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 2 ( $V_{CC}$ ) and TAB ( $V_{bb}$ ) is discharged before assembling the application circuit. Supply voltages higher than  $V_{bb(AZ)}$  require an external current limit for the GNDbb pin, e.g. with a  $15\Omega$  resistor in GNDbb connection. Operating at absolute maximum ratings can lead to a reduced lifetime.*

| Parameter<br>at $T_j = -40 \dots 135^\circ\text{C}$ , unless otherwise specified                                                                                                                                                                                          | Symbol         | Limit Values     |                  | Unit |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|------------------|------------------|------|
|                                                                                                                                                                                                                                                                           |                | min.             | max.             |      |
| Supply voltage input interface ( $V_{CC}$ )                                                                                                                                                                                                                               | $V_{CC}$       | -0.5             | 6.5              | V    |
| Supply voltage output interface ( $V_{bb}$ )                                                                                                                                                                                                                              | $V_{bb}$       | -1 <sup>1)</sup> | 45               |      |
| Continuous voltage at data inputs (D0 ... D7)                                                                                                                                                                                                                             | $V_{Dx}$       | -0.5             | 6.5              |      |
| Continuous voltage at pin $\overline{CS}$                                                                                                                                                                                                                                 | $V_{CS}$       | -0.5             | 6.5              |      |
| Continuous voltage at pin $\overline{WR}$                                                                                                                                                                                                                                 | $V_{WR}$       | -0.5             | 6.5              |      |
| Continuous voltage at pin $\overline{DIS}$                                                                                                                                                                                                                                | $V_{DIS}$      | -0.5             | 6.5              |      |
| Continuous voltage at pin $\overline{DIAG}$                                                                                                                                                                                                                               | $V_{DIAG}$     | -0.5             | 6.5              |      |
| Load current (short-circuit current)                                                                                                                                                                                                                                      | $I_L$          | —                | self limited     | A    |
| Reverse current through GNDbb <sup>1)</sup>                                                                                                                                                                                                                               | $I_{GNDbb}$    | -1.6             | —                |      |
| Operating Temperature                                                                                                                                                                                                                                                     | $T_j$          | -25              | internal limited | °C   |
| Extended Operation Temperature <sup>2)</sup>                                                                                                                                                                                                                              | $T_j$          | -40              | internal limited |      |
| Power Dissipation <sup>3)</sup>                                                                                                                                                                                                                                           | $P_{tot}$      | —                | 3.3              | W    |
| Inductive load switch-off energy dissipation <sup>4)</sup> single pulse, $T_j = 125^\circ\text{C}$ , $I_L = 1.2\text{A}$<br>one channel active<br>all channel simultaneously active (each channel)                                                                        | $E_{AS}$       | —                | 5<br>0.5         | J    |
| Load dump protection <sup>3)</sup> $V_{loadDump}^{5)} = V_A + V_S$<br>$V_{IN} = \text{low or high}$<br>$t_d = 400\text{ms}$ , $R_I = 2\Omega$ , $R_L = 27\Omega$ , $V_A = 13.5\text{V}$<br>$t_d = 350\text{ms}$ , $R_I = 2\Omega$ , $R_L = 57\Omega$ , $V_A = 27\text{V}$ | $V_{Loaddump}$ |                  | 90<br>117        | V    |
| Electrostatic discharge voltage (Human Body Model) according to JESD22-A114-B                                                                                                                                                                                             | $V_{ESD}$      |                  | 2                | kV   |
| Electrostatic discharge voltage (Charge Device Model) according to ESD STM5.3.1 - 1999                                                                                                                                                                                    | $V_{ESD}$      |                  | 1                | kV   |
| Continuous reverse drain current <sup>1)3)</sup> , each channel                                                                                                                                                                                                           | $I_S$          | —                | 4                | A    |

1) defined by  $P_{tot}$

2) not subject to production test, slight deviation of electrical parameters possible.

3) Device on 50mm\*50mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70μm thick) copper area for drain connection. PCB is vertical without blown air.

4) not subject to production test, specified by design

5)  $V_{Loaddump}$  is setup without the DUT connected to the generator per ISO7637-1 and DIN40839

## 4.2 Thermal Characteristics

| Parameter<br>at $T_j = -25 \dots 125^\circ\text{C}$ , $V_{bb}=15\dots 30\text{V}$ , $V_{CC}=3.0\dots 5.5\text{V}$ , unless otherwise specified | Symbol       | Limit Values |      |      | Unit | Test Condition |
|------------------------------------------------------------------------------------------------------------------------------------------------|--------------|--------------|------|------|------|----------------|
|                                                                                                                                                |              | min.         | typ. | max. |      |                |
| Thermal resistance junction - case                                                                                                             | $R_{thJC}$   | —            | —    | 1.5  | K/W  |                |
| Thermal resistance @ min. footprint                                                                                                            | $R_{th(JA)}$ | —            | —    | 50   |      |                |
| Thermal resistance @ 6cm <sup>2</sup> cooling area <sup>1)</sup>                                                                               | $R_{th(JA)}$ | —            | —    | 38   |      |                |

1) Device on 50mm\*50mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70μm thick) copper area for drain connection. PCB is vertical without blown air.

## 4.3 Load Switching Capabilities and Characteristics

| Parameter<br>at $T_j = -25 \dots 125^\circ\text{C}$ , $V_{bb}=15\dots 30\text{V}$ , $V_{CC}=3.0\dots 5.5\text{V}$ , unless otherwise specified                                                                                                          | Symbol         | Limit Values |                        |                         | Unit | Test Condition |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|--------------|------------------------|-------------------------|------|----------------|
|                                                                                                                                                                                                                                                         |                | min.         | typ.                   | max.                    |      |                |
| On-state resistance, $I_L = 0.5\text{A}$ , each channel<br>$T_j = 25^\circ\text{C}$<br>$T_j = 125^\circ\text{C}$<br>two parallel channels, $T_j = 25^\circ\text{C}$ : <sup>1)</sup><br>four parallel channels, $T_j = 25^\circ\text{C}$ : <sup>1)</sup> | $R_{ON}$       | —<br>—       | 150<br>270<br>75<br>38 | 200<br>320<br>100<br>50 | mΩ   |                |
| Nominal load current<br>Device on PCB 38K/W, $T_a = 85^\circ\text{C}$ , $T_j < 125^\circ\text{C}$<br>one channel: <sup>1)</sup><br>two parallel channels: <sup>1)</sup><br>four parallel channels: <sup>1)</sup>                                        | $I_{L(NOM)}$   |              | 1.4<br>2.2<br>4.4      |                         | A    |                |
| Turn-on time to 90% $V_{OUT}$ <sup>2)</sup><br>$R_L = 47\Omega$ , $V_{Dx} = 0$ to 5V                                                                                                                                                                    | $t_{on}$       | —            | 64                     | 120                     | μs   |                |
| Turn-off time to 10% $V_{OUT}$ <sup>2)</sup><br>$R_L = 47\Omega$ , $V_{Dx} = 5$ to 0V                                                                                                                                                                   | $t_{off}$      | —            | 89                     | 170                     |      |                |
| Slew rate on 10 to 30% $V_{OUT}$<br>$R_L = 47\Omega$ , $V_{bb} = 15\text{V}$                                                                                                                                                                            | $dV/dt_{on}$   | —            | 1                      | 2                       | V/μs |                |
| Slew rate off 70 to 40% $V_{OUT}$<br>$R_L = 47\Omega$ , $V_{bb} = 15\text{V}$                                                                                                                                                                           | $-dV/dt_{off}$ | —            | 1                      | 2                       |      |                |

1) not subject to production test, specified by design

2) The turn-on and turn-off time includes the switching time of the high-side switch and the transmission time via the coreless transformer in normal operating mode. During a failure on the coreless transformer transmission turn-on or turn-off time can increase by up to 50μs.

## 4.4 Operating Parameters

| Parameter<br>at $T_j = -25 \dots 125^\circ\text{C}$ , $V_{bb}=15\dots 30\text{V}$ , $V_{CC}=3.0\dots 5.5\text{V}$ , unless otherwise specified | Symbol              | Limit Values |      |      | Unit  | Test Condition                 |
|------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|--------------|------|------|-------|--------------------------------|
|                                                                                                                                                |                     | min.         | typ. | max. |       |                                |
| Common mode transient immunity <sup>1)</sup>                                                                                                   | $\Delta V_{ISO}/dt$ | -25          | -    | 25   | kV/μs | $\Delta V_{ISO} = 200\text{V}$ |
| Magnetic field immunity <sup>1)</sup>                                                                                                          | $H_{IM}$            | 100          |      |      | A/m   | IEC61000-4-8                   |

**Electrical Characteristics**

|                                               |                                                                                                |                        |     |     |      |         |                           |
|-----------------------------------------------|------------------------------------------------------------------------------------------------|------------------------|-----|-----|------|---------|---------------------------|
| Voltage domain $V_{bb}$<br>(Output interface) | Operating voltage                                                                              | $V_{bb}$               | 11  | —   | 35   | V       |                           |
|                                               | Undervoltage shutdown                                                                          | $V_{bb(under)}$        | 7   | —   | 10.5 |         |                           |
|                                               | Undervoltage restart                                                                           | $V_{bb(u\_rst)}$       | —   | —   | 11   |         |                           |
|                                               | Undervoltage hysteresis                                                                        | $\Delta V_{bb(under)}$ | —   | 0.5 | —    |         |                           |
|                                               | Undervoltage current                                                                           | $I_{bb(uvlo)}$         | —   | 1   | 2.5  | mA      | $V_{bb} < 7V$             |
|                                               | Operating current                                                                              | $I_{GNDL}$             | —   | 10  | 14   | mA      | All Channels ON - no load |
|                                               | Leakage output current<br>(included in $I_{bb(off)}$ )<br>$V_{Dx} = \text{low}$ , each channel | $I_{L(off)}$           | —   | 5   | 30   | $\mu A$ |                           |
| Voltage domain $V_{CC}$<br>(Input interface)  | Operating voltage                                                                              | $V_{CC}$               | 3.0 | —   | 5.5  | V       |                           |
|                                               | Undervoltage shutdown                                                                          | $V_{CC(under)}$        | 2.5 | —   | 2.9  |         |                           |
|                                               | Undervoltage restart                                                                           | $V_{CC(u\_rst)}$       | —   | —   | 3    |         |                           |
|                                               | Undervoltage hysteresis                                                                        | $\Delta V_{CC(under)}$ | —   | 0.1 | —    |         |                           |
|                                               | Undervoltage current                                                                           | $I_{CC(uvlo)}$         | —   | 1   | 2    | mA      | $V_{cc} < 2.5V$           |
|                                               | Operating current                                                                              | $I_{CC(on)}$           | —   | 4.5 | 6    | mA      |                           |

1) not subject to production test

**Electrical Characteristics**
**4.5 Output Protection Functions**

| Parameter <sup>1)</sup><br>at $T_j = -25 \dots 125^\circ\text{C}$ , $V_{bb}=15\dots30\text{V}$ , $V_{CC}=3.0\dots5.5\text{V}$ , unless<br>otherwise specified                                                                                                                      | Symbol          | Limit Values                                                              |                   |               | Unit | Test Condition |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------------------------------------------------------------------|-------------------|---------------|------|----------------|
|                                                                                                                                                                                                                                                                                    |                 | min.                                                                      | typ.              | max.          |      |                |
| Initial peak short circuit current limit, each channel<br>$T_j = -25^\circ\text{C}$ , $V_{bb} = 30\text{V}$ , $t_m = 700\mu\text{s}$<br>$T_j = 25^\circ\text{C}$<br>$T_j = 125^\circ\text{C}$<br><br>two parallel channels: <sup>3)</sup><br>four parallel channels: <sup>3)</sup> | $I_{L(SCp)}$    | —<br>—<br>1.4                                                             | —<br>3.0<br>—     | 4.5<br>—<br>— | A    |                |
|                                                                                                                                                                                                                                                                                    |                 | twice the current of one channel<br>four times the current of one channel |                   |               |      |                |
| Repetitive short circuit current limit <sup>3)</sup><br>$T_j = T_{jt}$ (see timing diagrams)<br><br>each channel:<br>two parallel channels: <sup>3)</sup><br>four parallel channels: <sup>3)</sup>                                                                                 | $I_{L(SCr)}$    | —                                                                         | 2.2<br>2.2<br>2.2 | —             |      |                |
| Output clamp (inductive load switch off)<br>at $V_{OUT} = V_{bb} - V_{ON(CL)}$                                                                                                                                                                                                     | $V_{ON(CL)}$    | 47                                                                        | 53                | 60            | V    |                |
| Overvoltage protection                                                                                                                                                                                                                                                             | $V_{bb(AZ)}$    | 47                                                                        | —                 | —             |      |                |
| Thermal overload trip temperature <sup>2)3)</sup>                                                                                                                                                                                                                                  | $T_{jt}$        | 135                                                                       | —                 | —             | °C   |                |
| Thermal hysteresis <sup>3)</sup>                                                                                                                                                                                                                                                   | $\Delta T_{jt}$ | —                                                                         | 10                | —             | K    |                |

- 1) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.
- 2) Higher operating temperature at normal function for each channel available
- 3) not subject to production test, specified by design

**4.6 Diagnostic Characteristics at pin  $\overline{\text{DIAG}}$** 

| Parameter<br>at $T_j = -25 \dots 125^\circ\text{C}$ , $V_{bb}=15\dots30\text{V}$ , $V_{CC}=3.0\dots5.5\text{V}$ , unless<br>otherwise specified | Symbol           | Limit Values |      |      | Unit | Test Condition                    |
|-------------------------------------------------------------------------------------------------------------------------------------------------|------------------|--------------|------|------|------|-----------------------------------|
|                                                                                                                                                 |                  | min.         | typ. | max. |      |                                   |
| Common diagnostic sink current<br>(overtemperature of any channel) $T_j = 135^\circ\text{C}$                                                    | $I_{diagsink}$   |              |      | 5    | mA   | $V_{diagon} < 0.25 \times V_{CC}$ |
| Common diagnostic source current                                                                                                                | $I_{diagsource}$ |              | 100  |      | μA   |                                   |

**Electrical Characteristics**
**4.7 Input Interface**

| Parameter<br>at $T_j = -25 \dots 125^\circ\text{C}$ , $V_{bb}=15\dots30\text{V}$ , $V_{CC}=3.0\dots5.5\text{V}$ , unless otherwise specified                         | Symbol      | Limit Values        |      |                     | Unit          | Test Condition |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|---------------------|------|---------------------|---------------|----------------|
|                                                                                                                                                                      |             | min.                | typ. | max.                |               |                |
| Input low state voltage<br>(D0 ... D7, $\overline{\text{DIS}}$ , $\overline{\text{CS}}$ , $\overline{\text{WR}}$ )                                                   | $V_{IL}$    | -0.3                | —    | $0.3 \times V_{CC}$ | V             |                |
| Input high state voltage<br>(D0 ... D7, $\overline{\text{DIS}}$ , $\overline{\text{CS}}$ , $\overline{\text{WR}}$ )                                                  | $V_{IH}$    | $0.7 \times V_{CC}$ | —    | $V_{CC} + 0.3$      |               |                |
| Input voltage hysteresis<br>(D0 ... D7, $\overline{\text{DIS}}$ , $\overline{\text{CS}}$ , $\overline{\text{WR}}$ )                                                  | $V_{IHys}$  |                     | 100  |                     | mV            |                |
| Input pull down current<br>(D0 ... D7, $\overline{\text{DIS}}$ )                                                                                                     | $I_{Idown}$ |                     | 100  |                     | $\mu\text{A}$ |                |
| Input pull up current<br>( $\overline{\text{CS}}$ , $\overline{\text{WR}}$ )                                                                                         | $-I_{Iup}$  |                     | 100  |                     |               |                |
| Output disable time (transition $\overline{\text{DIS}}$ to logic low) <sup>1)2)</sup><br>Normal operation<br>Turn-off time to 10% $V_{OUT}$<br>$R_L = 47\Omega$      | $t_{DIS}$   | ---                 | 85   | 170                 | $\mu\text{s}$ |                |
| Output disable time (transition $\overline{\text{DIS}}$ to logic low) <sup>1)2)3)</sup><br>Disturbed operation<br>Turn-off time to 10% $V_{OUT}$<br>$R_L = 47\Omega$ | $t_{DIS}$   | ---                 | ---  | 230                 |               |                |

- 1) The time includes the turn-on/off time of the high-side switch and the transmission time via the coreless transformer.
- 2) If Pin  $\overline{\text{DIS}}$  is set to low the outputs are set to low; after  $\overline{\text{DIS}}$  set to high a new write cycle is necessary to set the output again.
- 3) The parameter is not subject to production test - verified by design/characterization

**4.8 Parallel Interface Input Timing**

| Parameter<br>at $T_j = -25 \dots 125^\circ\text{C}$ , $V_{bb}=15\dots30\text{V}$ , $V_{CC}=3.0\dots5.5\text{V}$ , unless otherwise specified | Symbol     | Limit Values |      |      | Unit          | Test Condition |
|----------------------------------------------------------------------------------------------------------------------------------------------|------------|--------------|------|------|---------------|----------------|
|                                                                                                                                              |            | min.         | typ. | max. |               |                |
| $\overline{\text{WR}}$ pulse width                                                                                                           | $t_{WRPW}$ | 20           | —    | —    | ns            |                |
| Data setup time before $\overline{\text{WR}}$                                                                                                | $t_{DS}$   | 20           | —    | —    |               |                |
| Data hold time after $\overline{\text{WR}}$                                                                                                  | $t_{DH}$   | 10           | —    | —    |               |                |
| Chip select valid to $\overline{\text{WR}}$                                                                                                  | $t_{CSWR}$ | 0            | —    | —    |               |                |
| $\overline{\text{WR}}$ logic high to $\overline{\text{CS}}$ logic high                                                                       | $t_{WHCS}$ | 10           | —    | —    |               |                |
| Delay to next $\overline{\text{CS}}$ cycle                                                                                                   | $t_{CSD}$  | 20           | —    | —    | $\mu\text{s}$ |                |
| Output data refresh rate in direct control mode                                                                                              | $t_{OR}$   | 20           | —    | —    |               |                |

## 4.9 Reverse Voltage

| Parameter<br>at $T_j = -25 \dots 125^\circ\text{C}$ , $V_{bb}=15\dots30\text{V}$ , $V_{CC}=3.0\dots5.5\text{V}$ , unless otherwise specified | Symbol    | Limit Values |      |         | Unit | Test Condition |
|----------------------------------------------------------------------------------------------------------------------------------------------|-----------|--------------|------|---------|------|----------------|
|                                                                                                                                              |           | min.         | typ. | max.    |      |                |
| Reverse voltage <sup>1)2)</sup><br>$R_{GND} = 0 \Omega$<br>$R_{GND} = 150 \Omega$                                                            | $-V_{bb}$ | —            | —    | 1<br>45 | V    |                |
| Diode forward on voltage<br>$I_F = 1.25\text{A}$ , $V_{Dx} = \text{low}$ , each channel                                                      | $-V_{ON}$ | —            | —    | 1.2     |      |                |

1) defined by  $P_{tot}$

2) not subject to production test, specified by design

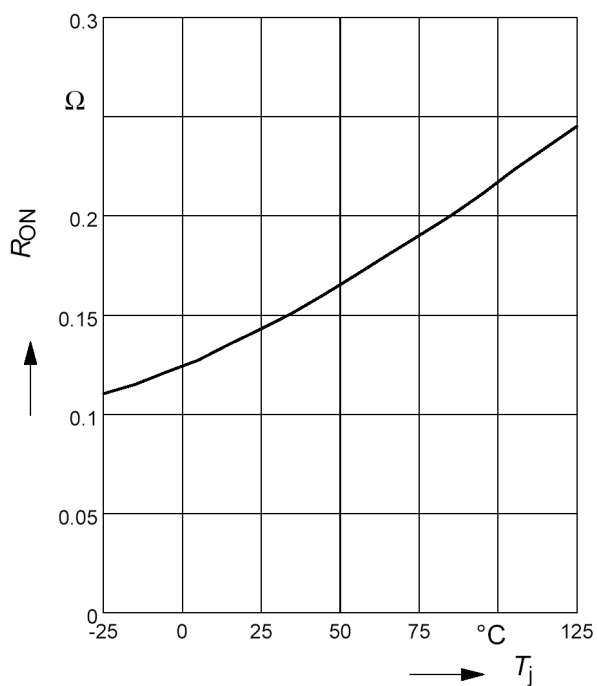
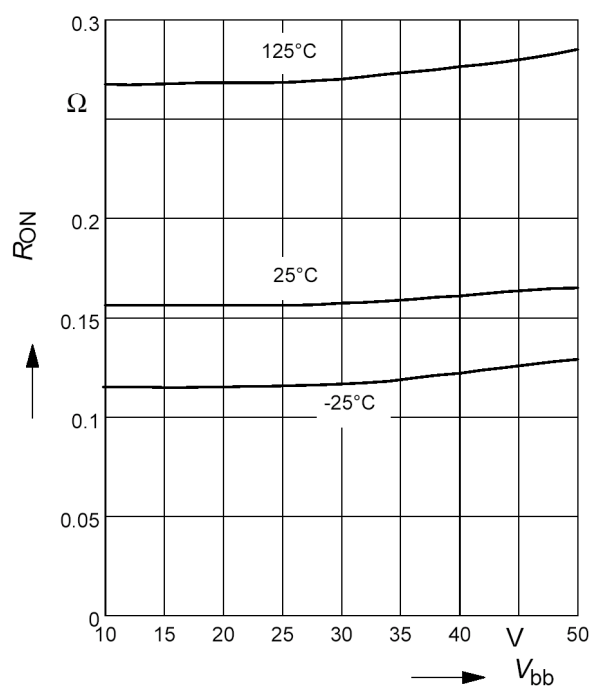
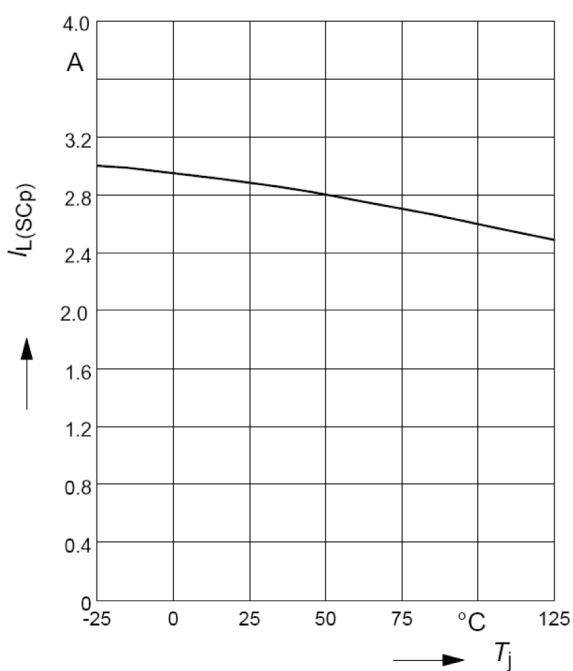
## 4.10 Isolation and Safety-Related Specification

| Parameter<br>Measured from input terminals to output terminals, unless otherwise specified | Value | Unit     | Conditions                             |
|--------------------------------------------------------------------------------------------|-------|----------|----------------------------------------|
| Rated dielectric isolation voltage $V_{ISO}$                                               | 500   | $V_{AC}$ | 1 - minute duration <sup>1)</sup>      |
| Short term temporary overvoltage                                                           | 1250  | V        | 5s acc. DIN EN60664-1 <sup>1)</sup>    |
| Minimum external air gap (clearance)                                                       | 2.6   | mm       | shortest distance through air.         |
| Minimum external tracking (creepage)                                                       | 2.6   | mm       | shortest distance path along body.     |
| Minimum Internal Gap                                                                       | 0.01  | mm       | Insulation distance through insulation |

1) The parameter is not subject to production test, verified by characterization; Production Test with 1100V, 100ms duration

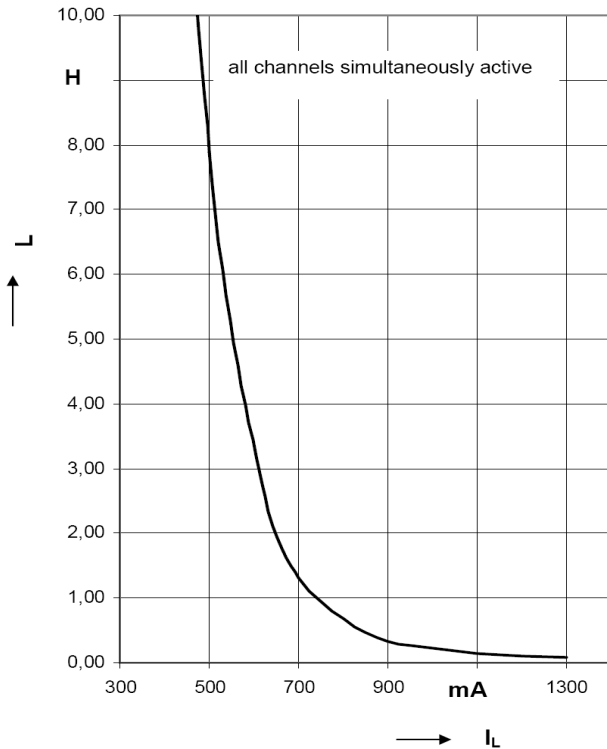
## 4.11 Reliability

For Qualification Report please contact your local Infineon Technologies office!

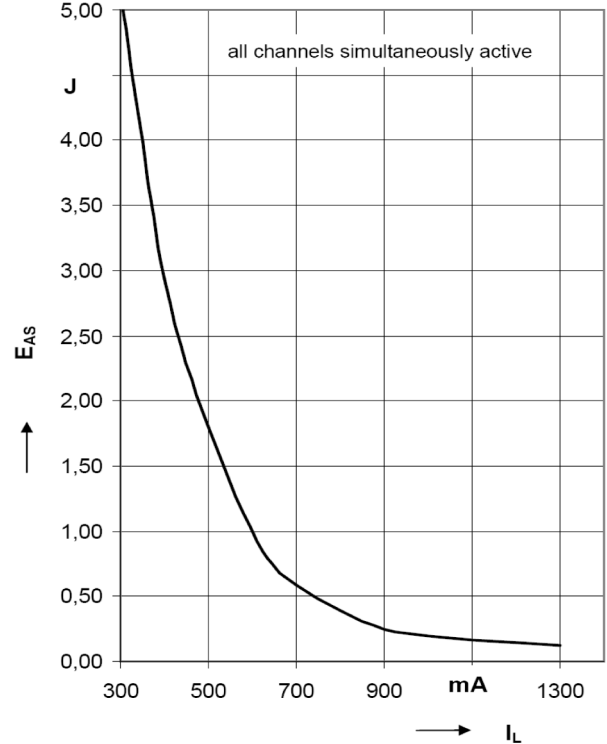
**Typ. on-state resistance**
 $R_{ON} = f(T_j)$  ;  $V_{bb} = 15V$  ;  $V_{in} = \text{high}$ 

**Typ. on-state resistance**
 $R_{ON} = f(V_{bb})$  ;  $I_L = 0.5A$  ;  $V_{in} = \text{high}$ 

**Typ. initial peak short circuit current limit**
 $I_{L(SCP)} = f(T_j)$  ;  $V_{bb} = 24V$ 


**Electrical Characteristics**

**Maximum allowable load inductance for a single switch off, calculated**  
 $L = f(I_L)$ ;  $T_{\text{istart}} = 125^\circ\text{C}$ ,  $V_{\text{bb}}=24\text{V}$ ,  $R_L=0\Omega$



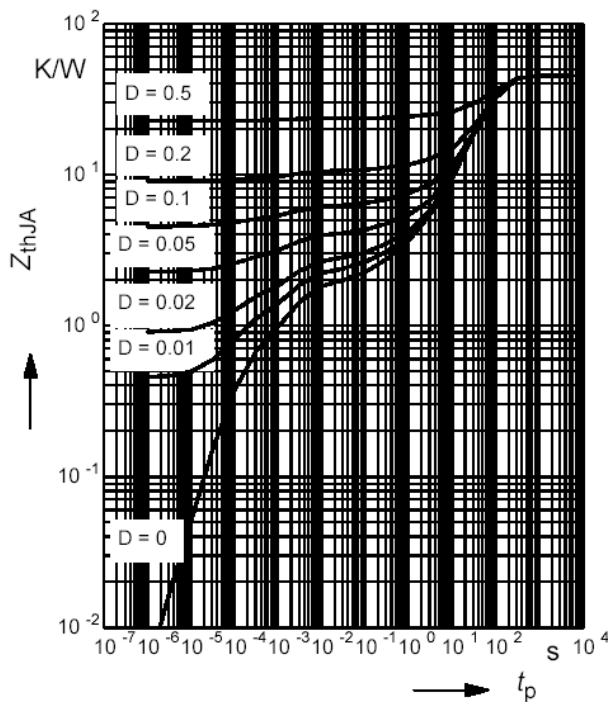
**Maximum allowable inductive switch-off Energy, single pulse**  
 $E_{\text{AS}} = f(I_L)$ ;  $T_{\text{istart}} = 125^\circ\text{C}$ ,  $V_{\text{bb}}=24\text{V}$



**Typ. transient thermal impedance**

$Z_{\text{thJA}}=f(t_p)$  @ min. footprint

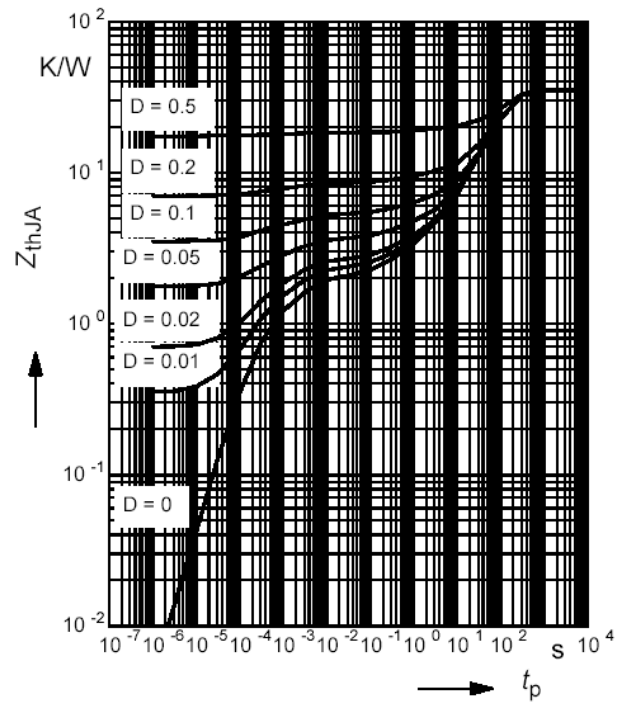
Parameter:  $D=t_p/T$



**Typ. transient thermal impedance**

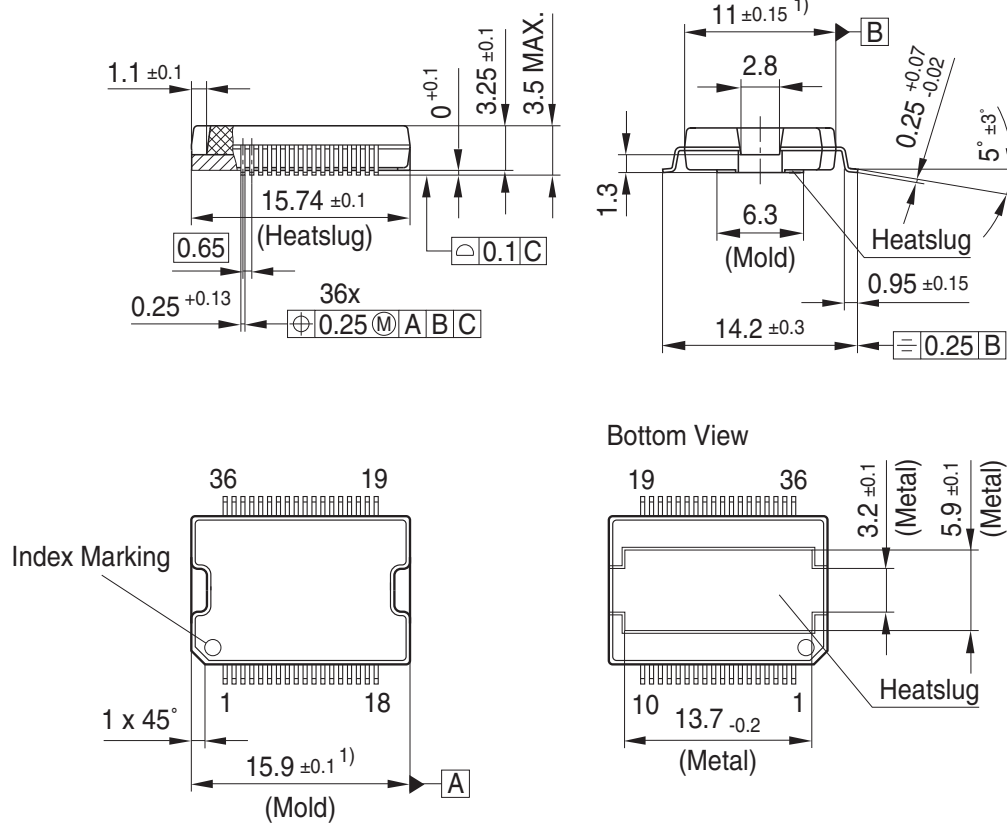
$Z_{\text{thJA}}=f(t_p)$  @ 6cm<sup>2</sup> heatsink area

Parameter:  $D=t_p/T$



## 5 Package Outlines

**PG-DSO-36**  
**(Plastic Dual Small Outline Package)**



<sup>1)</sup> Does not include plastic or metal protrusion of 0.15 max. per side

gps09181\_1

Figure 12 PG-DSO36

[www.infineon.com](http://www.infineon.com)

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)

Email: [org@lifeelectronics.ru](mailto:org@lifeelectronics.ru)

[www.lifeelectronics.ru](http://www.lifeelectronics.ru)