PCA9698

40-bit Fm+ I²C-bus advanced I/O port with $\overline{\text{RESET}}$, $\overline{\text{OE}}$ and $\overline{\text{INT}}$

Rev. 3 — 3 August 2010 Product data sheet

1. General description

The PCA9698 provides 40-bit parallel input/output (I/O) port expansion for I²C-bus applications organized in 5 banks of 8 I/Os. At 5 V supply voltage, the outputs are capable of sourcing 10 mA and sinking 25 mA with a total package load of 1 A to allow direct driving of 40 LEDs. Any of the 40 I/O ports can be configured as an input or output.

The PCA9698 is the first GPIO device in a new Fast-mode Plus (Fm+) family. Fm+ devices offer higher frequency (up to 1 MHz) and longer, more densely populated bus operation (up to 4000 pF).

The device is fully configurable: output ports can be programmed to be totem-pole or open-drain and logic states can change at either the Acknowledge (bank change) or the Stop Command (global change), each input port can be masked to prevent it from generating interrupts when its state changes, I/O data logic state can be inverted when read by the system master.

An open-drain interrupt output pin ($\overline{\text{INT}}$) allows monitoring of the input pins and is asserted each time a change occurs in one or several input ports (unless masked).

The Output Enable pin ($\overline{\text{OE}}$) 3-states any I/O selected as output and can be used as an input signal to blink or dim LEDs (PWM with frequency > 80 Hz and change duty cycle).

A ‘GPIO All Call’ command allows to program multiple Advanced GPIOs at the same time even if they have different I²C-bus addresses. This allows optimal code programming when more than one device needs to be programmed with the same instruction or if all outputs need to be turned on or off at the same time (for example, LED test).

The Device ID, hard coded in the PCA9698, allows the system master to read manufacturer, part type and revision information.

The SMBus Alert feature allows the $\overline{\text{SMBALERT}}$ pins of multiple devices with this feature to be connected together to form a wired-AND signal and to be used in conjunction with the SMBus Alert Response Address.

The internal Power-On Reset (POR) or hardware reset pin ($\overline{\text{RESET}}$) initializes the 40 I/Os as inputs. Three address select pins configure one of 64 slave addresses.

The PCA9698 is available in 56-pin TSSOP and HVQFN packages and is specified over the −40 °C to +85 °C industrial temperature range.

2. Features and benefits

- 1 MHz Fast-mode Plus I²C-bus serial interface
- Compliant with I²C-bus Fast-mode (400 kHz) and Standard-mode (100 kHz)

- 2.3 V to 5.5 V operation with 5.5 V tolerant I/Os
- 40 configurable I/O pins that default to inputs at power-up
- Outputs:
  - Programmable totem-pole (10 mA source, 25 mA sink) or open-drain (25 mA sink) with controlled edge rate output structure. Default to totem-pole on power-up.
  - Active LOW Output Enable ($\overline{OE}$) input pin 3-states all outputs. Polarity can be programmed to active HIGH through the I²C-bus. Defaults to $\overline{OE}$ on power-up.
  - Output state change programmable on the Acknowledge or the STOP Command to update outputs byte-by-byte or all at the same time respectively. Defaults to Acknowledge on power-up.
- Inputs:
  - Open-drain active LOW Interrupt ($\overline{INT}$) output pin allows monitoring of logic level change of pins programmed as inputs
  - Programmable Interrupt Mask Control for input pins that do not require an interrupt when their states change
  - Polarity Inverter register allows inversion of the polarity of the I/O pins when read
- Active LOW SMBus Alert ($\overline{SMBALERT}$) output pin allows to initiate SMBus 'Alert Response Address' sequence. Own slave address sent when sequence initiated.
- Active LOW Reset ($\overline{RESET}$) input pin resets device to power-up default state
- GPIO All Call address allows programming of more than one device at the same time with the same parameters
- 64 programmable slave addresses using 3 address pins
- Readable Device ID (manufacturer, device type and revision)
- Designed for live insertion in PICMG applications
  - Minimize line disturbance (I_{OFF} and power-up 3-state)
  - Signal transient rejection (50 ns noise filter and robust I²C-bus state machine)
- Low standby current
- −40 °C to +85 °C operation
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 which exceeds 100 mA
- Packages offered: TSSOP56, and HVQFN56

3. Applications

- Servers
- RAID systems
- Industrial control
- Medical equipment
- PLCs
- Cell phones
- Gaming machines
- Instrumentation and test measurement

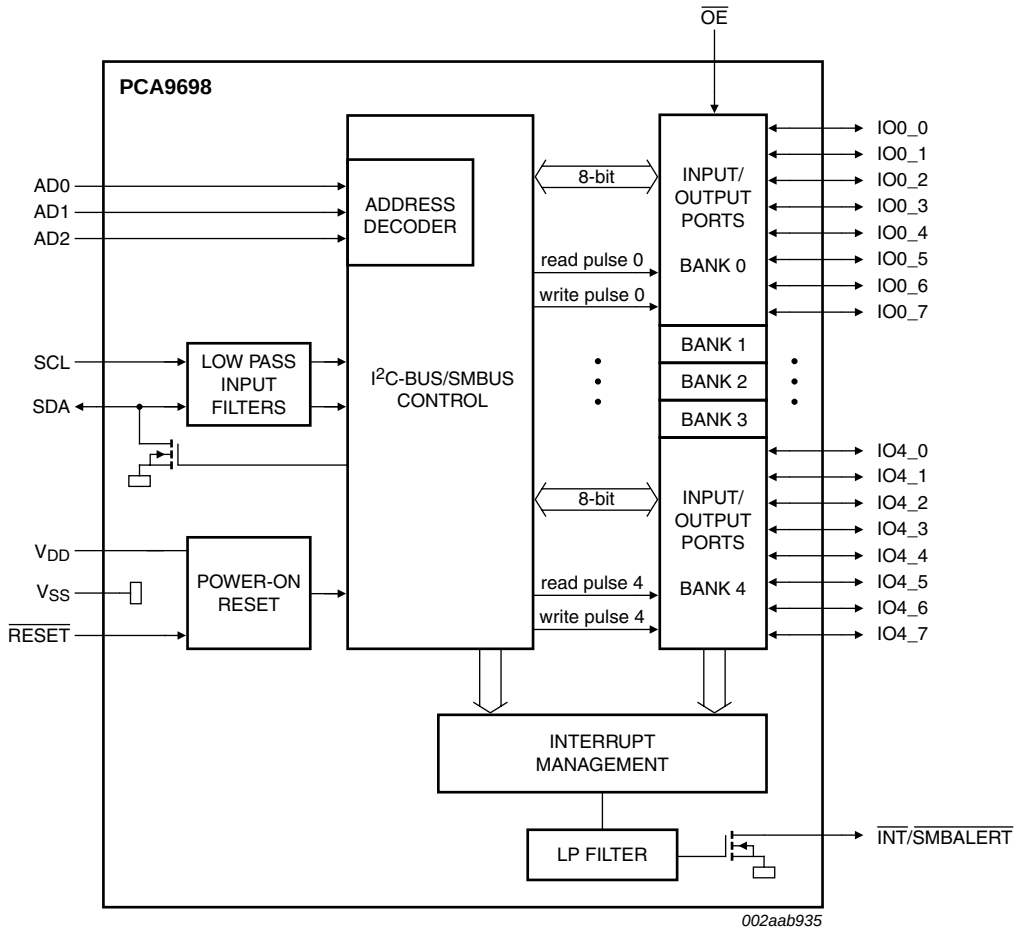
4. Ordering information

Table 1. Ordering information

T_{amb} = −40 °C to +85 °C

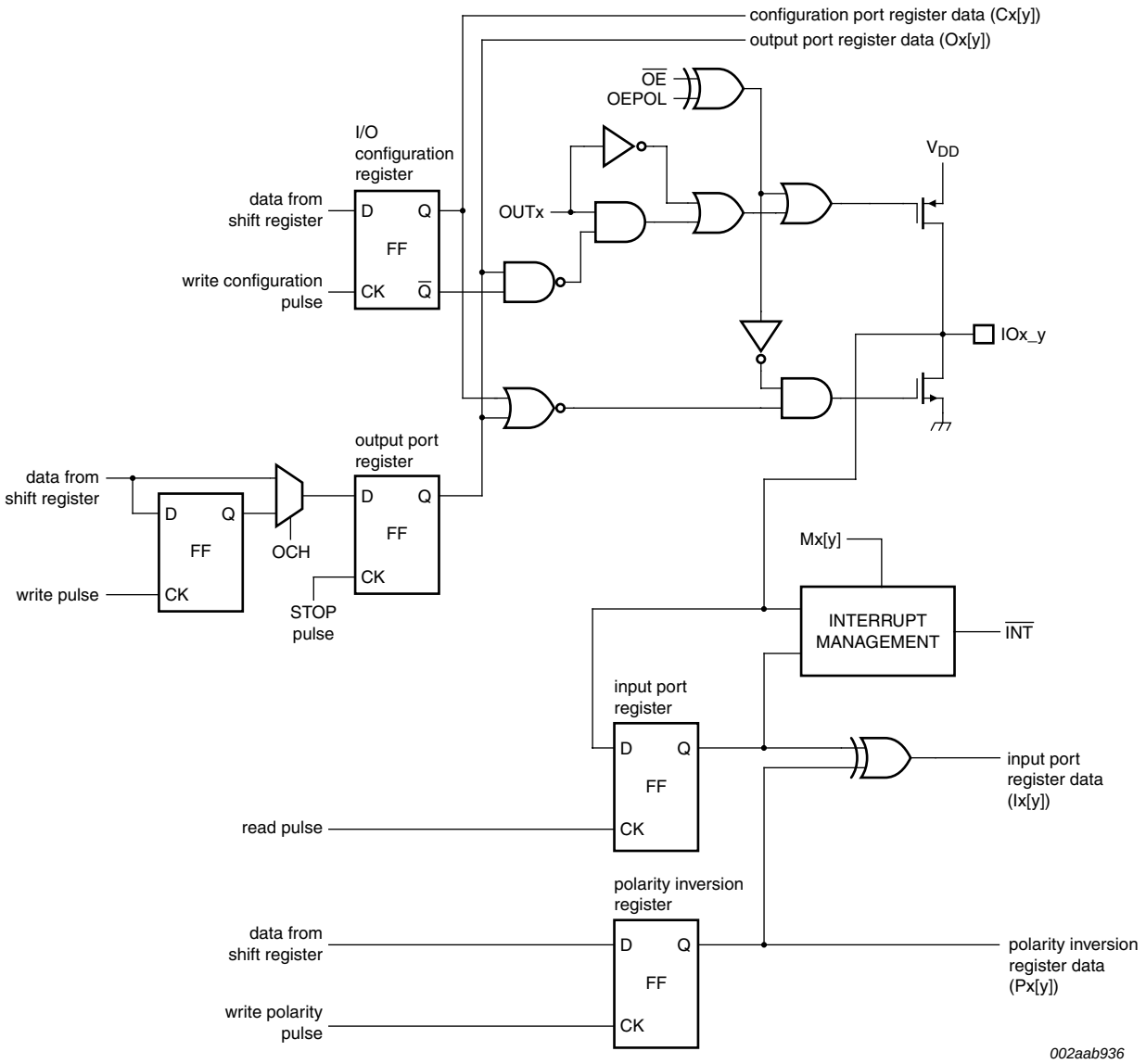
Type number	Topside mark	Package		
		Name	Description	Version
PCA9698DGG	PCA9698DGG	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
PCA9698BS	PCA9698BS	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-1

5. Block diagram



Remark: All I/Os are set to inputs at power-up and $\overline{\text{RESET}}$.

Fig 1. Block diagram of PCA9698



On power-up or RESET, all registers return to default values.

Fig 2. Simplified schematic of the I/Os (IO0_0 to IO4_7)

6. Pinning information

6.1 Pinning

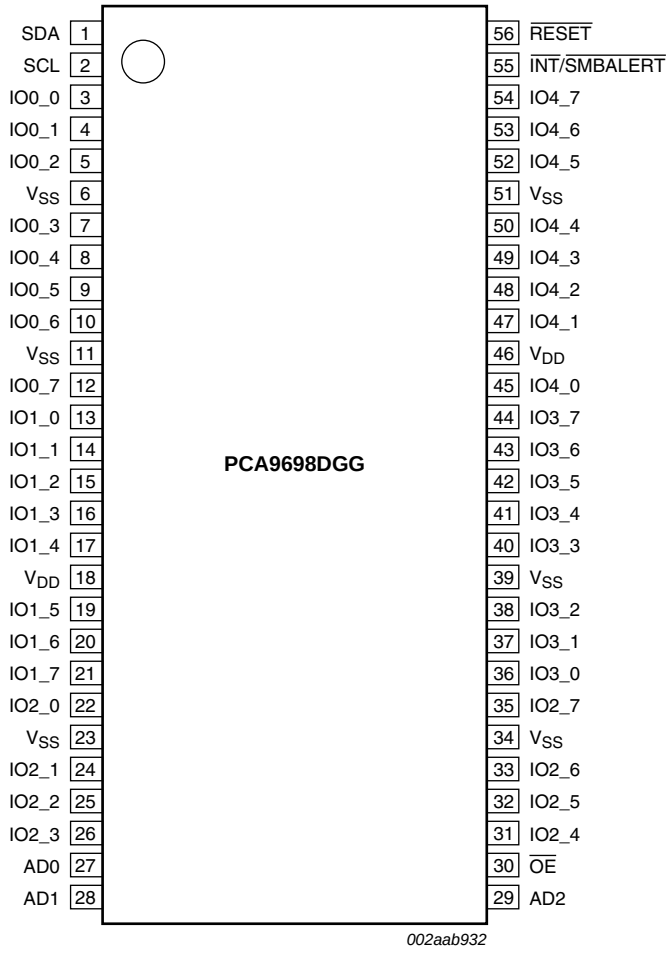


Fig 3. Pin configuration for TSSOP56

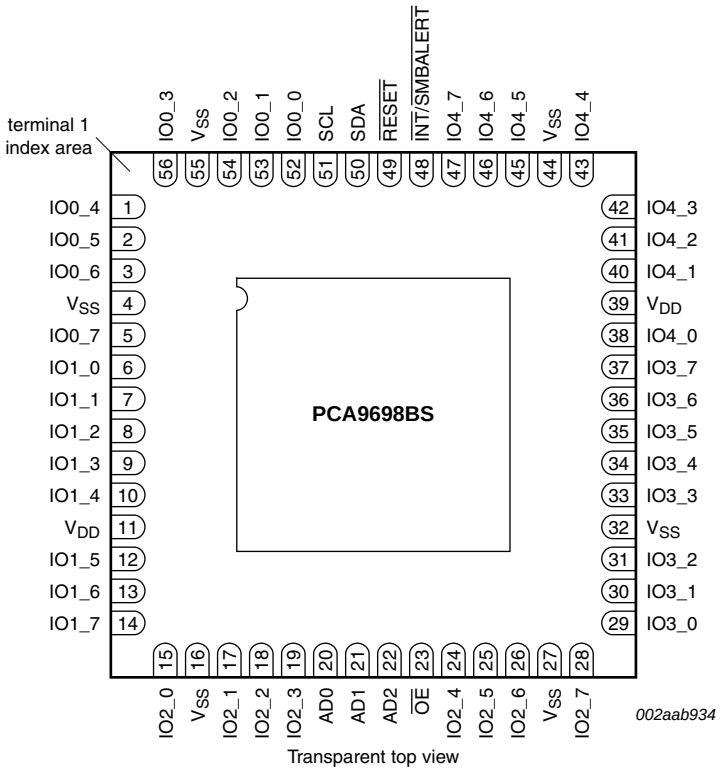


Fig 4. Pin configuration for HVQFN56

6.2 Pin description

Table 2. Pin description

Symbol	Pin		Type	Description
	TSSOP56	HVQFN56		
SDA	1	50	input/output	serial data line
SCL	2	51	input	serial clock line
IO0_0 to IO0_7	3, 4, 5, 7, 8, 9, 10, 12	52, 53, 54, 56, 1, 2, 3, 5	input/output	input/output bank 0
IO1_0 to IO1_7	13, 14, 15, 16, 17, 19, 20, 21	6, 7, 8, 9, 10, 12, 13, 14	input/output	input/output bank 1
IO2_0 to IO2_7	22, 24, 25, 26, 31, 32, 33, 35	15, 17, 18, 19, 24, 25, 26, 28	input/output	input/output bank 2
IO3_0 to IO3_7	36, 37, 38, 40, 41, 42, 43, 44	29, 30, 31, 33, 34, 35, 36, 37	input/output	input/output bank 3
IO4_0 to IO4_7	45, 47, 48, 49, 50, 52, 53, 54	38, 40, 41, 42, 43, 45, 46, 47	input/output	input/output bank 4
V_{SS}	6, 11, 23, 34, 39, 51	4, 16, 27, 32, 44, 55[1]	power supply	supply ground
V_{DD}	18, 46	11, 39	power supply	supply voltage
AD0	27	20	input	address input 0
AD1	28	21	input	address input 1

Table 2. Pin description *...continued*

Symbol	Pin		Type	Description
	TSSOP56	HVQFN56		
AD2	29	22	input	address input 2
$\overline{OE}$	30	23	input	active LOW output enable
$\overline{INT}$/$\overline{SMBALERT}$	55	48	output	active LOW interrupt output/ active LOW SMBus alert output
$\overline{RESET}$	56	49	input	active LOW reset input

[1] HVQFN56 package die supply ground is connected to both V_{SS} pins and exposed center pad. V_{SS} pins must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the printed-circuit board in the thermal pad region.

7. Functional description

Refer to Figure 1 “Block diagram of PCA9698”.

7.1 Device address

Following a START condition the bus master must send the address of the slave it is accessing and the operation it wants to perform (read or write). The address of the PCA9698 is shown in Figure 5. Slave address pins AD2, AD1 and AD0 choose 1 of 64 slave addresses. To conserve power, no internal pull-up resistors are incorporated on AD2, AD1 and AD0. Address values depending on AD2, AD1 and AD0 can be found in Table 12 “PCA9698 address map”.

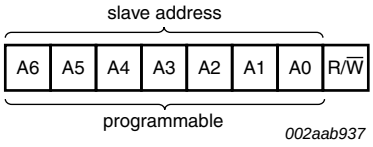


Fig 5. PCA9698 device address

The last bit of the first byte defines the operation to be performed. When set to logic 1 a read is selected while a logic 0 selects a write operation.

7.2 Alert response, GPIO All Call and Device ID addresses

Three other different addresses can be sent to the PCA9698.

- Alert Response address: allows to perform an ‘SMBus Alert’ operation as defined in the SMBus specification. This address is always used to perform a Read operation. See Section 7.11 “SMBus Alert output (SMBALERT)” for more information.
- GPIO All Call address: allows to program several Advanced GPIO devices at the same time. This address is always used to perform a Write operation. See Section 7.6 “GPIO All Call” for more information.
- Device ID address: allows to read ID information from the device (manufacturer, part identification, revision). See Section 7.5 “Device ID - PCA9698 ID field” for more information.

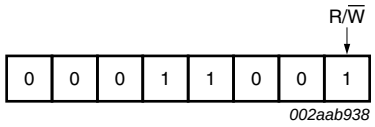


Fig 6. Alert Response address

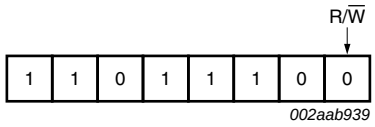


Fig 7. GPIO All Call address

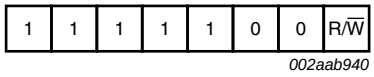


Fig 8. Device ID address

7.3 Command register

Following the successful acknowledgement of the slave address + R/W bit, the bus master will send a byte to the PCA9698, which will be stored in the Command register.

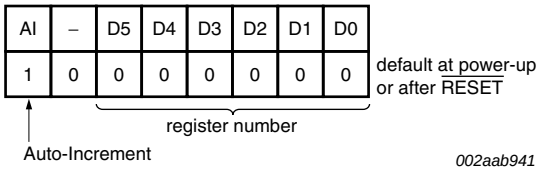


Fig 9. Command register

The lowest 6 bits are used as a pointer to determine which register will be accessed.

Registers are divided into 2 categories: 5-bank register category, and 1-bank register category.

Only a command register code with the 7 least significant bits equal to the 28 allowable values as defined in Table 3 “Register summary” will be acknowledged. Reserved or undefined command codes will not be acknowledged. At power-up, this register defaults to 80h, with the AI bit set to ‘1’, and the lowest 7 bits set to ‘0'.

During a write operation, the PCA9698 will acknowledge a byte sent to the OP, PI, IOC, MSK, OUTCONF, ALLBNK, and MODE registers, but will not acknowledge a byte sent to the IPx registers since these are read-only registers.

7.3.1 5-bank register category

- IP – Input registers
- OP – Output registers
- PI – Polarity Inversion registers
- IOC – I/O Configuration registers
- MSK – Mask interrupt registers

If the Auto-Increment flag is set (AI = 1), the 3 least significant bits are automatically incremented after a read or write. This allows the user to program and/or read the 5 register banks sequentially.

If more than 5 bytes of data are written and AI = 1, previous data in the selected registers will be overwritten or reread. Reserved registers are skipped and not accessed (refer to Table 3).

If the Auto-Increment flag is cleared (AI = 0), the 3 least significant bits are not incremented after data is read or written, only one register will be repeatedly read or written.

7.3.2 1-bank register category

- OUTCONF – Output Structure Configuration register
- ALLBNK – All Bank Control register
- MODE – Mode Selection register

If more than 1 byte of data is written or read, previous data in the same register is overwritten independently of the value of AI.

7.4 Register definitions

Table 3. Register summary

Reg #	D5	D4	D3	D2	D1	D0	Name	Type	Function
Input Port registers									
00h	0	0	0	0	0	0	IP0	read only	Input Port register bank 0
01h	0	0	0	0	0	1	IP1	read only	Input Port register bank 1
02h	0	0	0	0	1	0	IP2	read only	Input Port register bank 2
03h	0	0	0	0	1	1	IP3	read only	Input Port register bank 3
04h	0	0	0	1	0	0	IP4	read only	Input Port register bank 4
05h	0	0	0	1	0	1	-	-	reserved for future use
06h	0	0	0	1	1	0	-	-	reserved for future use
07h	0	0	0	1	1	1	-	-	reserved for future use

Table 3. Register summary *...continued*

Reg #	D5	D4	D3	D2	D1	D0	Name	Type	Function
Output Port registers									
08h	0	0	1	0	0	0	OP0	read/write	Output Port register bank 0
09h	0	0	1	0	0	1	OP1	read/write	Output Port register bank 1
0Ah	0	0	1	0	1	0	OP2	read/write	Output Port register bank 2
0Bh	0	0	1	0	1	1	OP3	read/write	Output Port register bank 3
0Ch	0	0	1	1	0	0	OP4	read/write	Output Port register bank 4
0Dh	0	0	1	1	0	1	-	-	reserved for future use
0Eh	0	0	1	1	1	0	-	-	reserved for future use
0Fh	0	0	1	1	1	1	-	-	reserved for future use
Polarity Inversion registers									
10h	0	1	0	0	0	0	PI0	read/write	Polarity Inversion register bank 0
11h	0	1	0	0	0	1	PI1	read/write	Polarity Inversion register bank 1
12h	0	1	0	0	1	0	PI2	read/write	Polarity Inversion register bank 2
13h	0	1	0	0	1	1	PI3	read/write	Polarity Inversion register bank 3
14h	0	1	0	1	0	0	PI4	read/write	Polarity Inversion register bank 4
15h	0	1	0	1	0	1	-	-	reserved for future use
16h	0	1	0	1	1	0	-	-	reserved for future use
17h	0	1	0	1	1	1	-	-	reserved for future use
I/O Configuration registers									
18h	0	1	1	0	0	0	IOC0	read/write	I/O Configuration register bank 0
19h	0	1	1	0	0	1	IOC1	read/write	I/O Configuration register bank 1
1Ah	0	1	1	0	1	0	IOC2	read/write	I/O Configuration register bank 2
1Bh	0	1	1	0	1	1	IOC3	read/write	I/O Configuration register bank 3
1Ch	0	1	1	1	0	0	IOC4	read/write	I/O Configuration register bank 4
1Dh	0	1	1	1	0	1	-	-	reserved for future use
1Eh	0	1	1	1	1	0	-	-	reserved for future use
1Fh	0	1	1	1	1	1	-	-	reserved for future use
Mask Interrupt registers									
20h	1	0	0	0	0	0	MSK0	read/write	Mask interrupt register bank 0
21h	1	0	0	0	0	1	MSK1	read/write	Mask interrupt register bank 1
22h	1	0	0	0	1	0	MSK2	read/write	Mask interrupt register bank 2
23h	1	0	0	0	1	1	MSK3	read/write	Mask interrupt register bank 3
24h	1	0	0	1	0	0	MSK4	read/write	Mask interrupt register bank 4
25h	1	0	0	1	0	1	-	-	reserved for future use
26h	1	0	0	1	1	0	-	-	reserved for future use
27h	1	0	0	1	1	1	-	-	reserved for future use
Miscellaneous									
28h	1	0	1	0	0	0	OUTCONF	read/write	output structure configuration
29h	1	0	1	0	0	1	ALLBNK	read/write	control all banks
2Ah	1	0	1	0	1	0	MODE	read/write	PCA9698 mode selection

7.4.1 IP0 to IP4 - Input Port registers

These registers are read-only. They reflect the incoming logic levels of the port pins regardless of whether the pin is defined as an input or an output by the I/O Configuration register. If the corresponding Px[y] bit in the PI registers is set to 0, or the inverted incoming logic levels if the corresponding Px[y] bit in the PI register is set to 1. Writes to these registers have no effect.

Table 4. IP0 to IP4 - Input Port registers (address 00h to 04h) bit description

*Legend: * default value 'X' determined by the externally applied logic level.*

Address	Register	Bit	Symbol	Access	Value	Description
00h	IP0	7 to 0	I0[7:0]	R	XXXX XXXX*	Input Port register bank 0
01h	IP1	7 to 0	I1[7:0]	R	XXXX XXXX*	Input Port register bank 1
02h	IP2	7 to 0	I2[7:0]	R	XXXX XXXX*	Input Port register bank 2
03h	IP3	7 to 0	I3[7:0]	R	XXXX XXXX*	Input Port register bank 3
04h	IP4	7 to 0	I4[7:0]	R	XXXX XXXX*	Input Port register bank 4

The Polarity Inversion register can invert the logic states of the port pins. The polarity of the corresponding bit is inverted when Px[y] bit in the PI register is set to 1. The polarity of the corresponding bit is not inverted when Px[y] bits in the PI register is set to 0.

7.4.2 OP0 to OP4 - Output Port registers

These registers reflect the outgoing logic levels of the pins defined as outputs by the I/O Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the values that are in the flip-flops controlling the output selection, **not** the actual pin values.

Ox[y] = 0: IOx_y = 0 if IOx_y defined as output (Cx[y] in IOC register = 0).

Ox[y] = 1: IOx_y = 1 if IOx_y defined as output (Cx[y] in IOC register = 0).

Where 'x' refers to the bank number (0 to 4); 'y' refers to the bit number (0 to 7).

Table 5. OP0 to OP4 - Output Port registers (address 08h to 0Ch) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
08h	OP0	7 to 0	O0[7:0]	R/W	0000 0000*	Output Port register bank 0
09h	OP1	7 to 0	O1[7:0]	R/W	0000 0000*	Output Port register bank 1
0Ah	OP2	7 to 0	O2[7:0]	R/W	0000 0000*	Output Port register bank 2
0Bh	OP3	7 to 0	O3[7:0]	R/W	0000 0000*	Output Port register bank 3
0Ch	OP4	7 to 0	O4[7:0]	R/W	0000 0000*	Output Port register bank 4

7.4.3 PI0 to PI4 - Polarity Inversion registers

These registers allow inversion of the polarity of the corresponding Input Port register.

Px[y] = 0: The corresponding Input Port register data polarity is retained.

Px[y] = 1: The corresponding Input Port register data polarity is inverted.

Where 'x' refers to the bank number (0 to 4); 'y' refers to the bit number (0 to 7).

Table 6. PI0 to PI4 - Polarity Inversion registers (address 10h to 14h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
10h	PI0	7 to 0	P0[7:0]	R/W	0000 0000*	Polarity Inversion register bank 0
11h	PI1	7 to 0	P1[7:0]	R/W	0000 0000*	Polarity Inversion register bank 1
12h	PI2	7 to 0	P2[7:0]	R/W	0000 0000*	Polarity Inversion register bank 2
13h	PI3	7 to 0	P3[7:0]	R/W	0000 0000*	Polarity Inversion register bank 3
14h	PI4	7 to 0	P4[7:0]	R/W	0000 0000*	Polarity Inversion register bank 4

7.4.4 IOC0 to IOC4 - I/O Configuration registers

These registers configure the direction of the I/O pins.

Cx[y] = 0: The corresponding port pin is an output.

Cx[y] = 1: The corresponding port pin is an input.

Where 'x' refers to the bank number (0 to 4); 'y' refers to the bit number (0 to 7).

Table 7. IOC0 to IOC4 - I/O Configuration registers (address 18h to 1Ch) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
18h	IOC0	7 to 0	C0[7:0]	R/W	1111 1111*	I/O Configuration register bank 0
19h	IOC1	7 to 0	C1[7:0]	R/W	1111 1111*	I/O Configuration register bank 1
1Ah	IOC2	7 to 0	C2[7:0]	R/W	1111 1111*	I/O Configuration register bank 2
1Bh	IOC3	7 to 0	C3[7:0]	R/W	1111 1111*	I/O Configuration register bank 3
1Ch	IOC4	7 to 0	C4[7:0]	R/W	1111 1111*	I/O Configuration register bank 4

7.4.5 MSK0 to MSK4 - Mask interrupt registers

These registers mask the interrupt due to a change in the I/O pins configured as inputs. ‘x’ refers to the bank number (0 to 4); ‘y’ refers to the bit number (0 to 7).

Mx[y] = 0: A level change at the I/O will generate an interrupt if IOx_y defined as input (Cx[y] in IOC register = 1).

Mx[y] = 1: A level change in the input port will not generate an interrupt if IOx_y defined as input (Cx[y] in IOC register = 1).

Table 8. MSK0 to MSK4 - Mask interrupt registers (address 20h to 24h) bit description

*Legend: * default value.*

Address	Register	Bit	Symbol	Access	Value	Description
20h	MSK0	7 to 0	M0[7:0]	R/W	1111 1111*	Mask Interrupt register bank 0
21h	MSK1	7 to 0	M1[7:0]	R/W	1111 1111*	Mask Interrupt register bank 1
22h	MSK2	7 to 0	M2[7:0]	R/W	1111 1111*	Mask Interrupt register bank 2
23h	MSK3	7 to 0	M3[7:0]	R/W	1111 1111*	Mask Interrupt register bank 3
24h	MSK4	7 to 0	M4[7:0]	R/W	1111 1111*	Mask Interrupt register bank 4

7.4.6 OUTCONF - output structure configuration register

Table 9. OUTCONF - output structure configuration register (address 28h) description

Bit	7	6	5	4	3	2	1	0
Symbol	OUT4	OUT3	OUT2	OUT1	OUT067	OUT045	OUT023	OUT001
Default	1	1	1	1	1	1	1	1

This register controls the configuration of the output ports as open-drain or totem-pole.

The 4 least significant bits control the output architecture for bank 0, 2 bits at a time.

OUT001 controls the output structure for IO0_0 and IO0_1

OUT023 controls the output structure for IO0_2 and IO0_3

OUT045 controls the output structure for IO0_4 and IO0_5

OUT067 controls the output structure for IO0_6 and IO0_7

The 4 most significant bits control the output architectures for bank 1 to bank 4, each bit controlling one bank.

OUT1 controls the output structure for bank 1 (IO1_0 to IO1_7)

OUT2 controls the output structure for bank 2 (IO2_0 to IO2_7)

OUT3 controls the output structure for bank 3 (IO3_0 to IO3_7)

OUT4 controls the output structure for bank 4 (IO4_0 to IO4_7)

OUTx = 0: The I/Os are configured with an open-drain structure.

OUTx = 1: The I/Os are configured with a totem-pole structure.

7.4.7 ALLBNK - All Bank control register

Table 10. ALLBNK - All Bank control register (address 29h) description

Bit	7	6	5	4	3	2	1	0
Symbol	BSEL	X	X	B4	B3	B2	B1	B0
Default	1	0	0	0	0	0	0	0

This register allows all the I/Os configured as outputs to be programmed with the same logic value. This programming is applied to all the banks or a selection of banks.

When this register is programmed, values in the Output Port registers are not changed and do not reflect the states of I/Os configured as outputs anymore.

- B0 to B4 controls the logic level to be applied to Bank 0 to Bank 4, respectively.
  - Bx = 0: All the I/Os configured as outputs in the corresponding Bank x are programmed with 0s.
  - Bx = 1: All the I/Os configured as outputs in the corresponding Bank x are programmed with 1s.
- Bit 5 and bit 6 are not used and can be programmed to either ‘1’ or ‘0’.
- BSEL is a filter bit that allows programming of some banks only, and not the others.
  - BSEL = 0:

    When Bx = 0, all the I/Os configured as output in the corresponding Bank x are programmed with 0s.

    When Bx = 1, all the I/Os configured as output in the corresponding Bank x are programmed with their actual value from the corresponding output register.
  - BSEL = 1:

    When Bx = 0, all the I/Os configured as output in the corresponding Bank x are programmed with their actual value from the corresponding output register.

    When Bx = 1, all the I/Os configured as output in the corresponding Bank x are programmed with 1s.

7.4.7.1 Examples

- If ALLBNK = 0XX0 0000:

  All I/Os configured as outputs in Bank 0 to Bank 4 will be programmed with 0s, overwriting values programmed in the five Output Port registers.
- If ALLBNK = 1XX1 1111:

  All I/Os configured as outputs in Bank 0 to Bank 4 will be programmed with 1s, overwriting values programmed in the five Output Port registers.
- If ALLBNK = 0XX0 0110:

  All I/Os configured as outputs in Banks 0, 3, and 4 only will be programmed with 0s, overwriting values programmed in the Output Port registers 0, 3, and 4, while I/Os configured as outputs in Bank 1 and Bank 2 are programmed with values in Output Port registers 1 and 2.

- If ALLBNK = 1XX0 1100:

  All I/Os configured as outputs in Bank 2 and 3 will be programmed with 1s, overwriting values programmed in the Output Port registers 2 and 3, while I/Os configured as outputs in Bank 0, 1, and 4 are programmed with values in Output Port registers 0, 1, and 4.

7.4.8 MODE - PCA9698 mode selection register

Table 11. MODE - mode selection register (address 2Ah) description

Bit	7	6	5	4	3	2	1	0
Symbol	X	X	X	SMBA	IOAC	X	OCH	OEPOL
Default	0	0	0	0	0	0	1	0

This register allows programming of the PCA9698 modes.

- OEPOL bit controls the polarity of $\overline{OE}$ pin.
  - OEPOL = 0: $\overline{OE}$ pin is active LOW.
  - OEPOL = 1: $\overline{OE}$ pin is active HIGH (equivalent to OE pin).
- OCH bit selects the I²C-bus event where the state of the I/Os configured as outputs change.
  - OCH = 0: outputs change on STOP command.
  - OCH = 1: outputs change on ACK.
- IOAC bit controls the ability of the device to respond to a ‘GPIO All Call’ command (see Section 7.6 “GPIO All Call” for more information), allowing programming of more than one device at the same time.
  - IOAC = 0: The device cannot respond to a ‘GPIO All Call’ command.
  - IOAC = 1: The device can respond to a ‘GPIO All Call’ command.

  Remark: The ‘GPIO ALL CALL’ command defined for the PCA9698 is different from the I²C-bus protocol ‘General Call’ command.
- SMBA bit controls the capability of the PCA9698 to respond to a SMBAlert command.
  - SMBA = 0: PCA9698 does not respond to an Alert Response Address.
  - SMBA = 1: PCA9698 responds to an Alert Response Address. Bits 5, 6 and 7 are reserved and must be programmed with 0s.
- Unused bits (bits 2, 5, 6 and 7) must be programmed with 0s for proper device operation.

7.5 Device ID - PCA9698 ID field

The Device ID field is a 3 byte read-only (24 bits) word giving the following information:

- 12 bits with the manufacturer name, unique per manufacturer (e.g., NXP)
- 9 bits with the part identification, assigned by manufacturer (e.g., PCA9698)
- 3 bits with the die revision, assigned by manufacturer (e.g., RevX)

The Device ID is read-only, hard-wired in the device and can be accessed as follows:

1. START command
2. The master sends the Reserved Device ID I²C-bus address followed by the R/$\overline{W}$ bit set to ‘0’ (write): ‘1111 1000’.
3. The master sends the I²C-bus slave address of the slave device it needs to identify. The LSB is a ‘Don’t care’ value. Only one device must acknowledge this byte (the one that has the I²C-bus slave address).
4. The master sends a Re-START command.

   Remark: A STOP command followed by a START command will reset the slave state machine and the Device ID Read cannot be performed. Also, a STOP command or a Re-START command followed by an access to another slave device will reset the slave state machine and the Device ID Read cannot be performed.
5. The master sends the Reserved Device ID I²C-bus address followed by the R/$\overline{W}$ bit set to ‘1’ (read): ‘1111 1001’.
6. The Device ID Read can be done, starting with the 12 manufacturer bits (first byte + 4 MSBs of the second byte), followed by the 9 part identification bits (4 LSBs of the second byte + 5 MSBs of the third byte), and then the 3 die revision bits (3 LSBs of the third byte).
7. The master ends the reading sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

   Remark: The reading of the Device ID can be stopped anytime by sending a NACK command.

   If the master continues to ACK the bytes after the third byte, the PCA9698 rolls back to the first byte and keeps sending the Device ID sequence until a NACK has been detected.

For the PCA9698, the Device ID is as shown in Figure 10.

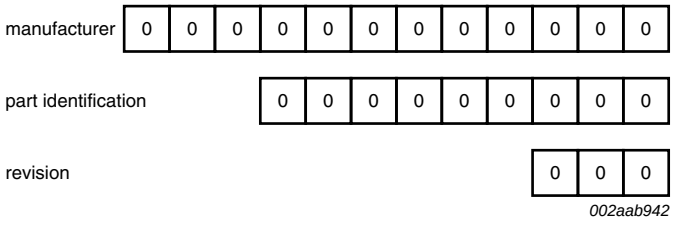


Fig 10. PCA9698 ID field

7.6 GPIO All Call

A ‘GPIO All Call’ command allows the programming of multiple advanced GPIOs with different I²C-bus addresses at the same time. This allows to optimize code programming when the master needs to send the same instruction to several devices. To respond to such a command and sequence, the PCA9698 needs to have its IOAC bit (register 2Ah, bit 3) set to 1. Devices that have this bit set to 0 do not participate in any ‘GPIO All Call’ sequence.

The ‘GPIO All Call’ command can be performed only for a write operation and cannot be used in conjunction with a read operation.

- Master initiates a command sequence with the START command, the ‘GPIO All Call’ command associated with a Write command: Start – 1101 110 + Write
- All the devices that are programmed to respond to this command will acknowledge
- The master then sends the data and all the devices that are programmed to respond acknowledge the byte(s)
- The master ends the sequence by sending a STOP or Repeated START command.

If the master initiates a ‘GPIO All Call’ sequence with a Read command, none of the slave devices acknowledge.

7.7 Output state change on ACK or STOP

State change of the I/Os programmed as outputs can be done either:

- during the ACK phase every time an Output Port register is modified. The output state is then updated one-by-one (at a bank level): OCH bit = 1 (register 2Ah, bit 1)
- at a STOP command allowing all the outputs to change at the exact same moment: OCH bit = 0 (register 2Ah, bit 1).

Change of the outputs at the STOP command allows synchronizing of all the programmed banks in a single device, and also allows synchronizing outputs of more than one PCA9698.

Example 1: Only one PCA9698 is used on the I²C-bus and all the outputs need to change at the same time.

- OCH bit (Mode Selection Register, bit 1) must be equal to ‘0’.
- The master accesses the device and programs the Output Port register(s) that has (have) to be changed (up to 5 ports).
- When done, the master must generate a STOP command.
- At the STOP command, the PCA9698 will update the Output Port register(s) that has (have) been programmed and change the output states all at the same time.

Example 2: More than one PCA9698 is used on the I²C-bus and all the outputs need to change at the same time.

- OCH bit (Mode Selection Register, bit 1) must be equal to ‘0’ in all the devices.
- The master device must access the devices one-by-one.
- Access to each device must be separated by a Re-START command.

- When all the devices have been accessed, the master must generate a STOP command.
- At the STOP command, all the PCA9698s that have been accessed will update their Output Port registers that have been programmed and change the output states all at the same time.

Remark: After programming a PCA9698, its state machine will be in a 'wait-for-STOP-condition' until a STOP condition is received to update the Output Port registers. Since this state machine will be in a 'wait-state', the part will not respond to its own address until this state machine gets out to the idle condition, which means that the device can be programmed only once and is not addressable again until a STOP condition has been received.

Remark: The PCA9698 has one level of buffers to store 5 bytes of data, and the actual Output Port registers will get updated on the STOP condition. If the master sends more than 5 bytes of data (with AI = 1), the data in the buffer will get overwritten.

7.8 Power-on reset

When power is applied to V_{DD}, an internal Power-On Reset (POR) holds the PCA9698 in a reset condition until V_{DD} has reached V_{POR}. At that point, the reset condition is released and the PCA9698 registers and I²C-bus/SMBus state machine will initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

7.9 $\overline{\text{RESET}}$ input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin LOW for a minimum of $t_{w(rst)}$. The PCA9698 registers and I²C-bus state machine will be held in their default state until the $\overline{\text{RESET}}$ input is once again HIGH.

7.10 Interrupt output ($\overline{\text{INT}}$)

The open-drain active LOW interrupt is activated when one of the port pins changes state and the port pin is configured as an input and the interrupt on it is not masked. The interrupt is deactivated when the port pin input returns to its previous state or the Input Port register is read.

It is highly recommended to program the MSK register, and the IOC registers during the initialization sequence after power-up, since any change to them during Normal mode operation may cause undesirable interrupt events to happen.

Remark: Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

Only a Read of the Input Port register that contains the bit(s) image of the input(s) that generated the interrupt clears the interrupt condition.

If more than one input register changed state before a read of the Input Port register is initiated, the interrupt is cleared when all the input registers containing all the inputs that changed are read.

Example: If IO0_5, IO2_3, and IO3_7 change state at the same time, the interrupt is cleared only when INREG0, INREG2, and INREG3 are read.

7.11 SMBus Alert output (SMBALERT)

The interrupt output pin (INT) can also be used as an Alert line (SMBALERT).

The SMBALERT pins of multiple devices with this feature can be connected together to form a wired-AND signal and can be used in conjunction with the SMBus Alert Response Address. 'SMBus Alert' message is 2 bytes long and allows the master to determine which device generated the Alert (SMBALERT going LOW).

When SMBA bit = 1 (register 2Ah, bit 4), the PCA9698 supports the SMBus Alert function and its INT/SMBALERT pin may be connected as an SMBus Alert signal.

When a master device senses that an 'SMBus Alert' condition is present on the ALERT line (SMBALERT pin of the PCA9698 and/or other devices going LOW):

- It accesses the slave device(s) through the Alert Response Address (ARA) associated with a Read Command: Start – 0001 100 + R/$\overline{W}$ = 1.
- If the PCA9698 is the device that generated the 'SMBus Alert' condition (and its SMBA bit = 1), it will acknowledge the SMBus Alert command and respond by transmitting its slave address on the SDA line. The 8th bit (LSB) of the slave address byte will be a zero.
- The device will acknowledge an ARA command only if the SMBALERT signal has been previously asserted (SMBALERT = LOW).
- If more than one device pulls its SMBALERT pin LOW, the highest priority (lowest I²C-bus address) device will win communication rights via standard I²C-bus arbitration during the slave address transfer.
- If the PCA9698 wins the arbitration, its SMBALERT pin will become inactive (will go HIGH) at the completion of the slave address transmission (9th clock pulse, NACK phase).
- If the PCA9698 loses the arbitration, its SMBALERT pin will remain active (will stay LOW).
- The master ends the sequence by sending a NACK and then STOP command.
- If the SMBALERT is still LOW after transfer is complete, it means that more than one device made the request. Another full transaction is then required.

Remark: If the master initiates an 'SMBus Alert' sequence with a Write Command, none of the slave devices acknowledge. The SMBALERT is open-drain and requires a pull-up resistor to V_{DD}.

Remark: If the master sends an ACK after reading the I²C-bus slave address, the slave device keeps sending '1's until a NACK is received.

7.12 Output enable input (OE)

The configurable active LOW or active HIGH output enable pin allows to enable or disable all the I/Os at the same time.

- When a LOW level is applied to the OE pin, with OEPOL = 0 (register 2Ah, bit 4) or a HIGH level is applied to the OE pin, with OEPOL = 1 (register 2Ah, bit 0), all the I/Os configured as outputs are enabled and the logic value programmed in their respective OP registers is applied to the pins.
- When a HIGH level is applied to the OE pin, with OEPOL = 0 (register 2Ah, bit 0) or a LOW level is applied to the OE pin, with OEPOL = 1 (register 2Ah, bit 0), all the I/Os configured as outputs are 3-stated.

For applications requiring LED blinking with brightness control, this pin can be used to control the brightness by applying a high frequency PWM signal on the OE pin. LEDs can be blinked using the Output Port registers and can be dimmed using the PWM signal on the OE pin thus controlling the brightness by adjusting the duty cycle.

Default is OEPOL = 0, so if the OE pin is held HIGH, the outputs are disabled. The OE pin needs to be pulled LOW or OEPOL changed to '1' to enable the outputs.

It is recommended to define the required polarity of the OE input by programing the value of OEPOL before programming the configuration registers (IOC register).

7.13 Live insertion

The PCA9698 is fully specified for live-insertion applications using I_{OFF}, power-up 3-states, robust state machine, and 50 ns noise filter. The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-states circuitry places the outputs in the high-impedance state during power-up and power-down, which prevents driver conflict and bus contention.

The robust state machine does not respond until it sees a valid START condition and the 50 ns noise filter will filter out any insertion glitches. The PCA9698 will not cause corruption of active data on the bus nor will the device be damaged or cause damage to devices already on the bus when similar featured devices are being used.

7.14 Standby

The PCA9698 goes into standby when the I²C-bus is idle. Standby supply current is lower than 1.0 μA (typical).

7.15 Address map

Table 12. PCA9698 address map

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	Address
V_{SS}	SCL	V_{SS}	0	0	1	0	0	0	0	20h
V_{SS}	SCL	V_{DD}	0	0	1	0	0	0	1	22h
V_{SS}	SDA	V_{SS}	0	0	1	0	0	1	0	24h
V_{SS}	SDA	V_{DD}	0	0	1	0	0	1	1	26h
V_{DD}	SCL	V_{SS}	0	0	1	0	1	0	0	28h
V_{DD}	SCL	V_{DD}	0	0	1	0	1	0	1	2Ah
V_{DD}	SDA	V_{SS}	0	0	1	0	1	1	0	2Ch
V_{DD}	SDA	V_{DD}	0	0	1	0	1	1	1	2Eh
V_{SS}	SCL	SCL	0	0	1	1	0	0	0	30h
V_{SS}	SCL	SDA	0	0	1	1	0	0	1	32h
V_{SS}	SDA	SCL	0	0	1	1	0	1	0	34h
V_{SS}	SDA	SDA	0	0	1	1	0	1	1	36h
V_{DD}	SCL	SCL	0	0	1	1	1	0	0	38h
V_{DD}	SCL	SDA	0	0	1	1	1	0	1	3Ah
V_{DD}	SDA	SCL	0	0	1	1	1	1	0	3Ch
V_{DD}	SDA	SDA	0	0	1	1	1	1	1	3Eh
V_{SS}	V_{SS}	V_{SS}	0	1	0	0	0	0	0	40h
V_{SS}	V_{SS}	V_{DD}	0	1	0	0	0	0	1	42h
V_{SS}	V_{DD}	V_{SS}	0	1	0	0	0	1	0	44h
V_{SS}	V_{DD}	V_{DD}	0	1	0	0	0	1	1	46h
V_{DD}	V_{SS}	V_{SS}	0	1	0	0	1	0	0	48h
V_{DD}	V_{SS}	V_{DD}	0	1	0	0	1	0	1	4Ah
V_{DD}	V_{DD}	V_{SS}	0	1	0	0	1	1	0	4Ch
V_{DD}	V_{DD}	V_{DD}	0	1	0	0	1	1	1	4Eh
V_{SS}	V_{SS}	SCL	0	1	0	1	0	0	0	50h
V_{SS}	V_{SS}	SDA	0	1	0	1	0	0	1	52h
V_{SS}	V_{DD}	SCL	0	1	0	1	0	1	0	54h
V_{SS}	V_{DD}	SDA	0	1	0	1	0	1	1	56h
V_{DD}	V_{SS}	SCL	0	1	0	1	1	0	0	58h
V_{DD}	V_{SS}	SDA	0	1	0	1	1	0	1	5Ah
V_{DD}	V_{DD}	SCL	0	1	0	1	1	1	0	5Ch
V_{DD}	V_{DD}	SDA	0	1	0	1	1	1	1	5Eh

Table 12. PCA9698 address map *...continued*

AD2	AD1	AD0	A6	A5	A4	A3	A2	A1	A0	Address
SCL	SCL	V_{SS}	1	0	1	0	0	0	0	A0h
SCL	SCL	V_{DD}	1	0	1	0	0	0	1	A2h
SCL	SDA	V_{SS}	1	0	1	0	0	1	0	A4h
SCL	SDA	V_{DD}	1	0	1	0	0	1	1	A6h
SDA	SCL	V_{SS}	1	0	1	0	1	0	0	A8h
SDA	SCL	V_{DD}	1	0	1	0	1	0	1	AAh
SDA	SDA	V_{SS}	1	0	1	0	1	1	0	ACh
SDA	SDA	V_{DD}	1	0	1	0	1	1	1	AEh
SCL	SCL	SCL	1	0	1	1	0	0	0	B0h
SCL	SCL	SDA	1	0	1	1	0	0	1	B2h
SCL	SDA	SCL	1	0	1	1	0	1	0	B4h
SCL	SDA	SDA	1	0	1	1	0	1	1	B6h
SDA	SCL	SCL	1	0	1	1	1	0	0	B8h
SDA	SCL	SDA	1	0	1	1	1	0	1	BAh
SDA	SDA	SCL	1	0	1	1	1	1	0	BCh
SDA	SDA	SDA	1	0	1	1	1	1	1	BEh
SCL	V_{SS}	V_{SS}	1	1	0	0	0	0	0	C0h
SCL	V_{SS}	V_{DD}	1	1	0	0	0	0	1	C2h
SCL	V_{DD}	V_{SS}	1	1	0	0	0	1	0	C4h
SCL	V_{DD}	V_{DD}	1	1	0	0	0	1	1	C6h
SDA	V_{SS}	V_{SS}	1	1	0	0	1	0	0	C8h
SDA	V_{SS}	V_{DD}	1	1	0	0	1	0	1	CAh
SDA	V_{DD}	V_{SS}	1	1	0	0	1	1	0	CCh
SDA	V_{DD}	V_{DD}	1	1	0	0	1	1	1	CEh
SCL	V_{SS}	SCL	1	1	1	0	0	0	1	E0h
SCL	V_{SS}	SDA	1	1	1	0	0	1	0	E2h
SCL	V_{DD}	SCL	1	1	1	0	0	1	1	E4h
SCL	V_{DD}	SDA	1	1	1	0	1	0	0	E6h
SDA	V_{SS}	SCL	1	1	1	0	1	0	1	E8h
SDA	V_{SS}	SDA	1	1	1	0	1	1	0	EAh
SDA	V_{DD}	SCL	1	1	1	0	1	1	1	ECh
SDA	V_{DD}	SDA	1	1	1	0	0	0	1	EEh

8. Characteristics of the I²C-bus

The I²C-bus is for 2-way, 2-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

8.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as control signals (see Figure 11).

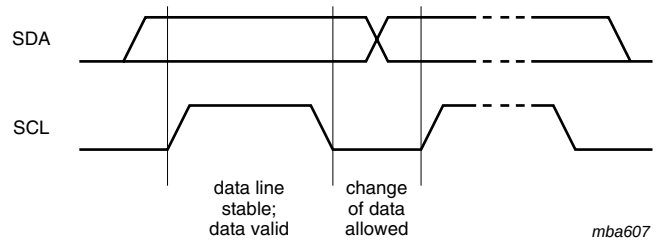


Fig 11. Bit transfer

8.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P) (see Figure 12.)

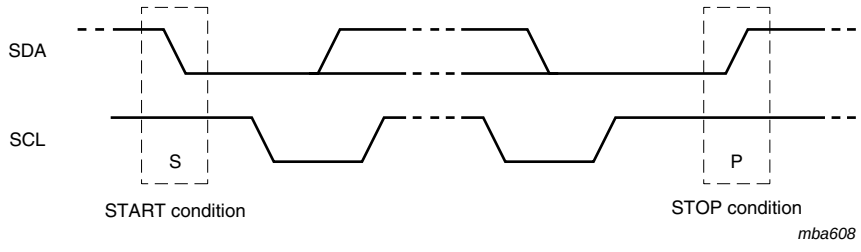


Fig 12. Definition of START and STOP conditions

8.2 System configuration

A device generating a message is a ‘transmitter’; a device receiving is the ‘receiver’. The device that controls the message is the ‘master’ and the devices which are controlled by the master are the ‘slaves’ (see Figure 13).

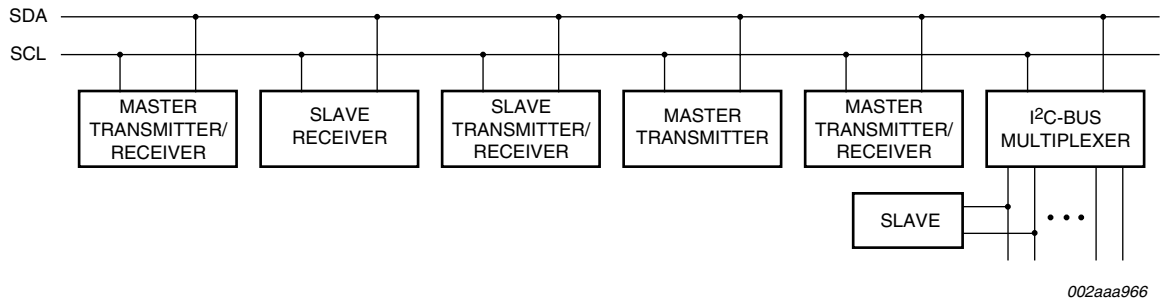


Fig 13. System configuration

8.3 Acknowledge

The number of data bytes transferred between the START and the STOP conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.

A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse; set-up and hold times must be taken into account.

A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

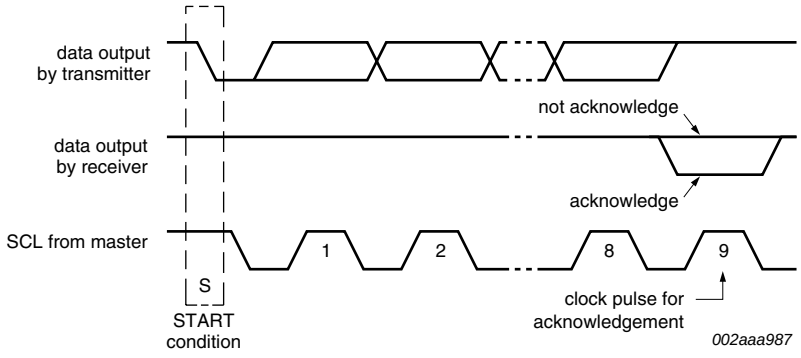
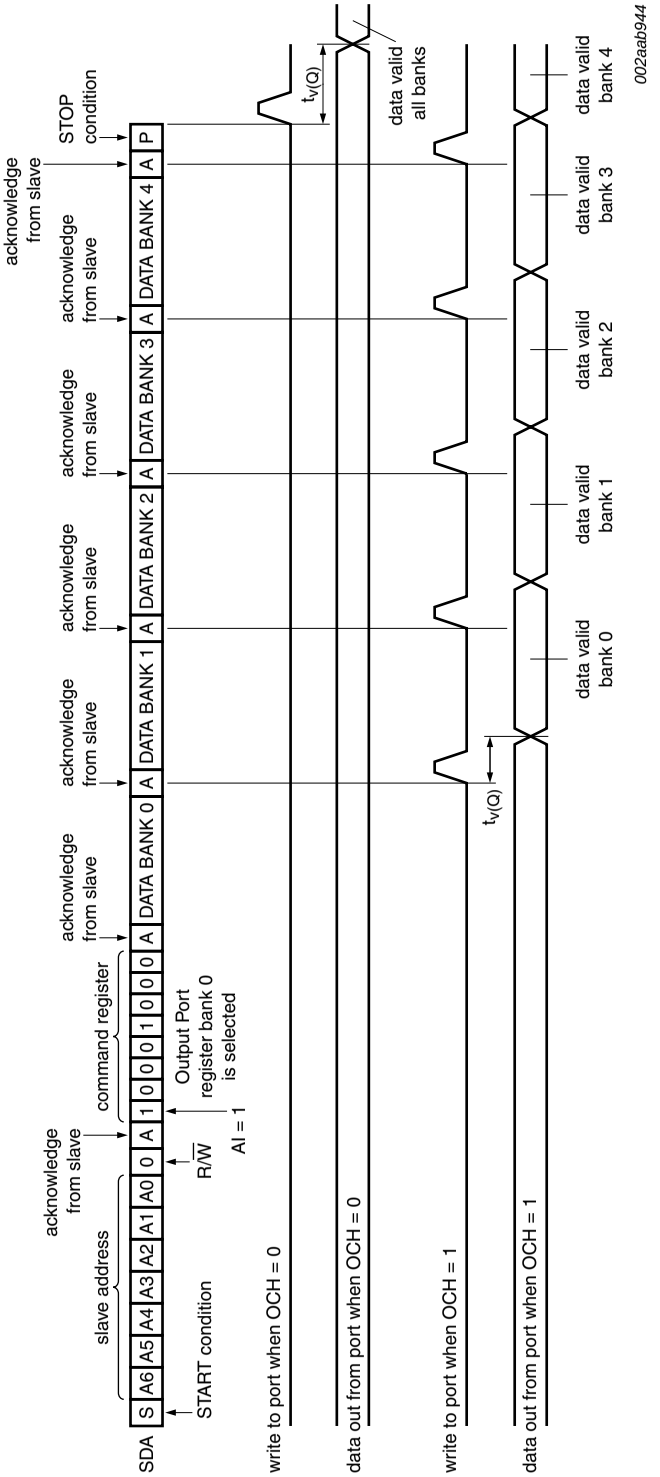


Fig 14. Acknowledgement on the I²C-bus

8.4 Bus transactions

Data is transmitted to the PCA9698 registers using ‘Write Byte’ transfers (see Figure 15, Figure 16, Figure 17, and Figure 18).

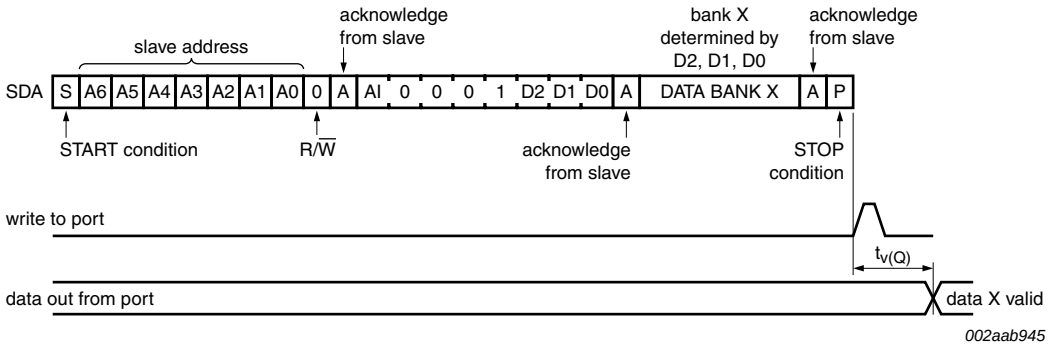
Data is read from the PCA9698 registers using ‘Read Byte’ and ‘Receive Byte’ transfers (see Figure 19 and Figure 20).



$\overline{OE}$ is LOW (with OEPOL = 0) or HIGH (with OEPOL = 1) to observe a change in the outputs.

If more than 5 bytes are written, previous data are overwritten.

Fig 15. Write to the 5 output ports

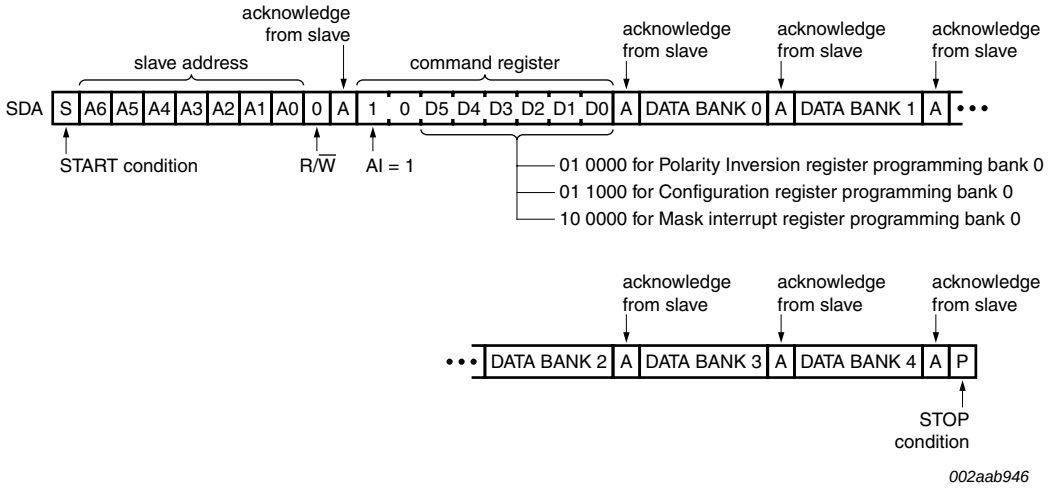


$\overline{OE}$ is LOW (with OEPOL = 0) or HIGH (with OEPOL = 1) to observe a change in the outputs.

OCH = 0. When OCH = 1, the change in the port happens at the acknowledge phase.

Two, three, or four adjacent banks can be programmed by using the Auto-Increment feature (AI = 1) and change at the corresponding output port becomes effective at the STOP command when OCH = 0, or at each acknowledge when OCH = 1.

Fig 16. Write to a specific output port

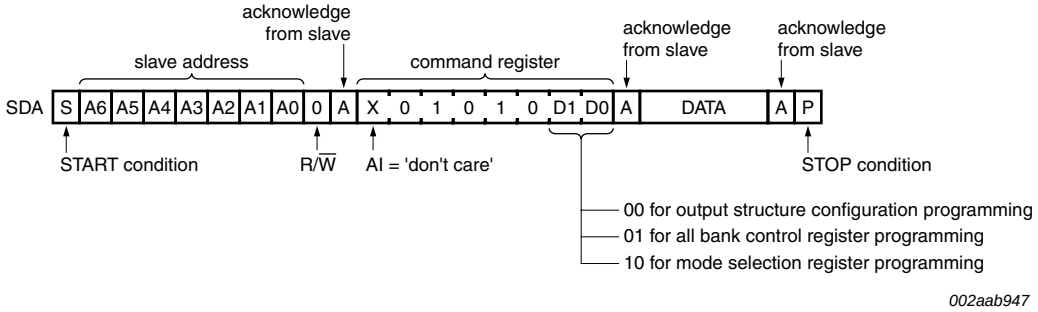


The programing becomes effective at the Acknowledge.

Less than 5 bytes can be programmed by using the same scheme. ‘D5 D4 D3 D2 D1 D0’ refers to the first register to be programmed.

If more than 5 bytes are written, previous data are overwritten (the sixth configuration register will roll over to the first addressed configuration register, the sixth Polarity Inversion register will roll over to the first addressed Polarity Inversion register, the sixth Mask interrupt register will roll over to the first addressed Mask interrupt register.

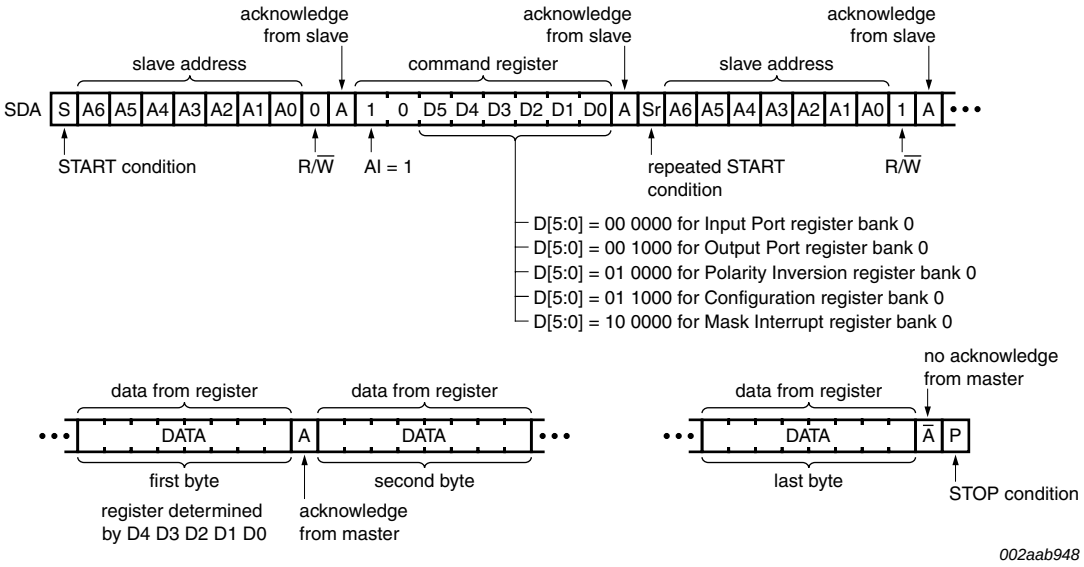
Fig 17. Write to the I/O Configuration, Polarity Inversion, or Mask interrupt registers (5 banks)



The programming becomes effective at the Acknowledge.

If more than 1 byte is written, previous data is overwritten.

Fig 18. Write to the output structure configuration, all bank control, or mode selection

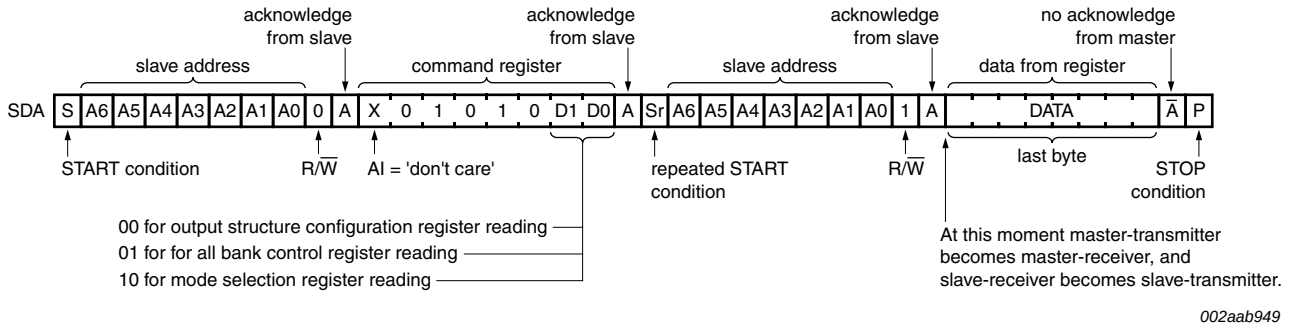


If AI = 0, the same register is read during the whole sequence.

If AI = 1, the register value is incremented after each read. When the last register bank is read, it rolls over to the first byte of the category (see category definition in Section 7.3 "Command register").

The $\overline{INT}$ signal is released only when the last register containing an input that changed has been read. For example, when IO2_4 and IO4_7 change at the same time and an Input Port register read sequence is initiated, starting with IP0, $\overline{INT}$ is released after IP4 is read (and not after IP2 is read).

Fig 19. Read from Input Port, Output Port, I/O Configuration, Polarity Inversion, or Mask interrupt registers



If AI = 0 or 1, the same register is read during the all sequence.

Fig 20. Read from output structure configuration, all bank control or mode selection registers

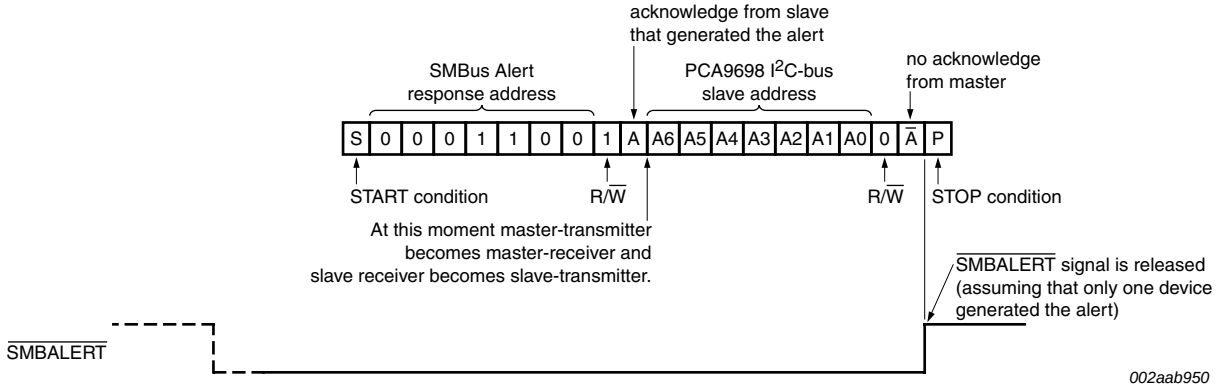
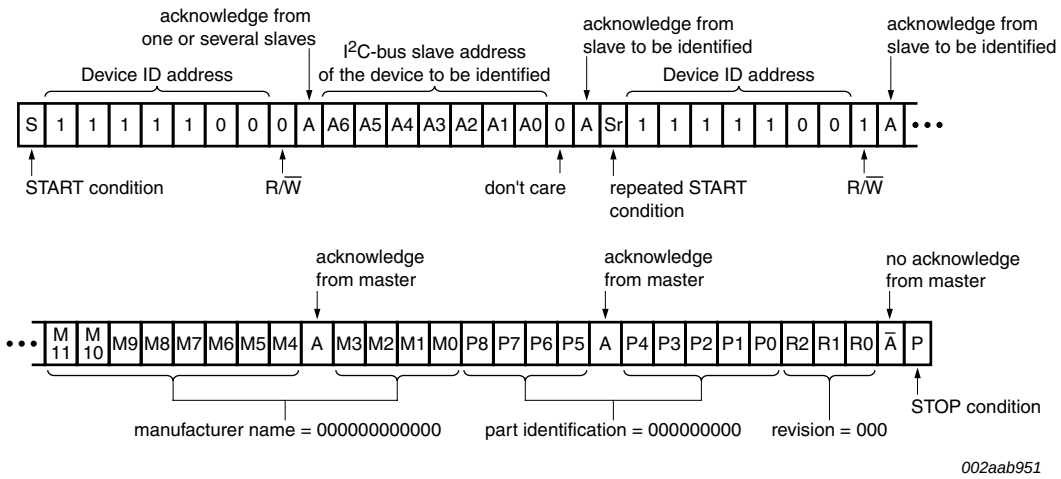
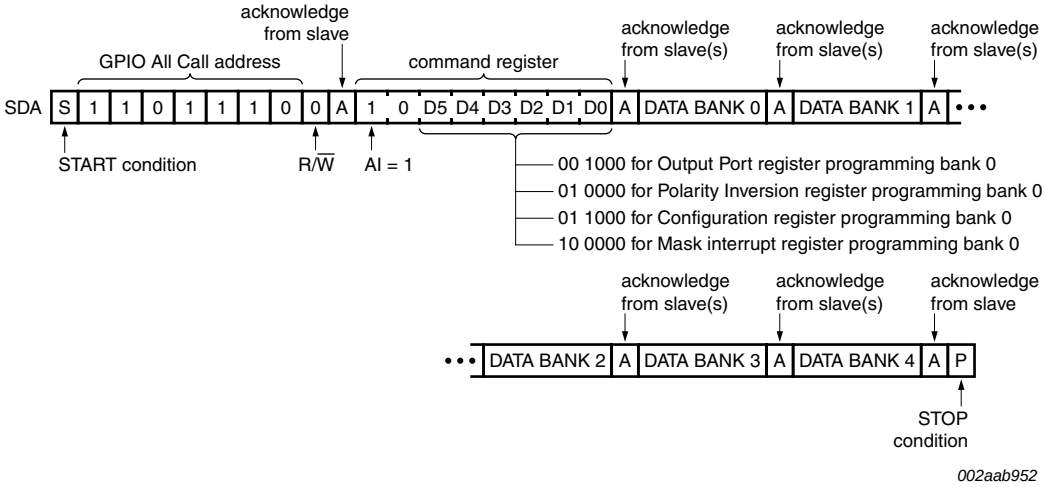


Fig 21. SMBus Alert procedure



If more than 3 bytes are read, the slave device loops back to the first byte (manufacturer byte) and keeps sending data until the master generates a 'No Acknowledge'.

Fig 22. Device ID field reading



Only slave devices with bit IOAC = 1 answer to the GPIO All Call transaction.

Output Port register programming becomes effective at the STOP command if OCH = 0, at each acknowledge if OCH = 1.

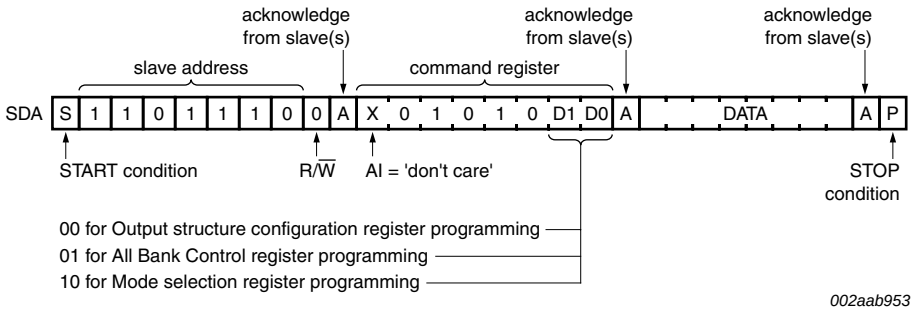
Configuration, Polarity Inversion, and Mask interrupt registers become effective at the acknowledge.

Less than 5 bytes can be programmed by using the same scheme.

'D5 D4 D3 D2 D1 D0' refers to the first register to be programmed.

If more than 5 bytes are written, previous data are overwritten (the sixth Configuration register will roll over to the first addressed Configuration register, the sixth Polarity Inversion register will roll over to the first addressed Polarity Inversion register, the sixth Mask interrupt register will roll over to the first addressed Mask interrupt register).

Fig 23. GPIO All Call write to the Output Port, I/O Configuration, Polarity Inversion, or Mask interrupt registers



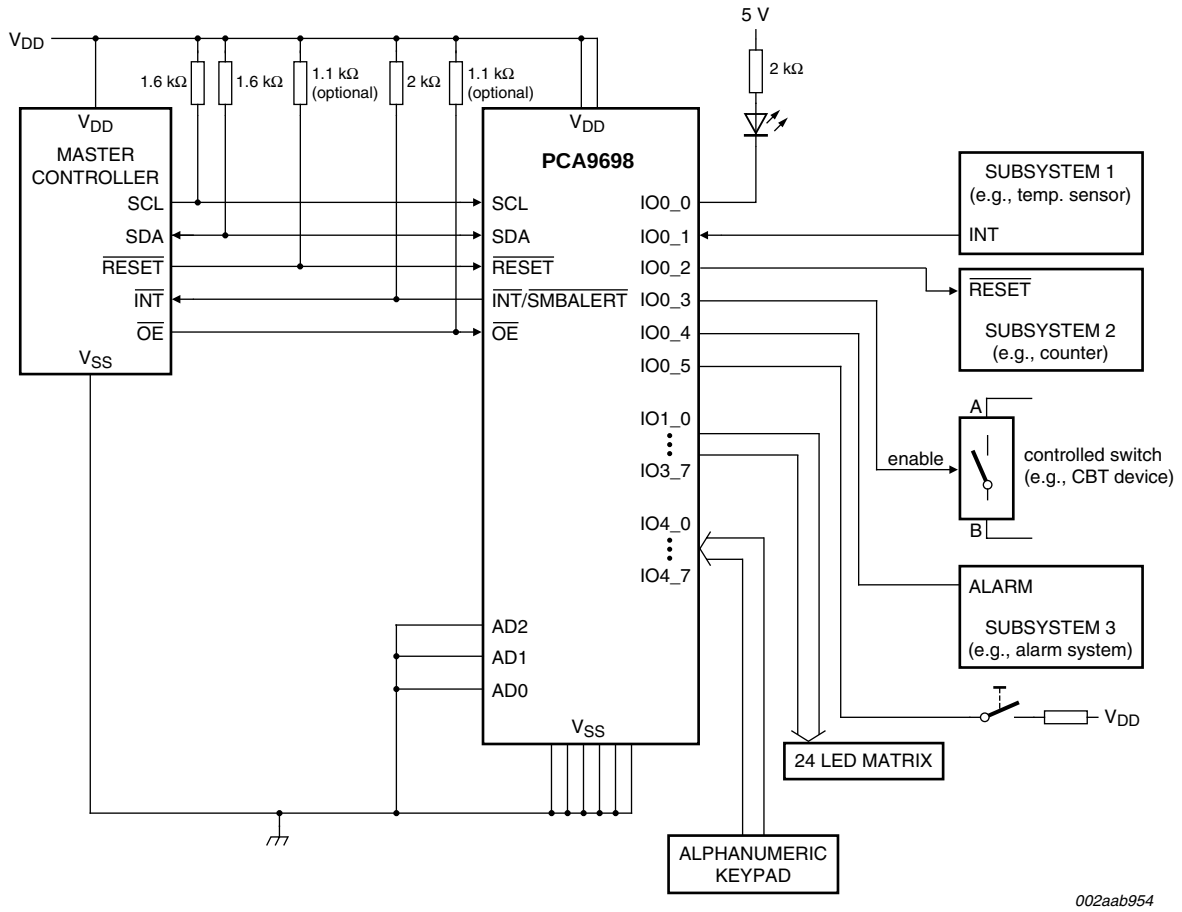
Only slave devices with bit 0 IOAC = 1 answer the GPIO All Call transaction.

The programming becomes effective at the acknowledge.

If more than 1 byte is written, previous data is overwritten.

Fig 24. GPIO All Call write to the Output structure configuration, All Bank Control, or Mode selection registers

9. Application design-in information



Device address configured as '0100 000x' for this example.

IO0_0, IO0_2, IO0_3, IO1_0 to IO3_7 are configured as outputs.

IO0_1, IO0_4, IO4_0 to IO4_7 are configured as inputs.

Fig 25. Typical application

10. Limiting values

Table 13. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+6	V
V_I	input voltage		V_{SS} − 0.5	5.5	V
I_I	input current		-	±20	mA
$V_{I/O}$	voltage on an input/output pin		V_{SS} − 0.5	5.5	V
$I_{O(IOx\_y)}$	output current on pin IOx_y		−20	+50	mA
I_{DD}	supply current		-	500	mA
I_{SS}	ground supply current		-	1100	mA
P_{tot}	total power dissipation		-	500	mW
T_{stg}	storage temperature		−65	+150	°C
T_{amb}	ambient temperature	operating	−40	+85	°C
T_j	junction temperature	operating	-	125	°C
		storage	-	150	°C

11. Static characteristics

Table 14. Static characteristics

V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.3	-	5.5	V
I_{DD}	supply current	Operating mode; no load; f_{SCL} = 1 MHz; AD0, AD1, AD2 = static H or L					
		V_{DD} = 2.3 V		-	135	200	µA
		V_{DD} = 3.3 V		-	250	400	µA
		V_{DD} = 5.5 V		-	550	800	µA
I_{stb}	standby current	no load; f_{SCL} = 0 kHz; I/O = inputs; $V_I = V_{DD}$					
		V_{DD} = 2.3 V		-	0.15	11	µA
		V_{DD} = 3.3 V		-	0.25	12	µA
		V_{DD} = 5.5 V		-	0.75	15.5	µA
V_{POR}	power-on reset voltage	no load; $V_I = V_{DD}$ or V_{SS}	[1]	-	1.70	2.0	V
Input SCL; input/output SDA							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.4 V		20	-	-	mA
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}		−1	-	+1	µA
C_i	input capacitance	$V_I = V_{SS}$		-	5	10	pF
I/Os							
V_{IL}	LOW-level input voltage			−0.5	-	$+0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			2	-	5.5	V
I_{OL}	LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 2.3 V	[2]	12	-	-	mA
		V_{OL} = 0.5 V; V_{DD} = 3.0 V	[2]	17	-	-	mA
		V_{OL} = 0.5 V; V_{DD} = 4.5 V	[2]	25	-	-	mA
$I_{OL(tot)}$	total LOW-level output current	V_{OL} = 0.5 V; V_{DD} = 4.5 V					
		TSSOP56 package	[2]	-	-	0.86	A
		HVQFN56 package	[2]	-	-	1.0	A
V_{OH}	HIGH-level output voltage	I_{OH} = −10 mA; V_{DD} = 2.3 V		1.6	-	-	V
		I_{OH} = −10 mA; V_{DD} = 3.0 V		2.3	-	-	V
		I_{OH} = −10 mA; V_{DD} = 4.5 V		4.0	-	-	V
I_{LIH}	HIGH-level input leakage current	V_{DD} = 3.6 V; $V_{I/O} = V_{DD}$		−1	-	+1	µA
I_{LIL}	LOW-level input leakage current	V_{DD} = 5.5 V; $V_{I/O} = V_{SS}$		−1	-	+1	µA
C_i	input capacitance			-	6	7	pF
C_o	output capacitance			-	6	7	pF

Table 14. Static characteristics *...continued*

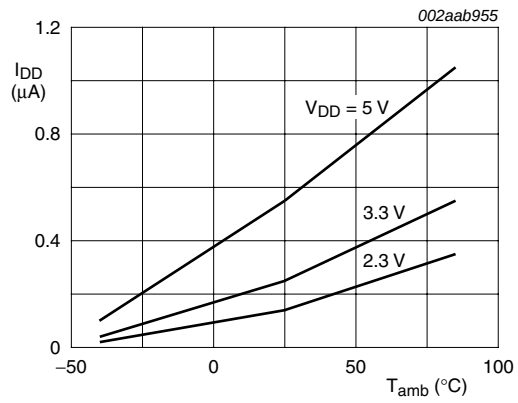
V_{DD} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Interrupt INT						
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	6	-	-	mA
C_o	output capacitance		-	3	5	pF
Inputs RESET and OE						
V_{IL}	LOW-level input voltage		−0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage		2	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance		-	3	5	pF
Inputs AD0, AD1, AD2						
V_{IL}	LOW-level input voltage		−0.5	-	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	5.5	V
I_{LI}	input leakage current		−1	-	+1	µA
C_i	input capacitance		-	3.5	5	pF

[1] V_{DD} must be lowered to 0.2 V in order to reset part.

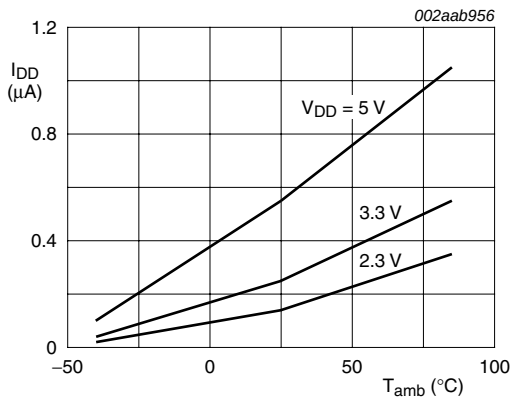
[2] Each bit must be limited to a maximum of 25 mA and the total package limited to the package maximum limit due to internal busing limits.

11.1 Performance curves



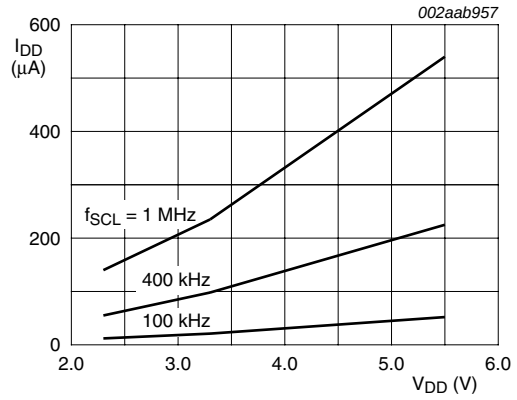
f_{SCL} = 400 kHz; all I/Os unloaded

Fig 26. Supply current as a function of temperature



SCL = V_{DD}; all I/Os unloaded

Fig 27. Standby current as a function of temperature



All I/Os unloaded; address pins static HIGH or LOW

Fig 28. Supply current as a function of supply voltage

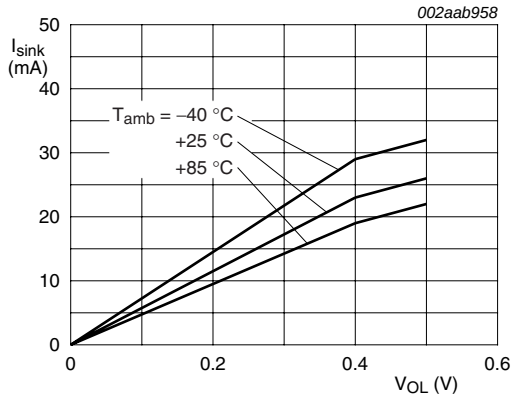


Fig 29. I/O sink current as a function of LOW-level output voltage (V_{DD} = 2.3 V)

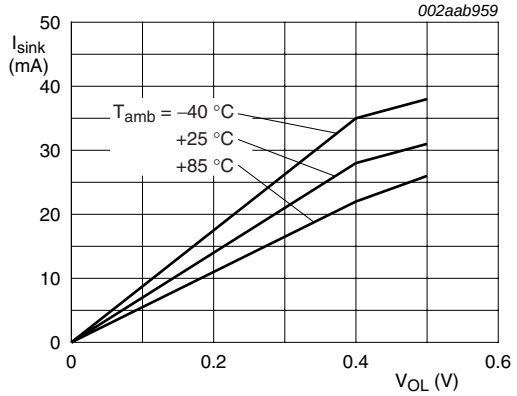


Fig 30. I/O sink current as a function of LOW-level output voltage (V_{DD} = 3.0 V)

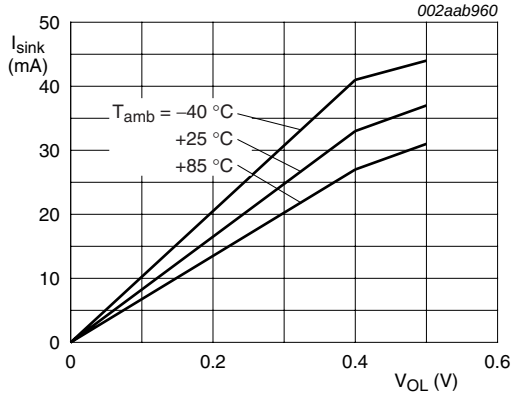


Fig 31. I/O sink current as a function of LOW-level output voltage (V_{DD} = 4.5 V)

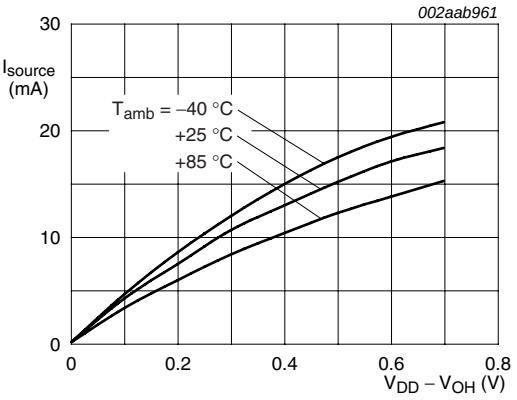


Fig 32. I/O source current as a function of HIGH-level output voltage (V_{DD} = 2 V)

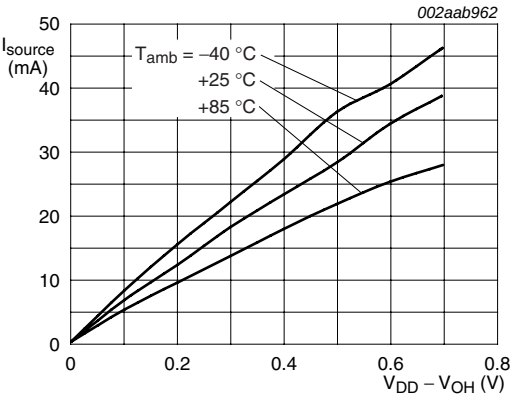


Fig 33. I/O source current as a function of HIGH-level output voltage (V_{DD} = 3.3 V)

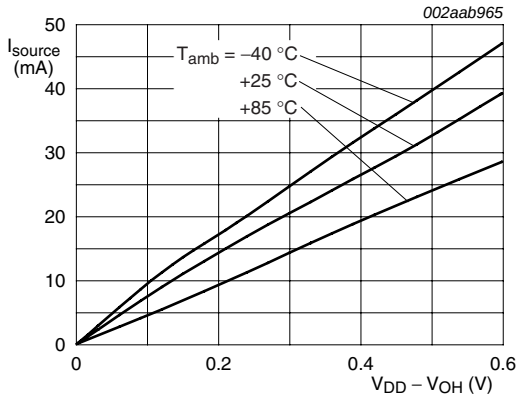
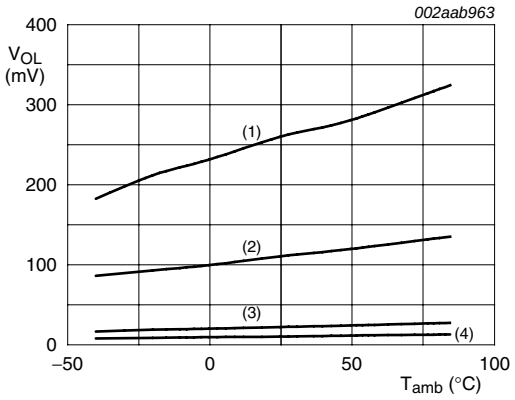
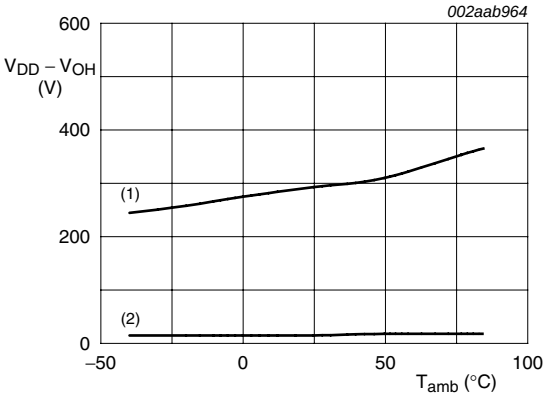


Fig 34. I/O source current as a function of HIGH-level output voltage (V_{DD} = 5 V)



(1) V_{DD} = 5 V; I_{sink} = 10 mA
(2) V_{DD} = 2.3 V; I_{sink} = 10 mA
(3) V_{DD} = 5 V; I_{sink} = 1 mA
(4) V_{DD} = 2.3 V; I_{sink} = 1 mA

Fig 35. I/O LOW-level output voltage as a function of temperature



(1) V_{DD} = 2.3 V; I_{source} = 10 mA
(2) V_{DD} = 5 V; I_{source} = 10 mA

Fig 36. HIGH-level output voltage as a function of temperature

12. Dynamic characteristics

Table 15. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I²C-bus		Fast-mode I²C-bus		Fast-mode Plus I²C-bus		Unit
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	[3]	0	100	0	400	0	1000	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	-	1.3	-	0.5	-	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	0.6	-	0.26	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	0.6	-	0.26	-	µs
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	0.6	-	0.26	-	µs
$t_{HD;DAT}$	data hold time		0	-	0	-	0	-	ns
$t_{VD;ACK}$	data valid acknowledge time	[1]	0.1	3.45	0.1	0.9	0.05	0.45	µs
$t_{VD;DAT}$	data valid time	[2]	300	-	75	-	75	450	ns
$t_{SU;DAT}$	data set-up time		250	-	100	-	50	-	ns
t_{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	0.5	-	µs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	0.26	-	µs
t_f	fall time of both SDA and SCL signals	[4][6]	-	300	$20 + 0.1C_b$ [5]	300	-	120	ns
t_r	rise time of both SDA and SCL signals	[4][6]	-	1000	$20 + 0.1C_b$ [5]	300	-	120	ns
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[7]	-	50	-	50	-	50	ns
Port timing									
t_{en}	enable time	output	-	80	-	80	-	80	ns
t_{dis}	disable time	output	-	40	-	40	-	40	ns
$t_{v(Q)}$	data output valid time		-	250	-	250	-	250	ns
$t_{su(D)}$	data input set-up time		100	-	100	-	100	-	ns
$t_{h(D)}$	data input hold time		250	-	250	-	250	-	ns
Interrupt timing									
$t_{v(INT\_N)}$	valid time on pin $\overline{INT}$		-	4	-	4	-	4	µs
$t_{rst(INT\_N)}$	reset time on pin $\overline{INT}$		-	4	-	4	-	4	µs
Reset									
$t_{w(rst)}$	reset pulse width		4	-	4	-	4	-	ns
$t_{rec(rst)}$	reset recovery time		0	-	0	-	0	-	ns
t_{rst}	reset time		100	-	100	-	100	-	ns

[1] $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA (out) LOW.

[2] $t_{VD;DAT}$ = minimum time for SDA data out to be valid following SCL LOW.

[3] Minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either SDA or SCL is held LOW for a minimum of 25 ms. Disable bus time-out feature for DC operation.

[4] A master device must internally provide a hold time of at least 300 ns for the SDA signal (refer to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.

[7] Input filters on the SDA and SCL inputs suppress noise spikes less than 50 ns.

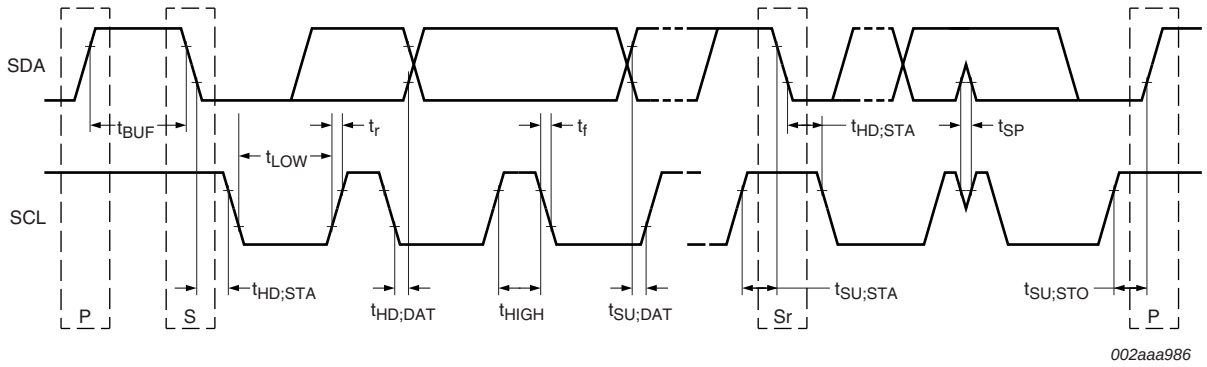
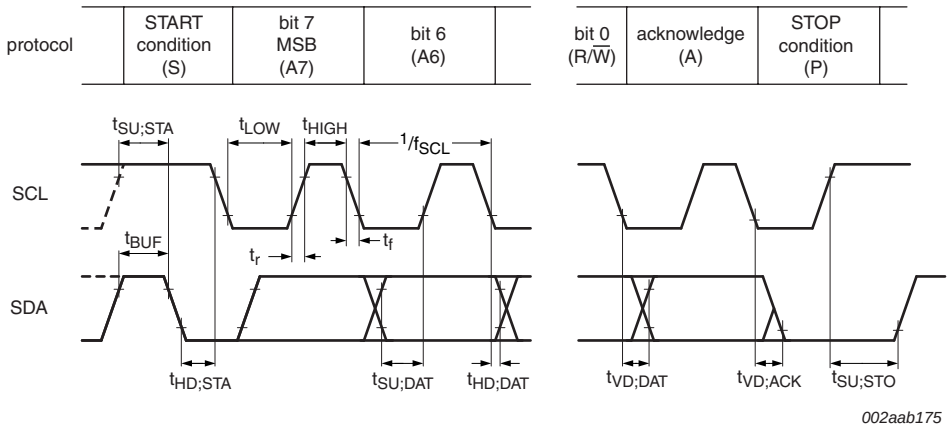


Fig 37. Definition of timing on the I²C-bus



Rise and fall times refer to V_{IL} and V_{IH}.

Fig 38. I²C-bus timing diagram

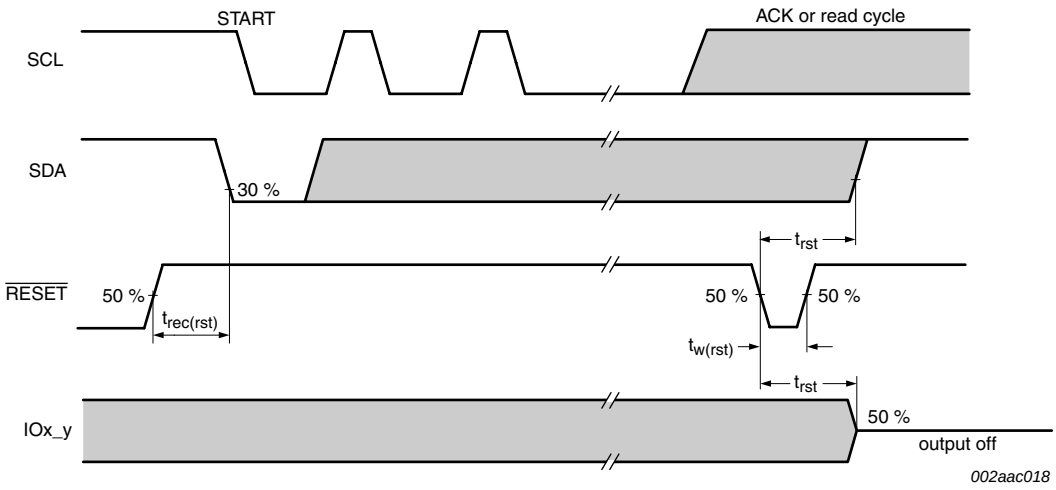
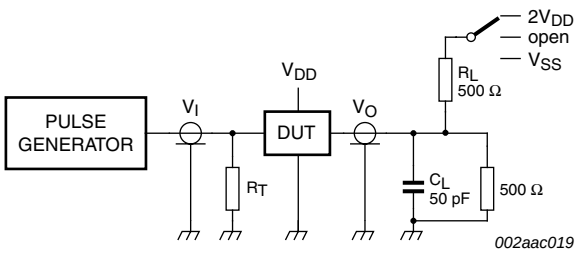


Fig 39. Reset timing

13. Test information



R_L = load resistance.

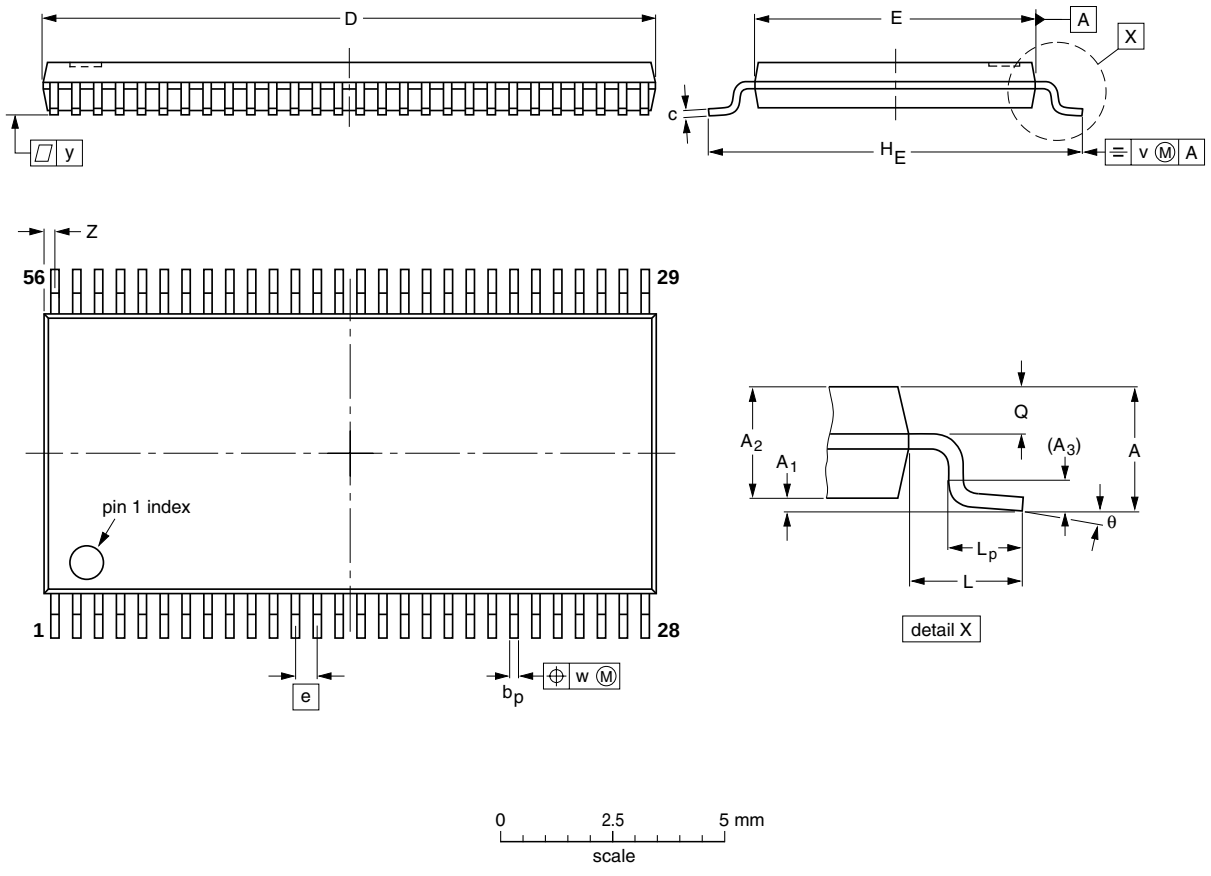
C_L = load capacitance includes jig and probe capacitance.

R_T = termination resistance should be equal to the output impedance Z_o of the pulse generators.

Fig 40. Test circuitry for switching times

14. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

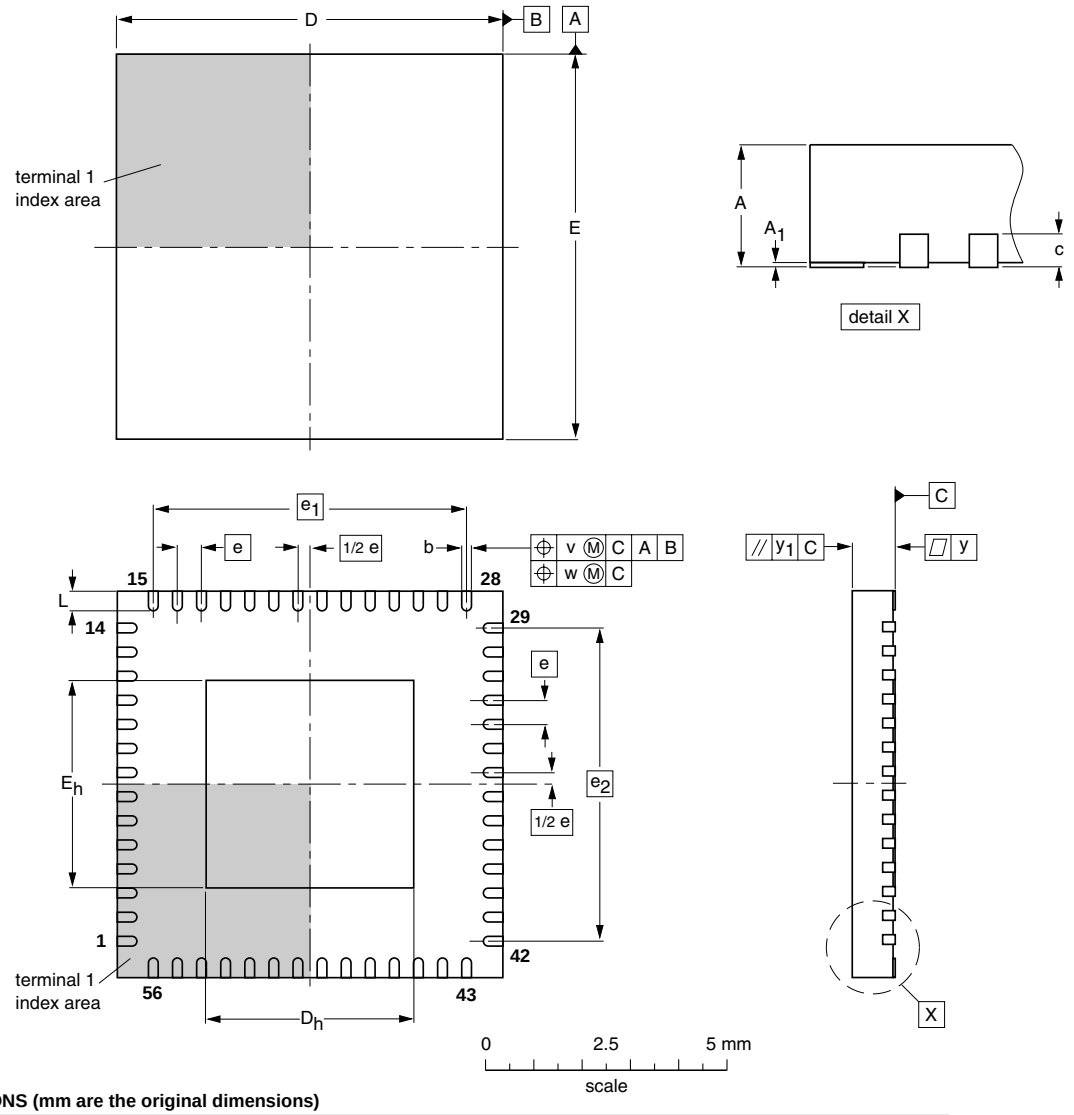
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT364-1		MO-153				~~99-12-27~~ 03-02-19

Fig 41. Package outline SOT364-1 (TSSOP56)

HVQFN56: plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm **SOT684-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	8.1 7.9	4.45 4.15	8.1 7.9	4.45 4.15	0.5	6.5	6.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT684-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

Fig 42. Package outline SOT684-1 (HVQFN56)

15. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 43) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16 and 17

Table 16. SnPb eutectic process (from J-STD-020C)

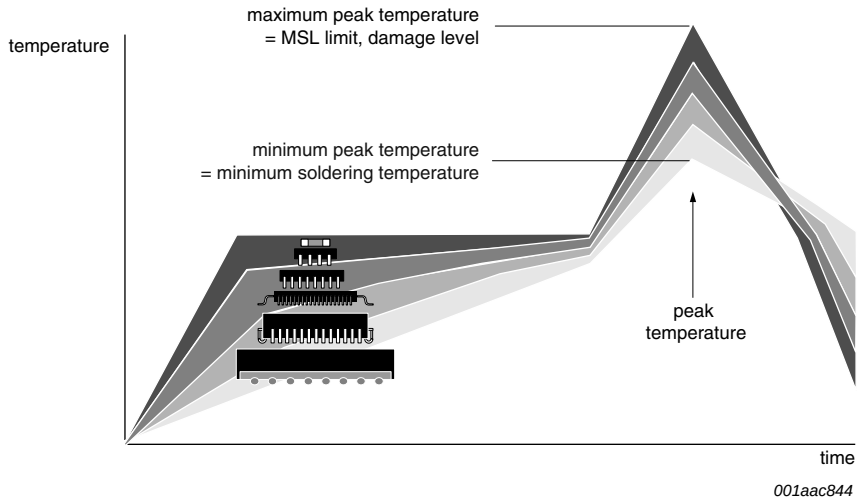
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 17. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 43.



MSL: Moisture Sensitivity Level

Fig 43. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 18. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input/Output
HBM	Human Body Model
I²C-bus	Inter-Integrated Circuit bus
LED	Light Emitting Diode
MM	Machine Model
PICMG	PCI Industrial Computer Manufacturers Group
PLC	Programmable Logic Controller
POR	Power-On Reset
PWM	Pulse Width Modulation
RAID	Redundant Array of Independent Discs
SMBus	System Management Bus

18. Revision history

Table 19. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9698 v.3	20100803	Product data sheet	-	PCA9698 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Figure 25 “Typical application”: text below figure corrected from “Device address configured as ‘0010 000x’ for this example.” to “Device address configured as ‘0100 000x’ for this example.” • Table 14 “Static characteristics”, sub-section “Inputs $\overline{\text{RESET}}$ and $\overline{\text{OE}}$” is corrected by removing I_{OH} specification.			
PCA9698 v.2	20060719	Product data sheet	-	PCA9698_1
PCA9698 v.1 (9397 750 13751)	20060224	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Date of release: 3 August 2010
Document identifier: PCA9698

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