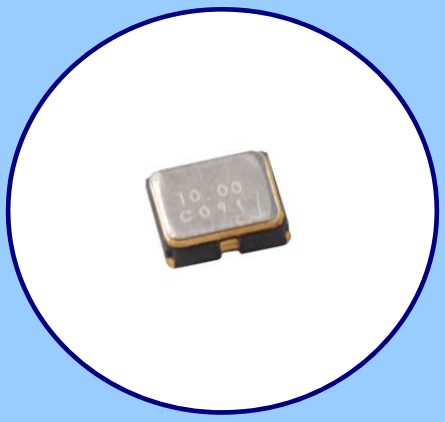
# Model 632

## HCMOS Clock Oscillator

### FEATURES

- **Standard 3.2mm x 2.5mm 4-Pad Surface Mount Package**
- **HCMOS Output**
- **Fundamental and 3rd Overtone Crystal Designs**
- Frequency Range 1 – 125 MHz
- Frequency Stability ±50 ppm Standard, ±25 ppm and ±20 ppm Available
- Operating Voltages +1.8Vdc, +2.5Vdc, +2.8Vdc, +3.3Vdc or +5.0Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging Standard, EIA-418
- **RoHS/Green Compliant [6/6]**



### APPLICATIONS

Model 632 is ideal for applications; such as broadband access, Ethernet/Gigabit Ethernet, microprocessors/DSP/FPGA, networking equipment computers and peripherals, digital video, cameras and other portable devices.

### ORDERING INFORMATION

632 □ □ □ □ □ □ M □ □ □ □ □

**SUPPLY VOLTAGE**

M = +1.8Vdc
N = +2.5Vdc
T = +2.8Vdc
L = +3.3Vdc
S = +5.0Vdc

**FREQUENCY STABILITY**

6 = ±20ppm [1]
5 = ±25ppm
3 = ±50ppm

**FREQUENCY IN MHz**

M - indicates MHz and decimal point. [2]

**TEMPERATURE RANGE**

C = -20°C to +70°C
I = -40°C to +85°C

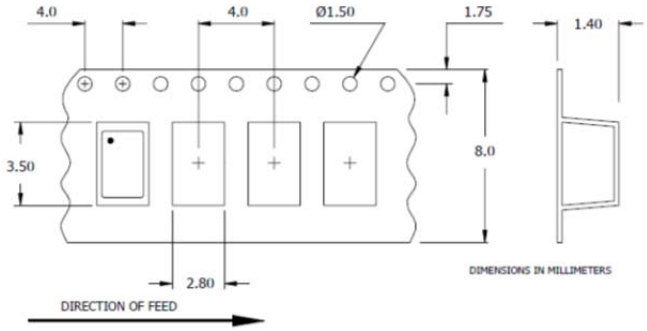
1] Consult factory for 6l Stability/Temperature availability.

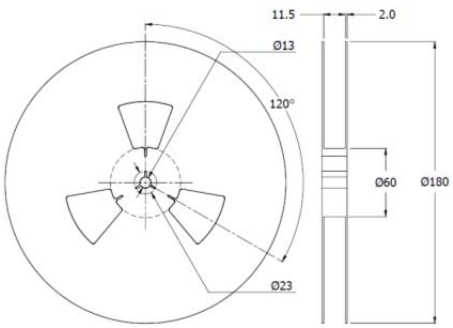
2] Frequency is recorded with three leading significant digits before the 'M' and 5 significant digits after the 'M' [including zeros].
[Ex. 3.579545 MHz, code as 003M57954; 14.31818 MHz, code as 014M31818; 125 MHz, code as 125M00000]

**Not all performance combinations and frequencies may be available.**
**Contact your local CTS Representative or CTS Customer Service for availability.**

### PACKAGING INFORMATION [reference]

Device quantity is 1k pcs. minimum and 3k pcs. maximum per 180mm reel. 8mm tape width.



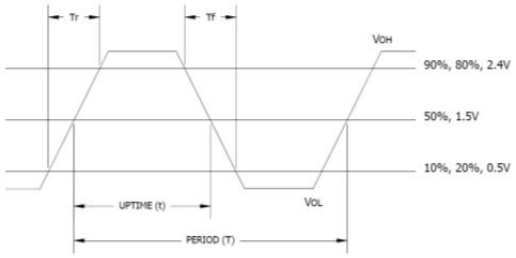



## ELECTRICAL CHARACTERISTICS

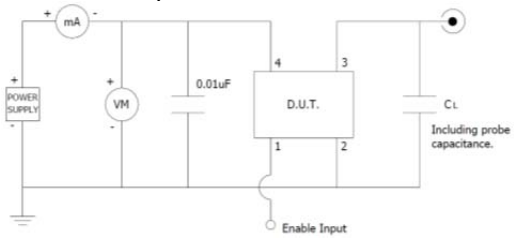
| | PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| ELECTRICAL PARAMETERS | Maximum Supply Voltage | $V_{CC}$ | - | -0.5 | - | 4.0 | V |
| | Storage Temperature | $T_{STG}$ | - | -40 | - | +100 | °C |
| | Frequency Range | $f_O$ | - | 1.0 | - | 125 | MHz |
| | Frequency Stability [See Note 1and Ordering Information] | $\Delta f/f_O$ | - | - | - | 20, 25, 50 | ± ppm |
| | Aging | $\Delta f/f_O$ | - | - | - | 3 | ± ppm/yr |
| | Operating Temperature<br>Commercial<br>Industrial | $T_A$ | - | <br>-20<br>-40 | <br>+25 | <br>+70<br>+85 | °C |
| | Supply Voltage<br>Model 632M<br>Model 632N<br>Model 632T<br>Model 632L<br>Model 632S | $V_{CC}$ | ± 10 % | <br>1.62<br>2.25<br>2.52<br>2.97<br>4.50 | <br>1.8<br>2.5<br>2.8<br>3.3<br>5.0 | <br>1.98<br>2.75<br>3.08<br>3.63<br>5.50 | V |
| | Supply Current<br>Model 632M<br>[+18V]<br>Model 632N, 632T<br>[+2.5V, +2.8V]<br>Model 632L, 632S<br>[+3.3V, +5.0V] | $I_{CC}$ | $C_L$ = 15pF<br>1.0 MHz to 100 MHz<br>100.1 MHz to 125 MHz<br>1.0 MHz to 100 MHz<br>100.1 MHz to 125 MHz<br>1.0 MHz to 100 MHz<br>100.1 MHz to 125 MHz | <br>-<br>-<br>-<br>-<br>-<br>- | <br>-<br>-<br>-<br>-<br>-<br>- | <br>7<br>12<br>10<br>20<br>15<br>25 | mA |
| | Output Load | $C_L$ | | - | - | 15 | pF |
| | Output Voltage Levels<br>Logic '1' Level<br>Logic '0' Level | <br>$V_{OH}$<br>$V_{OL}$ | <br>CMOS Load<br>CMOS Load | <br>90%$V_{CC}$<br>- | <br>-<br>- | <br>-<br>10%$V_{CC}$ | V |
| | Output Current<br>Logic '1' Level [M,N,T,L,S] | <br>$I_{OH}$ | <br>$V_{OH}$ = 90%$V_{CC}$ [1.8V, 2.5/2.8V, 3.3V, 5.0V] | <br>- | <br>- | <br>-2, -4, -8, -16 | mA |
| | Logic '0' Level [M,N,T,L,S] | $I_{OL}$ | $V_{OL}$ = 10%$V_{CC}$ [1.8V, 2.5/2.8V, 3.3V, 5.0V] | - | - | +2, +4, +8, +16 | |
| | Output Duty Cycle | SYM | @ 50% Level | 45 | - | 55 | % |
| | Rise and Fall Time<br>Model 632M<br>[+18V]<br>Model 632N, 632T<br>[+2.5V, +2.8V]<br>Model 632L, 632S<br>[+3.3V, +5.0V] | $T_R$, $T_F$ | @ 10% - 90% Levels, $C_L$ = 15pF<br>1.0 MHz to 20 MHz<br>20.1 MHz to 125 MHz<br>1.0 MHz to 20 MHz<br>20.1 MHz to 125 MHz<br>1.0 MHz to 20 MHz<br>20.1 MHz to 125 MHz | <br>-<br>-<br>-<br>-<br>-<br>- | <br>-<br>-<br>-<br>-<br>-<br>- | <br>5<br>4<br>4<br>3<br>3<br>2 | ns |
| | Start Up Time | $T_S$ | Application of $V_{CC}$ | - | - | 2 | ms |
| | Enable Function<br>Enable Input Voltage | <br>$V_{IH}$ | <br>Pin 1 Logic '1', Output Enabled | <br>0.7*$V_{CC}$ | <br>- | <br>- | V |
| | Disable Input Voltage | $V_{IL}$ | Pin 1 Logic '0', Output Disabled | - | - | 0.3*$V_{CC}$ | |
| | Enable Time [M,N,T,L,S] | $T_{PLZ}$ | Pin 1 Logic '1' | - | - | 2 | ms |
| | Standby Current | $I_{ST}$ | Pin 1 Logic '0', Output Disabled | - | - | 15 | µA |
| | Period Jitter, pk-pk | pjpk-pk | - | - | - | 40 | ps |
| | Phase Jitter, RMS | tjrms | Bandwidth 12 kHz - 20 MHz | - | - | 1 | |

Notes:
1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and aging.

**LVCMOS OUTPUT WAVEFORM**




**TEST CIRCUIT, CMOS LOAD**

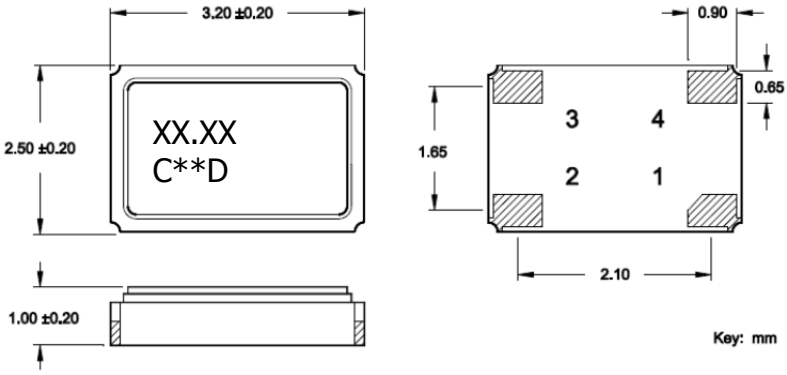



**ENABLE TRUTH TABLE**

| PIN 1 | PIN 3 |
|---|---|
| Logic '1' | Output |
| Open | Output |
| Logic '0' | High Imp. |

## MECHANICAL SPECIFICATIONS

### PACKAGE DRAWING




### MARKING INFORMATION

1. XX.XX – Frequency in MHz.
2. C – CTS and Pin 1 identifier.
3. ** - Manufacturing Site Code.
4. D – Manufacturing Date Code.
   [See Table 1 for codes.]
5. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.

### NOTES

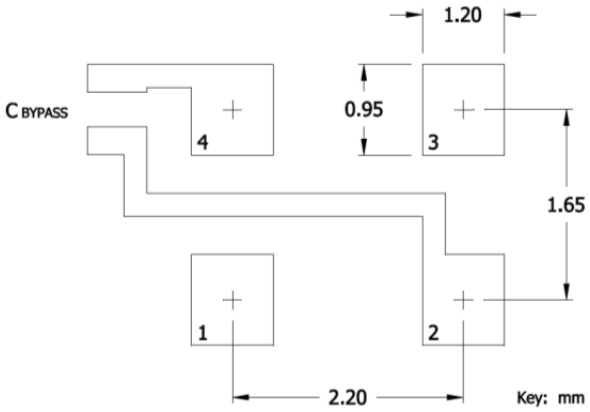
1. Termination pads (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
3. MSL = 1.

### TABLE I

| YEAR \ MONTH | JAN | FEB | MAR | APR | MAY | JUN | JUL | AUG | SEP | OCT | NOV | DEC |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2001 2005 2009 2013 2017 | A | B | C | D | E | F | G | H | J | K | L | M |
| 2002 2006 2010 2014 2018 | N | P | Q | R | S | T | U | V | W | X | Y | Z |
| 2003 2007 2011 2015 2019 | a | b | c | d | e | f | g | h | j | k | l | m |
| 2004 2008 2012 2016 2020 | n | p | q | r | s | t | u | v | w | x | y | z |

### SUGGESTED SOLDER PAD GEOMETRY

$C_{BYPASS}$ should be ≥ 0.01 uF.




### D.U.T. PIN ASSIGNMENTS

| PIN | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | EOH | Enable |
| 2 | GND | Circuit & Package Ground |
| 3 | Output | RF Output |
| 4 | $V_{CC}$ | Supply Voltage |

LifeElectronics
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**ООО «ЛайфЭлектроникс»** **“LifeElectronics” LLC**

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