

NCV7707

Door-Module Driver-IC

The NCV7707 is a powerful Driver-IC for automotive body control systems. The IC is designed to control several loads in the front door of a vehicle. The monolithic IC is able to control mirror functions like mirror positioning, heating and folding including the electro-chromic mirror feature. Besides two half-bridge outputs to control lock and safe-lock motors, the device features four high-side outputs to drive LEDs or incandescent bulbs (up to 10 W). To allow maximum flexibility, all lighting outputs can be PWM controlled thru PWM inputs (external signal source) or by an internal programmable PWM generator unit. The NCV7707 is controlled thru a 24 bit SPI interface with in-frame response.

Features

- Operating Range from 5.5 V to 28 V
- Six High-Side and Six Low-Side Drivers Connected as Half-Bridges
 - ◆ 2x Half-bridges $I_{load} = 0.75\text{ A}$; $R_{DS(on)} = 1.6\ \Omega @ 25^{\circ}\text{C}$
 - ◆ 2x Half-Bridges $I_{load} = 3\text{ A}$; $R_{DS(on)} = 300\text{ m}\Omega @ 25^{\circ}\text{C}$
 - ◆ 2x Half-Bridges $I_{load} = 6\text{ A}$; $R_{DS(on)} = 150\text{ m}\Omega @ 25^{\circ}\text{C}$
- Four High-Side Lamp Drivers
 - ◆ 2x LED; $I_{load} = 0.3\text{ A}$; $R_{DS(on)} = 1.4\ \Omega @ 25^{\circ}\text{C}$
 - ◆ 2x 10 W; configurable as LED Driver; $I_{load} = 2.5\text{ A}$; $R_{DS(on)} = 300\text{ m}\Omega @ 25^{\circ}\text{C}$
- One High-Side Driver for Mirror Heating; $I_{load} = 6\text{ A}$; $R_{DS(on)} = 100\text{ m}\Omega @ 25^{\circ}\text{C}$
- Electro Chromic Mirror Control
 - ◆ 1x 6-Bit Selectable Output Voltage Controller
 - ◆ 1x LS for EC Control; $I_{load} = 0.75\text{ A}$; $R_{DS(on)} = 1.6\ \Omega @ 25^{\circ}\text{C}$
- Independent PWM Functionality for All Outputs
- Integrated Programmable PWM Generator Unit for All Lamp Driver Outputs
- Programmable Soft-start Function to Drive Loads with Higher Inrush Currents as Current Limitation Value
- Multiplex Current Sense Analog Output for Advanced Load Monitoring
- Very Low Current Consumption in Standby Mode
- Charge Pump Output to Control an External Reverse Polarity Protection MOSFET
- 24-Bit SPI Interface for Output Control and Diagnostic
- Protection Against Short-circuit, Overvoltage and Over-temperature
- SSOP36-EP Power Package
- This is a Pb-Free Device

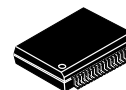
Typical Applications

- De-centralized Door Electronic Systems
- Body Control Units (BCUs)



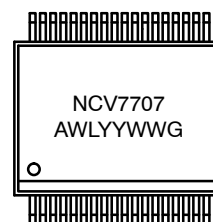
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SSOP36 EP
CASE 940AB

MARKING DIAGRAM



| | |
|----|---------------------|
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb-Free Package |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 36 of this data sheet.

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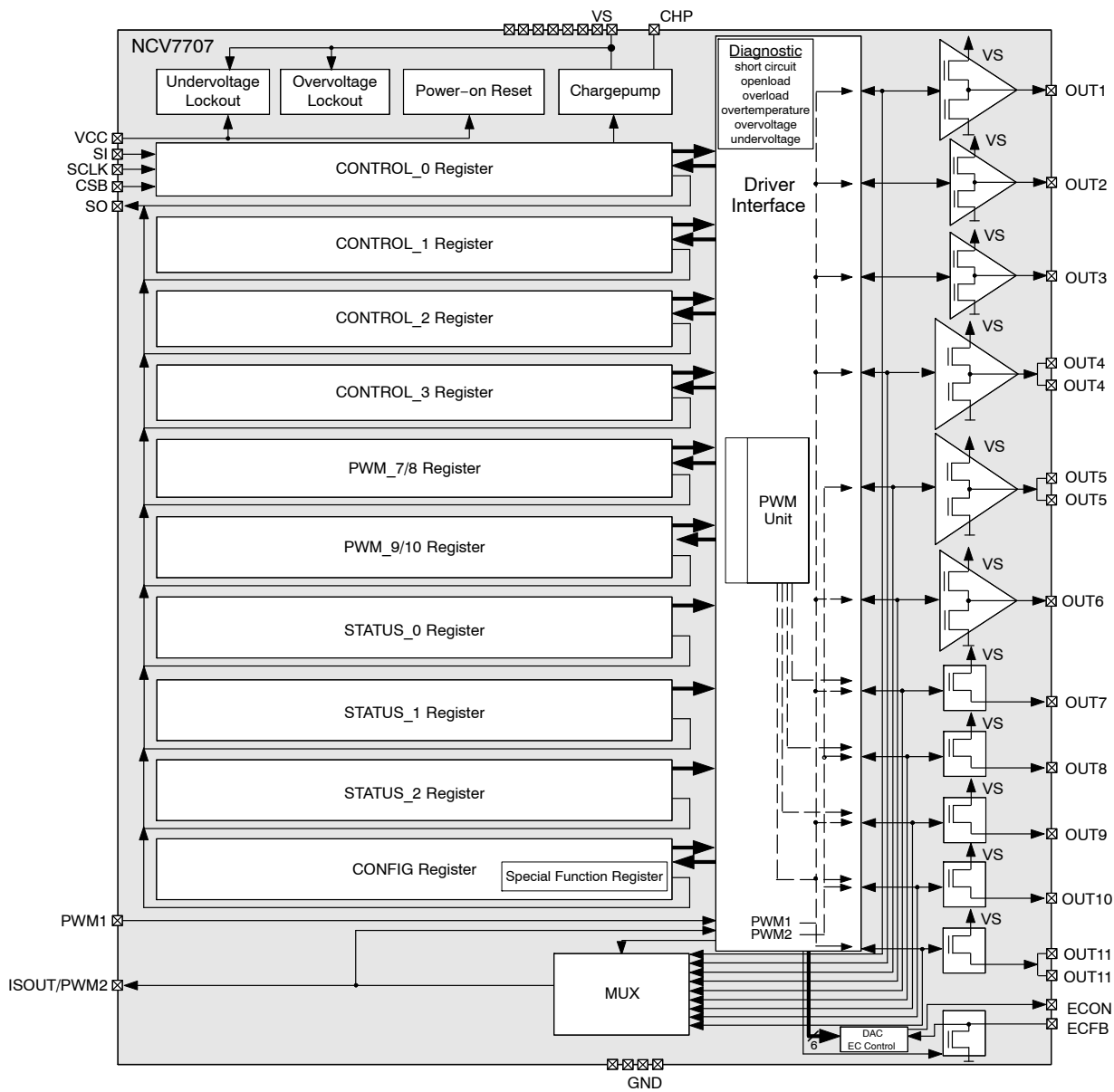


Figure 1. Block Diagram

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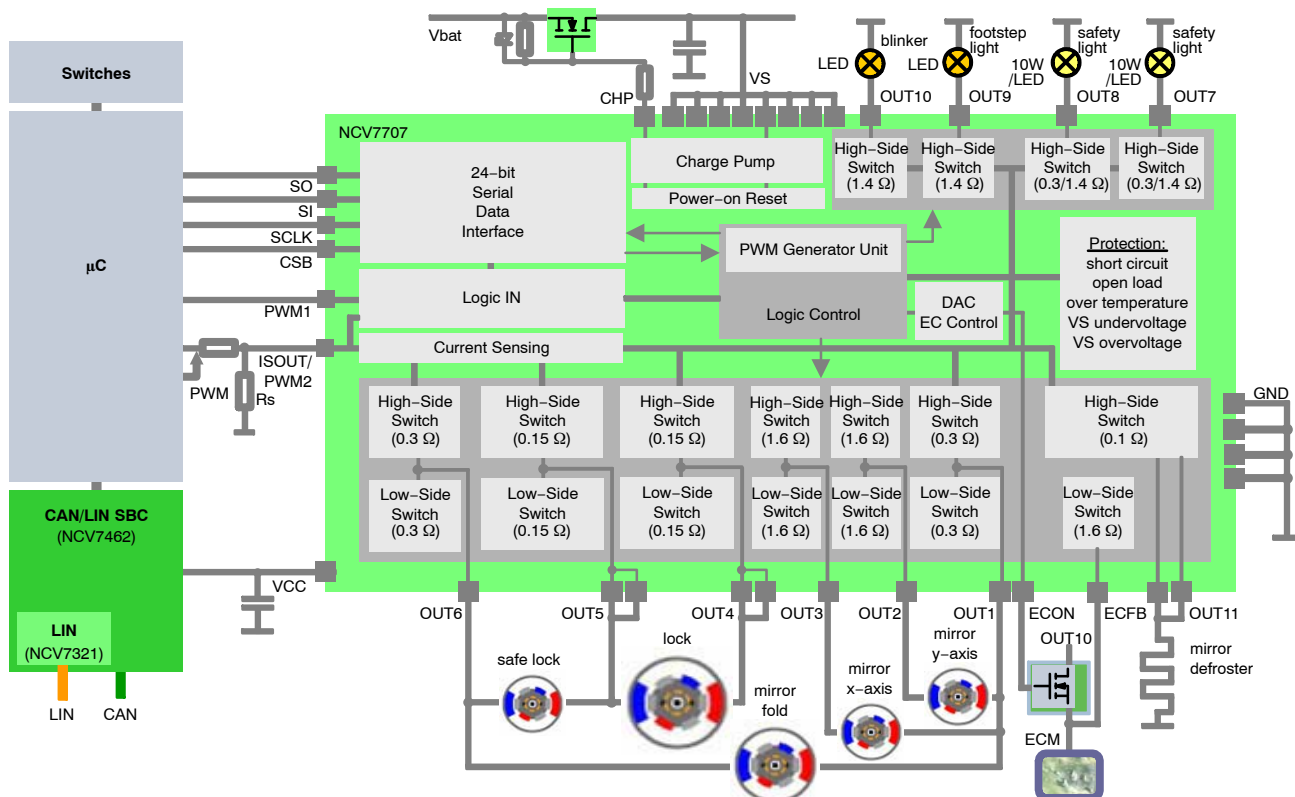


Figure 2. Application Diagram

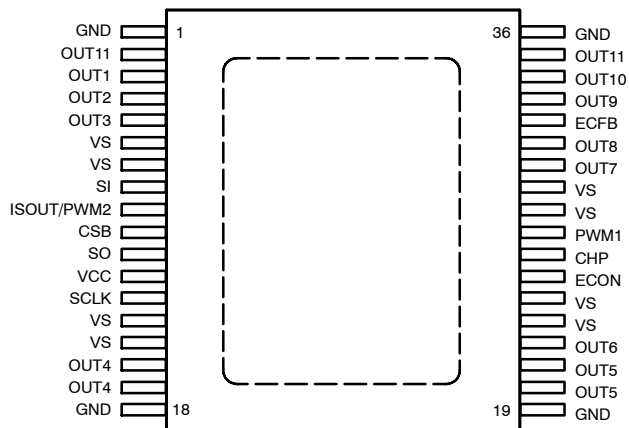


Figure 3. Pin Connections (Top View)

PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Pin Type | Description |
|---------|--------------|-------------------------------|---|
| 1 | GND | Ground | Ground Supply (all GND pins have to be connected externally) |
| 2 | OUT11 | HS driver Output | Heater Output (has to be connected externally to pin 35) |
| 3 | OUT1 | Half bridge driver Output | Mirror common Output |
| 4 | OUT2 | Half bridge driver Output | Mirror x/y control Output |
| 5 | OUT3 | Half bridge driver Output | Mirror x/y control Output |
| 6 | VS | Supply | Battery Supply Input (all VS pins have to be connected externally) |
| 7 | VS | Supply | Battery Supply Input (all VS pins have to be connected externally) |
| 8 | SI | Digital Input | SPI interface Serial Data Input |
| 9 | ISOUT / PWM2 | Digital Input / Analog Output | PWM control Input / Current Sense Output. This pin is a bidirectional pin. Depending on the selected multiplexer bits, an image of the instant current of the corresponding HS stage can be read out. This pin can also be used as PWM control input pin for OUT5, OUT8 and OUT10. |
| 10 | CSB | Digital Input | SPI interface Chip Select |
| 11 | SO | Digital Output | SPI interface Serial Data Output |
| 12 | VCC | Supply | Logic Supply Input |
| 13 | SCLK | Digital Input | SPI interface Shift Clock |
| 14 | VS | Supply | Battery Supply Input (all VS pins have to be connected externally) |
| 15 | VS | Supply | Battery Supply Input (all VS pins have to be connected externally) |
| 16 | OUT4 | Half bridge driver Output | Door Lock Output (has to be connected externally to pin 17) |
| 17 | OUT4 | Half bridge driver Output | Door Lock Output (has to be connected externally to pin 16) |
| 18 | GND | Ground | Ground Supply (all GND pins have to be connected externally) |
| 19 | GND | Ground | Ground Supply (all GND pins have to be connected externally) |
| 20 | OUT5 | Half bridge driver Output | Door Lock Output (has to be connected externally to pin 21) |
| 21 | OUT5 | Half bridge driver Output | Door Lock Output (has to be connected externally to pin 20) |
| 22 | OUT6 | Half bridge driver Output | Safe-Lock / Mirror Fold Output |
| 23 | VS | Supply | Battery Supply Input (all VS pins have to be connected externally) |
| 24 | VS | Supply | Battery Supply Input (all VS pins have to be connected externally) |
| 25 | ECON | ECM driver Output | Electrochromic mirror control DAC output. If the Electrochrome feature is selected, this output controls an external Mosfet, otherwise it remains in high-impedance state. If the electrochrome feature is not used in the application and not selected via SPI the pin can be connected to VS. |
| 26 | CHP | Analog Output | Reverse Polarity FET Control Output |
| 27 | PWM1 | Digital Input | PWM control Input for OUT1-4, OUT6/7, OUT9, OUT11 |
| 28 | VS | Supply | Battery Supply Input (all VS pins have to be connected externally) |
| 29 | VS | Supply | Battery Supply Input (all VS pins have to be connected externally) |
| 30 | OUT7 | HS driver Output | LED / Bulb Output |
| 31 | OUT8 | HS driver Output | LED / Bulb Output |
| 32 | ECFB | ECM Input / Output | Electrochromic Mirror Feedback Input, Fast discharge transistor Output |
| 33 | OUT9 | HS driver Output | LED Output |
| 34 | OUT10 | HS driver Output | LED Output |
| 35 | OUT11 | HS driver Output | Heater Output (has to be connected externally to pin 2) |
| 36 | GND | Ground | Ground Supply (all GND pins have to be connected externally) |
| | Heat slug | Ground | Substrate; Heat slug has to be connected to all GND pins |

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ABSOLUTE MAXIMUM RATINGS

| Symbol | Rating | Min | Max | Unit |
|--|---|----------------------------|---------------------------|------|
| V _s | Power supply voltage – Continuous supply voltage – Transient supply voltage (t < 500 ms, "clamped load dump") | -0.3 -0.3 | 28 40 | V |
| V _{CC} | Logic supply | -0.3 | 5.5 | V |
| V _{dig} | DC voltage at all logic pins (SO, SI, SCLK, CSB, PWM1) | -0.3 | V _{CC} + 0.3 | V |
| Visout/pwm2 | Current monitor output / PWM2 logic input | -0.3 | V _{CC} + 0.3 | V |
| V _{chp} | Charge pump output (the most stringent value is applied) | -25 V _s - 25 | 40 V _s + 15 | V |
| V _{outx} , V _{econ} , V _{ecfb} | Static output voltage (OUT1-11, ECON, ECFB) | -0.3 | V _s + 0.3 | V |
| I _{out1/6} | OUT1/6 Output current | -5 | 5 | A |
| I _{out2/3} | OUT2/3 Output current | -1.25 | 1.25 | A |
| I _{out4/5} | OUT4/5 Output current | -10 | 10 | A |
| I _{out7/8} | OUT7/8 Output current | -5 | 5 | A |
| I _{out9/10} | OUT9/10 Output current | -1.25 | 1.25 | A |
| I _{out11} | OUT11 Output current | -10 | 10 | A |
| I _{out_ecfb} | ECFB Output current | | 1.25 | A |
| ESD_HBM | ESD Voltage, Human Body Model (HBM); (100 pF, 1500 Ω) (Note 1) – All pins – Output pins OUT1-6 and ECFB to GND (all unzapped pins grounded) | -2 -4 | 2 4 | kV |
| ESD_CDM | ESD according to CDM (Charge Device Model) (Note 1) – All pins – Corner pins | -500 -750 | 500 750 | V |
| T _J | Operating junction temperature range | -40 | 150 | °C |
| T _{stg} | Storage temperature range | -55 | 150 | °C |
| MSL | Moisture sensitivity level (Note 2) | MSL3 | | |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)

ESD Charge Device Model tested per EIA/JES D22/C101, Field Induced Charge Model

2. For soldering information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

| Symbol | Rating | Value | Unit |
|------------------|--|-------|------|
| R _{θJA} | Thermal Characteristics, SSOP36-EP, 1 layer PCB Thermal Resistance, Junction-to-Air (Note 3) | 42 | °C/W |
| R _{θJA} | Thermal Characteristics, SSOP36-EP, 4 layers PCB Thermal Resistance, Junction-to-Air (Note 4) | 19.5 | °C/W |

3. Values based on PCB of 76.2 x 114.3 mm², 72 μm copper thickness, 20 % copper area coverage and FR4 PCB substrate.

4. Values based on PCB of 76.2 x 114.3 mm², 72 / 36 μm copper thickness (signal layers / internal planes), 20 / 90 % copper area coverage (signal layers / internal planes) and FR4 PCB substrate.

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ELECTRICAL CHARACTERISTICS

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------------|-----|-----|-----|------|
|--------|-----------|-----------------|-----|-----|-----|------|

SUPPLY

| | | | | | | |
|--------------------------|---|---|----------|-------------|------------|----|
| V _s | Supply voltage | Functional Parameter specification | 5.5 8 | | 28 18 | V |
| I _{s(standby)} | Supply Current (V _S), Standby mode | Standby mode, V _S = 16 V, 0 V ≤ V _{CC} ≤ 5.25 V, CSB = V _{CC} , OUTx/ECx = floating, SI = SCLK = 0 V, T _J < 85°C (T _J = 150°C) | | 3.5 (9) | 12 (25) | μA |
| I _{s(active)} | Supply current (V _S), Active mode | Active mode, V _S = 16 V, OUTx/ECx = floating | | 8 | 20 | mA |
| I _{CC(standby)} | Supply Current (V _{CC}), Standby mode | Standby mode, V _{CC} = 5.25 V, SI = SCLK = 0 V, T _J < 85°C (T _J = 150°C) | | 4.5 (15) | 6 (50) | μA |
| I _{CC(active)} | Supply current (V _{CC}), Active mode | Active mode, V _S = 16 V, OUTx/ECx = floating | | 6.5 | 8.4 | mA |
| I(standby) | Total Standby mode supply current (I _s + I _{CC}) | Standby mode, V _S = 16 V, T _J < 85°C, CSB = V _{CC} , OUTx/ECx = floating | | 8 | 18 | μA |

OVERVOLTAGE AND UNDERVOLTAGE DETECTION

| | | | | | | |
|--------------------------|---|--|-----|------|------|----|
| V _{uv_vs(on)} | V _S Undervoltage detection | V _S increasing | 5.6 | | 6.2 | V |
| V _{uv_vs(off)} | | V _S decreasing | 5.2 | | 5.8 | V |
| V _{uv_vs(hys)} | V _S Undervoltage hysteresis | V _{uv_vs(on)} - V _{uv_vs(off)} | | 0.65 | | V |
| V _{ov_vs(off)} | V _S Overvoltage detection | V _S increasing | 20 | | 24.5 | V |
| V _{ov_vs(on)} | | V _S decreasing | 18 | | 23.5 | V |
| V _{ov_vs(hys)} | V _S Overvoltage hysteresis | V _{ov_vs(off)} - V _{ov_vs(on)} | | 2 | | V |
| V _{uv_vcc(off)} | V _{CC} Undervoltage detection | V _{CC} increasing | | | 2.9 | V |
| V _{uv_vcc(on)} | | V _{CC} decreasing | 2 | | | V |
| V _{uv_vcc(hys)} | V _{CC} Undervoltage hysteresis | V _{uv_vcc(off)} - V _{uv_vcc(on)} | | 0.11 | | V |
| td _{uvov} | V _S Undervoltage / Overvoltage filter time | Time to set the power supply fail bit UOV_OC in the Global Status Byte | 6 | | 100 | μs |

CHARGE PUMP OUTPUT CHP

| | | | | | | |
|--------------------|---------------------------|---|----------------------|----------------------|---------------------|----|
| V _{chp8} | Chargepump Output Voltage | V _s = 8 V, I _{chp} = -60 μA | V _s + 6 | V _s + 9.5 | V _s + 13 | V |
| V _{chp10} | Chargepump Output Voltage | V _s = 10 V, I _{chp} = -80 μA | V _s + 8 | V _s + 11 | V _s + 13 | V |
| V _{chp12} | Chargepump Output Voltage | V _S > 12 V, I _{chp} = -100 μA | V _s + 9.5 | V _s + 11 | V _s + 13 | V |
| I _{chp} | Chargepump Output current | V _S = 13.5 V, V _{chp} = V _s + 10 V | -750 | | -95 | μA |

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|---|--|-----|-----|------------|------|
| MIRROR COMMON OUTPUT (X/Y, FOLD) OUT1 | | | | | | |
| Ron_out1 | On-resistance HS or LS | T _J = 25°C, I _{out1} = ±1.5 A | | 0.3 | | Ω |
| | | T _J = 125°C, I _{out1} = ±1.5 A | | | 0.6 | |
| loc1_hs | Overcurrent threshold HS | | -5 | | -3 | A |
| loc1_ls | Overcurrent threshold LS | | 3 | | 5 | A |
| Vlim1 | V _{ds} voltage limitation HS or LS | | 2 | | 3 | V |
| Iuld1_hs | Underload detection threshold HS | | -80 | | -5 | mA |
| Iuld1_ls | Underload detection threshold LS | | 10 | | 80 | mA |
| td_HS1(on) | Output delay time, HS Driver on | Time from CSB going high to V(OUT1) = 0.1·V _s / 0.9·V _s (on/off) | | 2.5 | 12 | μs |
| td_HS1(off) | Output delay time, HS Driver off | | | 3 | 12 | μs |
| td_LS1(on) | Output delay time, LS Driver on | Time from CSB going low to V(OUT1) = 0.9·V _s / 0.1·V _s (on/off) | | 1 | 12 | μs |
| td_LS1(off) | Output delay time, LS Driver off | | | 1.5 | 12 | μs |
| tdLH1 | Cross conduction protection time, low-to-high transition including LS slew-rate | | | 0.5 | 22 | μs |
| tdHL1 | Cross conduction protection time, high-to-low transition including HS slew-rate | | | 5.5 | 22 | μs |
| Ileak_act_hs1 | Output HS leakage current, Active mode | V(OUT1) = 0 V | -40 | -16 | | μA |
| Ileak_act_ls1 | Output pull-down current, Active mode | V(OUT1) = V _S | | 100 | 160 | μA |
| Ileak_stdby_hs1 | Output HS leakage current, Standby mode | V(OUT1) = 0 V | -5 | | | μA |
| Ileak_stdby_ls1 | Output pull-down current, Standby mode | V(OUT1) = V _S , T _J ≥ 25°C V(OUT1) = V _S , T _J < 25°C | | 80 | 120 175 | μA |
| td_uld1 | Underload blanking delay | | 430 | | 3000 | μs |
| td_old1 | Overload shutdown blanking delay | | 5 | | 25 | μs |
| frec1L | Recovery frequency, slow recovery mode | CONTROL_3.OCRF = 0 | 1 | | 4 | kHz |
| frec1H | Recovery frequency, fast recovery mode | CONTROL_3.OCRF = 1 | 2 | | 6 | kHz |
| dVout1 | Slew rate of HS driver | V _s = 13.5 V, R _{load} = 16 Ω to GND | 1 | 2 | 3 | V/μs |

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|---|--|-------|-----|------------|----------|
| MIRROR X/Y POSITIONING OUTPUTS OUT2, OUT3 | | | | | | |
| Ron_out2,3 | On-resistance HS or LS | T _J = 25°C, I _{out2,3} = ±0.5 A | | 1.6 | | Ω |
| | | T _J = 125°C, I _{out2,3} = ±0.5 A | | | 3 | Ω |
| Ioc2,3_hs | Overcurrent threshold HS | | -1.25 | | -0.75 | A |
| Ioc2,3_ls | Overcurrent threshold LS | | 0.75 | | 1.25 | A |
| Vlim2,3 | V _{ds} voltage limitation HS or LS | | 2 | | 3 | V |
| Iuld2,3_hs | Underload detection threshold HS | | -30 | -20 | -10 | mA |
| Iuld2,3_ls | Underload detection threshold LS | | 10 | 20 | 30 | mA |
| td_HS2,3(on) | Output delay time, HS Driver on | Time from CSB going high to V(OUT2,3) = 0.1·V _s / 0.9·V _s (on/off) | | 2.5 | 12 | μs |
| td_HS2,3(off) | Output delay time, HS Driver off | | | 3 | 12 | μs |
| td_LS2,3(on) | Output delay time, LS Driver on | Time from CSB going low to V(OUT2,3) = 0.9·V _s / 0.1·V _s (on/off) | | 1 | 12 | μs |
| td_LS2,3(off) | Output delay time, LS Driver off | | | 1 | 12 | μs |
| tdLH2,3 | Cross conduction protection time, low-to-high transition including LS slew-rate | | | 0.5 | 22 | μs |
| tdHL2,3 | Cross conduction protection time, high-to-low transition including HS slew-rate | | | 5.5 | 22 | μs |
| Ileak_act_hs2,3 | Output HS leakage current, Active mode | V(OUT2,3) = 0 V | -40 | -16 | | μA |
| Ileak_act_ls2,3 | Output pull-down current, Active mode | V(OUT2,3) = V _s | | 100 | 160 | μA |
| Ileak_stdby_hs2,3 | Output HS leakage current, Standby mode | V(OUT2,3) = 0 V | -5 | | | μA |
| Ileak_stdby_ls2,3 | Output pull-down current, Standby mode | V(OUT2,3) = V _s , T _J ≥ 25°C V(OUT2,3) = V _s , T _J < 25°C | | 80 | 120 175 | μA μA |
| td_uld2,3 | Underload blanking delay | | 430 | | 3000 | μs |
| td_old2,3 | Overload shutdown blanking delay | | 10 | | 100 | μs |
| frec2,3L | Recovery frequency, slow recovery mode | CONTROL_3.OCRf = 0 | 1 | | 4 | kHz |
| frec2,3H | Recovery frequency, fast recovery mode | CONTROL_3.OCRf = 1 | 2 | | 6 | kHz |
| dVout2,3 | Slew rate of HS driver | V _s = 13.5 V, R _{load} = 64 Ω to GND | 1 | 2 | 3 | V/μs |

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|-------------------------------------|---|--|------|------|------------|----------|
| DOOR LOCK OUTPUTS OUT4, OUT5 | | | | | | |
| Ron_out4,5 | On-resistance HS or LS | T _J = 25°C, I _{out4,5} = ±3 A | | 0.15 | | Ω |
| | | T _J = 125°C, I _{out4,5} = ±3 A | | | 0.3 | Ω |
| loc4,5_hs | Overcurrent threshold HS | T _J > 0°C | -10 | | -6 | A |
| loc4,5_hs_ct | Overcurrent threshold HS | T _J ≤ 0°C | -10 | | -5.75 | A |
| loc4,5_ls | Overcurrent threshold LS | | 6 | | 10 | A |
| Vlim4,5 | V _{ds} voltage limitation HS or LS | | 2 | | 3 | V |
| Iuld4,5_hs | Underload detection threshold HS | | -300 | | -60 | mA |
| Iuld4,5_ls | Underload detection threshold LS | | 60 | | 300 | mA |
| td_HS4,5 (on) | Output delay time, HS Driver on | Time from CSB going high to V(OUT4,5) = 0.1·V _s / 0.9·V _s (on/off) | | 2.5 | 12 | μs |
| td_HS4,5 (off) | Output delay time, HS Driver off | | | 3 | 12 | μs |
| td_LS4,5 (on) | Output delay time, LS Driver on | Time from CSB going low to V(OUT4,5) = 0.9·V _s / 0.1·V _s (on/off) | | 1 | 12 | μs |
| td_LS4,5 (off) | Output delay time, LS Driver off | | | 1.5 | 12 | μs |
| tdLH4,5 | Cross conduction protection time, low-to-high transition including LS slew-rate | | | 0.5 | 22 | μs |
| tdHL4,5 | Cross conduction protection time, high-to-low transition including HS slew-rate | | | 5.5 | 22 | μs |
| Ileak_act_hs4,5 | Output HS leakage current, Active mode | V(OUT4,5) = 0 V | -40 | -17 | | μA |
| Ileak_act_ls4,5 | Output pull-down current, Active mode | V(OUT4,5) = V _s | | 100 | 160 | μA |
| Ileak_stdby_hs4,5 | Output HS leakage current, Standby mode | V(OUT4,5) = 0 V | -5 | | | μA |
| Ileak_stdby_ls4,5 | Output pull-down current, Standby mode | V(OUT4,5) = V _s , T _J ≥ 25°C V(OUT4,5) = V _s , T _J < 25°C | | 80 | 120 175 | μA μA |
| td_uld4,5 | Underload blanking delay | | 430 | | 3000 | μs |
| td_ol4,5 | Overload shutdown blanking delay | | 10 | | 25 | μs |
| frec4,5L | Recovery frequency, slow recovery mode | CONTROL_3.OCRf = 0 | 1 | | 4 | kHz |
| frec4,5H | Recovery frequency, fast recovery mode | CONTROL_3.OCRf = 1 | 2 | | 6 | kHz |
| dVout4,5 | Slew rate of HS driver | V _s = 13.5 V, R _{load} = 4 Ω to GND | 1 | 2 | 3 | V/μs |

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|--|-----|-----|------------|----------|
| SAFE LOCK, MIRROR FOLD OUTPUT OUT6 | | | | | | |
| Ron_out6 | On-resistance HS or LS | T _J = 25°C, I _{out6} = ±1.5 A | | 0.3 | | Ω |
| | | T _J = 125°C, I _{out6} = ±1.5 A | | | 0.6 | |
| loc6_hs | Overcurrent threshold HS | | -5 | | -3 | A |
| loc6_ls | Overcurrent threshold LS | | 3 | | 5 | A |
| Vlim | V _{ds} voltage limitation HS or LS | | 2 | | 3 | V |
| I _{uld6_hs} | Underload detection threshold HS | | -80 | | -5 | mA |
| I _{uld6_ls} | Underload detection threshold LS | | 10 | | 80 | mA |
| td_HS6(on) | Output delay time, HS Driver on | Time from CSB going high to V(OUT6) = 0.1·V _s / 0.9·V _s (on/off) | | 2.5 | 12 | μs |
| td_HS6(off) | Output delay time, HS Driver off | | | 3 | 12 | μs |
| td_LS6(on) | Output delay time, LS Driver on | Time from CSB going low to V(OUT6) = 0.9·V _s / 0.1·V _s (on/off) | | 1 | 12 | μs |
| td_LS6(off) | Output delay time, LS Driver off | | | 1.5 | 12 | μs |
| tdLH6 | Cross conduction protection time, low-to-high transition including LS slew-rate | | | 0.5 | 22 | μs |
| tdHL6 | Cross conduction protection time, high-to-low transition including HS slew-rate | | | 5.5 | 22 | μs |
| I _{leak_act_hs6} | Output HS leakage current, Active mode | V(OUT6) = 0 V | -40 | -16 | | μA |
| I _{leak_act_ls6} | Output pull-down current, Active mode | V(OUT6) = V _s | | 100 | 160 | μA |
| I _{leak_stdby_hs6} | Output pull-down current, Standby mode | V(OUT6) = 0 V | -5 | | | μA |
| I _{leak_stdby_ls6} | Output LS leakage current, Standby mode | V(OUT6) = V _s , T _J ≥ 25°C V(OUT6) = V _s , T _J < 25°C | | 80 | 120 175 | μA μA |
| td_uld6 | Underload blanking delay | | 430 | | 3000 | μs |
| td_old6 | Overload shutdown blanking delay | | 5 | | 25 | μs |
| frec6L | Recovery frequency, slow recovery mode | CONTROL_3.OCRF = 0 | 1 | | 4 | kHz |
| frec6H | Recovery frequency, fast recovery mode | CONTROL_3.OCRF = 1 | 2 | | 6 | kHz |
| dVout6 | Slew rate of HS driver | V _s = 13.5 V, R _{load} = 16 Ω to GND | 1 | 2 | 3 | V/μs |

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|--|--|------|-----|------|------|
| BULB / LED DRIVER OUTPUTS OUT7, OUT8 | | | | | | |
| Ron_out7,8_ICB | On-resistance to supply, HS switch, Bulb mode | T _J = 25°C, I _{out7,8} = -1 A | | 0.3 | | Ω |
| | | T _J = 125°C, I _{out7,8} = -1 A | | | 0.6 | |
| Ron_out7,8_LED | On-resistance to supply, HS switch, LED mode | T _J = 25°C, I _{out7,8} = -0.2 A | | 1.4 | | Ω |
| | | T _J = 125°C, I _{out7,8} = -0.2 A | | | 3 | |
| Ilim7,8_ICB | Output current limitation to GND, Bulb mode | | -3.7 | | -2.5 | A |
| Ilim7,8_LED | Overcurrent threshold, LED mode | | -1.1 | | -0.5 | A |
| Iuld7,8_ICB | Underload detection threshold, Bulb mode | | -60 | | -5 | mA |
| Iuld7,8_LED | Underload detection threshold, LED mode | | -15 | | -5 | mA |
| td_OUT7,8_ICB(on) | Output delay time, Driver on, Bulb mode | Time from CSB going high to V(OUT7,8) = 0.1·Vs / 0.9·Vs (on/off); Rload = 16 Ω | | 15 | 48 | μs |
| td_OUT7,8_ICB(off) | Output delay time, Driver off, Bulb mode | | | 21 | 48 | |
| td_OUT7,8_LED(on) | Output delay time, Driver on, LED mode | Time from CSB going high to V(OUT7,8) = 0.1·Vs / 0.9·Vs (on/off); Rload = 64 Ω | | 15 | 48 | μs |
| td_OUT7,8_LED(off) | Output delay time, Driver off, LED mode | | | 21 | 48 | |
| Ileak_act7,8 | Output leakage current, Active mode | V(OUT7,8) = 0 V | -15 | | | μA |
| Ileak_stdby7,8 | Output leakage current, Standby mode | V(OUT7,8) = 0 V | -5 | | | μA |
| Ileak_out_vs7,8 | Output pull-down current | V(OUT7,8) = VS | | | 1 | mA |
| td_uld7,8 | Underload blanking delay | | 430 | | 3000 | μs |
| td_old_ICB7,8 | Overload shutdown blanking delay, Bulb mode | | 100 | | 160 | μs |
| td_old_LED7,8 | Overload shutdown blanking delay, LED mode only | | 10 | | 100 | μs |
| frec7,8L | Recovery frequency, slow recovery mode recovery | CONTROL_3.OCRFB = 0 | 1 | | 2.1 | kHz |
| frec7,8H | Recovery frequency, fast recovery mode (LED mode only) | CONTROL_3.OCRFB = 1 | 2 | | 6 | kHz |
| dVout7,8_ICB | Slew rate, Bulb mode | Vs = 13.5 V, Rload = 16 Ω | | 0.2 | | V/μs |
| dVout7,8_LED | Slew rate, LED mode | Vs = 13.5 V, Rload = 64 Ω | | 0.2 | | V/μs |
| dVout7,8_ocr | Slew rate in overcurrent recovery mode | Vs = 13.5 V, Rload = 5 Ω | 1 | 2 | 3 | V/μs |

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------------|-----|-----|-----|------|
|--------|-----------|-----------------|-----|-----|-----|------|

LED DRIVER OUTPUTS OUT9, OUT10

| | | | | | | |
|------------------|--|---|-------|-----|-------|------|
| Ron_out9,10 | On-resistance to supply, HS switch | T _J = 25°C, I _{out9,10} = -0.2 A | | 1.4 | | Ω |
| | | T _J = 125°C, I _{out9,10} = -0.2 A | | | 3 | Ω |
| Ioc9,10 | Overcurrent threshold | | -0.63 | | -0.38 | A |
| Iuld9,10 | Underload detection threshold | | -16 | | -4 | mA |
| td_OUT(on)9,10 | Output delay time, Driver on | Time from CSB going high to V(OUT9,10) = 0.1·Vs / 0.9·Vs (on/off) | | 18 | 48 | μs |
| td_OUT(off)9,10 | Output delay time, Driver off | | | 23 | 48 | |
| Ileak_act9,10 | Output leakage current, Active mode | V(OUT9,10) = 0 V | -10 | | | μA |
| Ileak_stdb9,10 | Output leakage current, Standby mode | V(OUT9,10) = 0 V | -5 | | | μA |
| Ileak_out_vs9,10 | Output pull-down current | V(OUT9,10) = VS | | | 1 | mA |
| td_uld9,10 | Underload blanking delay | | 250 | | 750 | μs |
| td_old_OUT9,10 | Overload shutdown blanking delay | | 10 | | 100 | μs |
| frec9,10L | Recovery frequency, slow recovery mode | CONTROL_3.OCRFB = 0 | 1 | | 4 | kHz |
| frec9,10H | Recovery frequency, fast recovery mode | CONTROL_3.OCRFB = 1 | 2 | | 6 | kHz |
| dVout9,10 | Slew rate | Vs = 13.5 V, Rload = 64 Ω | | 0.2 | | V/μs |

HEATER OUTPUT OUT11

| | | | | | | |
|----------------|--|---|------|-----|------|------|
| Ron_out11 | On-resistance to supply, HS switch | T _J = 25°C, I _{out11} = -3 A | | 0.1 | | Ω |
| | | T _J = 125°C, I _{out11} = -3 A | | | 0.2 | Ω |
| Ioc11 | Overcurrent threshold | | -10 | | -5.5 | A |
| Iuld11 | Underload detection threshold | | -300 | | -30 | mA |
| td_OUT11(on) | Output delay time, Driver on | Time from CSB going high to V(OUT11) = 0.1·Vs / 0.9·Vs (on/off) | | 3 | 12 | μs |
| td_OUT11(off) | Output delay time, Driver off | | | 3 | 12 | |
| Ileak_act11 | Output leakage current, Active mode | V(OUT11) = 0 V | -10 | | | μA |
| Ileak_stdb11 | Output leakage current, Standby mode | V(OUT11) = 0 V | -5 | | | μA |
| Ileak_out11_vs | Output pull-down current | V(OUT11) = VS | | | 1 | mA |
| td_uld11 | Underload blanking delay | | 430 | | 3000 | μs |
| td_old_OUT11 | Overload shutdown blanking delay | | 5 | | 25 | μs |
| frec11L | Recovery frequency, slow recovery mode | CONTROL_3.OCRFB = 0 | 1 | | 4 | kHz |
| frec11H | Recovery frequency, fast recovery mode | CONTROL_3.OCRFB = 1 | 2 | | 6 | kHz |
| dVout11 | Slew rate | Vs = 13.5 V, Rload = 4 Ω | 1 | 2 | 3 | V/μs |

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---------------|------|---------------|------|
| ELECTROCHROMIC MIRROR CONTROL (ECFB, ECON) | | | | | | |
| Ron_ecfb | On-resistance to GND, LS switch | T _J = 25°C, Iecfb = 0.5 A | | 1.6 | | Ω |
| | | T _J = 125°C, Iecfb = 0.5 A | | | 3 | Ω |
| Ilim_ecfb_src | Output current limitation to GND | V _s = 13.5V, V _{CC} = 5 V | 0.75 | | 1.25 | A |
| Vlim_ecfb | V _{ds} voltage limitation | Output enabled | 2 | | 3 | V |
| Iuld_ecfb | Underload detection threshold | V _s = 13.5 V, V _{CC} = 5 V | 10 | 20 | 30 | mA |
| td_ecfb(on) | Output delay time, LS Driver on | V _s = 13.5 V, V _{CC} = 5 V, Rload = 64 Ω, V(ECFB) = 0.9·V _S / 0.1·V _S (on /off) | | 1 | 12 | μs |
| td_ecfb(off) | Output delay time, LS Driver off | | | 2 | 12 | |
| Ileak_ecfb_stdby | Output leakage current, LS off | Vecfb = V _s , Standby mode | -15 | | 15 | μA |
| Ileak_ecfb_act | | Vecfb = V _s , Active mode | -10 | | 10 | μA |
| td_uld_ecfb | Underload blanking delay | | 430 | | 3000 | μs |
| td_ol_d_ecfb | Overload shutdown blanking delay | | 10 | | 100 | μs |
| dVecfb/dt(on/off) | Slew rate of ECFB, LS switch | V _s = 13.5 V, V _{CC} = 5 V, Rload = 64 Ω | | 15 | | V/μs |
| Vctrl_max | Maximum EC control voltage | CONTROL_2.FSR = 1 | 1.4 | | 1.6 | V |
| | | CONTROL_2.FSR = 0 | 1.12 | | 1.28 | V |
| DNL | Differential non linearity | 1 LSB = 23.8 mV | -1 | | 1 | LSB |
| dV_ecfb | Voltage deviation between target and ECFB | dV_ecfb = Vtarget - Vecfb, Iecon < 1 μA gain offset | -5% -1 LSB | | +5% +1 LSB | mV |
| dV_ecfb_lo | Difference voltage between target and ECFB sets flag if Vecfb is below target | dV_ecfb = Vtarget - Vecfb, Toggle bit STATUS_2.ECLO = 1 | | 120 | | mV |
| dV_ecfb_hi | Difference voltage between target and ECFB sets flag if Vecfb is above target | dV_ecfb = Vtarget - Vecfb, Toggle bit STATUS_2.ECHI = 1 | | -120 | | mV |
| Vecon_min_hi | ECON output voltage range | Iecon = -10 μA | 4.5 | | 5.5 | V |
| Vecon_max_lo | | Iecon = 10 μA | 0 | | 0.7 | |
| Iecon | ECON output current capability | Vtarget > Vecfb + 500 mV, Vecfb = 3.5 V | -100 | | -10 | μA |
| | | Vtarget < Vecfb - 500 mV, Vecon = 1 V, Vtarget = 1 LSB, Vecfb = 0.5 V | 10 | | 100 | μA |
| Recon_pd | Pull-down resistance at ECON in fast discharge mode | Vecon = 0.7 V, CONTROL_1.ECEN = 1, CONTROL_1.LSECFB = 1, CONTROL_1.DAC[5:0] = 0 | | | 5 | kΩ |
| Iq_econ | ECON quiescent current | Vecon = V _s , CONTROL_1.ECEN = 0 | | | 1 | μA |
| t_disc | Auto-discharge pulse width | Config.LSPWM=1 | 240 | 300 | 360 | ms |
| t_rec | Auto-discharge blanking time | Config.LSPWM=1 | 2.25 | 3 | 3.75 | ms |
| Vthdisc_abs | PWM discharge threshold level V(ECON) (Note 5) | Config.LSPWM=1 | 350 | 400 | 450 | mV |
| Vthdisc_diff | PWM discharge threshold level V(ECON) - V(ECFB) (Note 5) | Config.LSPWM=1 | -50 | 0 | 50 | mV |

5. If V(ECON) < Vthdisc_abs or V(ECON)-V(ECFB) < Vthdisc_diff then ECON_LOW =1; see description in paragraph Controller for Electro-chromic Glass

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|--|--|--|-------|---|------|
| CURRENT SENSE MONITOR OUTPUT ISOUT/PWM2 | | | | | | |
| Vis | Current Sense output functional voltage range | V _{CC} = 5 V, V _s = 8–20 V | 0 | | V _{CC} - 1 | V |
| Kis (Note 6) | Current Sense output ratio OUT1/6 and 7/8 (low on-resistance bulb mode) | K = I _{out} / I _{is} , 0 V ≤ Vis ≤ 4 V, V _{CC} = 5 V | | 10000 | | |
| | Current Sense output ratio OUT4/5 | | | 9200 | | |
| | Current Sense output ratio OUT9/10 and 7/8 (high on-resistance LED mode) | | | 2000 | | |
| | Current Sense output ratio OUT11 | | 4500 | | 18000 | |
| Iis,acc (Notes 7 and 8) | Current Sense output accuracy OUT1/6 | 0 V ≤ Vis ≤ 4 V, V _{CC} = 5 V I _{out1/6} = 1–1.6 A, T _J ≥ 25°C I _{out1/6} = 1–1.6 A, T _J < 25°C I _{out1/6} = 0.5–1 A; 1.6–2.9 A | -10% - 2% FS -10% - 2% FS -22% - 2% FS | | 10% + 2% FS 15% + 2% FS 22% + 2% FS | |
| | Current Sense output accuracy OUT4/5 | 0 V ≤ Vis ≤ 4 V, V _{CC} = 5 V, I _{out4/5} = 2.6–3.3 A, T _J ≥ 25°C I _{out4/5} = 2.6–3.3 A, T _J < 25°C I _{out4/5} = 0.5–2.6 A; 3.3–5.9 A | -10% - 2% FS -10% - 2% FS -22% - 3% FS | | 10% + 2% FS 19% + 2% FS 22% + 3% FS | |
| | Current Sense output accuracy OUT7/8 (low on-resistance bulb mode) | 0 V ≤ Vis ≤ 4 V, V _{CC} = 5 V I _{out7/8} = 0.6–0.7 A, T _J ≥ 25°C I _{out7/8} = 0.6–0.7 A, T _J < 25°C I _{out7/8} = 0.5–0.6 A; 0.7–1.3 A | -10% - 2% FS -10% - 2% FS -20% - 2% FS | | 10% + 2% FS 18% + 2% FS 20% + 2% FS | |
| | Current Sense output accuracy OUT7/8 (high on-resistance LED mode) | 0 V ≤ Vis ≤ 4 V, V _{CC} = 5 V I _{out7/8} = 0.14–0.16 A, T _J ≥ 25°C I _{out7/8} = 0.14–0.16 A, T _J < 25°C I _{out7/8} = 0.1–0.14 A; 0.16–0.3 A | -12% - 2% FS -12% - 2% FS -18% - 2% FS | | 12% + 2% FS 15% + 2% FS 18% + 2% FS | |
| | Current Sense output accuracy OUT9/10 | 0 V ≤ Vis ≤ 4 V, V _{CC} = 5 V I _{out9/10} = 0.15–0.25 A I _{out9/10} = 0.1–0.15 A; 0.25–0.4 A | -12% - 2% FS -18% - 2% FS | | 12% + 2% FS 18% + 2% FS | |
| tis | Current Sense settling time | 0 V to FSR (full scale range) | | 256 | | μs |

6. Kis trimmed at 150°C to higher value of spec range to be more centered over temp range.

7. Current sense output accuracy = I_{sout} - I_{sout_ideal} relative to I_{sout_ideal}

8. FS (Full scale) = I_{outmax}/Kis

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|-------------------------|---|---------------------|-----|---------------------|------|
| DIGITAL INPUTS CSB, SCLK, PWM1/2, SI | | | | | | |
| V _{inl} | Input low level | V _{CC} = 5 V | | | 0.3·V _{CC} | V |
| V _{inh} | Input high level | | 0.7·V _{CC} | | | V |
| V _{in_hyst} | Input hysteresis | | 500 | | | mV |
| R _{csb_pu} | CSB pull-up resistor | V _{CC} = 5 V _{CC} 0 V < V _{csb} < 0.7·V _{CC} | 30 | 120 | 250 | kΩ |
| R _{sclk_pd} | SCLK pull-down resistor | V _{CC} = 5 V, V _{sclk} = 1.5 V | 30 | 60 | 220 | kΩ |
| R _{si_pd} | SI pull-down resistor | V _{CC} = 5 V, V _{si} = 1.5 V | 30 | 60 | 220 | kΩ |
| R _{pwm1_pd} | PWM1 pull-down resistor | V _{CC} = 5 V, V _{pwm1} = 1.5 V | 30 | 60 | 220 | kΩ |
| R _{pwm2_pd} | PWM2 pull-down resistor | V _{CC} = 5 V, V _{pwm2} = 1.5 V, current sense disabled | 30 | 60 | 220 | kΩ |
| I _{leak_isout} | Output leakage current | current sense enabled | -1 | | 1 | μA |
| C _{csb / sclk / pwm1/2} | Pin capacitance | 0 V < V _{CC} < 5.25 V (Note 9) | | | 10 | pF |

DIGITAL INPUTS CSB, SCLK, SI; TIMING

| | | | | | | |
|---------------------------|---|---|-----|------|-----|----|
| t _{sclk} | Clock period | V _{CC} = 5 V | | 1000 | | ns |
| t _{sclk_h} | Clock high time | | 115 | | | ns |
| t _{sclk_l} | Clock low time | | 115 | | | ns |
| t _{set_csb} | CSB setup time, CSB low before rising edge of SCLK | | 400 | | | ns |
| t _{set_sclk} | SCLK setup time, SCLK low before rising edge of CSB | | 400 | | | ns |
| t _{set_si} | SI setup time | | 200 | | | ns |
| t _{hold_si} | SI hold time | | 200 | | | ns |
| t _{r_in} | Rise time of input signal SI, SCLK, CSB | | | | 100 | ns |
| t _{f_in} | Fall time of input signal SI, SCLK, CSB | | | | 100 | ns |
| t _{csb_hi_stdby} | Minimum CSB high time, switching from Standby mode | Transfer of SPI-command to input register, valid before t _{sact} mode transition delay expires | | 5 | 10 | μs |
| t _{csb_hi_min} | Minimum CSB high time, Active mode | | | 2 | 4 | μs |

9. Values based on design and/or characterization.

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|----------------------|----------------------------|---|---------------------|-----|---------------------|------|
| V _{sol} | Output low level | I _{so} = 5 mA | | | 0.2·V _{CC} | V |
| V _{soh} | Output high level | I _{so} = -5 mA | 0.8·V _{CC} | | | V |
| I _{leak_so} | Tristate leakage current | V _{csb} = V _{CC} , 0 V < V _{so} < V _{CC} | -10 | | 10 | μA |
| C _{so} | Tristate input capacitance | V _{csb} = V _{CC} , 0 V < V _{CC} < 5.25 V (Note 9) | | | 10 | pF |

DIGITAL OUTPUT SO; TIMING

| | | | | | | |
|--------------------------|---|--|--|-----|-----|----|
| t _{r_so} | SO rise time | C _{so} = 100 pF | | 80 | 140 | ns |
| t _{f_so} | SO fall time | C _{so} = 100 pF | | 50 | 100 | ns |
| t _{en_so_tril} | SO enable time from tristate to low level | C _{so} = 100 pF, I _{load} = 1 mA, pull-up load to V _{CC} | | 100 | 250 | ns |
| t _{dis_so_ltri} | SO disable time from low level to tristate | C _{so} = 100 pF, I _{load} = 4 mA, pull-up load to V _{CC} | | 380 | 450 | ns |
| t _{en_so_trih} | SO enable time from tristate to high level | C _{so} = 100 pF, I _{load} = -1 mA, pull-down load to GND | | 100 | 250 | ns |
| t _{dis_so_htri} | SO disable time from high level to tristate | C _{so} = 100 pF, I _{load} = -4 mA, pull-down load to GND | | 380 | 450 | ns |
| t _{d_so} | SO delay time | V _{so} < 0.3·V _{CC} , or V _{so} > 0.7·V _{CC} , C _{so} = 100 pF | | 50 | 250 | ns |

9. Values based on design and/or characterization.

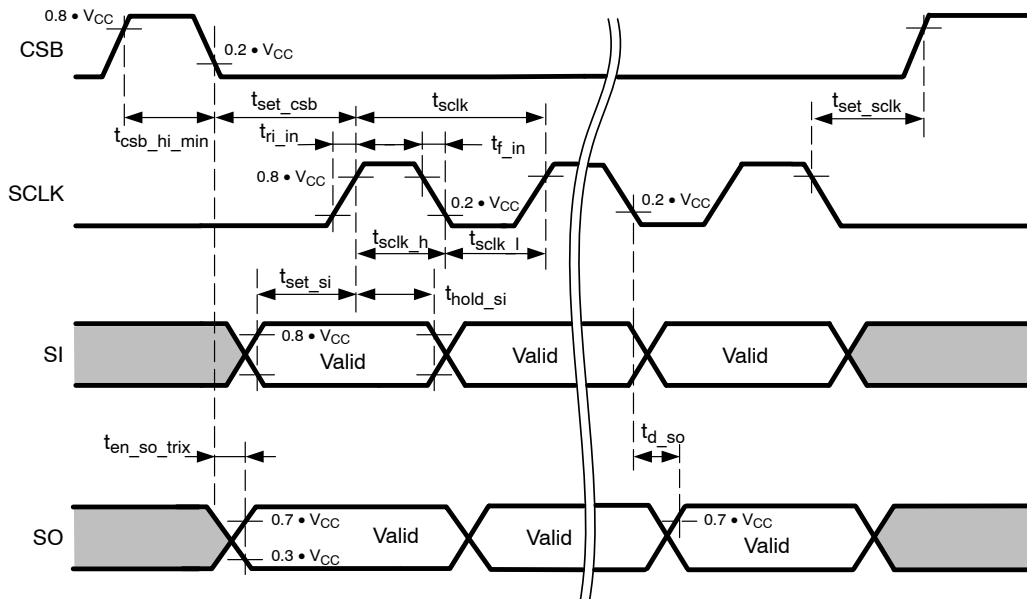


Figure 4. SPI Signals Timing Parameters

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ELECTRICAL CHARACTERISTICS (continued)

4.5 V < V_{CC} < 5.25 V, 8 V < V_s < 18 V, -40°C < T_J < 150°C; unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------|-----------|-----------------|-----|-----|-----|------|
|--------|-----------|-----------------|-----|-----|-----|------|

THEMAL PROTECTION

| | | | | | | |
|--------------|---|-----------------------------|-----|----|-----|----|
| Tjtw_on | Temperature warning threshold | Junction temperature | 140 | | 160 | °C |
| Tjtw_hys | Thermal warning hysteresis | | | 5 | | °C |
| Tjtd_on | Thermal shutdown threshold, T _J increasing | Junction temperature | 160 | | 180 | °C |
| Tjtd_off | Thermal shutdown threshold, T _J decreasing | Junction temperature | 160 | | | °C |
| Tjtd_hys | Thermal shutdown hysteresis | | | 5 | | °C |
| Tjtdtw_delta | Temperature difference between warning and shutdown threshold | | | 20 | | °C |
| td_tx | Filter time for thermal warning and shutdown | TW / TSD Global Status bits | 10 | | 100 | μs |

OPERATING MODES TIMING

| | | | | | | |
|-------|---|--|--|-----|-----|----|
| tact | Time delay for mode change from Unpowered mode into Standby mode | SPI communication ready after V _{CC} reached V _{uv_VCC(off)} threshold | | | 30 | μs |
| tsact | Time delay for mode change from Standby mode into Active mode | Time until output drivers are enabled after CSB going to high and CONTROL_0.MODE = 1 | | 170 | 300 | μs |
| tacts | Time delay for mode change from Active mode into Standby mode via SPI | Time until output drivers are disabled after CSB going to high and CONTROL_0.MODE = 0 | | | 300 | μs |

INTERNAL PWM CONTROL UNIT (OUT7 – OUT10)

| | | | | | | |
|-------|-------------------------------|------------------------------------|-----|-----|-----|----|
| PWMlo | PWM frequency, low selection | CONTROL_2.PWMI = 1, PWMx.FSELx = 0 | 135 | 170 | 190 | Hz |
| PWMhi | PWM frequency, high selection | CONTROL_2.PWMI = 1, PWMx.FSELx = 1 | 175 | 225 | 250 | Hz |

DETAILED OPERATING AND PIN DESCRIPTION

General

The NCV7707 provides six half-bridge drivers, five independent high-side outputs and a programmable PWM control unit for free configuration. Strict adherence to integrated circuit die temperature is necessary, with a static maximum die temperature of 150°C. This may limit the number of drivers enabled at one time. Output drive control and fault reporting are handled via the SPI (Serial Peripheral Interface) port. A SPI-controlled mode control provides a low quiescent sleep current mode when the device is not being utilized. A pull down is provided on the SI and SCLK inputs to ensure they default to a low state in the event of a severed input signal. A pull-up is provided on the CSB input disabling SPI communication in the event of an open CSB input.

Supply Concept

Power Supply Scheme – VS and VCC

The Vs power supply voltage is used to supply the half bridges and the high-side drivers. An all-internal chargepump is implemented to provide the gate-drive voltage for the n-channel type high-side transistors. The VCC voltage is used to supply the logic section of the IC, including the SPI interface.

Due to the independent logic supply voltage the control and status information will not be lost in case of a loss of Vs supply voltage. The device is designed to operate inside the specified parametric limits if the VCC supply voltage is within the specified voltage range (4.5 V to 5.25 V). Between the operational level and the VCC undervoltage threshold level (Vuv_VCC) it is guaranteed that the device remains in a safe functional state without any inadvertent change to logic information.

Device / Module Ground Concept

The high-side output stages OUT7–11 are designed to handle DC output voltage conditions down to –0.3 V and allow for short negative transient currents due to parasitic line inductances. Therefore the application has to take care that these ratings are not violated under abnormal operating conditions (module loss of GND, ground shift if load connected to external GND) by either implementing external bypass diodes connected to GND or a direct connection between load-GND and module-GND. Since these output stages are designed to drive resistive loads, restrictions on maximum inductance / clamping energy apply.

The heat slug is not hard-connected to internal GND rail. It has to be connected externally.

Power Up/Down Control

In order to prevent uncontrolled operation of the device during power/up down, an undervoltage lockout feature is implemented. Both supply voltages (VCC and Vs) are

monitored for undervoltage conditions supporting a safe power-up transition. When Vs drops below the undervoltage threshold Vuv_vs(off) (Vs undervoltage threshold) all output stages are switched to high-impedance state and the global status bit UOV_OC is set. This bit is a multi information bit in the Global Status Byte which is set in case of overcurrent, Vs over- and undervoltage. In case of undervoltage the status bit STATUS_2.VSUV is set, too.

Bit CONTROL_3.OVUVR (Vs under-/overvoltage recovery behavior) can be used to select the desired recovery behavior after a Vs under-voltage event. In case of OVUVR = 0, all output stages return to their programmed state as soon as Vs recovers back to its normal operating range. If OVUVR is set, the automatic recovery function is disabled thus the output stages will remain in high-impedance condition until the status bits have been cleared by the microcontroller. To avoid high current oscillations in case of output short to GND and low Vs voltage conditions, it is recommended to disable the Vs-auto-recovery by setting OVUVR = 1.

Chargepump

In Standby mode, the chargepump is disabled. After enabling the device by setting bit CONTROL_0.MODE to active (1), the internal oscillator is started and the voltage at the CHP output pin begins to increase. The output drivers are enabled after a delay of tsact once MODE was set to active.

Driver Outputs

Output PWM Control

For all half-bridge outputs as well as the high-side outputs the device features the possibility to logically combine the SPI-setting with a PWM signal that can be provided to the inputs PWM1 and ISOUT/PWM2, respectively. Each of the outputs has a fixed PWM signal assigned which is shown in Table 1. The PWM modulation is enabled by the respective bits in the control registers (CONTROL_2.OUTx_PWMx and CONTROL_3.OUTx_PWMx). In case of using pin ISOUT/PWM2, the application design has to take care of either disabling the current sense feature or to provide sufficient overdrive capability to maintain proper logic input levels for the PWM input.

In addition to the external signal control, all lighting outputs (OUT7–10) can also be PWM controlled via an internal PWM generator unit. While the PWM frequency can be individually selected between 170 Hz and 225 Hz thru bits PWMx.FSELx, the duty cycle can be programmed with 7-bits resolution PWMx.PW[6:0]. The selection between the different signal sources for these outputs is performed by programming bit CONTROL_2.PWMI. Default value is 0 (external signal source). The general principle of the PWM generation control scheme is shown in Figure 5.

Table 1. PWM CONTROL SCHEME

| Output | PWM Control Input | |
|--------|--------------------|--------------------|
| | CONTROL_2.PWMI = 0 | CONTROL_2.PWMI = 1 |
| OUT1 | PWM1 | PWM1 |
| OUT2 | PWM1 | PWM1 |
| OUT3 | PWM1 | PWM1 |
| OUT4 | PWM1 | PWM1 |
| OUT5 | ISOUT/PWM2 | ISOUT/PWM2 |
| OUT6 | PWM1 | PWM1 |
| OUT7 | PWM1 | PWM_7/8.PW7[6:0] |
| OUT8 | ISOUT/PWM2 | PWM_7/8.PW8[6:0] |
| OUT9 | PWM1 | PWM_9/10.PW9[6:0] |
| OUT10 | ISOUT/PWM2 | PWM_9/10.PW10[6:0] |
| OUT11 | PWM1 | PWM1 |

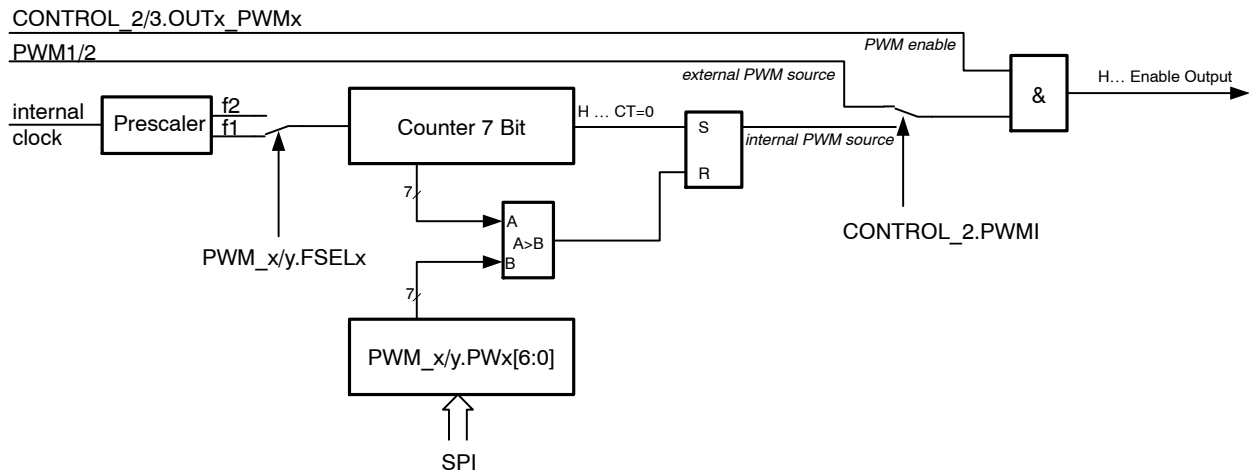


Figure 5. PWM Generation Diagram

Programmable Soft-start Function to Drive Loads with Inrush Current Behavior

Loads with startup currents higher than the overcurrent limits (e.g. inrush current of bulbs, block current of motors and cold resistance of heaters) can be driven using the programmable soft-start function (Overcurrent auto-recovery mode). Each output driver provides a corresponding overcurrent recovery bit (CONTROL_2/3.OCRx) to control the output behavior in case of a detected overcurrent event. If auto-recovery is enabled, the device automatically re-enables the output after a programmable recovery time. For all half-bridge outputs as well as the high-side outputs OUT9-11 and OUT7/8 in LED mode, the recovery frequency can be selected via SPI. OUT7/8 in bulb mode provides a fixed recovery frequency. The PWM modulated current will provide sufficient average current to power up the load (e.g. heat up the bulb) until the load reaches a steady state condition. The device itself cannot distinguish between a real overload and a non linear load like a bulb. Therefore a

real overload condition can only be qualified by time. It is recommended to only enable auto-recovery for a minimum amount of time to drive the connected load into a steady state condition. After turning off the auto-recovery function, the respective channel is automatically disabled if the overload condition still persists.

Inductive Loads

Each half bridge (OUT1-6) is built by internally connected low-side and high-side N-MOS transistors. Due to the built-in body diodes of the output transistors, inductive loads can be driven at the outputs without external free-wheeling diodes. The high-side drivers OUT7 to OUT11 are designed to drive resistive loads. Therefore only a limited clamping energy ($W < 1 \text{ mJ}$) can be dissipated by the device. For inductive loads ($L > 100 \mu\text{H}$) an external freewheeling diode connected between GND and the corresponding output is required.

The low-side driver at ECFB does not feature any freewheeling diode or clamping structure to handle inductive loads.

Current Sensing

Current Sense Output / PWM2 Input (Bidirectional Pin ISOUT/PWM2)

The current sense output allows a more precise analysis of the actual state of the load rather than the basic detection of an under- or overload condition. The sense output provides an image of the actual load current at the selected high side driver transistor. The current monitor function is available for all high current half-bridge outputs (OUT1, OUT4, OUT5 and OUT6), the high current high-side output (OUT11) as well as for the all bulb and LED outputs (OUT7-10).

The current sense ratio is fixed for the low resistance outputs OUT1/6/11 and OUT7/8 (bulb mode) to 1/10000, for door lock outputs OUT4/5 to 1/9200 and for the high ohmic outputs OUT9/10 and OUT7/8 (LED mode) to 1/2000. To prevent from false readouts, the signal at pin ISOUT is blanked after switching on the driver until correct settlement of the circuitry ($> 64 \mu\text{s}$). Bits CONTROL_3.IS[3:0] are used to select the output to be multiplexed to the current sense output.

The NCV7707 provides a sample-and-hold functionality for the current sense output to enable precise and simple load current diagnostics even during PWM operation of the respective output. While in active high-side output state, the current provided at ISOUT reflects a (low-pass-filtered) image of the actual output current, the IS-output current is sampled and held constant as soon as the HS output transistor is commanded off via PWM (low-side or high-impedant on half-bridge outputs, high-impedant on HS-outputs). In case no previous current information is available in the Sample-and-hold stage (current sense channel changed while actual channel is commanded off) the sample stage is reset so that it reflects zero output current.

Electro Chromic Mirror

Controller for Electro-chromic Glass

The voltage of the electro-chromic element connected at pin ECFB can be controlled to a target value which is set by Control Register 1 (bits CONTROL_1.DAC[5:0]). Setting bit CONTROL_1.ECEN enables this function. At the same time OUT10 is enabled, regardless of its own control bit CONTROL_1.HS10 and the respective PWM setting. An on-chip differential amplifier is used to control an external logic-level N-MOS pass device that delivers the power to

the electro-chromic element. The target voltage at ECFB is binary coded with a selectable full scale range (bit CONTROL_2.FSR). The default clamping value for the output voltage (CONTROL_2.FSR = 0) is 1.2 V, by setting CONTROL_2.FSR to "1", the maximum output voltage is 1.5 V. The resolution of the DAC output voltage is independent of the full-scale-range selection.

The charging of the mirror (positive slope) is determined by the positive slew rate of the transconductance amplifier and the compensation capacitor, while in case of capacitive loads, the negative slope is mainly determined by the current consumption thru the load and its capacitance. To allow fast settling time changing from higher to lower output voltage values, the device provides two modes of operation:

1. Fast discharge: When the target output voltage is set to 0 V and bit CONTROL_1.LS_ECFB is set, the voltage at pin ECFB is pulled to ground by a 1.6Ω low-side switch.
2. PWM discharge: In case of PWM discharge being activated (CONFIG.ECM_LSPWM = 1 and CONTROL_1.LS_ECFB = 1) (Figure 6):
 - a. The circuit regulation starts in normal regulation. The DAC value is turned to new lower value.
 - b. If the loop is detected out of regulation for a time longer than t_{rec} ($\sim 3 \text{ ms}$), the ECON voltage is detected low (internal signal ECON_LOW = 1), the regulator is switched off (DAC voltage at 0) and the fast discharge transistor is activated for $\sim 300 \text{ ms}$ (t_{disc}). During this fast discharge, the ECON output is pulled low to prevent from shoot-thru currents.
 - c. At the end of the discharge pulse t_{disc} the fast discharge is switched off and the regulation loop is activated again (with DAC to the correct wanted value), so the loop goes back to step b.) and the ECON_LOW comparator is observed again. Before starting a discharge pulse, the ECLO and ECHI comparator data is latched.

The feedback loop out of regulation is monitored by comparing $V(\text{ECON})$ versus $V(\text{ECFB})$ and versus 400 mV. If the regulation is activated and ECON is below ECFB, or below 400 mV, then the loop is detected as out of regulation and internal signal ECON_LOW is made 1. By activating the PWM discharge feature, the overcurrent recovery function is automatically disabled, regardless of the setting in CONTROL_2.OCR_ECFB.

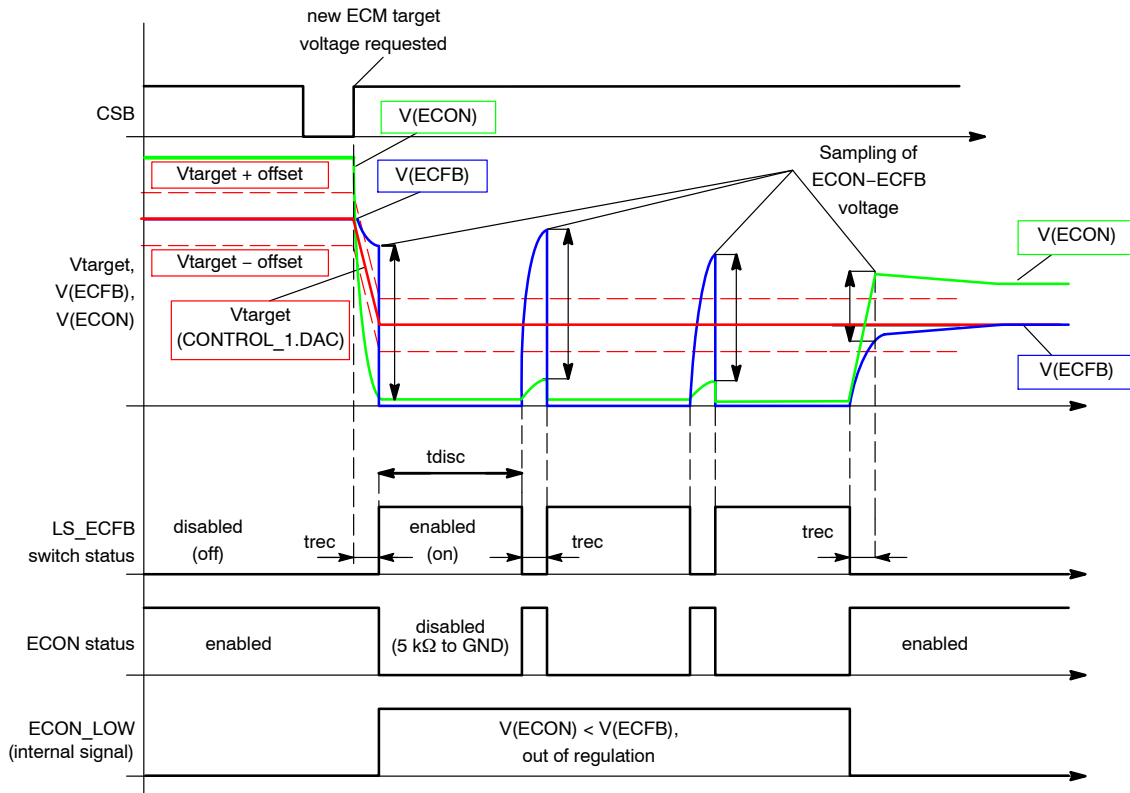


Figure 6. PWM Discharge Mode for ECFB

The controller provides a chip-internal diode from ECFB (Anode) to pin ECON (Cathode) to protect the external MOSFET. A capacitor of at least 4.7 nF has to be added to pin ECON for stability of the control loop. It is recommended to place 220 nF capacitor between ECFB and ground to increase the stability.

The status of the voltage control loop is reported via SPI. Bit STATUS_2.ECHI = 1 indicates that the voltage on ECFB is higher than the programmed target value, STATUS_2.ECLO = 1 indicates that the ECFB voltage is below the programmed value. Both status bits are valid if they are stable for at least 150 μs (settling time of the

regulation loop). If PWM discharge is enabled (CONFIG.ECM_LSPWM = 1), STATUS_2.ECHI is latched at the end of the discharge cycle, therefore if set it indicates that the device is in active discharge operation.

Since OUT10 is the output of a high-side driver, it contains the same diagnostic functions as the other high-side drivers (e.g. switch-off during overcurrent condition). In electro-chrome mode, OUT10 can't be controlled by PWM. For noise immunity reasons, it is recommended to place the loop capacitors at ECON as well as another capacitor between ECFB and GND as close as possible to the respective pins.

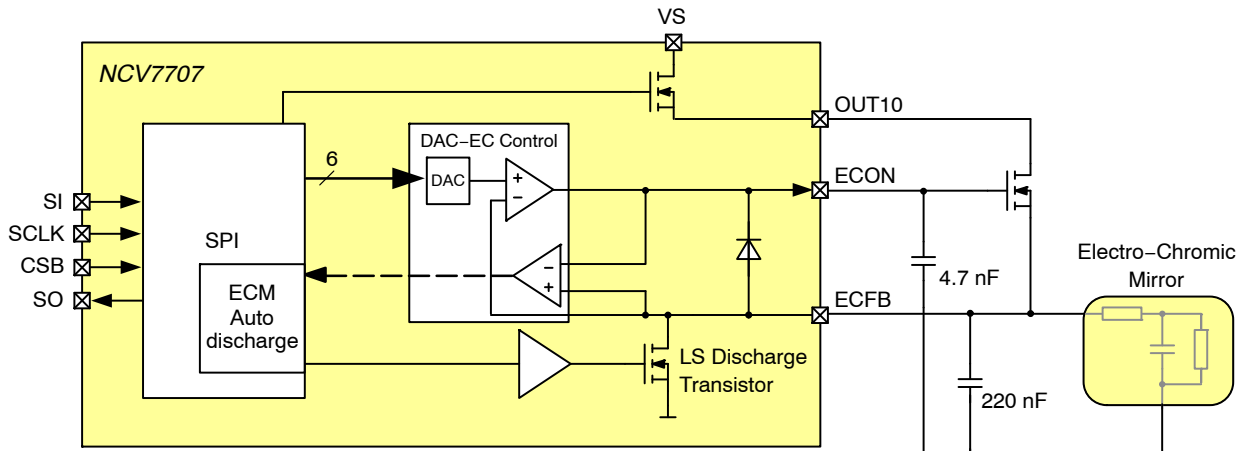


Figure 7. Electro Chromic Mirror Application Diagram

Diagnostic Functions

All diagnostic functions (overcurrent, underload, power supply monitoring, thermal warning and thermal shutdown) are internally filtered. The failure condition has to be valid for the minimum specified filtering time (td_{old} , td_{uld} , td_{uvov} and td_{tx}) before the corresponding status bit in the status register is set. The filter function is used to improve the noise immunity of the device. The undercurrent and temperature warning functions are intended for information purpose and do not affect the state of the output drivers. An overcurrent condition disables the corresponding output driver while a thermal shutdown event disables all outputs into high impedance state. Depending on the setting of the overcurrent recovery bits in the input register, the driver can either perform an auto-retry or remain latched off until the microcontroller clears the corresponding status bits. Overtemperature shutdown is latch-off only, without auto-retry functionality.

Overvoltage / Undervoltage Shutdown

If the supply voltage V_s rises above the switch off voltage $V_{ov_vs(off)}$ or falls below $V_{uv_vs(off)}$, all output transistors are switched to high-impedance state and the global status bit UOV_OC (multi information) is set. The status flag $STATUS_2.VSOV$, resp. $STATUS_2.VSUV$ is set, too, to log the over-/under-voltage event. The bit $CONTROL_3.OVUVR$ can be used to determine the recovery behavior once the V_s supply voltage gets back into the specified nominal operating range. $OVUVR = 0$ enables auto-recovery, with $OVUVR = 1$ the output stages remain in high impedance condition until the status flags have been cleared. Once set, $STATUS2.VSOV / VSUV$ can only be reset by a read&clear access to the status register $STATUS_2$.

Thermal Warning and Overtemperature Shutdown

The device provides a dual-stage overtemperature protection. If the junction temperature rises above T_{jtw_on} , a temperature warning flag (TW) is set in the Global Status Byte and can be read via SPI. The control software can then react onto this overload condition by a controlled disable of individual outputs. If however the junction temperature reaches the second threshold T_{jtd_on} , the thermal shutdown bit TSD is set in the Global Status Byte and all output stages are switched into high impedance state to protect the device. The minimum shutdown delay for overtemperature is td_{tx} . The output channels can be re-enabled after the device cooled down and the TSD flag has been reset by the microcontroller by setting $CONTROL_0.MODE = 0$.

Openload (Underload) Detection

The openload detection monitors the load current in the output stage while the transistor is active. If the load current is below the openload detection threshold for at least td_{uld} , the corresponding bit ($ULDx$) is set in the status registers $STATUS_1/2$. The status of the output remains unchanged. Once set, $ULDx$ remains set regardless of the actual load condition. It has to be reset by a read&write access to the corresponding status register.

Overload Detection

An overcurrent condition is indicated by the flag (UOV_OC) in the Global Status Byte after a filter time of at least td_{old} . The channel dependent overcurrent flags are set in the status registers ($STATUS_0/2.OCx$) and the corresponding driver is switched into high impedance state to protect the device. Each low-side and high-side driver stage provides its own overcurrent flag. Resetting this overcurrent flag automatically re-enables the respective output (provided it is still enabled thru the Control register). If the over current recovery function is enabled, the internal chip logic automatically resets the overcurrent flag after a fixed delay time, generating a PWM modulated current with a programmable duty cycle. Otherwise the status bits have to be cleared by the microcontroller by a read&clear access to the corresponding status register.

Cross-current Protection

All six half-bridges are protected against cross-currents by internal circuitry. If one driver is turned off (LS or HS), the activation of the other driver of the same output will be automatically delayed by the cross current protection mechanism until the active driver is safely turned off.

Mode Control

Wake-up and Mode Control

Two different modes are available:

- Active mode
- Standby mode

After power-up of VCC the device starts in Standby mode. Pulling the chip-select signal CSB to low level causes the device to change into Active mode (analog part active).

After at least 10 μs delay, the first SPI communication is valid and bit $CONTROL_0.MODE$ can be used to set the desired mode of operation. If bit $MODE$ remains reset (0), the device returns to the Standby mode after an internal delay of max. 8 μs , clearing all register content and setting all output stages into high impedance state.

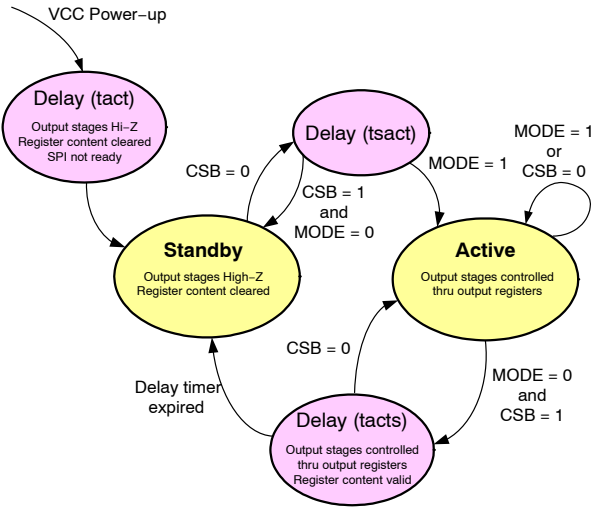


Figure 8. Mode Transitions Diagram

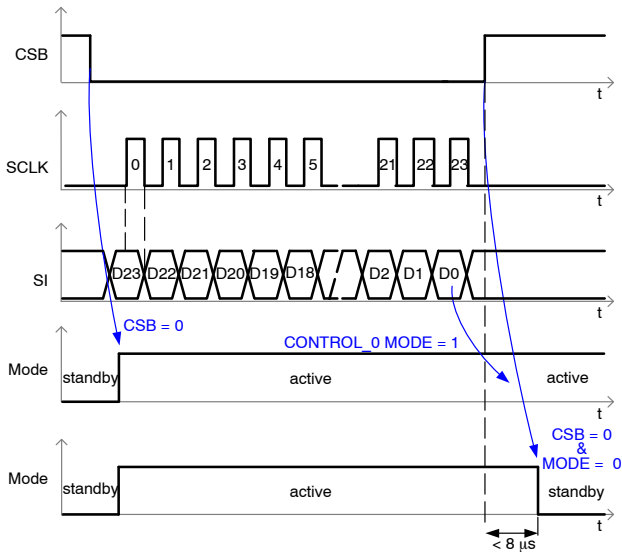


Figure 9. Mode Timing Diagram

SPI Control

General Description

The 4-wire SPI interface establishes a full duplex synchronous serial communication link between the NCV7707 and the application's microcontroller. The NCV7707 always operates in slave mode whereas the controller provides the master function. A SPI access is performed by applying an active-low slave select signal at CSB. SI is the data input, SO the data output. The SPI master provides the clock to the NCV7707 via the SCLK input. The digital input data is sampled at the rising edge at SCLK. The data output SO is in high impedance state (tri-state) when CSB is high. To readout the global error flag without sending a complete SPI frame, SO indicates the corresponding value as soon as CSB is set to active. With the first rising edge at SCLK after the high-to-low transition of CSB, the content of the selected register is transferred into the output shift register.

The NCV7707 provides four control registers (CONTROL_0/1/2/3), two PWM configuration registers (PWM_7/8 and PWM_9/10), three status registers (STATUS_0/1/2) and one general configuration register (CONFIG). Each of these register contains 16-bit data, together with the 8-bit frame header (access type, register address), the SPI frame length is therefore 24 bits. In addition to the read/write accessible registers, the NCV7707 provides five 8-bit ID registers (ID_HEADER, ID_VERSION, ID_CODE1/2 and ID_SPI-FRAME) with 8-bit data length. The content of these registers can still be read out by a 24-bit access, the data is then transferred in the MSB section of the data frame.

SPI Frame Format

Figure 10 shows the general format of the NCV7707 SPI frame.

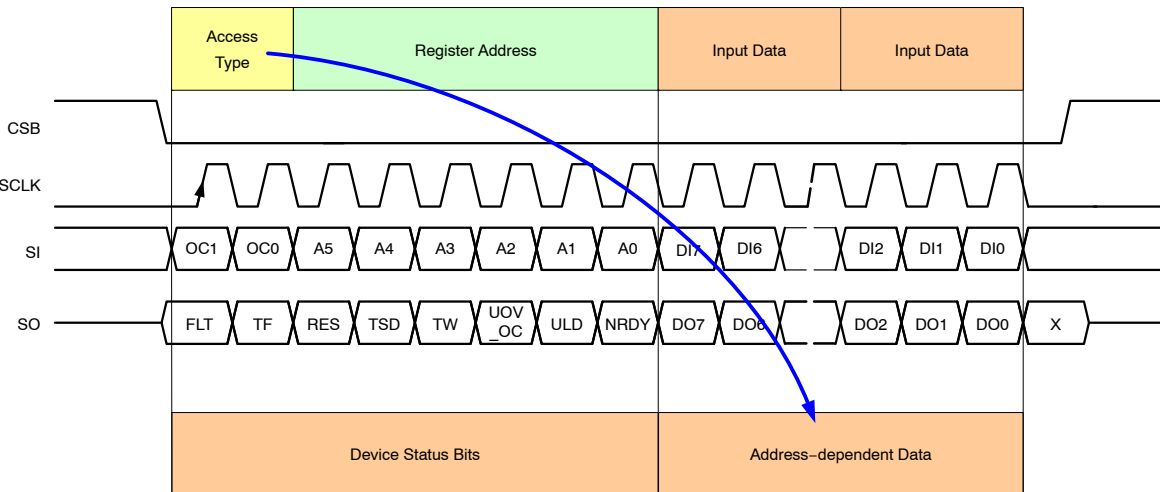


Figure 10. SPI Frame Format

24-bit SPI Interface

Both 24-bit input and output data are MSB first. Each SPI-input frame consists of a command byte followed by two data bytes. The data returned on SO within the same frame always starts with the global status byte. It provides general status information about the device. It is then followed by 2 data bytes (in-frame response) which content depends on the information transmitted in the command byte. For write access cycles, the global status byte is followed by the previous content of the addressed register.

Chip Select Bar (CSB)

CSB is the SPI input pin which controls the data transfer of the device. When CSB is high, no data transfer is possible and the output pin SO is set to high impedance. If CSB goes low, the serial data transfer is allowed and can be started. The communication ends when CSB goes high again.

Serial Clock (SCLK)

If CSB is set to low, the communication starts with the rising edge of the SCLK input pin. At each rising edge of SCLK, the data at the input pin Serial IN (SI) is latched. The data is shifted out thru the data output pin SO after the falling edges of SCLK. The clock SCLK must be active only within the frame time, means when CSB is low. The correct transmission is monitored by counting the number of clock pulses during the communication frame. If the number of SCLK pulses does not correspond to the frame width indicated in the SPI-frame-ID (Chip ID Register, address 3Eh) the frame will be ignored and the communication failure bit “TF” in the global status byte will be set. Due to this safety functionality, daisy chaining the SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSB signal of the connected ICs is recommended.

Serial Data In (SI)

During the rising edges of SCLK (CSB is low), the data is transferred into the device thru the input pin SI in a serial

way. The device features a stuck-at-one detection, thus upon detection of a command = FFFFFFFh, the device will be forced into the Standby mode. All output drivers are switched off.

Serial Data Out (SO)

The SO data output driver is activated by a logical low level at the CSB input and will go from high impedance to a low or high level depending on the global status bit, FLT (Global Error Flag). The first rising edge of the SCLK input after a high to low transition of the CSB pin will transfer the content of the selected register into the data out shift register. Each subsequent falling edge of the SCLK will shift the next bit thru SO out of the device.

Command Byte / Global Status Byte

Each communication frame starts with a command byte (Table 2). It consists of an operation code (OP[1:0], Table 3) which specifies the type of operation (Read, Write, Read & Clear, Readout Device Information) and a six bit address (A[5:0], Table 4). If less than six address bits are required, the remaining bits are unused but are reserved. Both Write and Read mode allow access to the internal registers of the device. A “Read & Clear”-access is used to read a status register and subsequently clear its content. The “Read Device Information” allows to read out device related information such as ID-Header, Product Code, Silicon Version and Category and the SPI-frame ID. While receiving the command byte, the global status byte is transmitted to the microcontroller. It contains global fault information for the device, as shown in Table 6.

ID Register

Chip ID Information is stored in five special 8-bit ID registers (Table 5). The content can be read out at the beginning of the communication.

Table 2. COMMAND BYTE / GLOBAL STATUS BYTE STRUCTURE

| Bit | Command Byte (IN) / Global Status Byte (OUT) | | | | | | | |
|-------------|--|-----|------|-----|----|--------|-----|------|
| | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| NCV7707 IN | OP1 | OP0 | A5 | A4 | A3 | A2 | A1 | A0 |
| NCV7707 OUT | FLT | TF | RESB | TSD | TW | UOV_OC | ULD | NRDY |
| Reset Value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

Table 3. COMMAND BYTE, ACCESS MODE

| OP1 | OP0 | Description |
|-----|-----|----------------------------|
| 0 | 0 | Write Access (W) |
| 0 | 1 | Read Access (R) |
| 1 | 0 | Read and Clear Access (RC) |
| 1 | 1 | Read Device ID (RDID) |

Table 4. COMMAND BYTE, REGISTER ADDRESS

| A[5:0] | Access | Description | Content |
|--------|--------|----------------------------------|---|
| 00h | R/W | Control Register CONTROL_0 | Device mode control, Bridge outputs control |
| 01h | R/W | Control Register CONTROL_1 | High-side outputs control, ECM control |
| 02h | R/W | Control Register CONTROL_2 | Bridge outputs recovery control, PWM enable, ECM setup |
| 03h | R/W | Control Register CONTROL_3 | High-side outputs recovery control, PWM enable, Current Sense selection |
| 08h | R/W | PWM Control Register PWM_7/8 | PWM control register for OUT7,8 |
| 09h | R/W | PWM Control Register PWM_9/10 | PWM control register for OUT9,10 |
| 10h | R/RC | Status Register STATUS_0 | Bridge outputs Overcurrent diagnosis |
| 11h | R/RC | Status Register STATUS_1 | Bridge outputs Underload diagnosis |
| 12h | R/RC | Status Register STATUS_2 | HS outputs Overcurrent and Underload diagnosis, Vs Over- and Under-voltage, EC-mirror |
| 3Fh | R/W | Configuration Register CONFIG | Mask bits for global fault bits |

Table 5. CHIP ID INFORMATION

| A[5:0] | Access | Description | Content |
|--------|--------|----------------|---------|
| 00h | RDID | ID header | 4300h |
| 01h | RDID | Version | 0400h |
| 02h | RDID | Product Code 1 | 7700h |
| 03h | RDID | Product Code 2 | 0700h |
| 3Eh | RDID | SPI-Frame ID | 0200h |

Table 6. Global Status Byte Content

| FLT | | Global Fault Bit |
|--------|---------------------|---|
| 0 | No fault Condition | Failures of the Global Status Byte, bits [6:0] are always linked to the Global Fault Bit FLT. This bit is generated by an OR combination of all failure bits of the device (RESB inverted). It is reflected via the SO pin while CSB is held low and NO clock signal is present (before first positive edge of SCLK). The flag will remain valid as long as CSB is held low. This operation does not cause the Transmission error Flag in the Global Status Byte to be set. Signals TW and ULD can be masked. |
| 1 | Fault Condition | |
| TF | | SPI Transmission Error |
| 0 | No Error | If the number of clock pulses within the previous frame was unequal 0 (FLT polling) or 24. The frame was ignored and this flag was set. |
| 1 | Error | |
| RESB | | Reset Bar (Active low) |
| 0 | Reset | Bit is set to "0" after a Power-on-Reset or a stuck-at-1 fault at SI (SPI-input data = FFFFFFFh) has been detected. All outputs are disabled. |
| 1 | Normal Operation | |
| TSD | | Overtemperature Shutdown |
| 0 | No Thermal Shutdown | Thermal Shutdown Status indication. In case of a Thermal Shutdown, all output drivers including the charge pump output are deactivated (high impedance). The TSD bit has to be cleared thru a SW reset to reactivate the output drivers and the chargepump output. |
| 1 | Thermal Shutdown | |
| TW | | Thermal Warning |
| 0 | No Thermal Warning | This bit indicates a pre-warning level of the junction temperature. It is maskable by the Configuration Register (CONFIG.NO_TW). |
| 1 | Thermal Warning | |
| UOV_OC | | VS Monitoring, Overcurrent Status |
| 0 | No Fault | This bit represents a logical OR combination of under-/overvoltage signals (VS) and overcurrent signals. |
| 1 | Fault | |
| ULD | | Underload |
| 0 | No Underload | This bit represents a logical OR combination of all underload signals. It is maskable by the Configuration Register (CONFIG.NO_ULDX). It is also possible to deactivate this flag for HS1 or LS1, only (CONFIG.NO_ULD_HS1/LS1). |
| 1 | Underload | |
| NRDY | | Not Ready |
| 0 | Device Ready | After transition from Standby to Active mode, an internal timer is started to allow the internal chargepump to settle before any outputs can be activated. This bit is cleared automatically after the startup is completed. |
| 1 | Device Not Ready | |

NCV7707

SPI REGISTERS CONTENT

CONTROL_0 Register

Address: 00h

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|------|
| Access type | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | - | - | - | RW |
| Bit name | HS1 | LS1 | HS2 | LS2 | HS3 | LS3 | HS4 | LS4 | HS5 | LS5 | HS6 | LS6 | 0 | 0 | 0 | MODE |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | HSx | LSx | | Description | Remark |
|--|-----|-----|---------|---------------------|--|
| HS/LS Outputs OUT1-6 Driver Control | 0 | 0 | default | OUTx High impedance | If a driver is enabled by the control register AND the corresponding PWM enable bit is set in CONTROL_2 register, the output is only activated if PWM1 (PWM2) input signal is high. Since OUT1..OUT6 are half-bridge outputs, activating both HS and LS at the same time is prevented by internal logic. |
| | 0 | 1 | | LSx enabled | |
| | 1 | 0 | | HSx enabled | |
| | 1 | 1 | | OUTx High impedance | |

| | MODE | | Description | Remark |
|---------------------|------|---------|-------------|--|
| Mode Control | 0 | default | Standby | If MODE is set, the device is switched to Active mode. Resetting MODE forces the device to transition into Standby mode, all internal memory is cleared and all output stages are switched into their default state (off). |
| | 1 | | Active | |

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CONTROL_1 Register

Address: 01h

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------|-------|-------|-------|-----|------|------|---------|------|------|------|------|------|------|------|----|
| Access type | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | - |
| Bit name | HS7.1 | HS7.0 | HS8.1 | HS8.0 | HS9 | HS10 | HS11 | LS ECFB | DAC5 | DAC4 | DAC3 | DAC2 | DAC1 | DAC0 | ECEN | 0 |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| HS Outputs OUT7,8 Control | HSx.1 | HSx.0 | | Description | Remark |
|---------------------------------|-------|-------|---------|---|--|
| | 0 | 0 | default | OUTx High impedance | If a driver is enabled by the control register AND the corresponding PWM enable bit is set in CONTROL_3 register, the output is only activated if the corresponding PWM input signal (PWM pin or internal PWM signal) is high. |
| | 0 | 1 | | Output enabled, low current mode (LED mode) | |
| | 1 | 0 | | Output enabled, high current mode (bulb mode) | |
| | 1 | 1 | | OUTx High impedance | |

| HS Outputs OUT9-11 Control | HSx | | Description | Remark |
|----------------------------------|-----|---------|---------------------|--|
| | 0 | default | OUTx High impedance | If a driver is enabled by the control register AND the corresponding PWM enable bit is set in CONTROL_3 register, the output is only activated if the corresponding PWM input signal (PWM pin or internal PWM signal) is high. |
| | 1 | | OUTx enabled | |

| ECFB Pull-down Output Control | LS ECFB | | Description | Remark |
|-------------------------------------|---------|---------|--|---|
| | 0 | default | Pull-down transistor disabled (high impedance) | The ECFB-pull-down transistor can only be activated if the DAC output voltage is set to 0 V (DAC[5:0]=0). If the PWM enable bit CONTROL_2.ECFB_PWM1 is set, the output will only be activated when the PWM1 signal input is high. |
| | 1 | | Pull-down transistor enabled | |

| Electrochrom. Mirror Reference Voltage | DAC[5:0] | | Description | Remark |
|---|----------|---------|--|---|
| | 0 | default | Reference voltage for ECON/ECFB differential amplifier | If bit CONTROL_2.FSR=0, the output voltage is clamped to 1.2 V. |
| | n | | | |

| Electrochrom. Mirror Enable | ECEN | | Description | Remark |
|--------------------------------|------|---------|---|--|
| | 0 | default | Electrochromic mirror controller disabled | By enabling the electrochromic mirror controller (ECEN=1), the output driver for the external pass transistor (ECON) is enabled. In addition, OUT10 is activated, regardless of the setting of CONTROL_1.HS10. |
| | 1 | | Electrochromic mirror controller enabled | |

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CONTROL_2 Register

Address: 02h

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------|------|------|------|------|------|-------------|------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|-----|
| Access type | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Bit name | OCR1 | OCR2 | OCR3 | OCR4 | OCR5 | OCR6 | OCR ECFB | PWMI | OUT1 PWM1 | OUT2 PWM1 | OUT3 PWM1 | OUT4 PWM1 | OUT5 PWM2 | OUT6 PWM1 | ECFB PWM1 | FSR |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | OCRx | | Description | Remark |
|----------------------|------|---------|-------------------------------|---|
| Overcurrent Recovery | 0 | default | Overcurrent Recovery disabled | During an overcurrent event the overcurrent status bit STATUS_0/2.OCx is set and the dedicated output is switched off. (The global multi bit UOV_OC is set, also). When the overcurrent recovery bit is enabled, the output will be reactivated automatically after a programmable delay time (CONTROL_3.OCRF). |
| | 1 | | Overcurrent Recovery enabled | |

| | PWMI | | Description | Remark |
|----------|------|---------|----------------------------|--|
| PWM Unit | 0 | default | Internal PWM unit disabled | The device has three different PWM sources: external pins PWM1, PWM2 and the internal PWM unit which can be used to control the lamp drivers in an additional way. PWMI selects the internal PWM unit. |
| | 1 | | Internal PWM unit enabled | |

| | OUTx PWM | | Description | Remark |
|------------------|----------|---------|-------------------|--|
| PWM1/2 Selection | 0 | default | PWMx not selected | For the half-bridge outputs it is possible to select the PWM input pins PWM1 or PWM2. In this case the dedicated output (selected in CONTROL_0 register) is on if the PWM input signal is high. OUT5 is controlled by PWM2, all other half-bridges are controlled by PWM1. |
| | 1 | | PWMx selected | |

| | FSR | | Description | Remark |
|------------------------------|-----|---------|---|---|
| DAC Full-scale Range Control | 0 | default | $V_{out} = 1.5 / 2^6 \cdot DAC[5:0]$ clamped at 1.2 V | The default voltage at ECFB in electrochrome mode is clamped at 1.2 V, when FSR=1 the maximum value is 1.5 V. |
| | 1 | | $V_{out} = 1.5 / 2^6 \cdot DAC[5:0]$ | |

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CONTROL_3 Register

Address: 03h

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------|------|------|-------|-------|-----------|-----------|-----------|------------|------------|------|-------|-----|-----|-----|-----|
| Access Type | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Bit name | OCR7 | OCR8 | OCR9 | OCR10 | OCR11 | OUT7 PWM1 | OUT8 PWM2 | OUT9 PWM1 | OUT10 PWM2 | OUT11 PWM1 | OCRF | OVUVR | IS3 | IS2 | IS1 | IS0 |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | OCRx | | Description | Remark |
|----------------------|------|---------|-------------------------------|---|
| Overcurrent Recovery | 0 | default | Overcurrent Recovery disabled | During an overcurrent event the overcurrent status bit STATUS_0/2.OCx is set and the dedicated output is switched off. (The global multi bit UOV_OC is set, also). When the overcurrent recovery bit is enabled, the output will be reactivated automatically after a programmable delay time (CONTROL_3.OCRF). |
| | 1 | | Overcurrent Recovery enabled | |

| | OUTx PWM | | Description | Remark |
|------------------|----------|---------|-------------------|---|
| PWM1/2 Selection | 0 | default | PWMx not selected | For the HS outputs it is possible to select the PWM input pins PWM1, PWM2 or internal PWM1 unit (OUT7-10 only). In this case the dedicated output (selected in CONTROL_1 register) is on if the PWM input signal is high. OUT8 and OUT10 are controlled by PWM2, OUT7,9 and OUT11 are controlled by PWM1. |
| | 1 | | PWMx selected | |

| | OCRF | | Description | Remark |
|--|------|---------|--------------------------------|--|
| Overcurrent Recovery Frequency Selection | 0 | default | Slow Overcurrent recovery mode | If the overcurrent recovery bit is set, the output will be switched on automatically after a delay time. The recovery behavior of OUT7,8 in bulb mode is not affected by this bit. |
| | 1 | | Fast Overcurrent recovery mode | |

| | OVUVR | | Description | Remark |
|--------------------------------|-------|---------|--|---|
| Over- / Under-voltage Recovery | 0 | default | Over- and undervoltage recovery function enabled | If the OV/UV recovery is disabled by setting OVUVR=1, the status register STATUS_2 bits VSOV or VSUV have to be cleared after an OV/UV event. |
| | 1 | | No over- and undervoltage recovery | |

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| Current Sensing Selection | IS3 | IS2 | IS1 | IS0 | Description | Remark |
|----------------------------------|-----|-----|-----|-----------------------------|-----------------------------|---|
| | 0 | 0 | 0 | 0 | OUT1 | The current in all high-side power stages (except of OUT2/3) can be monitored at the bidirectional multifunctional pin ISOUT/PWM2. This pin is a multifunctional pin and can be activated as output by setting the current selection bits IS[3:0]. The selected high-side output will be multiplexed to the output ISOUT. |
| | 0 | 0 | 0 | 1 | current sensing deactivated | |
| | 0 | 0 | 1 | 0 | current sensing deactivated | |
| | 0 | 0 | 1 | 1 | OUT4 | |
| | 0 | 1 | 0 | 0 | OUT5 | |
| | 0 | 1 | 0 | 1 | OUT6 | |
| | 0 | 1 | 1 | 0 | OUT7 | |
| | 0 | 1 | 1 | 1 | OUT8 | |
| | 1 | 0 | 0 | 0 | OUT9 | |
| | 1 | 0 | 0 | 1 | OUT10 | |
| | 1 | 0 | 1 | 0 | OUT11 | |
| | 1 | 0 | 1 | 1 | current sensing deactivated | |
| | 1 | 1 | 0 | 0 | current sensing deactivated | |
| | 1 | 1 | 0 | 1 | current sensing deactivated | |
| | 1 | 1 | 1 | 0 | current sensing deactivated | |
| 1 | 1 | 1 | 1 | current sensing deactivated | | |

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PWM_7/8 Register

Address: 08h

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Access Type | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Bit Name | FSEL7 | PW7.6 | PW7.5 | PW7.4 | PW7.3 | PW7.2 | PW7.1 | PW7.0 | FSEL8 | PW8.6 | PW8.5 | PW8.4 | PW8.3 | PW8.2 | PW8.1 | PW8.0 |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| PWM Duty Cycle selector for OUT7 | PW7[6:0] | | Description | Remark |
|----------------------------------|----------|---------|--|---|
| | 0 | default | Duty Cycle for OUT7 = (PW7[6:0] + 1) / 128 | It is possible to control OUT7 by the internal PWM unit if bit PWMI is set in the control register CONTROL_2. |
| | 1 .. 7Fh | | | |

| PWM Frequency selector for OUT7 | FSEL7 | | Description | Remark |
|---------------------------------|-------|---------|-----------------|--|
| | 0 | default | f(PWM) = 170 Hz | Bit FSEL7 selects between 170 and 225 Hz PWM frequency for OUT7. |
| | 1 | | f(PWM) = 225 Hz | |

| PWM Duty Cycle selector for OUT8 | PW8[6:0] | | Description | Remark |
|----------------------------------|----------|---------|--|---|
| | 0 | default | Duty Cycle for OUT8 = (PW8[6:0] + 1) / 128 | It is possible to control OUT8 by the internal PWM unit if bit PWMI is set in the control register CONTROL_2. |
| | 1 .. 7Fh | | | |

| PWM Frequency selector for OUT8 | FSEL8 | | Description | Remark |
|---------------------------------|-------|---------|-----------------|--|
| | 0 | default | f(PWM) = 170 Hz | Bit FSEL8 selects between 170 and 225 Hz PWM frequency for OUT8. |
| | 1 | | f(PWM) = 225 Hz | |

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PWM_9/10 Register

Address: 09h

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|--------|--------|--------|--------|--------|--------|--------|--------|
| Access Type | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Bit Name | FSEL9 | PW9.6 | PW9.5 | PW9.4 | PW9.3 | PW9.2 | PW9.1 | PW9.0 | FSEL10 | PW10.6 | PW10.5 | PW10.4 | PW10.3 | PW10.2 | PW10.1 | PW10.0 |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| PWM Duty Cycle selector for OUT9 | PW9[6:0] | | Description | Remark |
|----------------------------------|----------|---------|--|---|
| | 0 | default | Duty Cycle for OUT9 = (PW9[6:0] + 1) / 128 | It is possible to control OUT9 by the internal PWM unit if bit PWMI is set in the control register CONTROL_2. |
| | 1 .. 7Fh | | | |

| PWM Frequency selector for OUT9 | FSEL9 | | Description | Remark |
|---------------------------------|-------|---------|-----------------|--|
| | 0 | default | f(PWM) = 170 Hz | Bit FSEL9 selects between 170 and 225 Hz PWM frequency for OUT9. |
| | 1 | | f(PWM) = 225 Hz | |

| PWM Duty Cycle selector for OUT10 | PW10[6:0] | | Description | Remark |
|-----------------------------------|-----------|---------|--|--|
| | 0 | default | Duty Cycle for OUT10 = (PW10[6:0] + 1) / 128 | It is possible to control OUT10 by the internal PWM unit if bit PWMI is set in the control register CONTROL_2. |
| | 1 .. 7Fh | | | |

| PWM Frequency selector for OUT10 | FSEL10 | | Description | Remark |
|----------------------------------|--------|---------|-----------------|--|
| | 0 | default | f(PWM) = 170 Hz | Bit FSEL10 selects between 170 and 225 Hz PWM frequency for OUT10. |
| | 1 | | f(PWM) = 225 Hz | |

STATUS_0 Register

Address: 10h

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|----|----|----|----|
| Access Type | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | - | - | - | - |
| Bit Name | OC HS1 | OC LS1 | OC HS2 | OC LS2 | OC HS3 | OC LS3 | OC HS4 | OC LS4 | OC HS5 | OC LS5 | OC HS6 | OC LS6 | 0 | 0 | 0 | 0 |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | OCx | Description | Remark |
|-------------------------------------|-----|-------------------------|--|
| OUT1-6 Overcurrent Detection | 0 | No overcurrent detected | During an overcurrent event in one of the HS or LS, the belonging overcurrent status bit STATUS_0.OCx is set and the dedicated output is switched off. (The global multi bit UOV_OC is set, also). When the overcurrent recovery bit is enabled, the output will be reactivated automatically after a programmable delay time (CONTROL_3.OCRF). If the overcurrent recovery bit is not set the microcontroller has to clear the OC failure bit and to reactivate the output stage again. |
| | 1 | Overcurrent detected | |

STATUS_1 Register

Address: 11h

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|----|----|----|----|
| Access Type | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | - | - | - | - |
| Bit Name | ULD HS1 | ULD LS1 | ULD HS2 | ULD LS2 | ULD HS3 | ULD LS3 | ULD HS4 | ULD LS4 | ULD HS5 | ULD LS5 | ULD HS6 | ULD LS6 | 0 | 0 | 0 | 0 |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | ULDx | Description | Remark |
|-----------------------------------|------|-----------------------|---|
| OUT1-6 Underload Detection | 0 | No underload detected | For each output stage an underload status bit ULD is available. The underload detection is done in "on-mode". If the load current is below the undercurrent detection threshold for at least td_uld , the corresponding underload bit ULDx is set. If an ULD event occurs the global status bit ULD will be set. For ULD_HS1 and ULD_LS1 it is possible to deactivate the global ULD failure bit by setting the configuration bits CONFIG.NO_ULD_HS1/LS1. With setting CONFIG.NO_ULD_OUTn the global ULD failure bit is deactivated in general. |
| | 1 | Underload detected | |

STATUS_2 Register

Address: 12h

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------|---------|--------|---------|--------|---------|---------|----------|---------|----------|---------|----------|------|------|------|------|
| Access type | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC | R/RC |
| Bit name | OC HS7 | ULD HS7 | OC HS8 | ULD HS8 | OC HS9 | ULD HS9 | OC HS10 | ULD HS10 | OC HS11 | ULD HS11 | OC ECFB | ULD ECFB | VSUV | VSOV | ECLO | ECHI |
| Reset value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | OCx | Description | Remark |
|--------------------------------------|-----|-------------------------|---|
| OUT7-11 Overcurrent Detection | 0 | No overcurrent detected | During an overcurrent event in one of the HS the belonging overcurrent status bit STATUS_2.OCx is set and the dedicated output is switched off. (The global multi bit UOV_OC is set, also). When the overcurrent recovery bit is enabled, the output will be reactivated automatically after a programmable delay time (CONTROL_3.OCRF). If the overcurrent recovery bit is not set the microcontroller has to clear the OC failure bit and to reactivate the output stage again. |
| | 1 | Overcurrent detected | |

| | ULDx | Description | Remark |
|------------------------------------|------|-----------------------|--|
| OUT7-11 Underload Detection | 0 | No underload detected | For each output stage an underload status bit ULD is available. The underload detection is done in "on-mode". If the load current is below the undercurrent detection threshold for at least td_uld, the corresponding underload bit ULDx is set. If an ULD event occurs the global status bit ULD will be set. It is possible to deactivate the global ULD failure bit by setting the configuration bits CONFIG.NO_ULD_OUTn. |
| | 1 | Underload detected | |

| | VSUV | Description | Remark |
|------------------------|------|--------------------------|--|
| Vs Undervoltage | 0 | No undervoltage detected | In case of an Vs undervoltage event, the output stages will be deactivated immediately and the corresponding failure flag will be set. By default the output stages will be reactivated automatically after Vs is recovered unless the control bit CONTROL_3.OVUVR is set. If this is the case (OVUVR=1) the bit VSUV has to be cleared after an UV event. |
| | 1 | Undervoltage detected | |

| | VSOV | Description | Remark |
|-----------------------|------|-------------------------|---|
| Vs Overvoltage | 0 | No overvoltage detected | In case of an Vs overvoltage event, the output stages will be deactivated immediately and the corresponding failure flag will be set. By default the output stages will be reactivated automatically after Vs is recovered unless the control bit CONTROL_3.OVUVR is set. If this is the case (OVUVR=1) the bit VSOV has to be cleared after an OV event. |
| | 1 | Overvoltage detected | |

| | ECLO | ECHI | Description | Remark |
|---------------------------------|------|------|--------------------------------|---|
| EC Mirror Control Status | 0 | 0 | ECM output regulation in range | Two comparators monitor the voltage at pin ECFB (feedback) in electrochrome mode. If this voltage is below / above the programmed target these bits signal the difference after at least 32 µs. The bits are not latched and may toggle after at least 32 µs, if the ECFB voltage has not yet reached the target. They are not assigned to the Global Error Flag. |
| | 0 | 1 | ECM output V > Vregulation | |
| | 1 | 0 | ECM output V > Vregulation | |
| | 1 | 1 | not used | |

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CONFIG Register

Address: 3Fh

| Bit | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----|-----|-----|-----|-----|-----|----|----|--------------|----|---------------|---------------|-----------|----|----------------|----|
| Access Type | - | - | - | - | - | - | - | - | RW | - | RW | RW | RW | - | RW | - |
| Bit Name | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ECM LSPWM | 0 | NO_ULD HS1 | NO_ULD LS1 | NO_ TW | 0 | NO_ULD OUTn | 0 |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | NO_ULD HS1 | NO_ULD LS1 | | Description | Remark |
|-------------------------------|---------------|---------------|---------|---|--|
| Global Underload Flag HS1/LS1 | 0 | 0 | default | Global underload flag at HS1/LS1 active | For ULD_HS1 and ULD_LS1 it is possible to deactivate the global ULD failure bit by setting the configuration bits CONFIG.NO_ULD_HS1/LS1. With setting CONFIG.NO_ULD_OUTn the global ULD failure bit is deactivated in general. |
| | 0 | 1 | | No global underload flag at LS1 | |
| | 1 | 0 | | No global underload flag at HS1 | |
| | 1 | 1 | | No global underload flag at HS1/LS1 | |

| | NO_TW | | Description | Remark |
|-------------------------|-------|---------|--------------------------------|---|
| No Thermal Warning Flag | 0 | default | Thermal warning flag active | The global thermal warning bit TW can be deactivated. |
| | 1 | | No thermal warning flag active | |

| | NO_ULD_OUTn | | Description | Remark |
|----------------------------|-------------|---------|---------------------------------|---|
| Global Underload Flag OUTn | 0 | default | Global underload flag active | By setting CONFIG.NO_ULD_OUTn the global ULD failure bit is deactivated in general. |
| | 1 | | No global underload flag active | |

| | ECM_LSPWM | | Description | Remark |
|-------------------|-----------|---------|-------------------------|--|
| ECM PWM Discharge | 0 | default | LS PWM feature disabled | If this bit is set, automatic PWM discharge on the ECM output is enabled. In case of PWM discharge the Overcurrent recovery feature is disabled, regardless of the setting of CONTROL_2.OC_ECFB. |
| | 1 | | LS PWM feature enabled | |

ORDERING INFORMATION

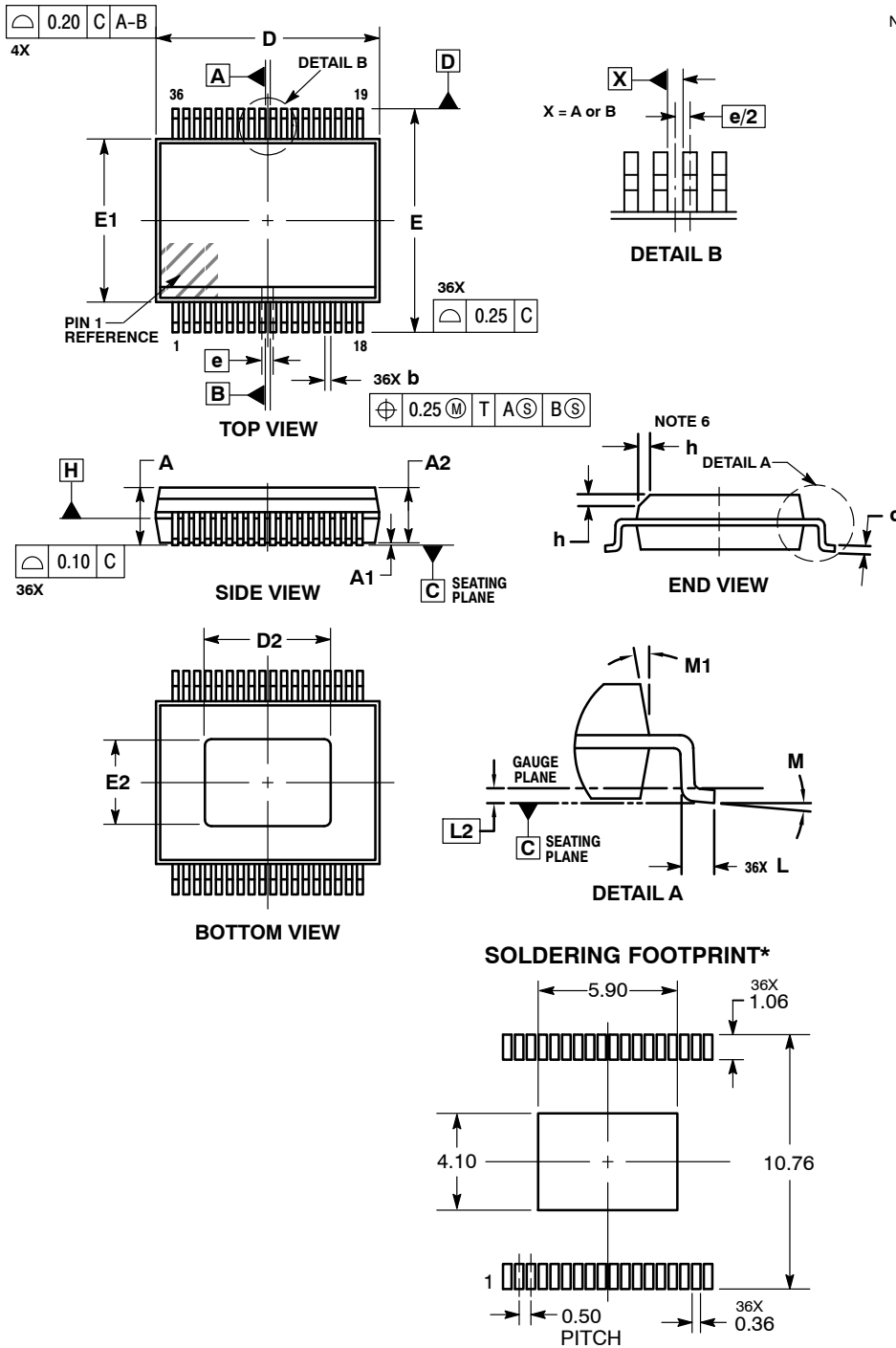
| Device | Package | Shipping [†] |
|--------------|------------------------|-----------------------|
| NCV7707DQR2G | SSOP36-EP (Pb-Free) | 1500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCV7707

PACKAGE DIMENSIONS

SSOP36 EP
CASE 940AB
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MMC.
4. DIMENSION b SHALL BE MEASURED BETWEEN 0.10 AND 0.25 FROM THE TIP.
5. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSIONS D AND E1 SHALL BE DETERMINED AT DATUM H.
6. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, A PIN ONE IDENTIFIER MUST BE LOCATED WITHIN THE INDICATED AREA.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | --- | 2.65 |
| A1 | --- | 0.10 |
| A2 | 2.35 | 2.60 |
| b | 0.18 | 0.36 |
| c | 0.23 | 0.32 |
| D | 10.30 BSC | |
| D2 | 5.70 | 5.90 |
| E | 10.30 BSC | |
| E1 | 7.50 BSC | |
| E2 | 3.90 | 4.10 |
| e | 0.50 BSC | |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| L2 | 0.25 BSC | |
| M | 0° | 8° |
| M1 | 5° | 15° |

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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