KAI-02170

1920 (H) x 1080 (V) Interline CCD Image Sensor

ON Semiconductor®

www.onsemi.com

Description

The KAI−02170 Image Sensor is a 2-megapixel CCD in a 1 inch optical format. Based on the TRUESENSE 7.4 micron Interline Transfer CCD Platform, the sensor provides very high smear rejection and up to 82 dB linear dynamic range through the use of a unique dual-gain amplifier. A flexible readout architecture enables use of 1, 2, or 4 outputs for full resolution readout up to 60 frames per second, while a vertical overflow drain structure suppresses image blooming and enables electronic shuttering for precise exposure control.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CCD, Progressive Scan
Total Number of Pixels	1984 (H) × 1124 (V)
Number of Effective Pixels	1936 (H) × 1096 (V)
Number of Active Pixels	1920 (H) × 1080 (V)
Pixel Size	7.4 μm (H) × 7.4 μm (V)
Active Image Size	14.2 mm (H) × 8.00 mm (V), 16.3 mm (Diagonal), 1″ Optical Format
Aspect Ratio	16:9
Number of Outputs	1, 2, or 4
Charge Capacity	44,000 electrons
Output Sensitivity	8.7 μV/e⁻ (Low), 33 μV/e⁻ (High)
Quantum Efficiency Pan (−ABA, −PBA, −QBA) R, G, B (−CBA) R, G, B (−FBA)	 52% 38%, 42%, 43% 37%, 42%, 41%
Read Noise (f = 40 MHz)	12 e⁻ rms
Dark Current Photodiode VCCD	 3 e⁻/s 145 e⁻/s
Dark Current Doubling Temp. Photodiode VCCD	 7°C 9°C
Dynamic Range High Gain Amp (40 MHz) Dual Amp, 2×2 Bin (40 MHz)	 70 dB 82 dB
Charge Transfer Efficiency	0.999999
Blooming Suppression	> 1000 X
Smear	−115 dB
Image Lag	< 10 electrons
Maximum Pixel Clock Speed	40 MHz
Maximum Frame Rate Quad Output Dual Output Single Output	 60 fps 30 fps 15 fps
Package	68 Pin PGA
Cover Glass	AR Coated, 2 Sides

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.

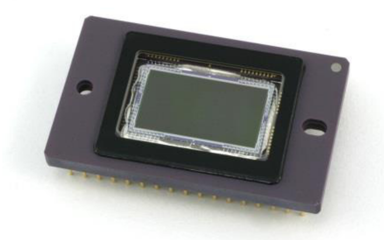


Figure 1. KAI−02170 Interline CCD Image Sensor

Features

- Superior Smear Rejection
- Up to 82 dB Linear Dynamic Range
- Bayer Color Pattern, TRUESENSE Sparse Color Filter Pattern, and Monochrome Configurations
- Progressive Scan & Flexible Readout Architecture
- High Frame Rate
- High Sensitivity − Low Noise Architecture
- Package Pin Reserved for Device Identification

Application

- Industrial Imaging and Inspection
- Traffic
- Surveillance

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

The sensor is available with the TRUESENSE Sparse Color Filter Pattern, a technology which provides a 2x improvement in light sensitivity compared to a standard color Bayer part.

The sensor shares common pin-out and electrical configurations with a full family of Truesense Imaging Interline Transfer CCD image sensors, allowing a single camera design to be leveraged in support of multiple devices.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAI−02170 IMAGE SENSOR

Part Number	Description	Marking Code
KAI−02170−ABA−JD−BA	Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Standard Grade	KAI−021570−ABA Serial Number
KAI−02170−ABA−JD−AE	Monochrome, Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	
KAI−02170−FBA−JD−BA	Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Standard Grade	KAI−021570−FBA Serial Number
KAI−02170−FBA−JD−AE	Gen2 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	
KAI−02170−QBA−JD−BA	Gen2 Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Standard Grade	KAI−02170−QBA Serial Number
KAI−02170−QBA−JD−AE	Gen2 Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	
KAI−02170−CBA−JD−BA*	Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Standard Grade	KAI−02170−CBA Serial Number
KAI−02170−CBA−JD−AE*	Gen1 Color (Bayer RGB), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	
KAI−02170−PBA−JD−BA*	Gen1 Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Standard Grade	KAI−02170−PBA Serial Number
KAI−02170−PBA−JD−AE*	Gen1 Color (TRUESENSE Sparse CFA), Telecentric Microlens, PGA Package, Sealed Clear Cover Glass with AR Coating (Both Sides), Engineering Grade	

*Not recommended for new designs.

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
G2−FPGA−BD−14−40−A−GEVK	FPGA Board for IT−CCD Evaluation Hardware
KAI−68PIN−HEAD−BD−A−GEVB	68 Pin Imager Board for IT−CCD Evaluation Hardware
LENS−MOUNT−KIT−A−GEVK	Lens Mount Kit for IT−CCD Evaluation Hardware
KAI−68PIN−N−PROBE−CARD−A−GEVB	68 Pin Probe Card (Narrow Socket)
KAI−68PIN−W−PROBE−CARD−A−GEVB	68 Pin Probe Card (Wide Socket)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

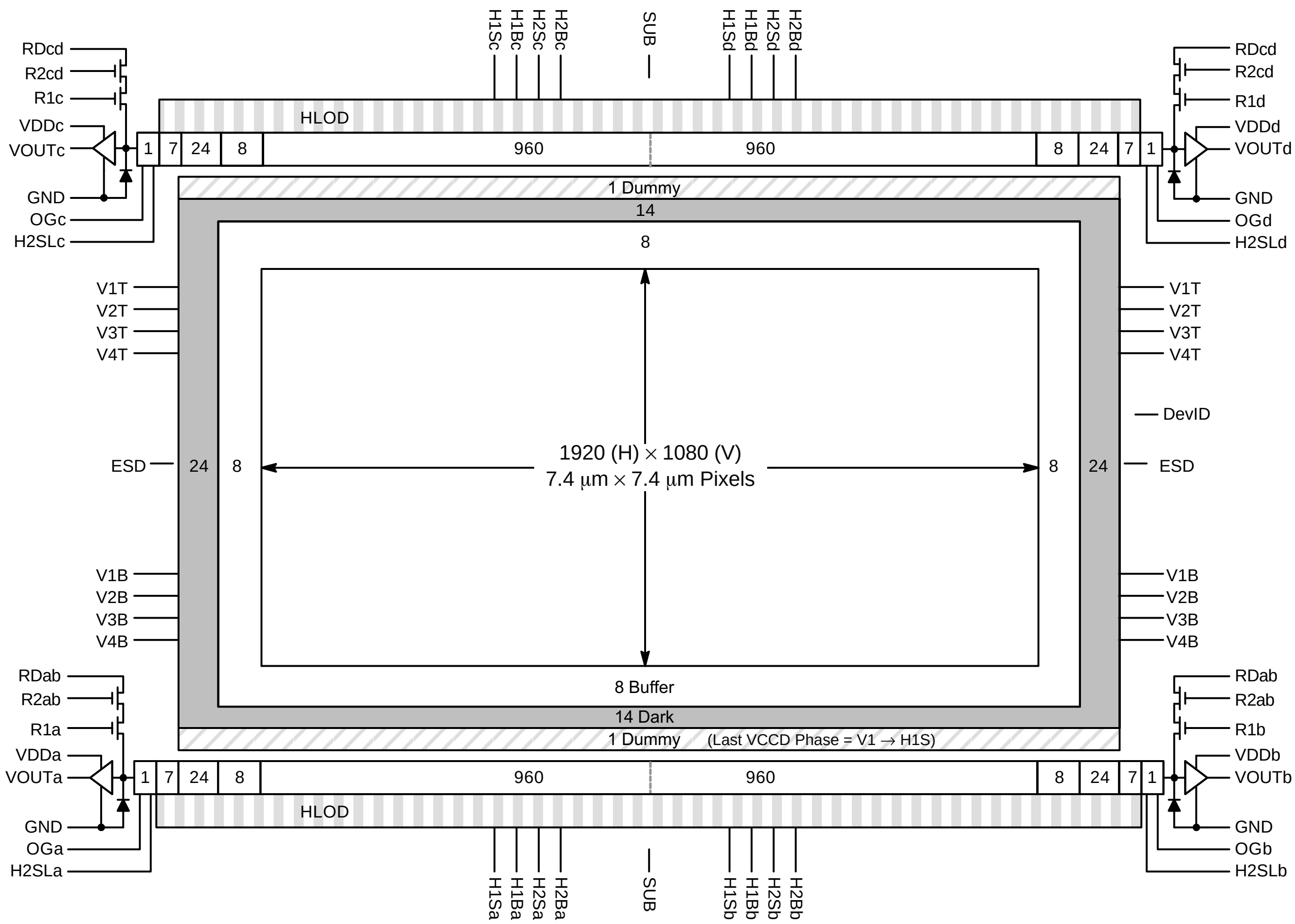


Figure 2. Block Diagram

Dark Reference Pixels

There are 14 dark reference rows at the top and 14 dark rows at the bottom of the image sensor. The 24 dark columns on the left or right side of the image sensor should be used as a dark reference.

Under normal circumstances use only the center 22 columns of the 24 column dark reference due to potential light leakage.

Dummy Pixels

Within each horizontal shift register there are 8 leading additional shift phases. These pixels are designated as dummy pixels and should not be used to determine a dark reference level.

In addition, there is one dummy row of pixels at the top and bottom of the image.

Active Buffer Pixels

8 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non-uniformities.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photosite. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

ESD Protection

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor. See Power-Up and Power-Down Sequence section.

Bayer Color Filter Pattern

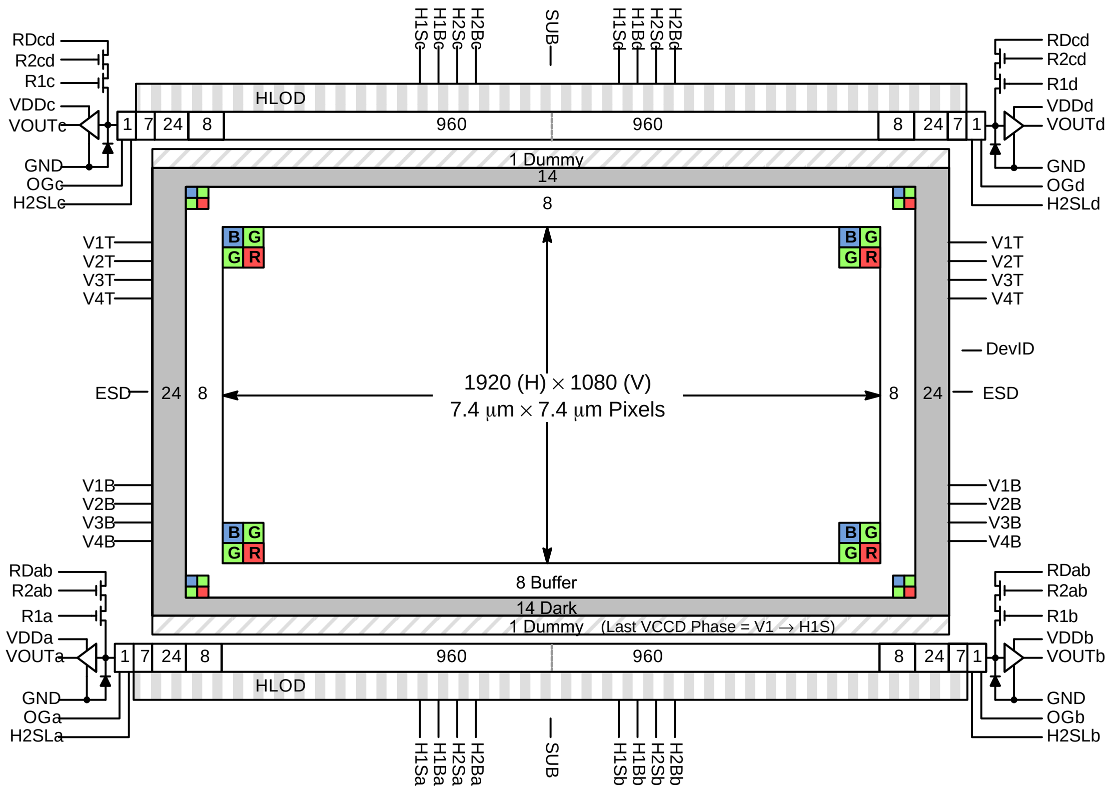


Figure 3. Bayer Color Filter Pattern

TRUESENSE Sparse Color Filter Pattern

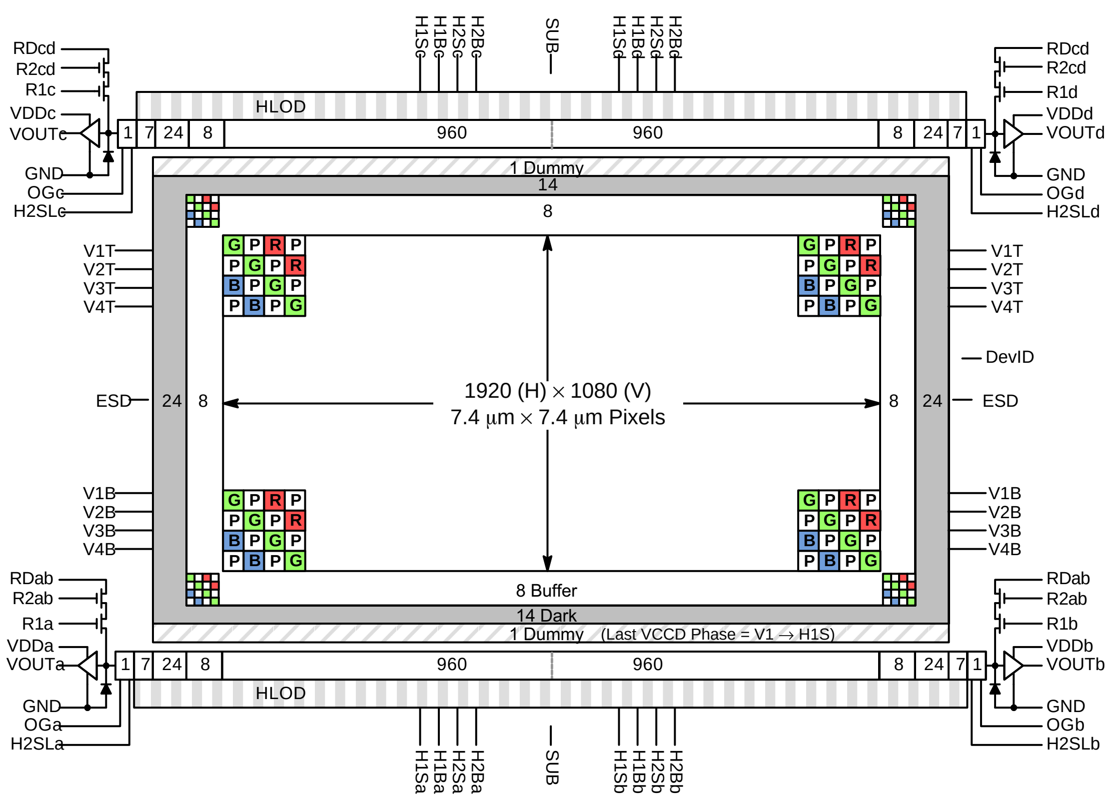


Figure 4. TRUESENSE Sparse Color Filter Pattern

Physical Description

Pin Description and Device Orientation

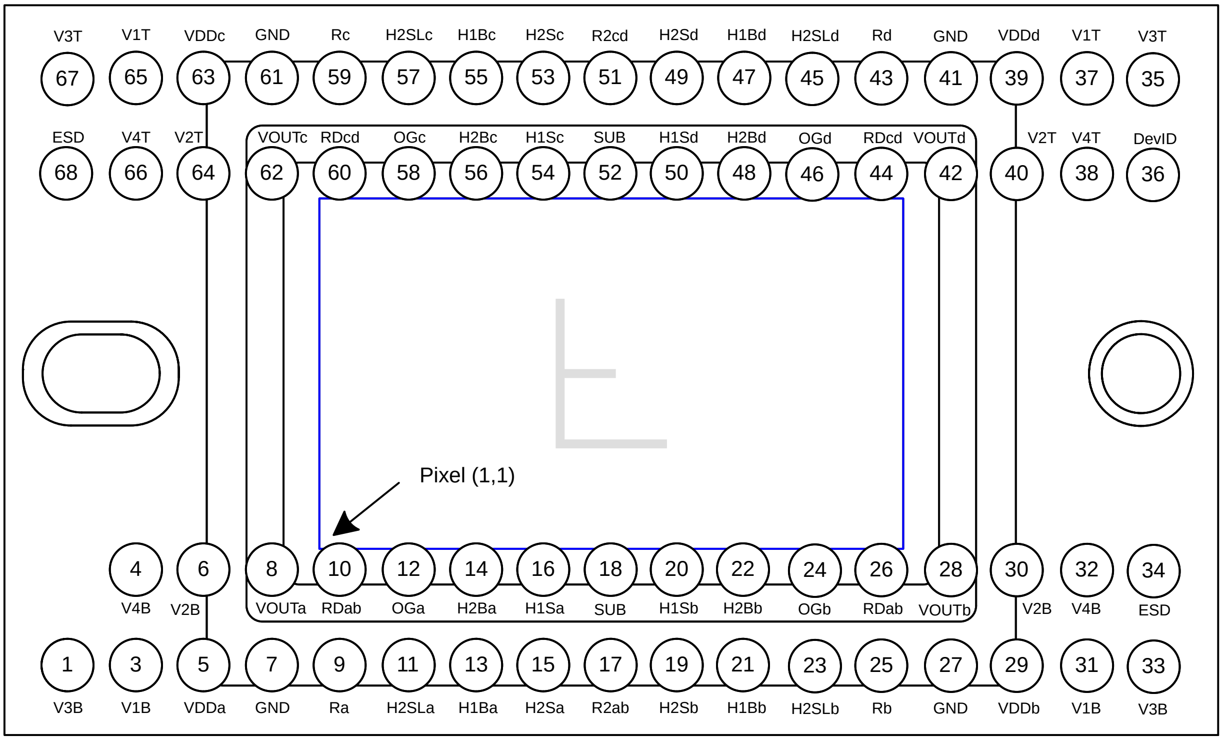


Figure 5. Package Pin Designations − Top View

Table 4. PACKAGE PIN DESCRIPTION

Pin	Name	Description
1	V3B	Vertical CCD Clock, Phase 3, Bottom
3	V1B	Vertical CCD Clock, Phase 1, Bottom
4	V4B	Vertical CCD Clock, Phase 4, Bottom
5	VDDa	Output Amplifier Supply, Quadrant a
6	V2B	Vertical CCD Clock, Phase 2, Bottom
7	GND	Ground
8	VOUTa	Video Output, Quadrant a
9	Ra	Reset Gate, Standard (High) Gain, Quadrant a
10	RDab	Reset Drain, Quadrants a & b
11	H2SLa	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant a
12	OGa	Output Gate, Quadrant a
13	H1Ba	Horizontal CCD Clock, Phase 1, Barrier, Quadrant a
14	H2Ba	Horizontal CCD Clock, Phase 2, Barrier, Quadrant a
15	H2Sa	Horizontal CCD Clock, Phase 2, Storage, Quadrant a
16	H1Sa	Horizontal CCD Clock, Phase 1, Storage, Quadrant a
17	R2ab	Reset Gate, Low Gain, Quadrants a & b
18	SUB	Substrate
19	H2Sb	Horizontal CCD Clock, Phase 2, Storage, Quadrant b
20	H1Sb	Horizontal CCD Clock, Phase 1, Storage, Quadrant b
21	H1Bb	Horizontal CCD Clock, Phase 1, Barrier, Quadrant b
22	H2Bb	Horizontal CCD Clock, Phase 2, Barrier, Quadrant b

Table 4. PACKAGE PIN DESCRIPTION (continued)

Pin	Name	Description
23	H2SLb	Horizontal CCD Clock, Phase 1, Storage, Last Phase, Quadrant b
24	OGb	Output Gate, Quadrant b
25	Rb	Reset Gate, Standard (High) Gain, Quadrant b
26	RDab	Reset Drain, Quadrants a & b
27	GND	Ground
28	VOUTb	Video Output, Quadrant b
29	VDDb	Output Amplifier Supply, Quadrant b
30	V2B	Vertical CCD Clock, Phase 2, Bottom
31	V1B	Vertical CCD Clock, Phase 1, Bottom
32	V4B	Vertical CCD Clock, Phase 4, Bottom
33	V3B	Vertical CCD Clock, Phase 3, Bottom
34	ESD	ESD Protection Disable
35	V3T	Vertical CCD Clock, Phase 3, Top
36	DevID	Device Identification
37	V1T	Vertical CCD Clock, Phase 1, Top
38	V4T	Vertical CCD Clock, Phase 4, Top
39	VDDd	Output Amplifier Supply, Quadrant d
40	V2T	Vertical CCD Clock, Phase 2, Top
41	GND	Ground
42	VOUTd	Video Output, Quadrant d
43	Rd	Reset Gate, Standard (High) Gain, Quadrant d
44	RDcd	Reset Drain, Quadrants c & d
45	H2SLd	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant d
46	OGd	Output Gate, Quadrant d
47	H1Bd	Horizontal CCD Clock, Phase 1, Barrier, Quadrant d
48	H2Bd	Horizontal CCD Clock, Phase 2, Barrier, Quadrant d
49	H2Sd	Horizontal CCD Clock, Phase 2, Storage, Quadrant d
50	H1Sd	Horizontal CCD Clock, Phase 1, Storage, Quadrant d
51	R2cd	Reset Gate, Low Gain, Quadrants c & d
52	SUB	Substrate
53	H2Sc	Horizontal CCD Clock, Phase 2, Storage, Quadrant c
54	H1Sc	Horizontal CCD Clock, Phase 1, Storage, Quadrant c
55	H1Bc	Horizontal CCD Clock, Phase 1, Barrier, Quadrant c
56	H2Bc	Horizontal CCD Clock, Phase 2, Barrier, Quadrant c
57	H2SLc	Horizontal CCD Clock, Phase 2, Storage, Last Phase, Quadrant c
58	OGc	Output Gate, Quadrant c
59	Rc	Reset Gate, Standard (High) Gain, Quadrant c
60	RDcd	Reset Drain, Quadrants c & d
61	GND	Ground
62	VOUTc	Video Output, Quadrant c
63	VDDc	Output Amplifier Supply, Quadrant c
64	V2T	Vertical CCD Clock, Phase 2, Top
65	V1T	Vertical CCD Clock, Phase 1, Top
66	V4T	Vertical CCD Clock, Phase 4, Top
67	V3T	Vertical CCD Clock, Phase 3, Top
68	ESD	EDS Protection Disable

1. Liked named pins are internally connected and should have a common drive signal.

IMAGING PERFORMANCE

Table 5. TYPICAL OPERATIONAL CONDITIONS

(Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions.)

Description	Condition	Notes
Light Source	Continuous Red, Green and Blue LED Illumination.	1
Operation	Nominal Operating Voltages and Timing.	

1. For monochrome sensor, only green LED used.

Specifications

Table 6. PERFORMANCE SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Unit	Sampling Plan	Temperature Tested at (°C)
ALL CONFIGURATIONS							
Dark Field Global Non-Uniformity	DSNU	−	−	2.0	mVpp	Die	27, 40
Bright Field Global Non-Uniformity (Note 1)		−	2.0	5.0	% rms	Die	27, 40
Bright Field Global Peak to Peak Non-Uniformity (Note 1)	PRNU	−	5.0	15.0	% pp	Die	27, 40
Bright Field Center Non-Uniformity (Note 1)		−	1.0	2.0	% rms	Die	27, 40
Maximum Photoresponse Non-Linearity High Gain (4,000 to 20,000 electrons) High Gain (4,000 to 40,000 electrons) Low Gain (8,000 to 80,000 electrons)	 NL_HG1 NL_HG2 NL_LG1	 − − −	 2 3 6	 − − −	%	Design	
Maximum Gain Difference between Outputs (Note 2)	ΔG	−	10	−	%	Design	
Horizontal CCD Charge Capacity	H_{Ne}	−	90	−	ke^-	Design	
Vertical CCD Charge Capacity	V_{Ne}	−	60	−	ke^-	Design	
Photodiode Charge Capacity (Note 3)	P_{Ne}	−	44	−	ke^-	Die	27, 40
Floating Diffusion Capacity − High Gain	FNe_HG	40	−	−	ke^-	Die	27, 40
Floating Diffusion Capacity − Low Gain	FNe_LG	160	−	−	ke^-	Die	27, 40
Horizontal CCD Charge Transfer Efficiency	HCTE	0.999995	0.999999	−		Die	
Vertical CCD Charge Transfer Efficiency	VCTE	0.999995	0.999999	−		Die	
Photodiode Dark Current	I_{PD}	−	7	70	e/p/s	Die	40
Vertical CCD Dark Current	I_{VD}	−	140	400	e/p/s	Die	40
Image Lag	Lag	−	−	10	e^-	Design	
Anti-Blooming Factor	X_{AB}	1,000	−	−		Design	
Vertical Smear	Smr	−	−115	−	dB	Design	
Read Noise (Note 4) High Gain Low Gain	n_{e-T}	−	 12 45	−	e^- rms	Design	
Dynamic Range, Standard (Notes 4, 5)	DR	−	70.5	−	dB	Design	
Dynamic Range, Extended Linear Dynamic Range Mode (XLDR) (Notes 4, 5)	XLDR	−	82.5	−	dB	Design	
Output Amplifier DC Offset	V_{ODC}	−	9.0	−	V	Die	27, 40
Output Amplifier Bandwidth (Note 6)	f_{-3db}	−	250	−	MHz	Die	
Output Amplifier Impedance	R_{OUT}	−	127	−	Ω	Die	27, 40
Output Amplifier Sensitivity High Gain Low Gain	$\Delta V/\Delta N$	 − −	 33 8.7	 − −	$\mu V/e^-$	Design	

Table 6. PERFORMANCE SPECIFICATIONS (continued)

Description	Symbol	Min.	Nom.	Max.	Unit	Sampling Plan	Temperature Tested at (°C)
KAI−02170−ABA, KAI−02170−PBA AND KAI−02170−QBA CONFIGURATIONS							
Peak Quantum Efficiency	QE_{MAX}	−	52	−	%	Design	
Peak Quantum Efficiency Wavelength	λQE	−	500	−	nm	Design	
KAI−02170−FBA AND KAI−02170−QBA GEN2 COLOR CONFIGURATIONS							
Peak Quantum Efficiency Blue Green Red	QE_{MAX}	 − − −	 41 42 37	 − − −	%	Design	
Peak Quantum Efficiency Wavelength Blue Green Red	λQE	 − − −	 460 535 610	 − − −	nm	Design	
KAI−02170−CBA AND KAI−02170−PBA GEN1 COLOR CONFIGURATIONS (Note 7)							
Peak Quantum Efficiency Blue Green Red	QE_{MAX}	 − − −	 43 42 38	 − − −	%	Design	
Peak Quantum Efficiency Wavelength Blue Green Red	λQE	 − − −	 470 540 620	 − − −	nm	Design	

1. Per color.
2. Value is over the range of 10% to 90% of linear signal level saturation.
3. The operating value of the substrate voltage, V_{AB}, will be marked on the shipping container for each device. The value of V_{AB} is set such that the photodiode charge capacity is 440 mV. This value is determined while operating the device in the low gain mode. V_{AB} value assigned is valid for both modes; high gain or low gain.
4. At 40 MHz.
5. Uses 20LOG (P_{Ne} / n_{e-T}).
6. Assumes 5 pF load.
7. This color filter set configuration (Gen1) is not recommended for new designs.

Linear Signal Range

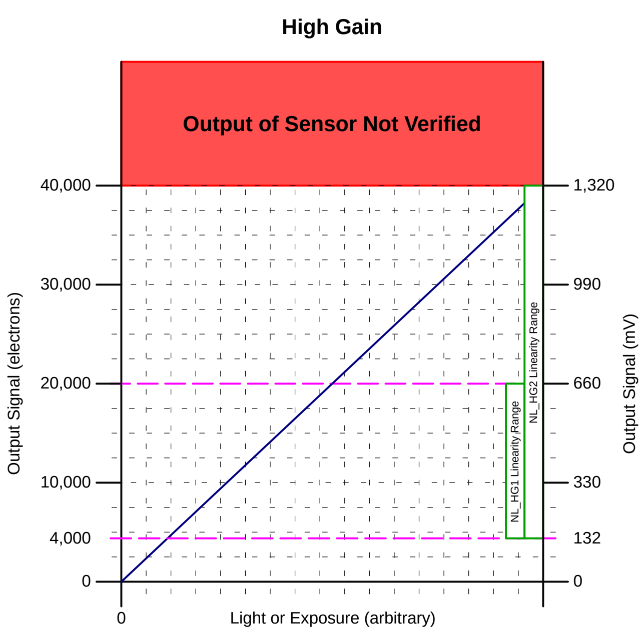


Figure 6. High Gain Linear Signal Range

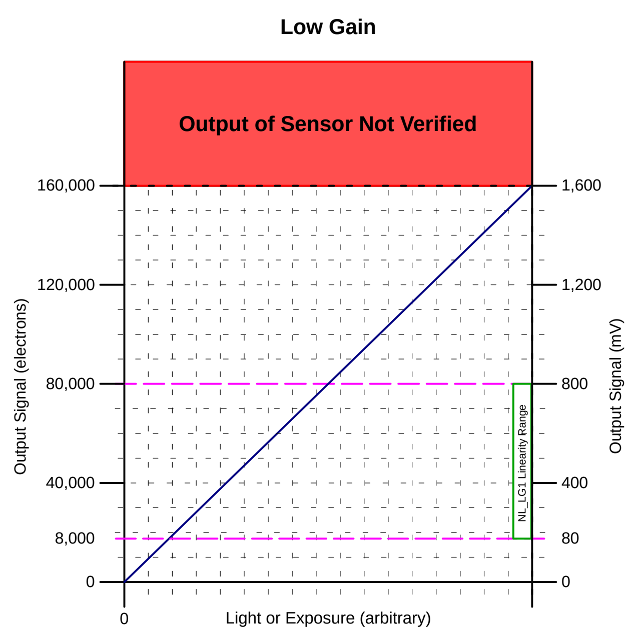


Figure 7. Low Gain Linear Signal Range

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

Monochrome with Microlens

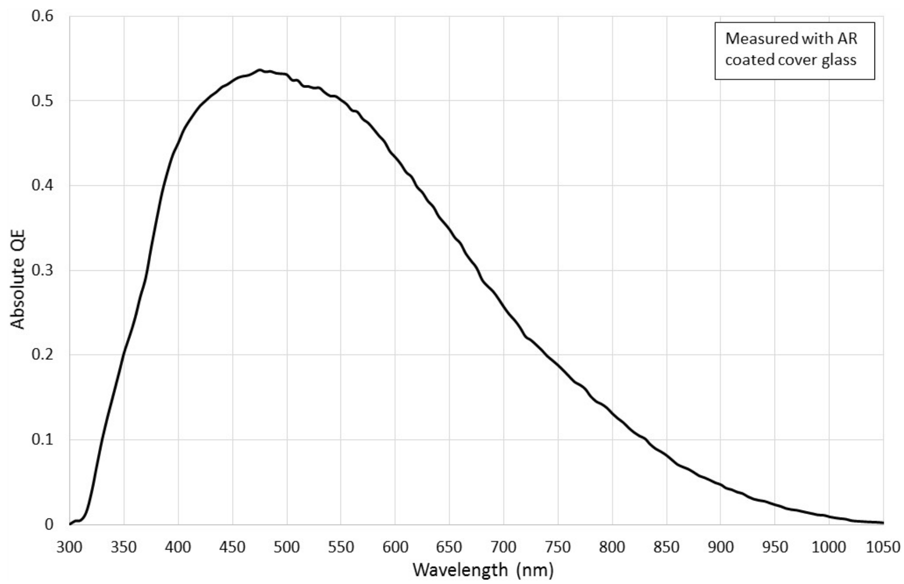


Figure 8. Monochrome with Microlens Quantum Efficiency

Color (Bayer RGB) with Microlens

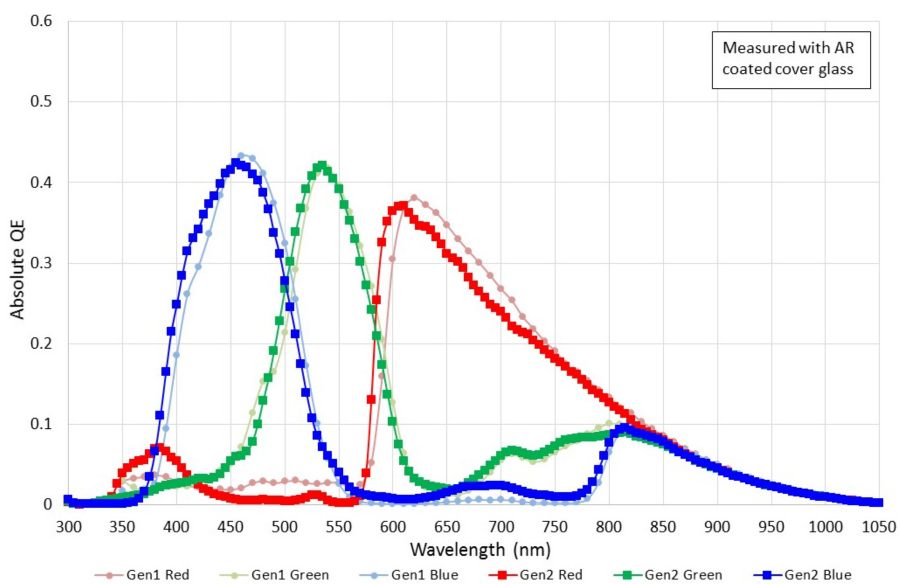


Figure 9. Color (Bayer RGB) with Microlens Quantum Efficiency

Color (TRUESENSE Sparse CFA) with Microlens

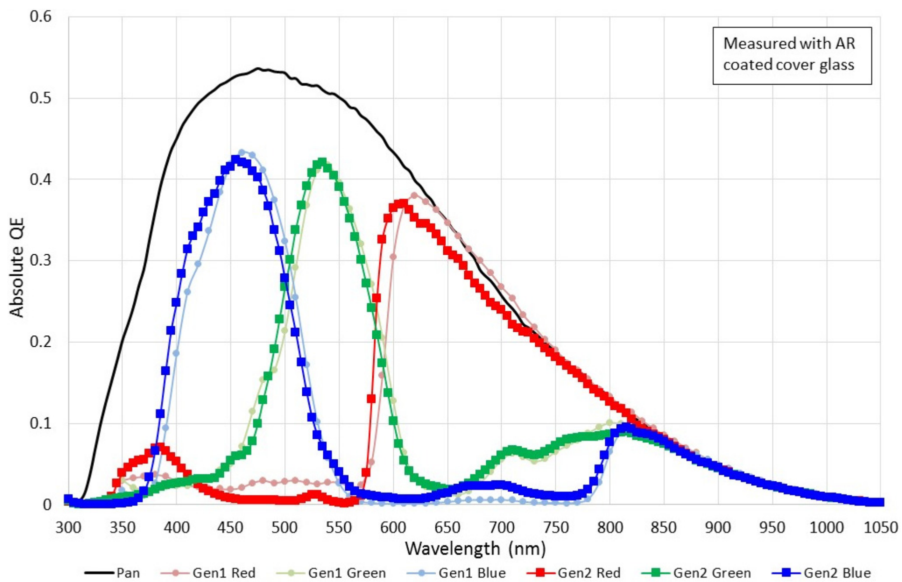


Figure 10. Color (TRUESENSE Sparse CFA) with Microlens Quantum Efficiency

Angular Quantum Efficiency

For the curves marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD. For the curves marked “Vertical”, the incident light angle is varied in a plane parallel to the VCCD.

Monochrome with Microlens

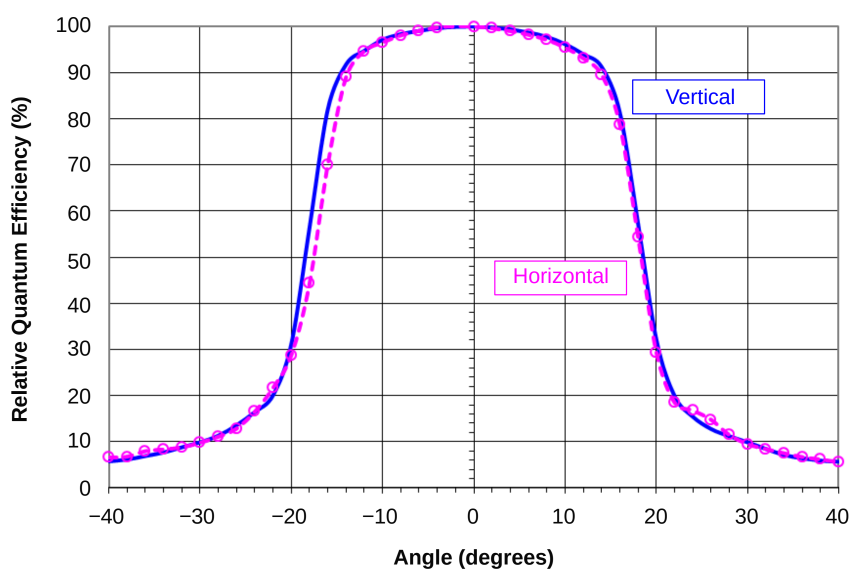


Figure 11. Monochrome with Microlens Angular Quantum Efficiency

Color (Bayer RGB) with Microlens

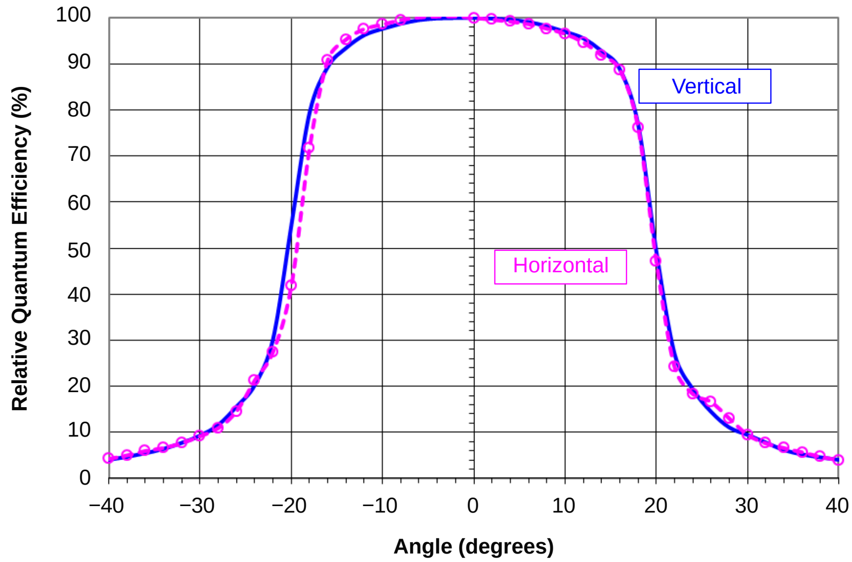


Figure 12. Color (Bayer RGB) with Microlens Angular Quantum Efficiency

Dark Current vs. Temperature

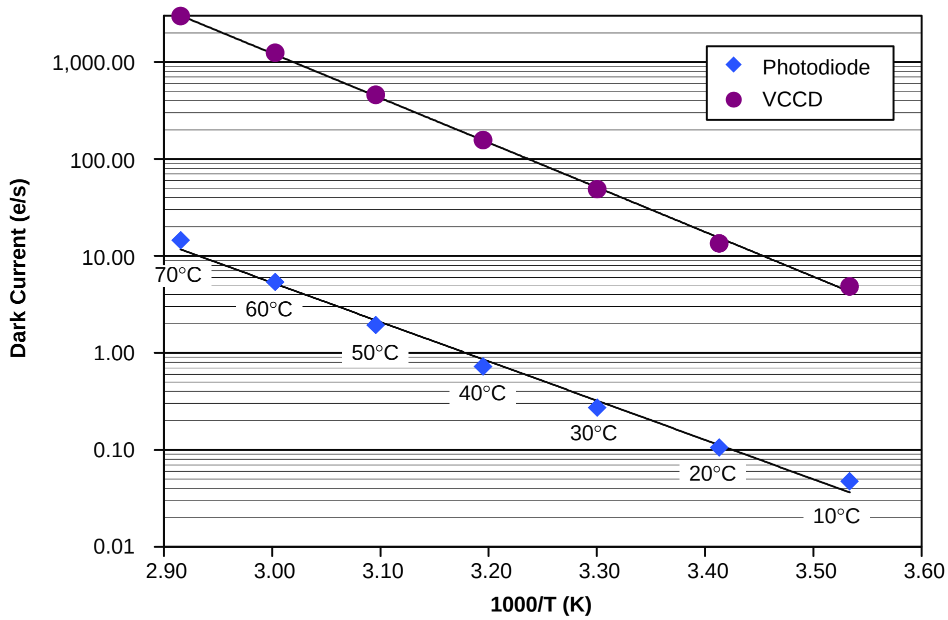


Figure 13. Dark Current vs. Temperature

Power-Estimated

Power-Estimated − Full Resolution

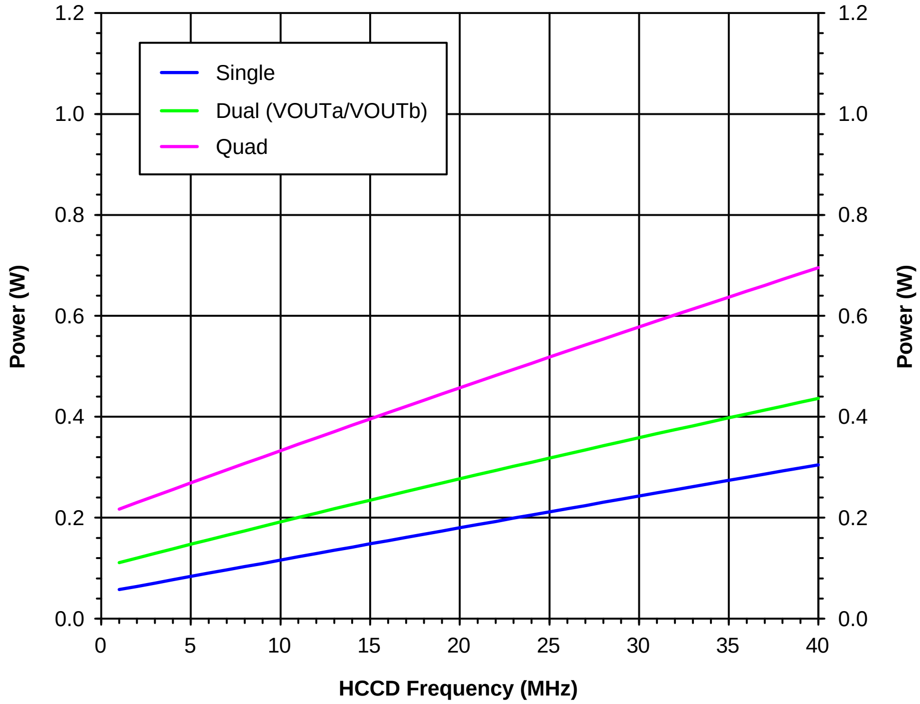


Figure 14. Power − Full Resolution

Power-Estimated − 1/4 Resolution − 2×2 Binning

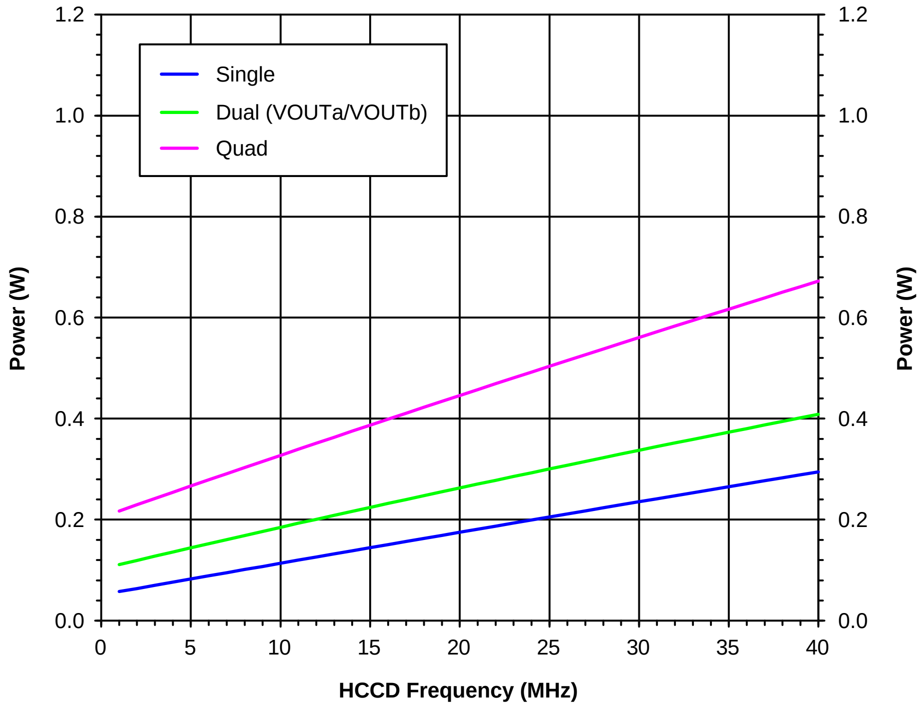


Figure 15. Power − 1/4 Resolution − Constant HCCD

Power-Estimated − 1/4 Resolution − 2×2 Binning using Variable HCCD XLDR

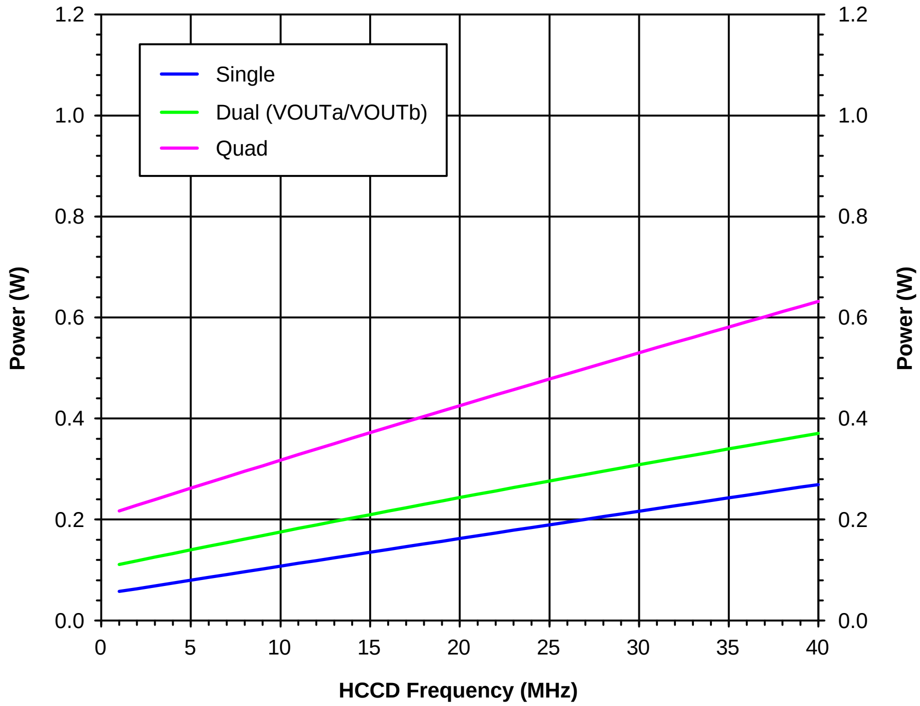


Figure 16. Power − 1/4 Resolution − Variable HCCD XLDR

Power-Estimated − 1/4 Resolution − 2×2 Binning using Constant HCCD XLDR

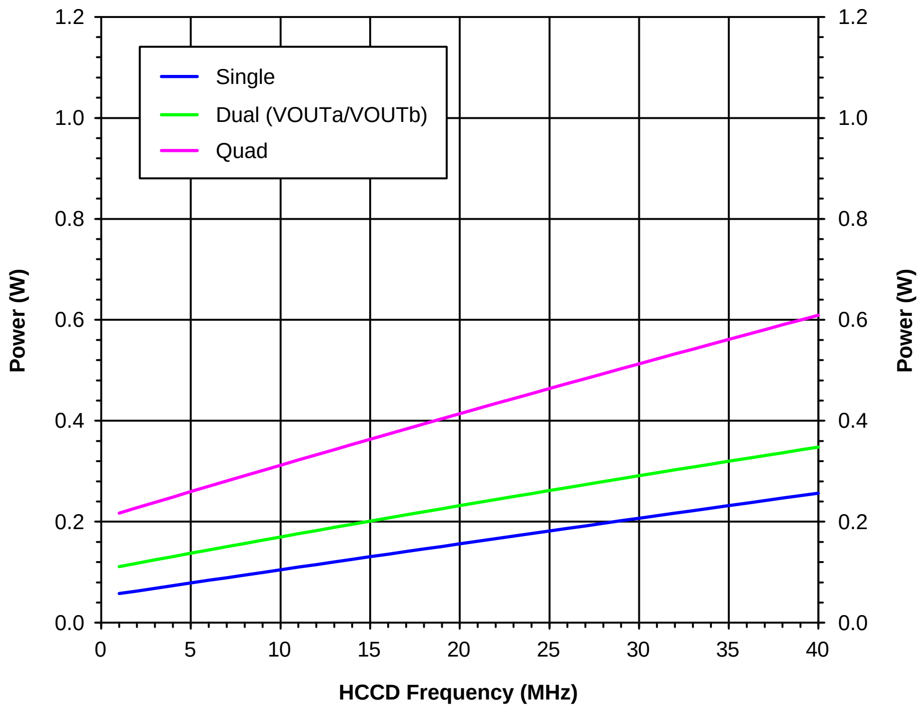


Figure 17. Power − 1/4 Resolution − Constant HCCD XLDR

Frame Rates

Frame Rates − Full Resolution

Frame rates are for low and high gain modes of operation.

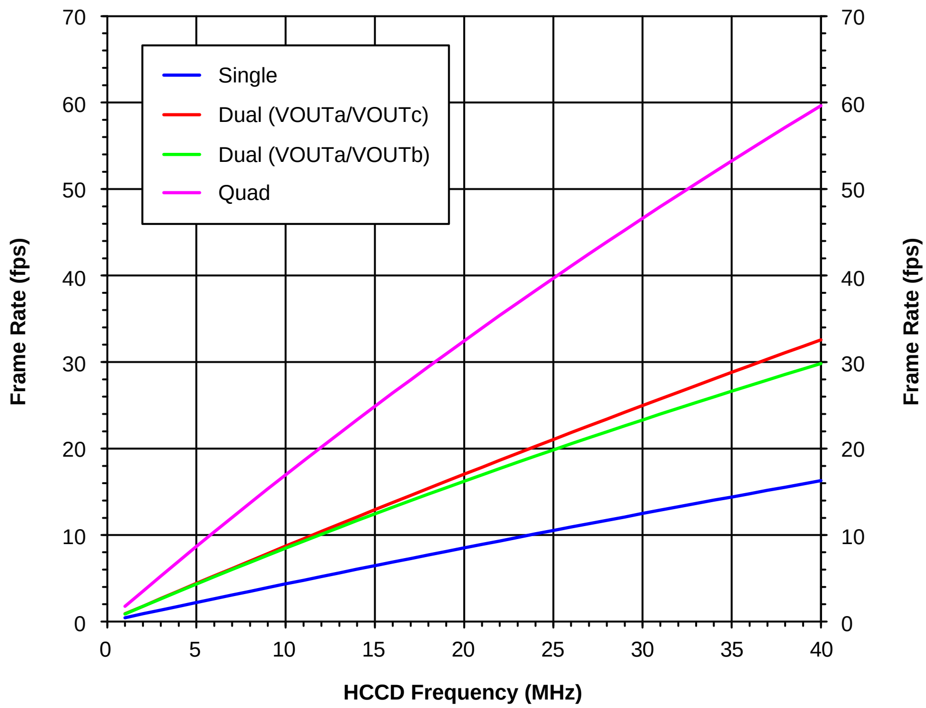


Figure 18. Frame Rates − Full Resolution

Frame Rates − 1/4 Resolution − 2×2 Binning

Frame rates are for low and high gain modes of operation.

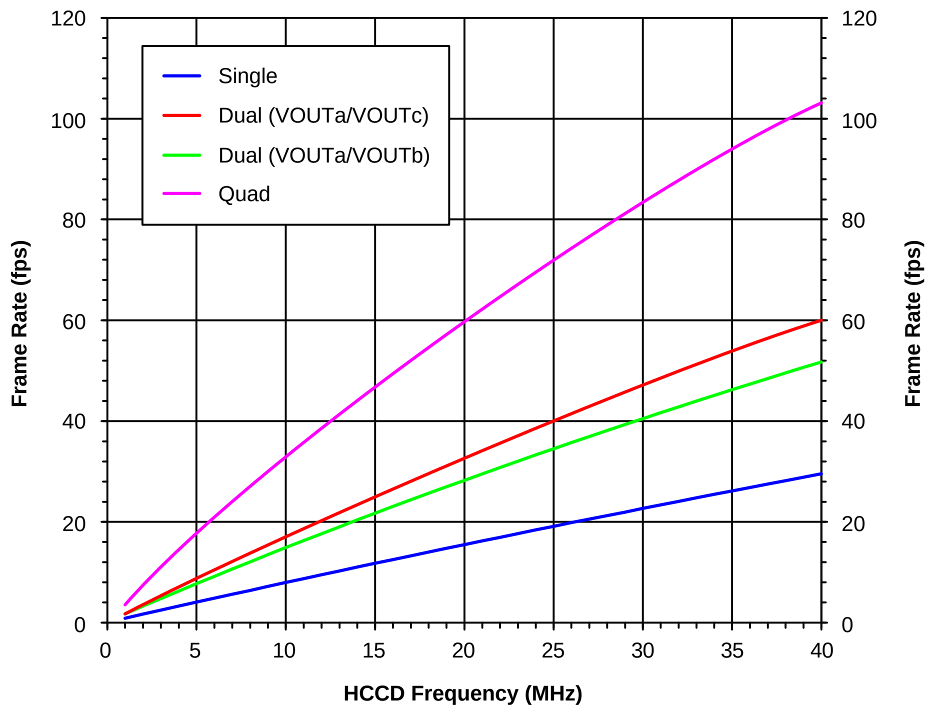


Figure 19. Frame Rates − 1/4 Resolution − Constant HCCD

Frame Rates − 1/4 Resolution − 2×2 Binning using Variable HCCD XLDR

Frame rates for variable HCCD modes of operation.

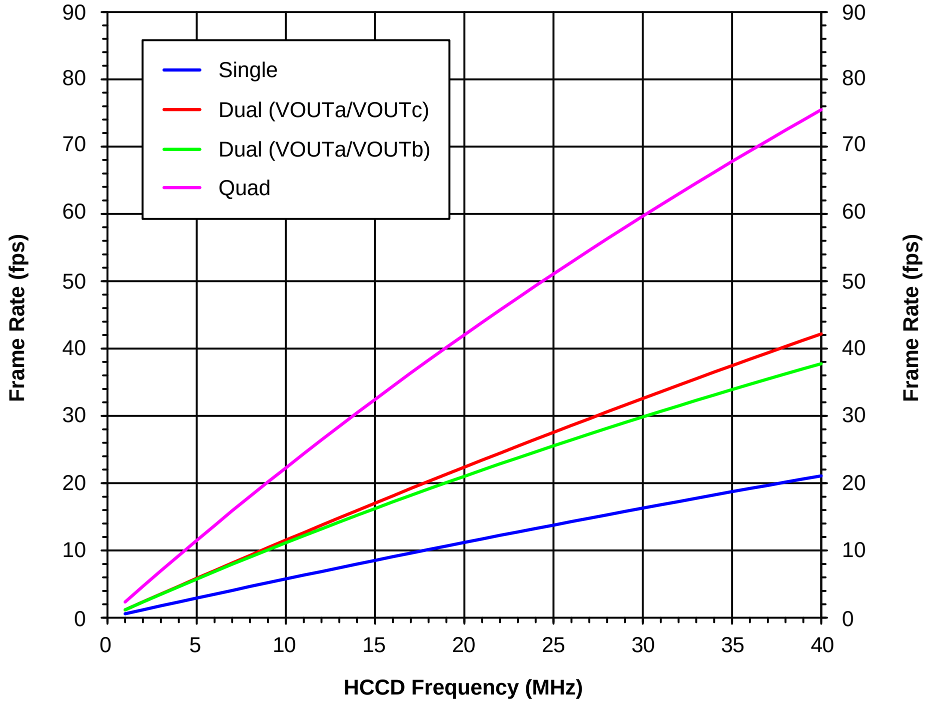


Figure 20. Frame Rates − 1/4 Resolution − Variable HCCD XLDR

Frame Rates − 1/4 Resolution − 2×2 Binning using Constant HCCD XLDR

Frame rates for a constant HCCD mode of operation.

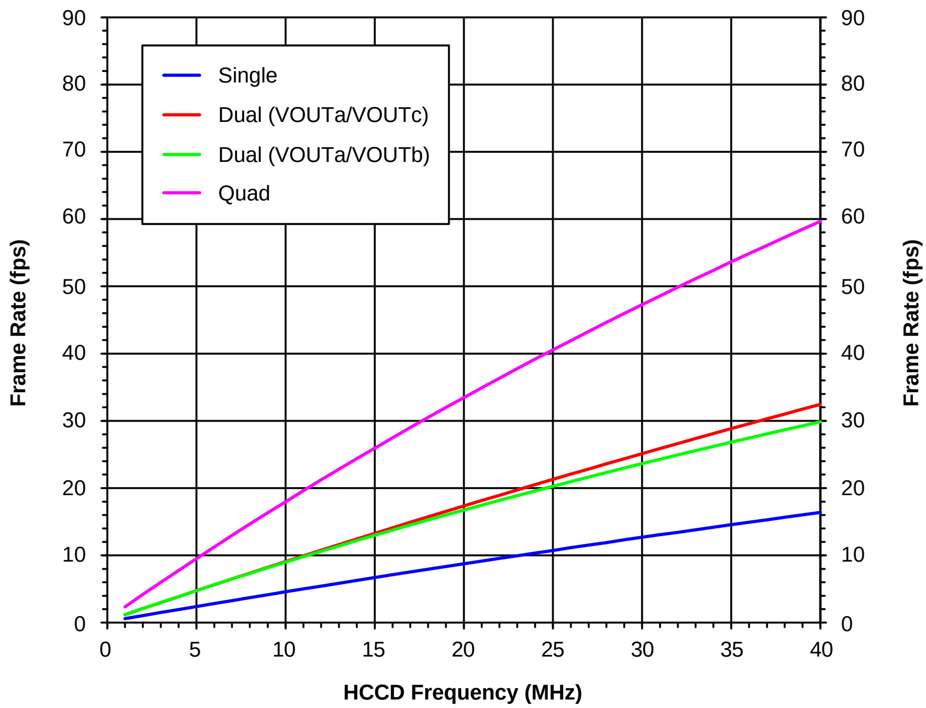


Figure 21. Frame Rates − 1/4 Resolution − Constant HCCD XLDR

DEFECT DEFINITIONS

Table 7. OPERATION CONDITIONS FOR DEFECT TESTING AT 40°C

Description	Condition	Notes
Operational Mode	One Output, Using VOUTa, Continuous Readout	
HCCD Clock Frequency	20 MHz	
Pixels per Line	1,992	
Lines per Frame	1,124	
Line Time	103.6 μs	
Frame Time	116.5 ms	
Photodiode Integration Time (PD_Tint)	PD_Tint = Frame Time = 116.5 ms, No Electronic Shutter Used	
Temperature	40°C	
Light Source	Continuous Red, Green and Blue LED Illumination	1
Operation	Nominal Operating Voltages and Timing	

1. For monochrome sensor, only the green LED is used.

Table 8. DEFECT DEFINITIONS FOR TESTING AT 40°C

Description	Definition	Standard Grade	Notes
Major Dark Field Defective Bright Pixel	Defect ≥ 40 mV	20	1
Major Bright Field Defective Pixel	−12% ≥ Defect ≥ 12%	20	1
Minor Dark Field Defective Bright Pixel	Defect ≥ 20 mV	200	
Cluster Defect	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defect horizontally.	8	2
Column Defect	A group of more than 10 contiguous major defective pixels along a single column.	0	2

1. For the color devices (KAI−02170−CBA and KAI−02170−PBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Table 9. OPERATION CONDITIONS FOR DEFECT TESTING AT 27°C

Description	Condition	Notes
Operational Mode	One Output, Using VOUTa, Continuous Readout	
HCCD Clock Frequency	20 MHz	
Pixels per Line	1,992	
Lines per Frame	1,124	
Line Time	103.6 μs	
Frame Time	116.5 ms	
Photodiode Integration Time (PD_Tint)	PD_Tint = Frame Time = 116.5 ms, No Electronic Shutter Used	
Temperature	27°C	
Light Source	Continuous Red, Green and Blue LED Illumination	1
Operation	Nominal Operating Voltages and Timing	

1. For monochrome sensor, only the green LED is used.

Table 10. DEFECT DEFINITIONS FOR TESTING AT 27°C

Description	Definition	Standard Grade	Notes
Major Dark Field Defective Bright Pixel	Defect ≥ 13 mV	20	1
Major Bright Field Defective Pixel	−12% ≥ Defect ≥ 12%	20	1
Cluster Defect	A group of 2 to 10 contiguous major defective pixels, but no more than 2 adjacent defect horizontally.	8	2
Column Defect	A group of more than 10 contiguous major defective pixels along a single column.	0	2

1. For the color devices (KAI−02170−CBA and KAI−02170−PBA), a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than two (2) good pixels in any direction (excluding single pixel defects).

Defect Map

The defect map supplied with each sensor is based upon testing at an ambient (27°C) temperature. Minor point defects are not included in the defect map. All defective pixels are reference to pixel 1, 1 in the defect maps. See Figure 22 for the location of pixel 1, 1.

TEST DEFINITIONS

Test Regions of Interest

Image Area ROI:	Pixel (1, 1) to Pixel (1936, 1096)
Active Area ROI:	Pixel (9, 9) to Pixel (1928, 1088)
Center ROI:	Pixel (919, 499) to Pixel (1018, 598)

Only the Active Area ROI pixels are used for performance and defect tests.

Overclocking

The test system timing is configured such that the sensor is overclocked in both the vertical and horizontal directions. See Figure 22 for a pictorial representation of the regions of interest.

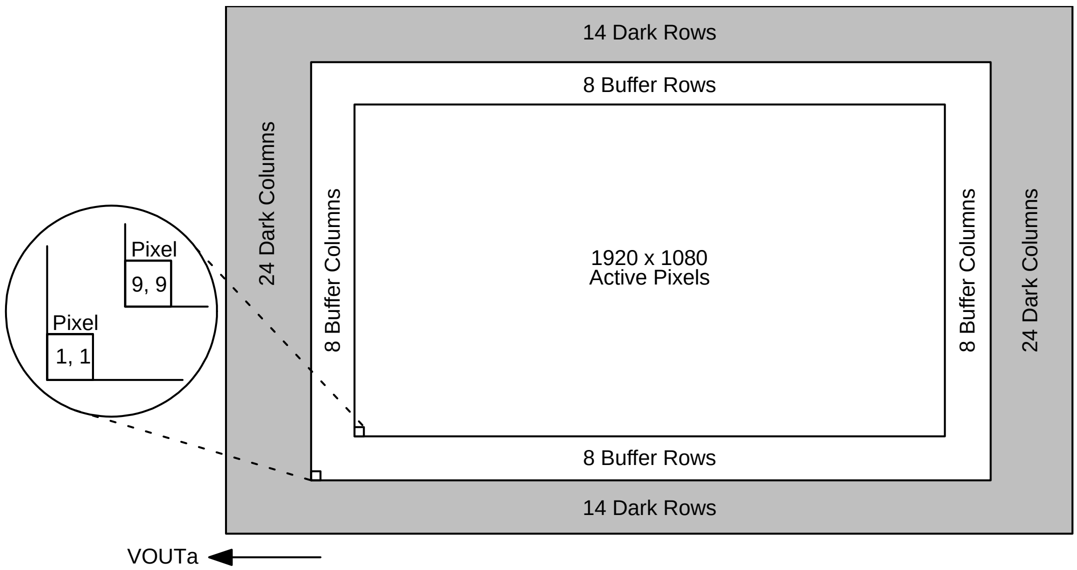


Figure 22. Regions of Interest

Tests

Dark Field Global Non-Uniformity

This test is performed under dark field conditions. The sensor is partitioned into 144 sub regions of interest, each of which is 120 by 120 pixels in size. The average signal level of each of the 144 sub regions of interest is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI[i]} = (\text{ROI Average in Counts} - \text{Horizontal Overclock Average in Counts}) \cdot \text{mV per Count}$$

Units : mVpp (millivolts Peak to Peak)

Where i = 1 to 144. During this calculation on the 144 sub regions of interest, the maximum and minimum signal levels are found. The dark field global uniformity is then calculated as the maximum signal found minus the minimum signal level found.

Global Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1,320 mV. Global non-uniformity is defined as:

$$\text{Global Non−Uniformity} = 100 \cdot \left(\frac{\text{Active Area Standard Deviation}}{\text{Active Area Signal}}\right)$$

Units : % rms

Active Area Signal = Active Area Average − Dark Column Average

Global Peak to Peak Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1,320 mV. The sensor is partitioned into 144 sub regions of interest, each of which is 120 by 120 pixels in size. The average signal level of each of the 144 sub regions of interest (ROI) is calculated. The signal level of each of the sub regions of interest is calculated using the following formula:

$$\text{Signal of ROI[i]} = (\text{ROI Average in Counts} - \text{Horizontal Overclock Average in Counts}) \cdot \text{mV per Count}$$

Where i = 1 to 144. During this calculation on the 144 sub regions of interest, the maximum and minimum signal levels are found. The global peak to peak uniformity is then calculated as:

$$\text{Global Uniformity} = 100 \cdot \left(\frac{\text{Max. Signal} - \text{Min. Signal}}{\text{Active Area Signal}}\right)$$

Units : % pp

Center Non-Uniformity

This test is performed with the imager illuminated to a level such that the output is at 70% of saturation (approximately 924 mV). Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1,320 mV. Defects are excluded for the calculation of this test. This test is performed on the center 100 by 100 pixels of the sensor. Center uniformity is defined as:

$$\text{Center ROI Uniformity} = 100 \cdot \left(\frac{\text{Center ROI Standard Deviation}}{\text{Center ROI Signal}}\right)$$

Units : % rms

Center ROI Signal = Center ROI Average − Dark Colum Average

Dark Field Defect Test

This test is performed under dark field conditions. The sensor is partitioned into 256 sub regions of interest, each of which is 120 by 120 pixels in size. In each region of interest, the median value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the defect threshold specified in the “Defect Definitions” section.

Bright Field Defect Test

This test is performed with the imager illuminated to a level such that the output is at approximately 924 mV. Prior to this test being performed the substrate voltage has been set such that the charge capacity of the sensor is 1,320 mV. The average signal level of all active pixels is found. The bright and dark thresholds are set as:

$$\text{Dark Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

$$\text{Bright Defect Threshold} = \text{Active Area Signal} \cdot \text{Threshold}$$

The sensor is then partitioned into 144 sub regions of interest, each of which is 120 by 120 pixels in size. In each region of interest, the average value of all pixels is found. For each region of interest, a pixel is marked defective if it is greater than or equal to the median value of that region of interest plus the bright threshold specified or if it is less than or equal to the median value of that region of interest minus the dark threshold specified.

Example for Major Bright Field Defective Pixels:

- Average value of all active pixels is found to be 924 mV.
- Dark defect threshold: 924 mV · 12 % = 111 mV.
- Bright defect threshold: 924 mV · 12 % = 111 mV.
- Region of interest #1 selected. This region of interest is pixels 9, 9 to pixels 128, 128.
  - Median of this region of interest is found to be 920 mV.
  - Any pixel in this region of interest that is ≤ (920 − 111 mV) 809 mV in intensity will be marked defective.
  - Any pixel in this region of interest that is ≥ (920 + 111 mV) 1,031 mV in intensity will be marked defective.
- All remaining 144 sub regions of interest are analyzed for defective pixels in the same manner.

OPERATION

Absolute Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce MTTF.

Table 11. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Unit	Notes
Operating Temperature	T_{OP}	−50	70	°C	1
Humidity	RH	5	90	%	2
Output Bias Current	I_{OUT}	−	60	mA	3
Off-Chip Load	C_L	−	10	pF	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Noise performance will degrade at higher temperatures.
2. T = 25°C. Excessive humidity will degrade MTTF.
3. Total for all outputs. Maximum current is −15 mA for each output. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

Table 12. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND

Description	Minimum	Maximum	Unit	Notes
VDDα, VOUTα	−0.4	17.5	V	1
RDα	−0.4	15.5	V	1
V1B, V1T	ESD − 0.4	ESD + 24.0	V	
V2B, V2T, V3B, V3T, V4B, V4T	ESD − 0.4	ESD + 14.0	V	
H1Sα, H1Bα, H2Sα, H2Bα, H2SLα, R1α, R2α, OGα	ESD − 0.4	ESD + 14.0	V	1
ESD	−10.0	0.0	V	
SUB	−0.4	40.0	V	2

1. α denotes a, b, c or d.
2. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*

KAI−02150 Compatibility

The KAI−02170 is pin-for-pin compatible with a camera designed for the KAI−02150 image sensor under the following conditions:

- To operate in accordance with a system designed for KAI−02150, the target substrate voltage should be set to be 2.0 V higher than the value recorded on the KAI−02170 shipping container. This setting will cause the charge capacity to be limited to 20 ke$^-$ (or 660 mV).
- On the KAI−02170, pins 17 (R2ab) and 51 (R2cd) should be left floating per the KAI−02150 Device Performance Specification.
- The KAI−02170 will operate in only the high gain mode (33 μV/e).
- All timing and voltages are taken from the KAI−02150 specification sheet.
- The number of horizontal and vertical CCD clock cycles is reduced as appropriate.

In addition, if the intent is to operate the KAI−02170 image sensor in a camera designed for the KAI−02150 sensor that has been modified to accept and process the full 40,000 e$^-$ (1,320 mV) output, the following changes to the RD bias must be made:

Table 13.

Pins	Names	KAI−02150	KAI−02170
10, 26, 44, 60	RDa, RDb, RDc, RDd	12.02 V per the Specification	Increase to 12.6 V

To make use of the low or dual gains modes the KAI−02170 voltages and timing specifications must be used.

Reset Pin, Low Gain (R2ab and R2cd)

The R2ab and R2bc (pins 17 and 51) each have an internal circuit to bias the pins to 4.3 V. This feature assures the device is set to operate in the high gain mode when pins 17 and 51 are not connected in the application to a clock driver (for KAI−02150 compatibility). Typical capacitor coupled drivers will not drive this structure.

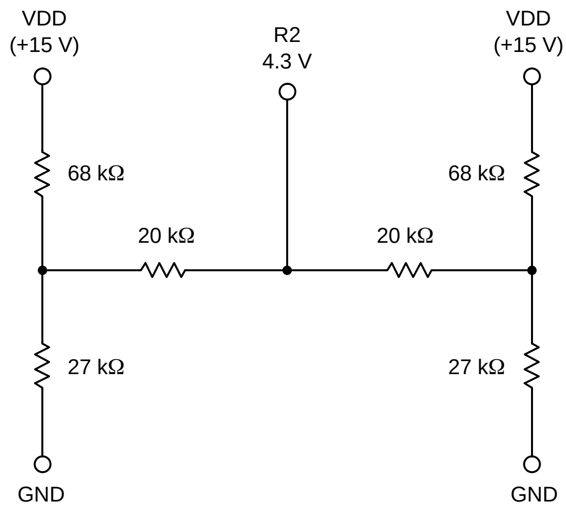
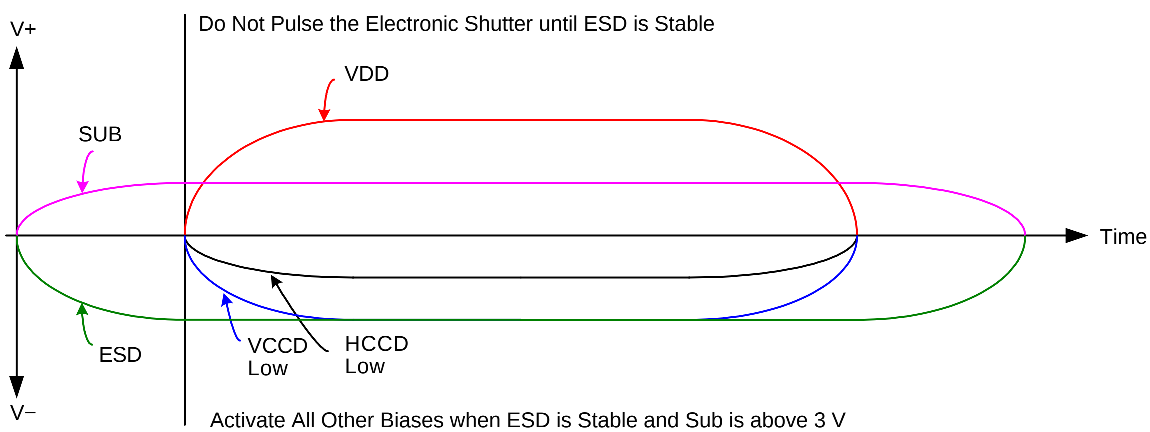


Figure 23. Equivalent Circuit for Reset Gate, Low Gain (R2ab and R2cd)

Power-Up and Power-Down Sequence

Adherence to the power-up and power-down sequence is critical. Failure to follow the proper power-up and power-down sequences may cause damage to the sensor.



Notes:
1. Activate all other biases when ESD is stable and SUB is above 3 V.
2. Do not pulse the electronic shutter until ESD is stable.
3. VDD cannot be +15 V when SUB is 0 V.
4. The image sensor can be protected from an accidental improper ESD voltage by current limiting the SUB current to less than 10 mA. SUB and VDD must always be greater than GND. ESD must always be less than GND. Placing diodes between SUB, VDD, ESD and ground will protect the sensor from accidental overshoots of SUB, VDD and ESD during power on and power off. See the figure below.

Figure 24. Power-Up and Power-Down Sequence

The VCCD clock waveform must not have a negative overshoot more than 0.4 V below the ESD voltage.

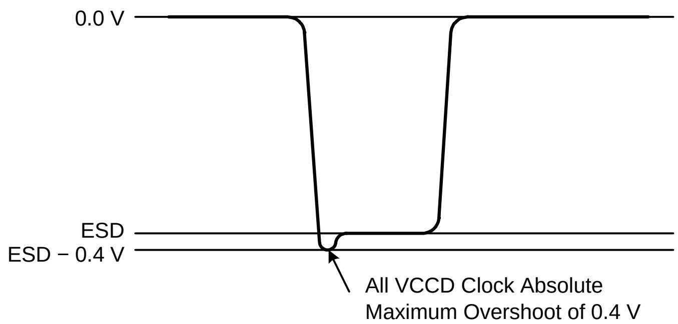


Figure 25. VCCD Clock Waveform

Example of external diode protection for SUB, VDD and ESD. α denotes a, b, c or d.

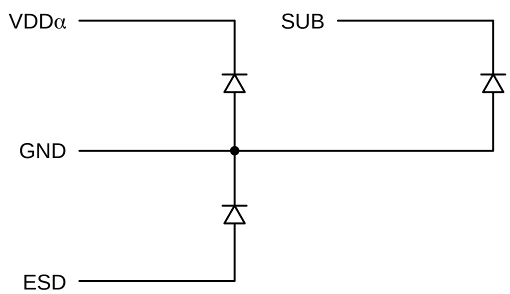


Figure 26. Example of External Diode Protection

DC Bias Operating Conditions

Table 14. DC BIAS OPERATING CONDITIONS

Description	Pins	Symbol	Min.	Nom.	Max.	Unit	Max. DC Current	Notes
Reset Drain	RDα	RD	12.4	12.6	12.8	V	10 μA	1, 9
Output Gate	OGα	OG	−2.2	−2.0	−1.8	V	10 μA	1
Output Amplifier Supply	VDDα	V_{DD}	14.5	15.0	15.5	V	11.0 mA	1, 2
Ground	GND	GND	0.0	0.0	0.0	V	−1.0 mA	
Substrate	SUB	V_{SUB}	5.0	V_{AB}	V_{DD}	V	50 μA	3, 8
ESD Protection Disable	ESD	ESD	−9.2	−9.0	Vx_L	V	50 μA	6, 7, 10
Output Bias Current	VOUTα	I_{OUT}	−3.0	−5.0	−10.0	mA	−	1, 4, 5

1. α denotes a, b, c or d.
2. The maximum DC current is for one output. $I_{DD} = I_{OUT} + I_{SS}$. See Figure 27.
3. The operating value of the substrate voltage, V_{AB}, will be marked on the shipping container for each device. The value of V_{AB} is set such that the photodiode charge capacity is the nominal P_{Ne} (see Specifications).
4. An output load sink must be applied to each VOUT pin to activate each output amplifier.
5. Nominal value required for 40 MHz operation per output. May be reduced for slower data rates and lower noise.
6. Adherence to the power-up and power-down sequence is critical. See Power Up and Power Down Sequence section.
7. ESD maximum value must be less than or equal to V1_L + 0.4 V and V2_L + 0.4 V.
8. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*
9. 12.0 V may be used if the total output signal desired is 20,000 e⁻ or less.
10. Where Vx_L is the level set for V1_L, V2_L, V3_L, or V4_L in the application.

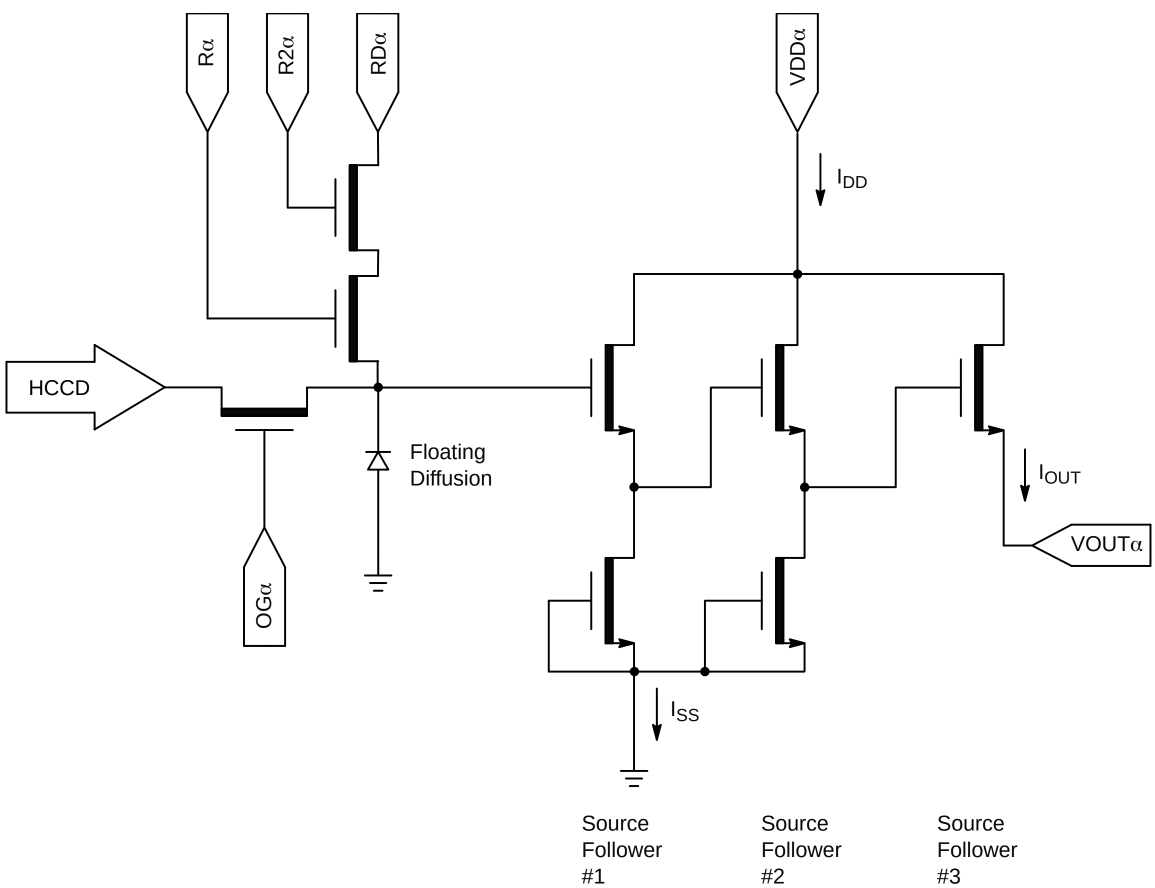


Figure 27. Output Amplifier

AC Operating Conditions

Table 15. CLOCK LEVELS

Description	Pins (Note 1)	Symbol	Level	Min.	Nom.	Max.	Unit
Vertical CCD Clock, Phase 1	V1B, V1T	V1_L	Low	−8.2	−8.0	−7.8	V
		V1_M	Mid	−0.2	0.0	0.2	
		V1_H	High	11.5	12.0	12.5	
Vertical CCD Clock, Phase 2	V2B, V2T	V2_L	Low	−8.2	−8.0	−7.8	V
		V2_H	High	−0.2	0.0	0.2	
Vertical CCD Clock, Phase 3	V3B, V3T	V3_L	Low	−8.2	−8.0	−7.8	V
		V3_H	High	−0.2	0.0	0.2	
Vertical CCD Clock, Phase 4	V4B, V4T	V4_L	Low	−8.2	−8.0	−7.8	V
		V4_H	High	−0.2	0.0	0.2	
Horizontal CCD Clock, Phase 1 Storage	H1Sα	H1S_L	Low	−5.2	−4.0	−3.8	V
		H1S_A	Amplitude (Note 3)	3.8	4.0	5.2	
Horizontal CCD Clock, Phase 1 Barrier	H1Bα	H1B_L	Low	−5.2	−4.0	−3.8	V
		H1B_A	Amplitude (Note 3)	3.8	4.0	5.2	
Horizontal CCD Clock, Phase 2 Storage	H2Sα	H2S_L	Low	−5.2	−4.0	−3.8	V
		H2S_A	Amplitude (Note 3)	3.8	4.0	5.2	
Horizontal CCD Clock, Phase 2 Barrier	H2Bα	H2B_L	Low	−5.2	−4.0	−3.8	V
		H2B_A	Amplitude (Note 3)	3.8	4.0	5.2	
Horizontal CCD Clock, Last Phase (Note 2)	H2SLα	H2SL_L	Low	−5.2	−5.0	−4.8	V
		H2SL_A	Amplitude (Note 3)	4.8	5.0	5.2	
Reset Gate	R1α	R_L	Low	−3.2	−3.0	−2.8	V
		R_A	Amplitude	6.0	−	6.4	
Reset Gate	R2α	R_L	Low	−2.0	−1.8	−1.6	V
		R_A	Amplitude	6.0	−	6.4	
Electronic Shutter (Note 4)	SUB	VES	High	29.0	30.0	40.0	V

1. α denotes a, b, c or d.
2. Use separate clock driver for improved speed performance.
3. The horizontal clock amplitude should be set such that the high level reaches 0.0 V. Examples:
   a. If the minimum horizontal low voltage of −5.2 V is used, then a 5.2 V amplitude clock is required for a clock swing of −5.2 V to 0.0 V.
   b. If the maximum horizontal low voltage of −3.8 V is used, then a 3.8 V amplitude clock is required for a clock swing of −3.8 V to 0.0 V.
4. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*

The figure below shows the DC bias (VSUB) and AC clock (VES) applied to the SUB pin. Both the DC bias and AC clock are referenced to ground.

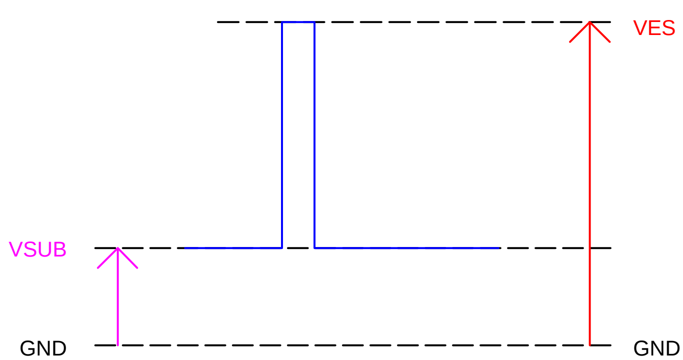


Figure 28. DC Bias and AC Clock Applied to the SUB Pin

Capacitance

Table 16. CAPACITANCE

	V1B	V2B	V3B	V4B	V1T	V2T	V3T	V4T	GND	All Pins	Unit
V1B	X	2.2	1.5	1.8	0.8	0.7	0.8	0.5	3.2	11.6	nF
V2B	X	X	2.8	1.3	0.7	0.4	0.5	0.4	0.9	9.8	nF
V3B	X	X	X	2.5	0.8	0.7	0.8	0.5	1.1	10.9	nF
V4B	X	X	X	X	0.7	0.5	0.7	0.4	3.0	10.0	nF
V1T	X	X	X	X	X	1.8	1.5	2.2	3.2	11.3	nF
V2T	X	X	X	X	X	X	2.1	0.8	2.9	9.9	nF
V3T	X	X	X	X	X	X	X	2.5	1.5	11.1	nF
V4T	X	X	X	X	X	X	X	X	0.7	9.6	nF
VSUB	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	1.5	1.5	nF

	H2S	H1B	H2B	GND	All Pins	Unit
H1S	15	25	15	65	120	pF
H2S	X	16	14	94	123	pF
H1B	X	X	4	105	108	pF
H2B	X	X	X	98	98	pF

1. Tables show typical cross capacitance between pins of the device.
2. Capacitance is total for all like pins.
3. Capacitance values are estimated.

Device Identification

The device identification pin (DevID) may be used to determine which Truesense Imaging 7.4 micron pixel interline CCD sensor is being used.

Table 17. DEVICE IDENTIFICATION

Description	Pins	Symbol	Min.	Nom.	Max.	Unit	Max. DC Current	Notes
Device Identification	DevID	DevID	14,000	16,000	18,000	Ω	50 μA	1, 2, 3

1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R_DeviceID resistor.

Recommended Circuit

Note that V1 must be a different value than V2.

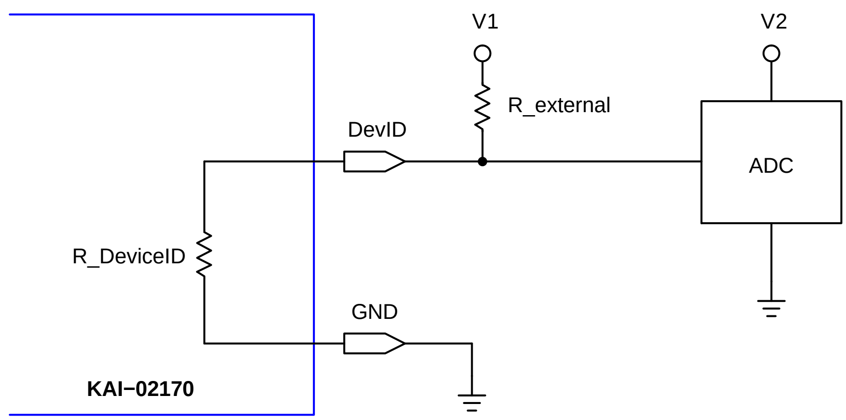


Figure 29. Device Identification Recommended Circuit

TIMING

Requirements and Characteristics

Table 18. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Min.	Nom.	Max.	Unit	Notes
Photodiode Transfer	t_{PD}	1.0	−	−	μs	
VCCD Leading Pedestal	t_{3P}	4.0	−	−	μs	
VCCD Trailing Pedestal	t_{3D}	4.0	−	−	μs	
VCCD Transfer Delay	t_D	1.0	−	−	μs	
VCCD Transfer	t_V	1.2	−	−	μs	
VCCD Clock Cross-Over	V_{VCR}	75	−	100	%	1
VCCD Rise, Fall Times	t_{VR}, t_{VF}	5	−	10	%	1, 2
HCCD Delay	t_{HS}	2.0	−	−	μs	
HCCD Transfer	t_e	25.0	−	−	ns	
Shutter Transfer	t_{SUB}	1.0	−	−	μs	
Shutter Delay	t_{HD}	1.0	−	−	μs	
Reset Pulse	t_R	2.5	−	−	ns	
Reset − Video Delay	t_{RV}	−	2.2	−	ns	
H2SL − Video Delay	t_{HV}	−	3.1	−	ns	
Line Time	t_{LINE}	29.8	−	−	μs	Dual HCCD Readout
		54.6	−	−	μs	Single HCCD Readout
Frame Time	t_{FRAME}	16.8	−	−	ms	Quad HCCD Readout
		33.5	−	−	ms	Dual HCCD Readout
		61.4	−	−	ms	Single HCCD Readout
Line Time (XLDR Bin 2×2)	t_{LINE}	59.6	−	−	μs	Dual HCCD Readout
		109.2	−	−	μs	Single HCCD Readout
Frame Time (XLDR Bin 2×2) Constant HCCD Timing	t_{FRAME}	16.8	−	−	ms	Quad HCCD Readout
		33.5	−	−	ms	Dual HCCD Readout
		61.4	−	−	ms	Single HCCD Readout
Frame Time (XLDR Bin 2×2) Variable HCCD Timing	t_{FRAME}	13.3	−	−	ms	Quad HCCD Readout
		26.5	−	−	ms	Dual HCCD Readout
		47.4	−	−	ms	Single HCCD Readout

1. Refer to Figure 47: VCCD Clock Rise Time, Fall Time, and Edge Alignment.
2. Relative to the VCCD Transfer pulse width, t_V.

Timing Flow Charts

In the timing flow charts the number of HCCD clock cycles per row, NH, and the number of VCCD clock cycles per frame, NV, are shown in the following table.

Table 19. VALUES FOR NH AND NV WHEN OPERATING THE SENSOR IN THE VARIOUS MODES OF RESOLUTION

	Full Resolution		1/4 Resolution		XLDR	
	NV	NH	NV	NH	NV	NH
Quad	562	1004	281	502	281	502
Dual VOUTa, VOUTc	562	2008	281	1008	281	1004
Dual VOUTa, VOUTb	1124	1004	562	502	562	502
Single VOUTa	1124	2008	562	1004	562	1004

1. The time to read out one line t_{LINE} = Line Timing + NH / (Pixel Frequency).
2. The time to read out one frame $t_{FRAME} = NV \cdot t_{LINE}$ + Frame Timing.
3. Line Timing: See Table 21: Line Timing.
4. Frame Timing: See Table 20: Frame Timing.
5. XLDR: eXtended Linear Dynamic Range.

No Electronic Shutter

In this case the photodiode exposure time is equal to the time to read out an image. This flow chart applies to both full and 1/4 resolution modes.

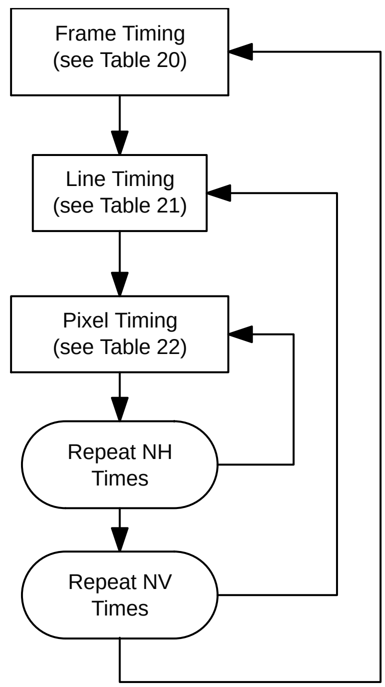
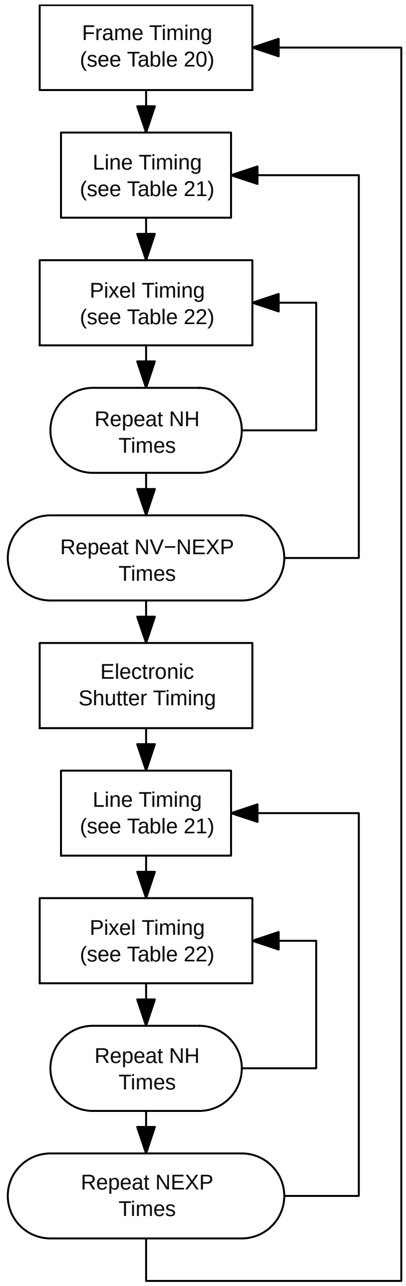


Figure 30. Timing Flow when Electronic Shutter is Not Used

Using the Electronic Shutter

This flow chart applies to both the full and 1/4 resolution modes. The exposure time begins on the falling edge of the electronic shutter pulse on the SUB pin. The exposure time ends on the falling edge of the photodiode transfer (t_{PD}) of the V1T and V1B pins. The electronic shutter timing is shown in Figure 38.



NOTE: NEXP: Exposure time in increments of number of lines.

Figure 31. Timing Flow Chart using the Electronic Shutter for Exposure Control

Timing Tables

Frame Timing

This timing table is for transferring charge from the photodiodes to the VCCD. See Figure 32 and Figure 33 for frame timing diagrams.

Table 20. FRAME TIMING

Device Pin	Full Resolution, High Gain or Low Gain				1/4 Resolution, High Gain or Low Gain				1/4 Resolution XLDR			
	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa
V1T	F1T		F1B		F1T		F1B		F1T		F1B	
V2T	F2T		F4B		F2T		F4B		F2T		F4B	
V3T	F3T		F3B		F3T		F3B		F3T		F3B	
V4T	F4T		F2B		F4T		F2B		F4T		F2B	
V1B	F1B				F1B				F1B			
V2B	F2B				F2B				F2B			
V3B	F3B				F3B				F3B			
V4B	F4B				F4B				F4B			
H1Sa	P1				P1Q				P1XL			
H1Ba	P1				P1Q				P1XL			
H2Sa	P2				P2Q				P2XL			
H2Ba	P2				P2Q				P2XL			
Ra	RHG/RLG				RHGQ/RLGQ				RXL			
H1Sb	P1				P1Q				P1XL			
H1Bb	P1	P2	P1	P2	P1Q	P2Q	P1Q	P2Q	P1XL	P2XL	P1XL	P2XL
H2Sb	P2				P2Q				P2XL			
H2Bb	P2	P1	P2	P1	P2Q	P1Q	P2Q	P1Q	P2XL	P1XL	P2XL	P1XL
Rb	RHG/ RLG	(Note 1)	RHG/ RLG	(Note 1)	RHGQ/ RLGQ	(Note 1)	RHGQ/ RLGQ	(Note 1)	RXL	(Note 1)	RXL	(Note 1)
R2ab	R2HG/R2LG				R2HGQ/R2LGQ				R2XL			
H1Sc	P1		(Note 1)		P1Q		(Note 1)		P1XL		(Note 1)	
H1Bc	P1		(Note 1)		P1Q		(Note 1)		P1XL		(Note 1)	
H2Sc	P2		(Note 1)		P2Q		(Note 1)		P2XL		(Note 1)	
H2Bc	P2		(Note 1)		P2Q		(Note 1)		P2XL		(Note 1)	
Rc	RHG/RLG		(Note 1)		RHGQ/RLGQ		(Note 1)		RXL		(Note 1)	
H1Sd	P1		(Note 1)		P1Q		(Note 1)		P1XL		(Note 1)	
H1Bd	P1	P2	(Note 1)		P1Q	P2Q	(Note 1)		P1XL	P2XL	(Note 1)	
H2Sd	P2		(Note 1)		P2Q		(Note 1)		P2XL		(Note 1)	
H2Bd	P2	P1	(Note 1)		P2Q	P1Q	(Note 1)		P2XL	P1XL	(Note 1)	
Rd	RHG/ RLG	(Note 1)	(Note 1)		RHGQ/ RLGQ	(Note 1)	(Note 1)		RXL	(Note 1)	(Note 1)	
R2cd	R2HG/R2LG		(Note 1)		R2HGQ/R2LGQ		(Note 1)		R2XL		(Note 1)	
SHP (Note 2)	SHP1				SHPQ				(Note 4)			
SHD (Note 2)	SHD1				SHDQ				(Note 5)			

1. This clock should be held at its high level voltage (0 V) or held at +5.0 V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products.
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor.
3. This note intentionally left empty.
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal.
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal.

Line Timing

This timing is for transferring one line of charge from the VCCD to the HCCD. See Figure 34, Figure 35, Figure 36 and Figure 37 for line timing diagrams.

Table 21. LINE TIMING

Device Pin	Full Resolution, High Gain or Low Gain				1/4 Resolution, High Gain or Low Gain				1/4 Resolution XLDR			
	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa
V1T	L1T		L1B		2× L1T		2× L1B		2× L1T		2× L1B	
V2T	L2T		L4B		2× L2T		2× L4B		2× L2T		2× L4B	
V3T	L3T		L3B		2× L3T		2× L3B		2× L3T		2× L3B	
V4T	L4T		L2B		2× L4T		2× L2B		2× L4T		2× L2B	
V1B	L1B				2× L1B				2× L1B			
V2B	L2B				2× L2B				2× L2B			
V3B	L3B				2× L3B				2× L3B			
V4B	L4B				2× L4B				2× L4B			
H1Sa	P1L				P1LQ				P1XL			
H1Ba	P1L				P1LQ				P1XL			
H2Sa	P2L				P2LQ				P2XL			
H2Ba	P2L				P2LQ				P2XL			
Ra	RHG/RLG				RHGQ/RLGQ				RXL			
H1Sb	P1L				P1LQ				P1XL			
H1Bb	P1L	P2L	P1L	P2L	P1LQ	P2LQ	P1LQ	P2LQ	P1XL	P2XL	P1XL	P2XL
H2Sb	P2L				P2LQ				P2XL			
H2Bb	P2L	P1L	P2L	P1L	P2LQ	P1LQ	P2LQ	P1LQ	P2XL	P1XL	P2XL	P1XL
Rb	RHG/ RLG	(Note 1)	RHG/ RLG	(Note 1)	RHGQ/ RLGQ	(Note 1)	RHGQ/ RLGQ	(Note 1)	RXL	(Note 1)	RXL	(Note 1)
R2ab	R2HG/R2LG				R2HGQ/R2LGQ				R2XL			
H1Sc	P1L		(Note 1)		P1LQ		(Note 1)		P1XL		(Note 1)	
H1Bc	P1L		(Note 1)		P1LQ		(Note 1)		P1XL		(Note 1)	
H2Sc	P2L		(Note 1)		P2LQ		(Note 1)		P2XL		(Note 1)	
H2Bc	P2L		(Note 1)		P2LQ		(Note 1)		P2XL		(Note 1)	
Rc	RHG/RLG		(Note 1)		RHGQ/RLGQ		(Note 1)		RXL		(Note 1)	
H1Sd	P1L		(Note 1)		P1LQ		(Note 1)		P1XL		(Note 1)	
H1Bd	P1L	P2L	(Note 1)		P1LQ	P2LQ	(Note 1)		P1XL	P2XL	(Note 1)	
H2Sd	P2L		(Note 1)		P2LQ		(Note 1)		P2XL		(Note 1)	
H2Bd	P2L	P1L	(Note 1)		P2LQ	P1LQ	(Note 1)		P2XL	P1XL	(Note 1)	
Rd	RHG/ RLG	(Note 1)	(Note 1)		RHGQ/ RLGQ	(Note 1)	(Note 1)		RXL	(Note 1)	(Note 1)	
R2cd	R2HG/R2LG		(Note 1)		R2HGQ/R2LGQ		(Note 1)		R2XL		(Note 1)	
SHP (Note 2)	SHP1				SHPQ				(Note 4)			
SHD (Note 2)	SHD1				SHDQ				(Note 5)			

1. This clock should be held at its high level voltage (0 V) or held at +5.0 V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products.
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor.
3. The notation 2× L1B means repeat the L1B timing twice for every line. This sums two rows into the HCCD.
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal.
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal.

Pixel Timing

This timing is for transferring one pixel from the HCCD to the output amplifier.

Table 22. PIXEL TIMING

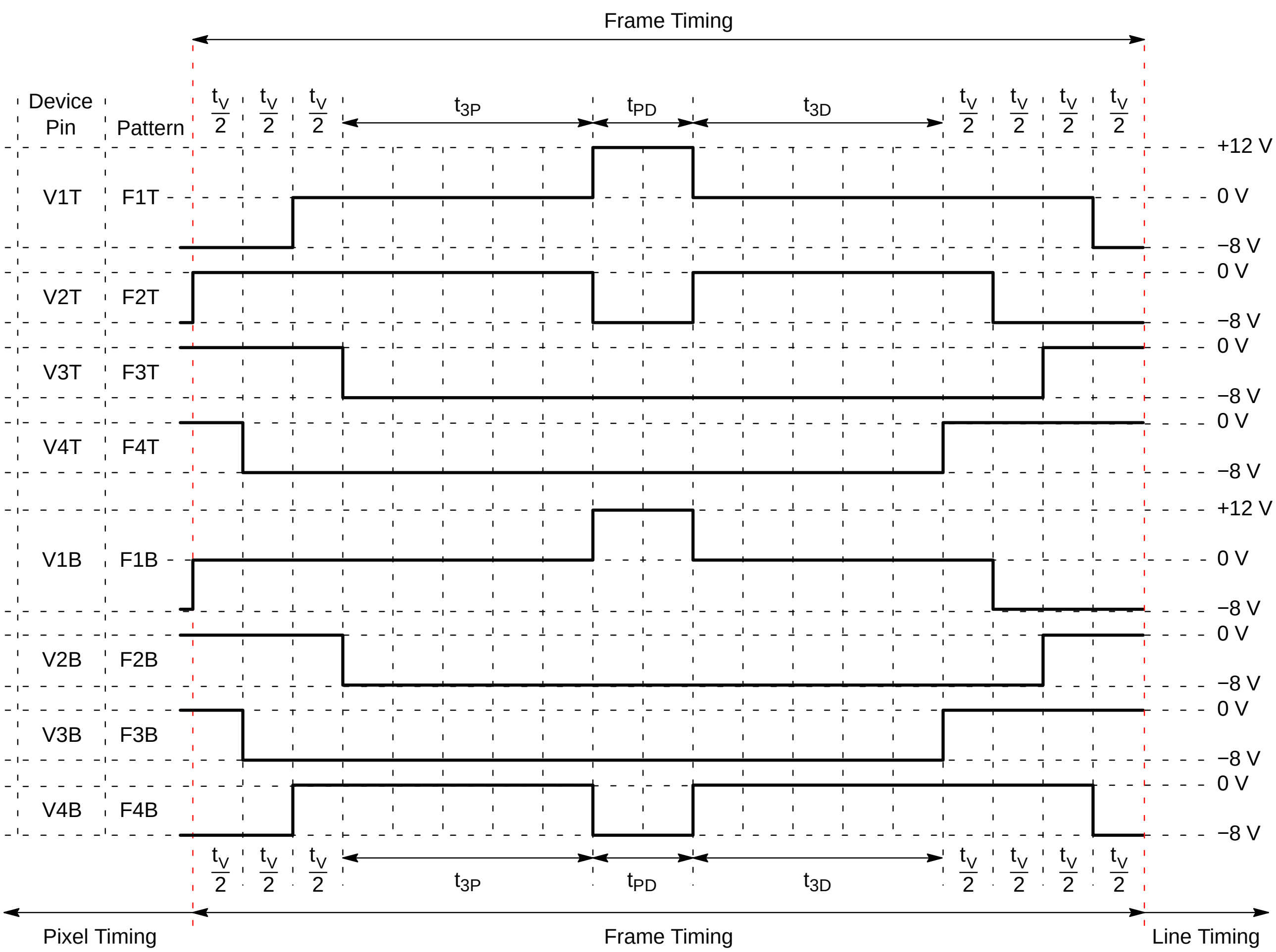
Device Pin	Full Resolution, High Gain or Low Gain				1/4 Resolution, High Gain or Low Gain				1/4 Resolution XLDR			
	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa	Quad	Dual VOUTa VOUTc	Dual VOUTa VOUTb	Single VOUTa
V1T	−9 V				−9 V				−9 V			
V2T	−9 V				−9 V				−9 V			
V3T	0 V				0 V				0 V			
V4T	0 V				0 V				0 V			
V1B	−9 V				−9 V				−9 V			
V2B	0 V				0 V				0 V			
V3B	0 V				0 V				0 V			
V4B	−9 V				−9 V				−9 V			
H1Sa	P1				P1Q				P1XL			
H1Ba	P1				P1Q				P1XL			
H2Sa	P2				P2Q				P2XL			
H2Ba	P2				P2Q				P2XL			
Ra	RHG/RLG				RHGQ/RLGQ				RXL			
H1Sb	P1				P1Q				P1XL			
H1Bb	P1	P2	P1	P2	P1Q	P2Q	P1Q	P2Q	P1XL	P2XL	P1XL	P2XL
H2Sb	P2				P2Q				P2XL			
H2Bb	P2	P1	P2	P1	P2Q	P1Q	P2Q	P1Q	P2XL	P1XL	P2XL	P1XL
Rb	RHG/ RLG	(Note 1)	RHG/ RLG	(Note 1)	RHGQ/ RLGQ	(Note 1)	RHGQ/ RLGQ	(Note 1)	RXL	(Note 1)	RXL	(Note 1)
R2ab	R2HG/R2LG				R2HGQ/R2LGQ				R2XL			
H1Sc	P1		(Note 1)		P1Q		(Note 1)		P1XL		(Note 1)	
H1Bc	P1		(Note 1)		P1Q		(Note 1)		P1XL		(Note 1)	
H2Sc	P2		(Note 1)		P2Q		(Note 1)		P2XL		(Note 1)	
H2Bc	P2		(Note 1)		P2Q		(Note 1)		P2XL		(Note 1)	
Rc	RHG/RLG		(Note 1)		RHGQ/RLGQ		(Note 1)		RXL		(Note 1)	
H1Sd	P1		(Note 1)		P1Q		(Note 1)		P1XL		(Note 1)	
H1Bd	P1	P2	(Note 1)		P1Q	P2Q	(Note 1)		P1XL	P2XL	(Note 1)	
H2Sd	P2		(Note 1)		P2Q		(Note 1)		P2XL		(Note 1)	
H2Bd	P2	P1	(Note 1)		P2Q	P1Q	(Note 1)		P2XL	P1XL	(Note 1)	
Rd	RHG/ RLG	(Note 1)	(Note 1)		RHGQ/ RLGQ	(Note 1)	(Note 1)		RXL	(Note 1)	(Note 1)	
R2cd	R2HG/R2LG		(Note 1)		R2HGQ/R2LGQ		(Note 1)		R2XL		(Note 1)	
SHP (Note 2)	SHP1				SHPQ				(Note 4)			
SHD (Note 2)	SHD1				SHDQ				(Note 5)			

1. This clock should be held at its high level voltage (0 V) or held at +5.0 V for compatibility with TRUESENSE 5.5 micron Interline Transfer CCD family of products.
2. SHP and SHD are the sample clocks for the analog front end (AFE) signal processor.
3. This note intentionally left empty.
4. Use SHPLG for the AFE processing the low gain signal. Use SHPHG for the AFE processing the high gain signal.
5. Use SHDLG for the AFE processing the low gain signal. Use SHDHG for the AFE processing the high gain signal.

Timing Diagrams

The charge in the photodiodes its transfer to the VCCD on the rising edge of the +12 V pulse and is completed by the falling edge of the +12 V pulsed on F1T and F1B. During the time period when F1T and F1B are at +12 V (t_{PD}) anti-blooming protection is disabled. The photodiode integration time ends on the falling edge of the +12 V pulse.

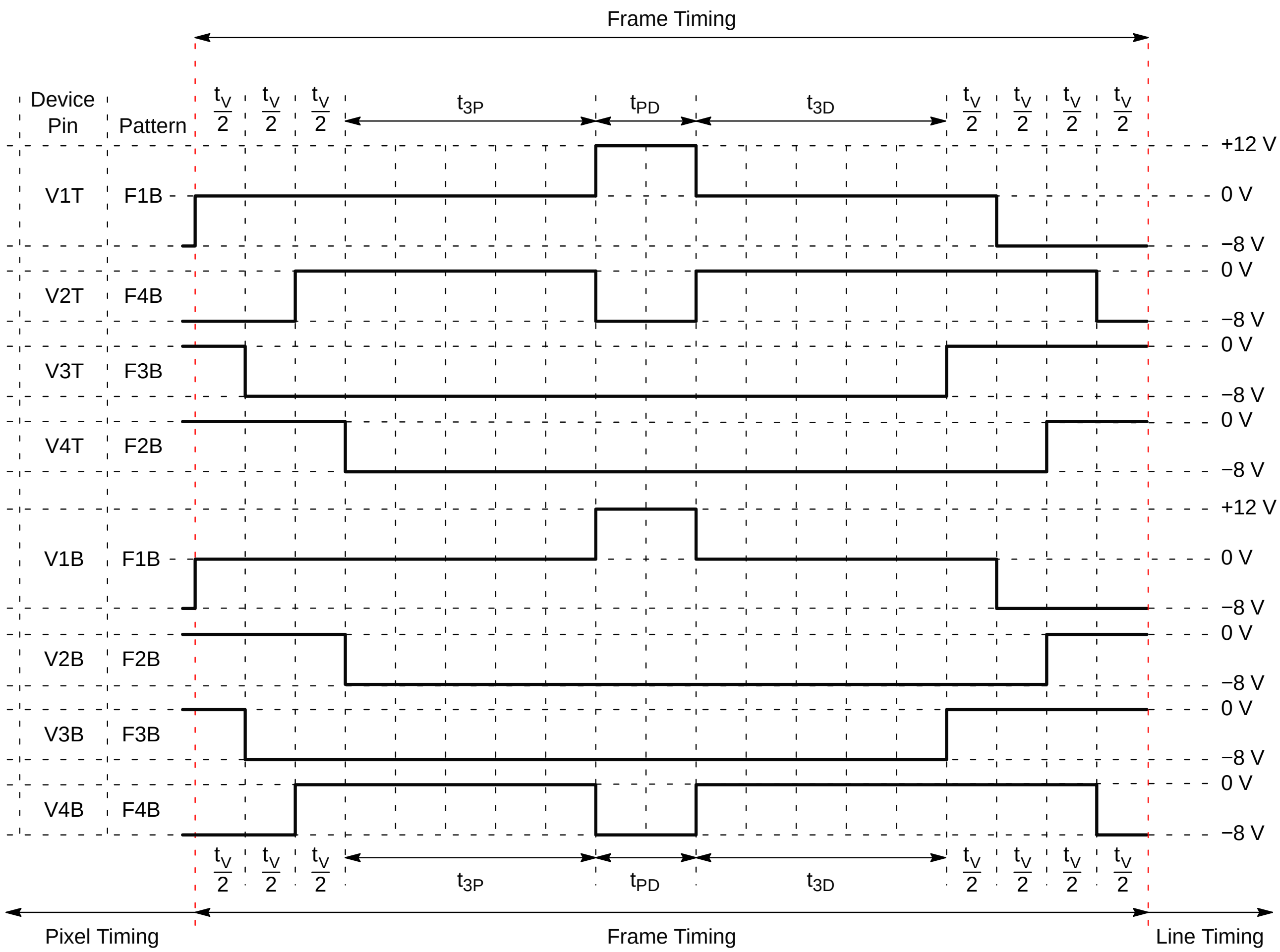
Frame Timing − Quadrant and Dual VOUTa/VOUTc Readout Modes



NOTE: See Table 20 for pin assignments.

Figure 32. Frame Timing Diagram Quadrant and Dual VOUTa/VOUTc Readout Modes

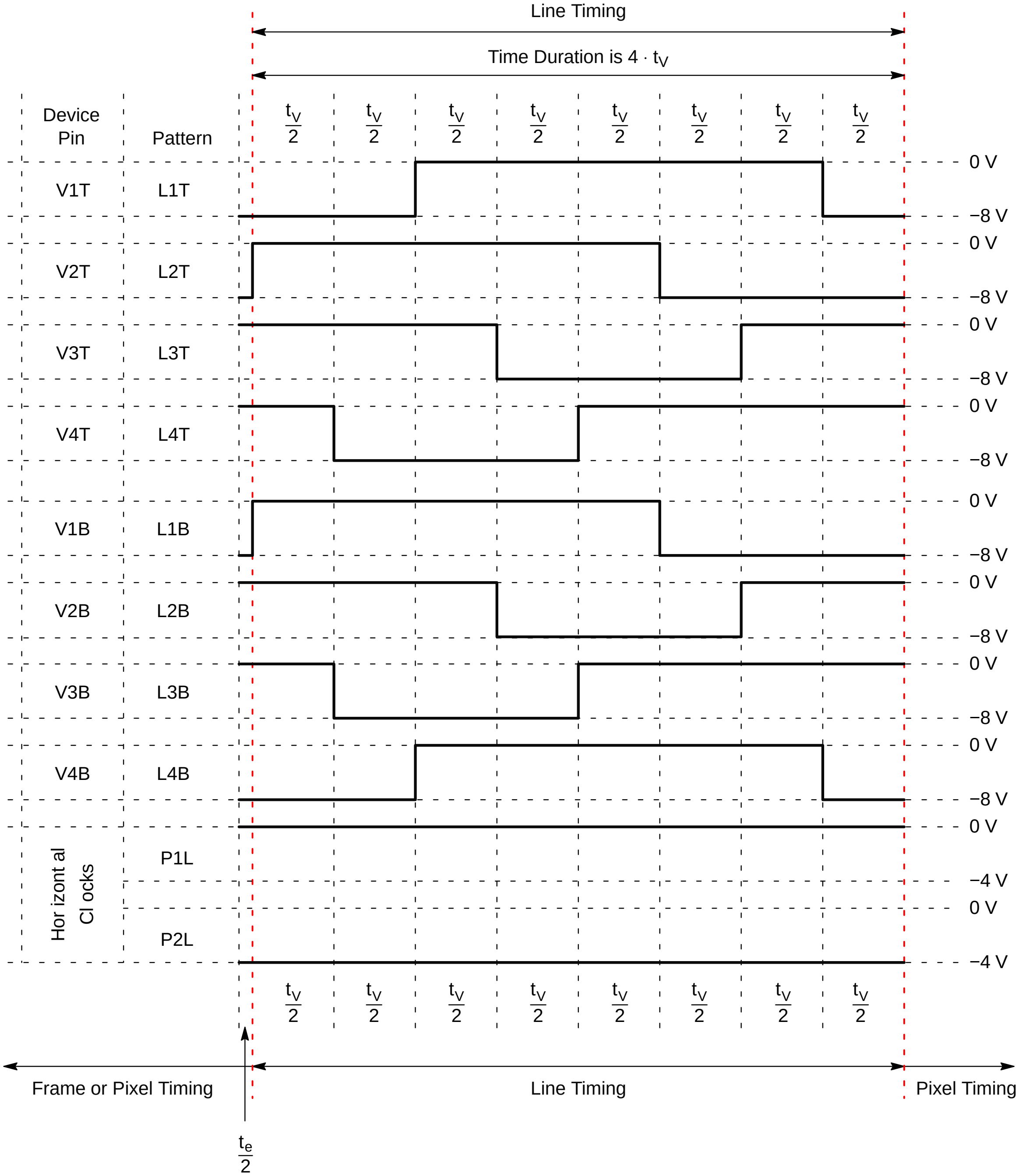
Frame Timing − Single and Dual VOUTa/VOUTb Readout Modes



NOTE: See Table 20 for pin assignments.

Figure 33. Frame Timing Diagram Single and Dual VOUTa/VOUTb Readout Modes

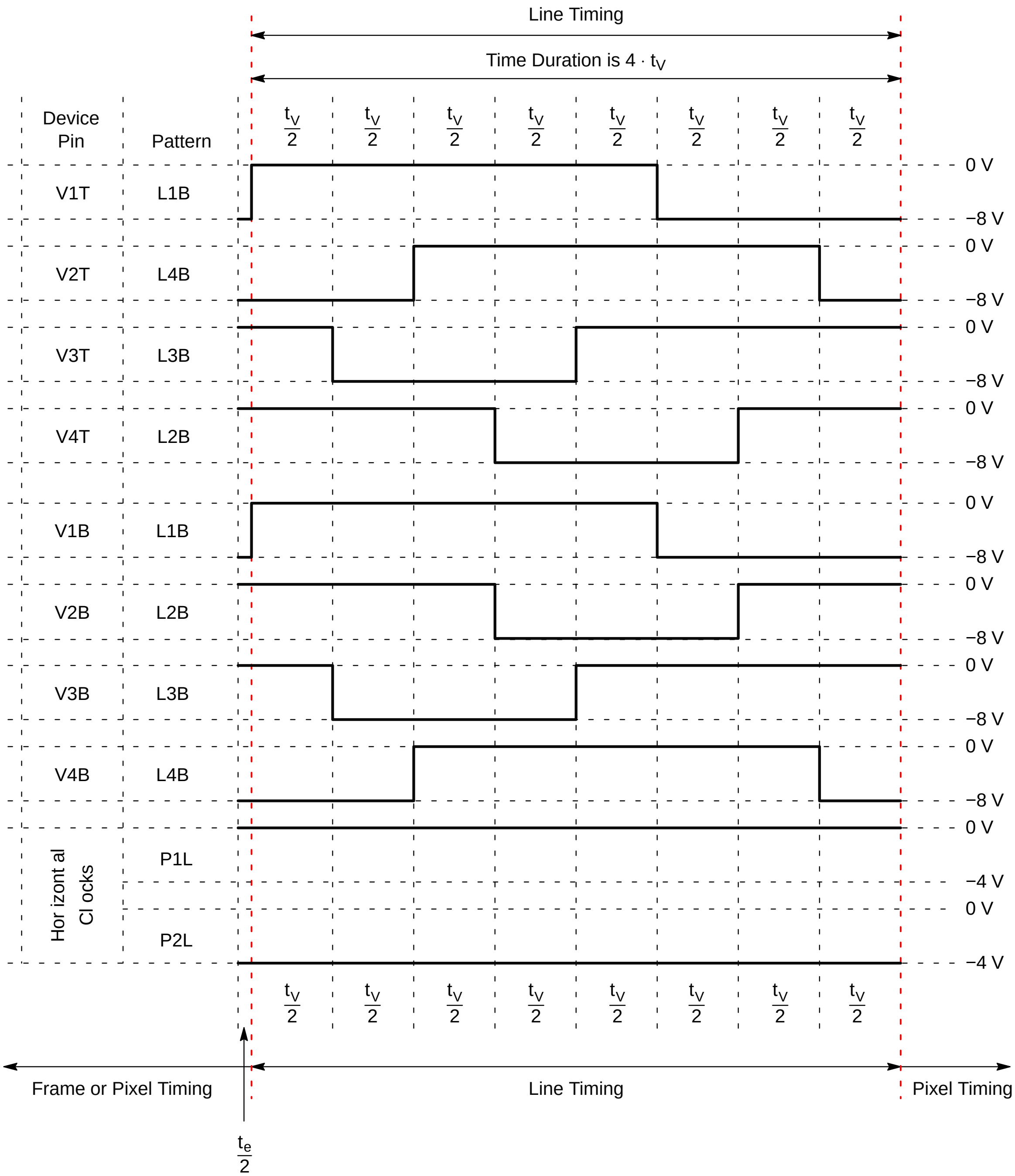
Line Timing −Full Resolution − Quadrant and Dual VOUTa/VOUTc Readout Modes



NOTE: See Table 21 for pin assignments.

Figure 34. Line Timing Diagram − Full Resolution − Quadrant and Dual VOUTa/VOUTc Readout Modes

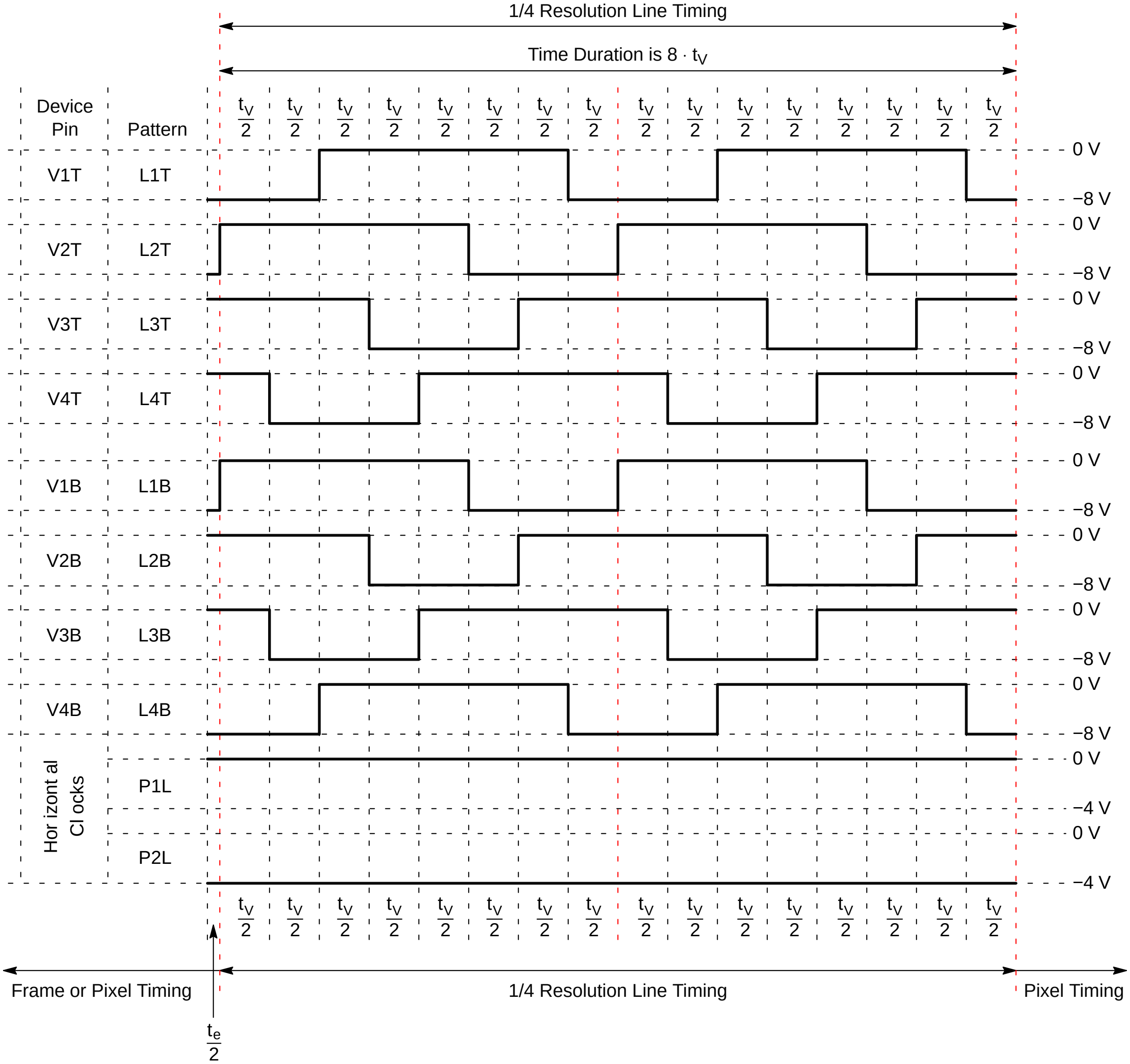
Line Timing −Full Resolution − Single and Dual VOUTa/VOUTb Readout Modes



NOTE: See Table 21 for pin assignments.

Figure 35. Line Timing Diagram − Full Resolution − Single and Dual VOUTa/VOUTb Readout Modes

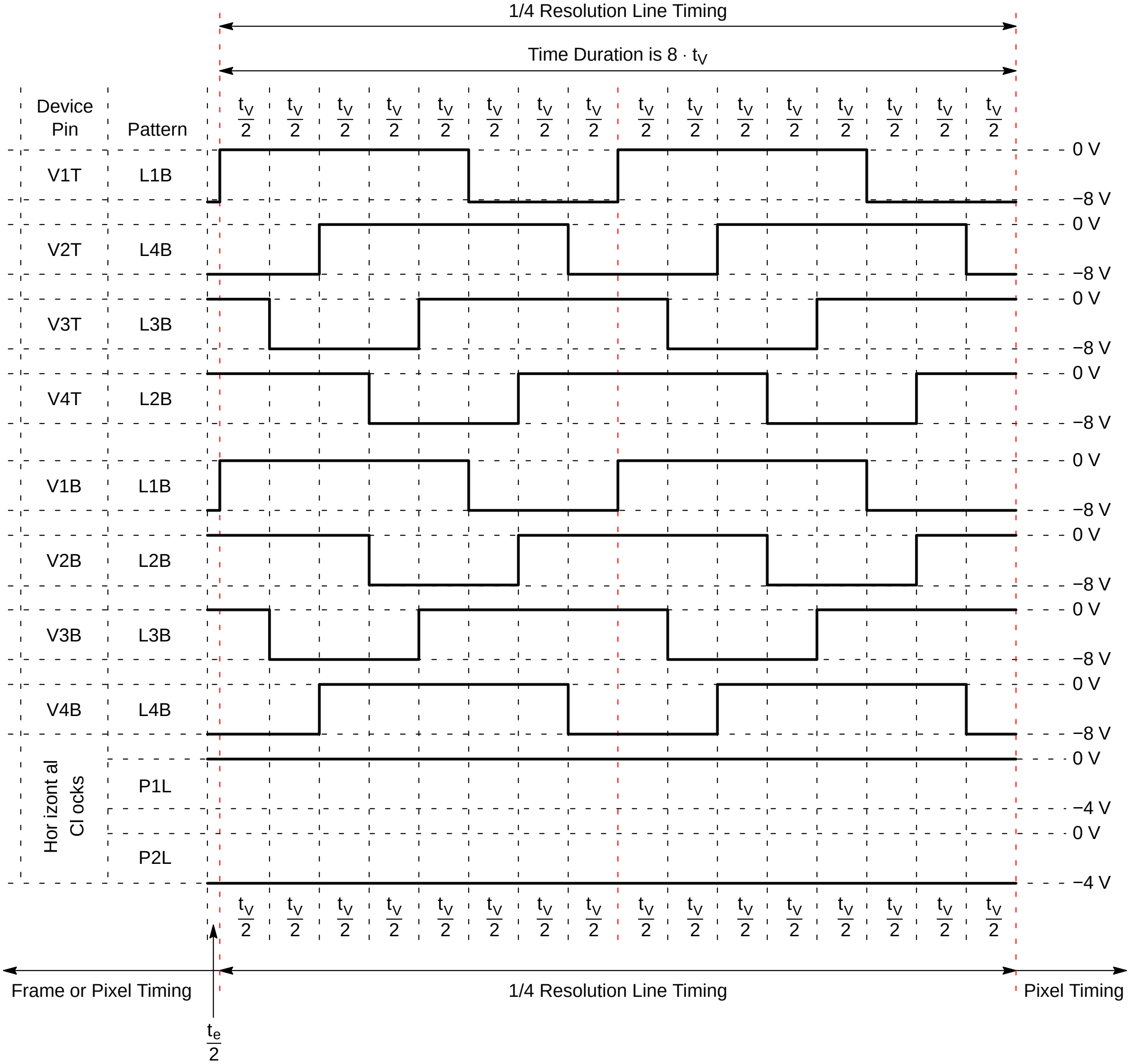
Line Timing − Low Gain, High Gain and XLDR 1/4 Resolution − Quadrant and Dual VOUTa/VOUTc Readout Modes



NOTE: See Table 21 for pin assignments.

Figure 36. Line Timing Diagram − 1/4 Resolution − Quadrant and Dual VOUTa/VOUTc Readout Modes

Line Timing − Low Gain, High Gain and XLDR 1/4 Resolution − Single and Dual VOUTa/VOUTb Readout Modes



NOTE: See Table 21 for pin assignments.

Figure 37. Line Timing Diagram − 1/4 Resolution − Single and Dual VOUTa/VOUTb Readout Modes

Electronic Shutter Timing Diagrams

The electronic shutter pulse can be inserted at the end of any line of the HCCD timing. The HCCD should be empty when the electronic shutter is pulsed. A recommended position for the electronic shutter is just after the last pixel is read out of a line. The VCCD clocks should not resume until at least $t_V/2$ after the electronic shutter pulse has finished. The HCCD clocks can be run during the electronic shutter pulse as long as the HCCD does not contain valid image data.

For short exposures less than one line time, the electronic shutter pulse can appear inside the frame timing. Any electronic shutter pulse transition should be $t_V/2$ away from any VCCD clock transition.

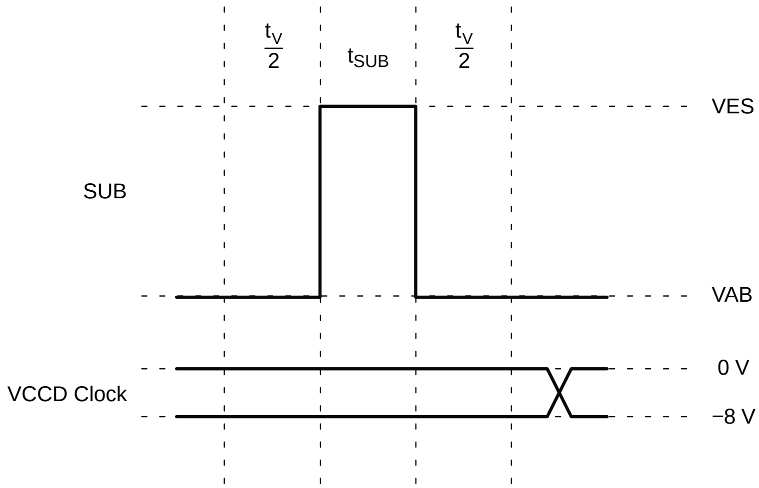


Figure 38. Electronic Shutter Timing

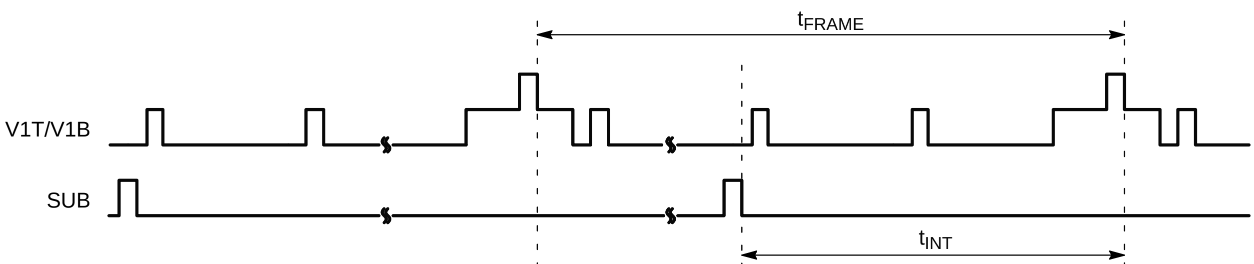


Figure 39. Frame/Electrical Shutter Timing

Pixel Timing − Full Resolution − High Gain Pixel Timing

Use this timing to read out every pixel at high gain. If the sensor is to be permanently operated at high gain, the R2ab and R2cd pins can be left floating or set to any DC voltage between +3 V and +5 V. Note the R2ab and R2cd pins are internally biased to +4.3 V when left floating. The SHP1 and SHD1 pulses indicate where the camera electronics should sample the video waveform. The SHP1 and SHD1 pulses are not applied to the image sensor.

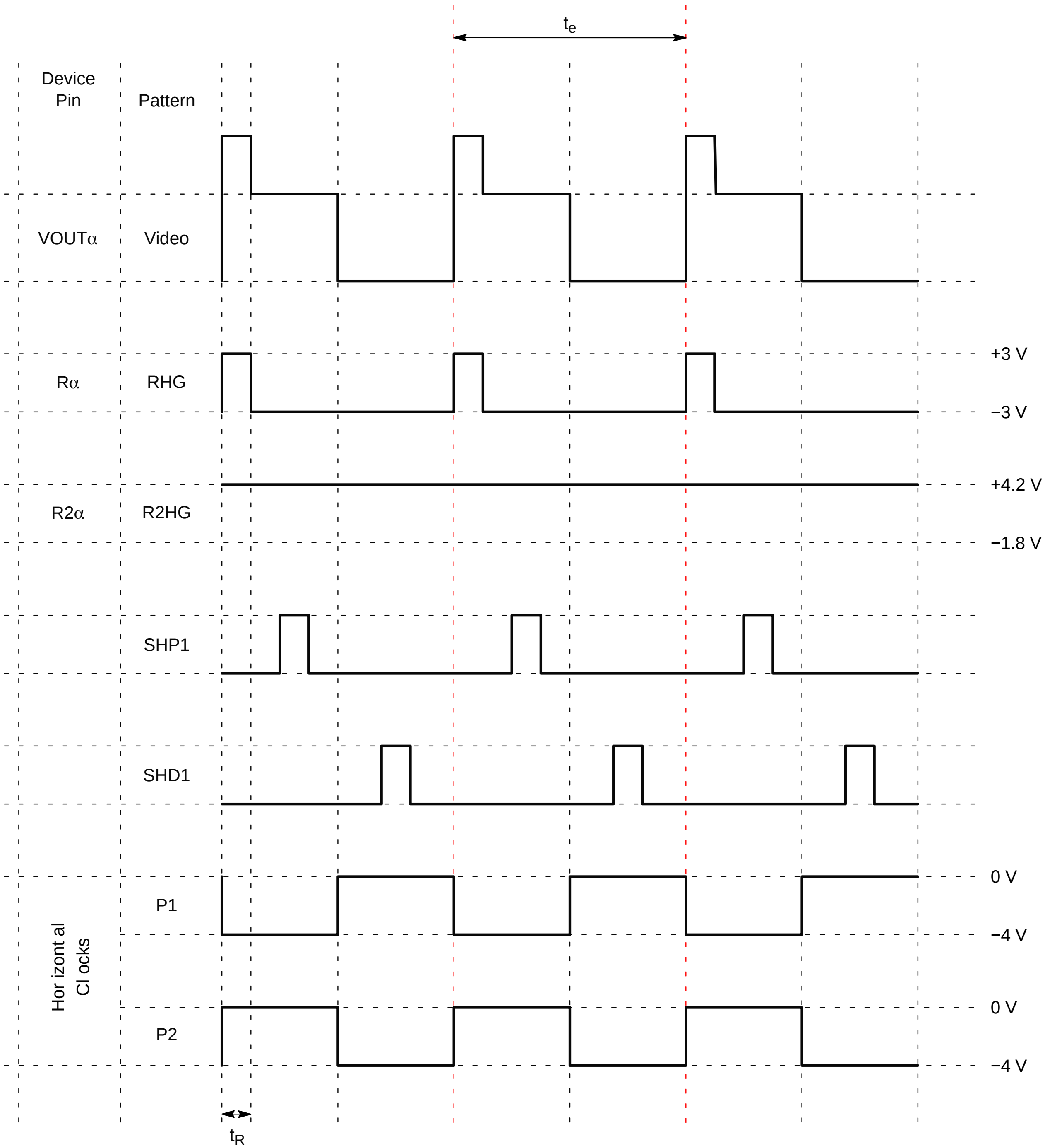


Figure 40. Pixel Timing Diagram − Full Resolution − High Gain

Pixel Timing − Full Resolution − Low Gain Pixel Timing

Use this pixel timing to read out every pixel at low gain. If the sensor is to be permanently operated at low gain, the Ra, Rb, Rc and Rd pins should be set to any DC voltage between +3 V and +5 V. The SHP1 and SHD1 pulses indicate where the camera electronics should sample the video waveform. The SHP1 and SHD1 pulses are not applied to the image sensor.

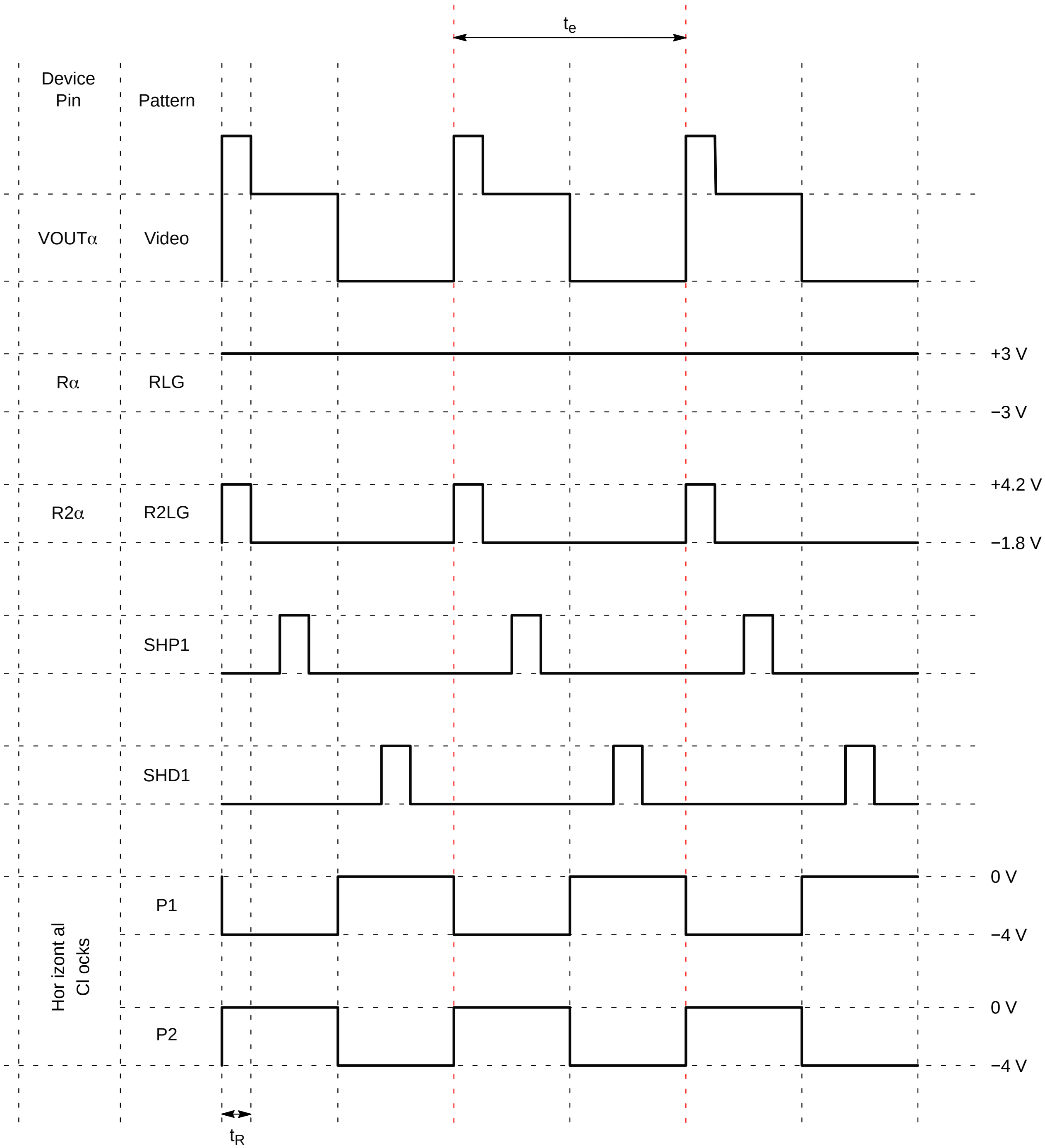


Figure 41. Pixel Timing Diagram − Full Resolution − Low Gain

Pixel Timing − 1/4 Resolution − High Gain Pixel Timing

Use this timing to read out two pixels summed on the output amplifier sense node at high gain. If the sensor is to be permanently operated at high gain, the R2ab and R2cd pins can be left floating or set to any DC voltage between +3 V and +5 V. Note the R2ab and R2cd pins are internally biased to +4.3 V when left floating. The SHPQ and SHDQ pulses indicate where the camera electronics should sample the video waveform. The SHPQ and SHDQ pulses are not applied to the image sensor.

The Ra, Rb, Rc, and Rd pins are pulsed at half the frequency of the horizontal CCD clocks. This causes two pixels to be summed on the output amplifier sense node. The SHPQ and SHDQ clocks are also half the frequency of the horizontal CCD clocks.

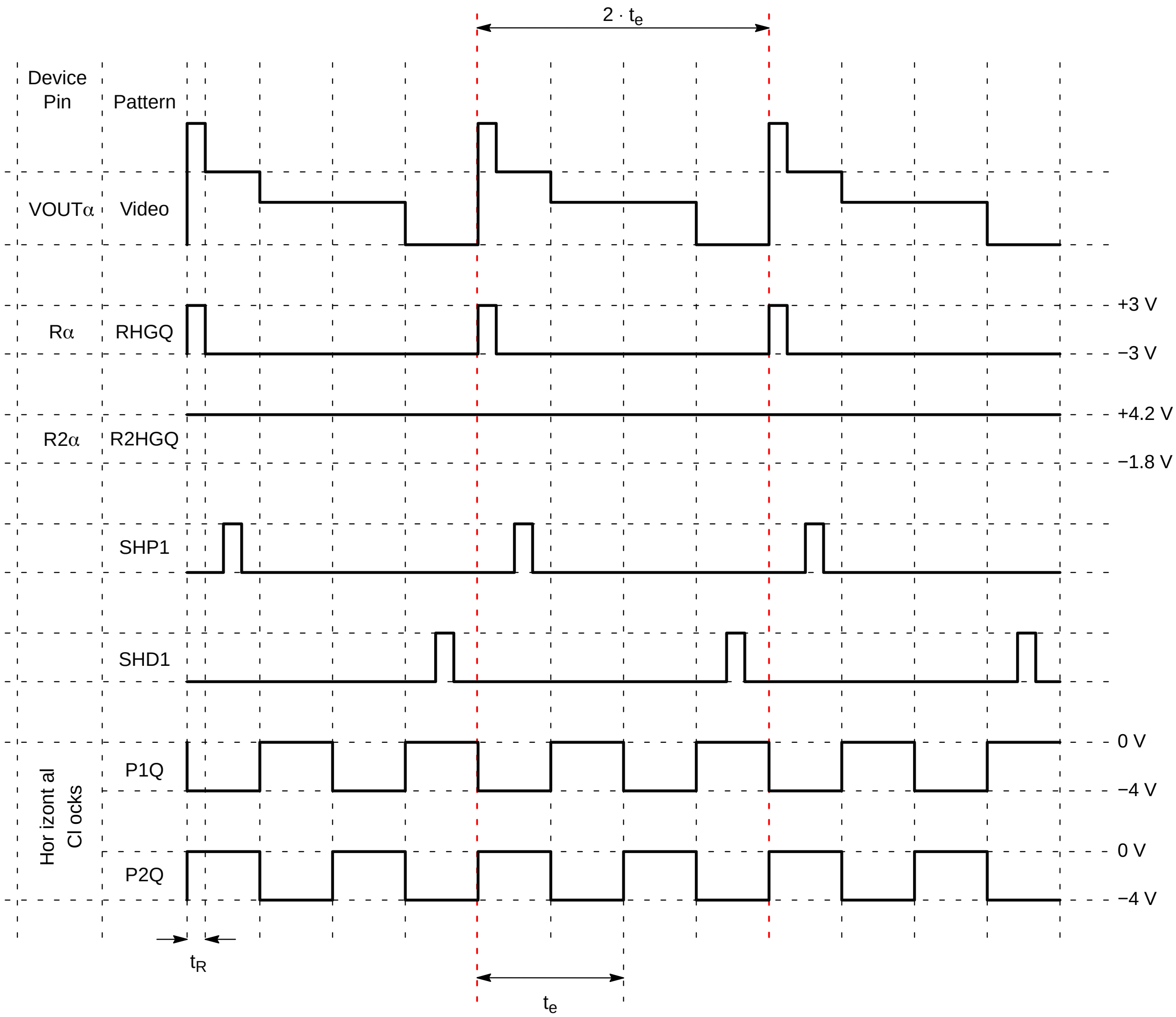


Figure 42. Pixel Timing Diagram − 1/4 Resolution − High Gain

Pixel Timing − 1/4 Resolution − Low Gain Pixel Timing

Use this timing to read out two pixels summed on the output amplifier sense node at low gain. If the sensor is to be permanently operated at low gain, the Ra, Rb, Rc and Rd pins can be set to any DC voltage between +3 V and +5 V. The SHPQ and SHDQ pulses indicate where the camera electronics should sample the video waveform. The SHPQ and SHDQ pulses are not applied to the image sensor.

The R2ab and R2cd pins are pulsed at half the frequency of the horizontal CCD clocks. This causes two pixels to be summed on the output amplifier sense node. The SHPQ and SHDQ clocks are also half the frequency of the horizontal CCD clocks.

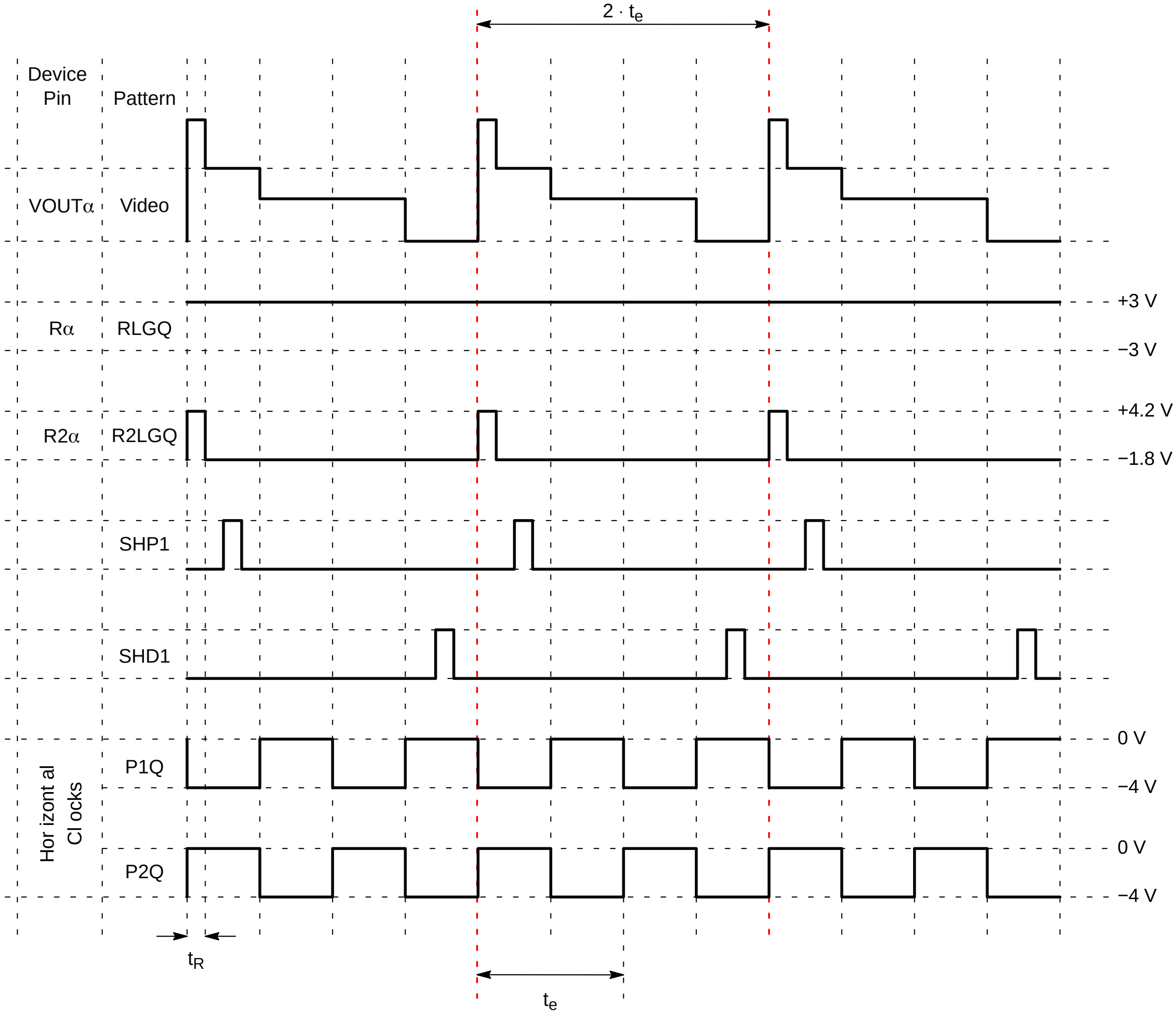


Figure 43. Pixel Timing Diagram − 1/4 Resolution − Low Gain

XLDR Pixel Timing

To operate the sensor in extended linear dynamic range (XLDR) mode, the following pixel timing should be used. This mode requires two sets of analog front end (AFE) signal processing electronic units for each output. As shown in Figure 44 one AFE samples the pixel at low gain (SHPLG and SHDLG) and the other AFE samples the pixel at high gain (SHPHG and SHDHG).

Two HCCD pixels are summed on the output amplifier node to obtain enough charge to fully use the 82 dB range of the XLDR timing. Combined with two-line VCCD summing, a total of 160,000 electrons of signal ($4 \times 40,000$) can be sampled with 12 electrons or less noise. Note that a linear dynamic range of 82 dB is very large. Ensure that the camera optics is capable of focusing an 82 dB dynamic range image on the sensor. Lens flare caused by inexpensive optics or even dust on the lens will limit the dynamic range.

The timing shown in Figure 46 shows the HCCD not being clocked at a constant frequency. If the HCCD cannot be clocked at a variable frequency, then the HCCD may be clocked at a constant frequency (Figure 45) at the expense of about 33% slower frame rate.

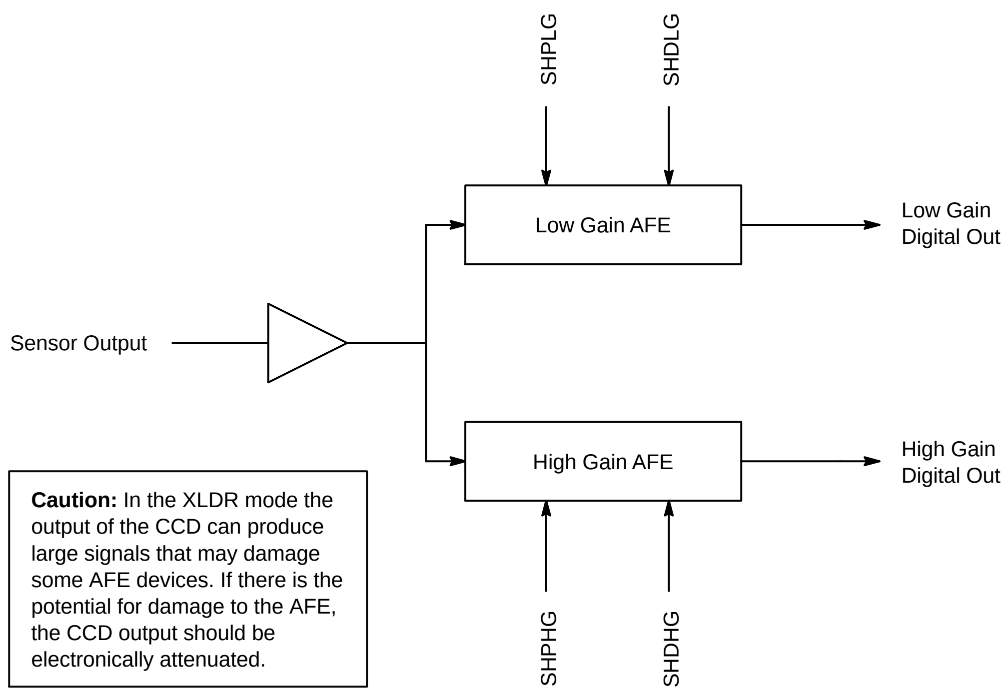


Figure 44. XLDR Timing − AFE Connections Block Diagram

Pixel Timing − 1/4 Resolution − XLDR Pixel Timing − Constant HCCD Timing

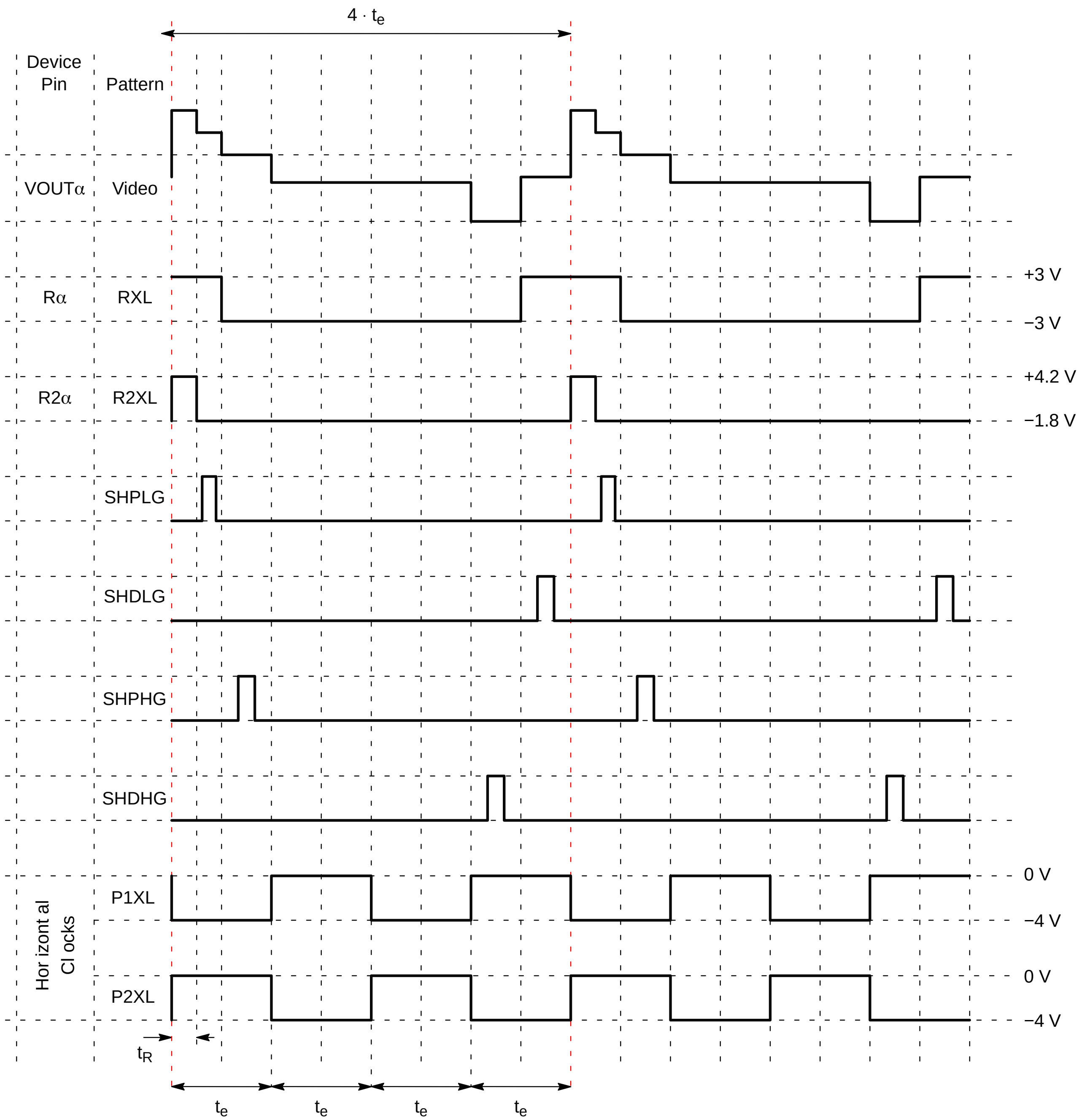


Figure 45. Pixel Timing Diagram − 1/4 Resolution − XLDR − Constant HCCD Timing

Pixel Timing − 1/4 Resolution − XLDR Pixel Timing − Variable HCCD Timing

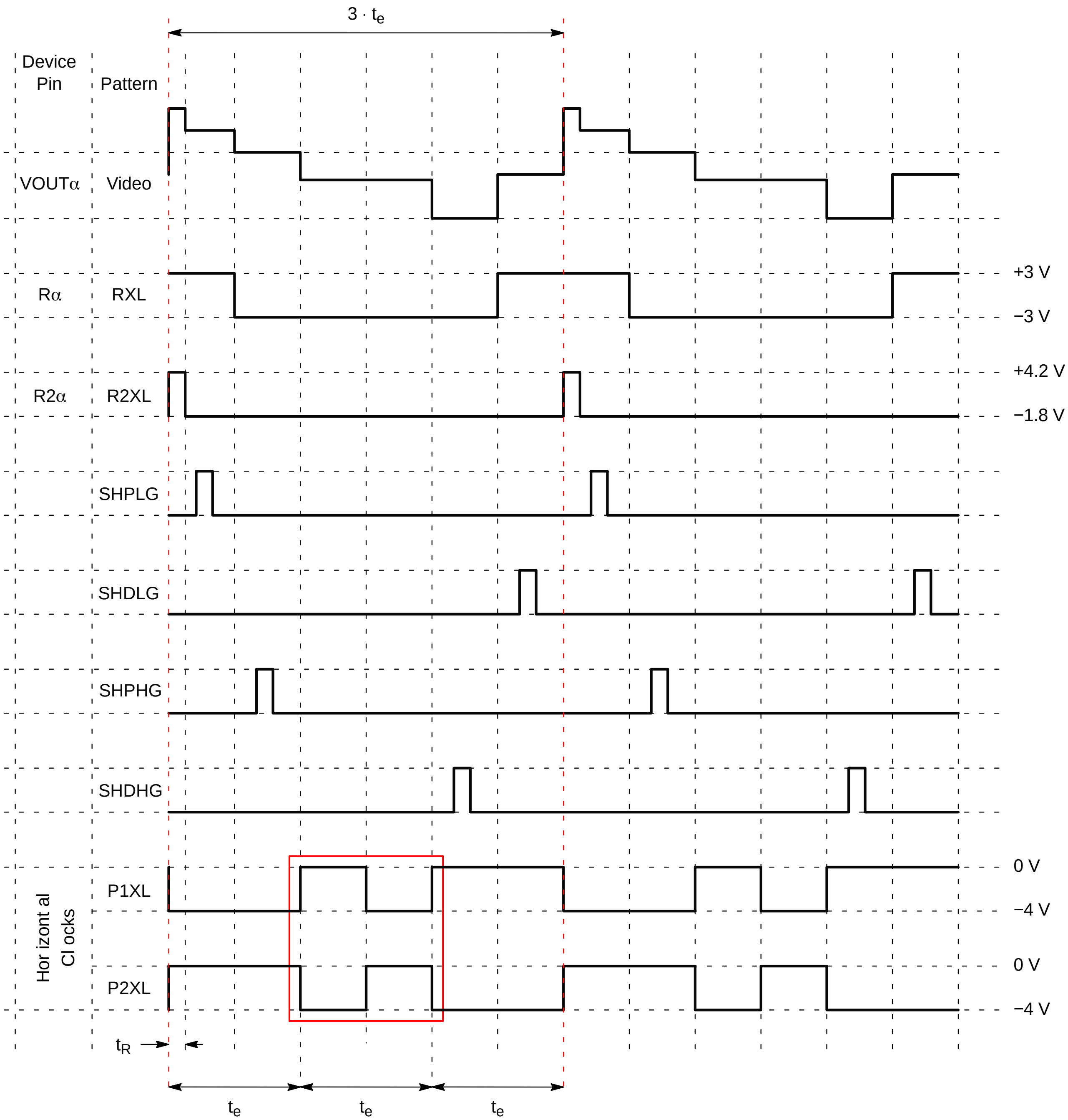


Figure 46. Pixel Timing Diagram − 1/4 Resolution − XLDR − Variable HCCD Timing

VCCD Clock Edge Alignment

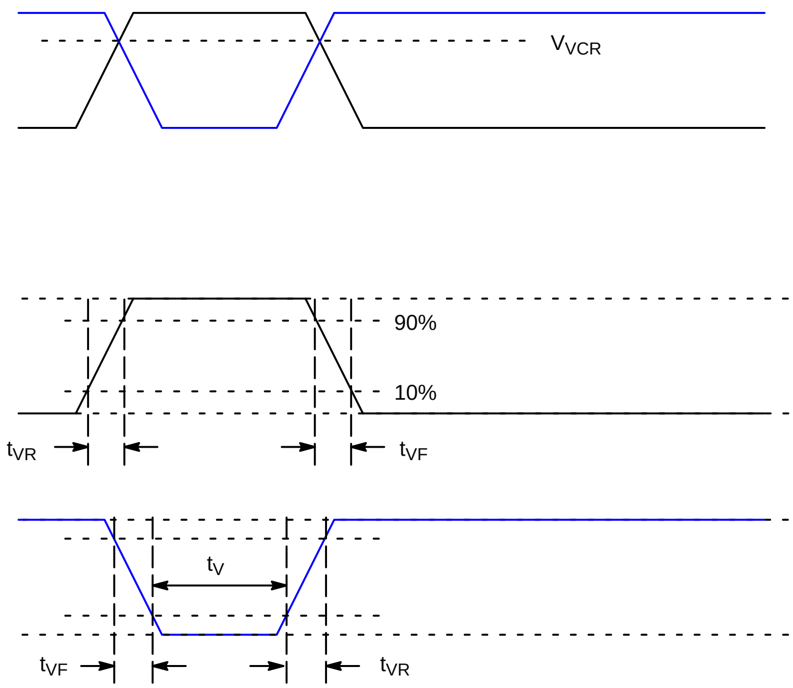


Figure 47. VCCD Clock Rise Time, Fall Time and Edge Alignment

REFERENCES

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

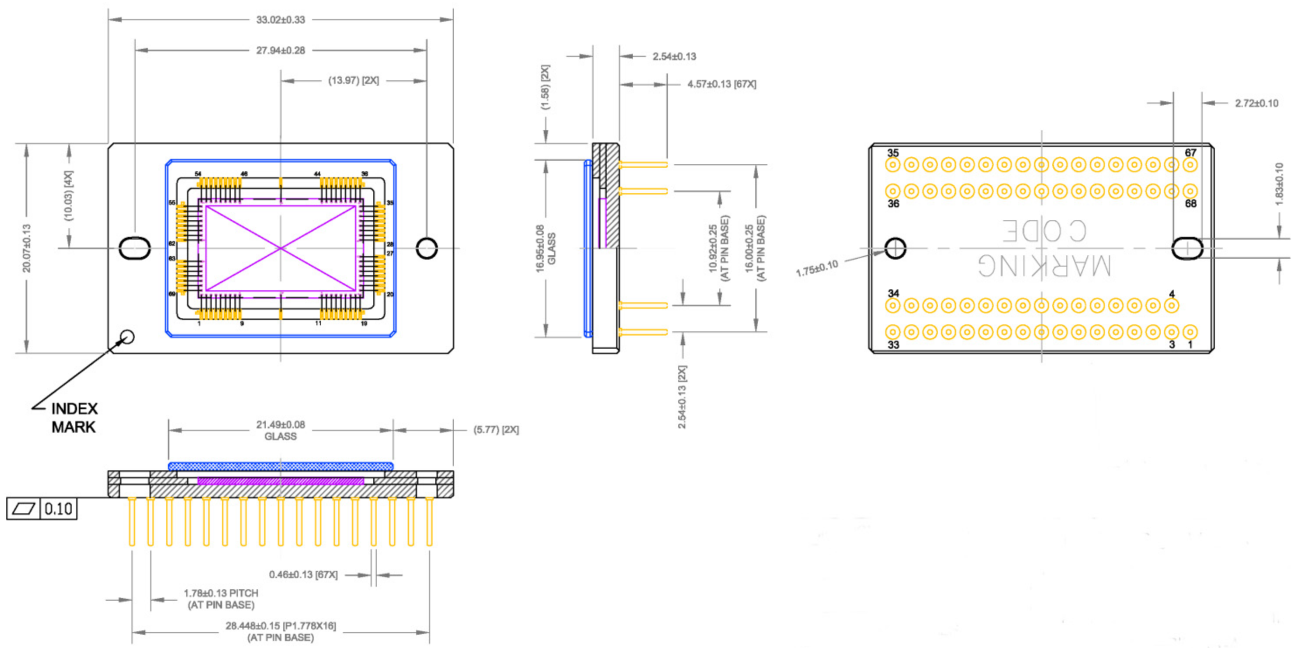
For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

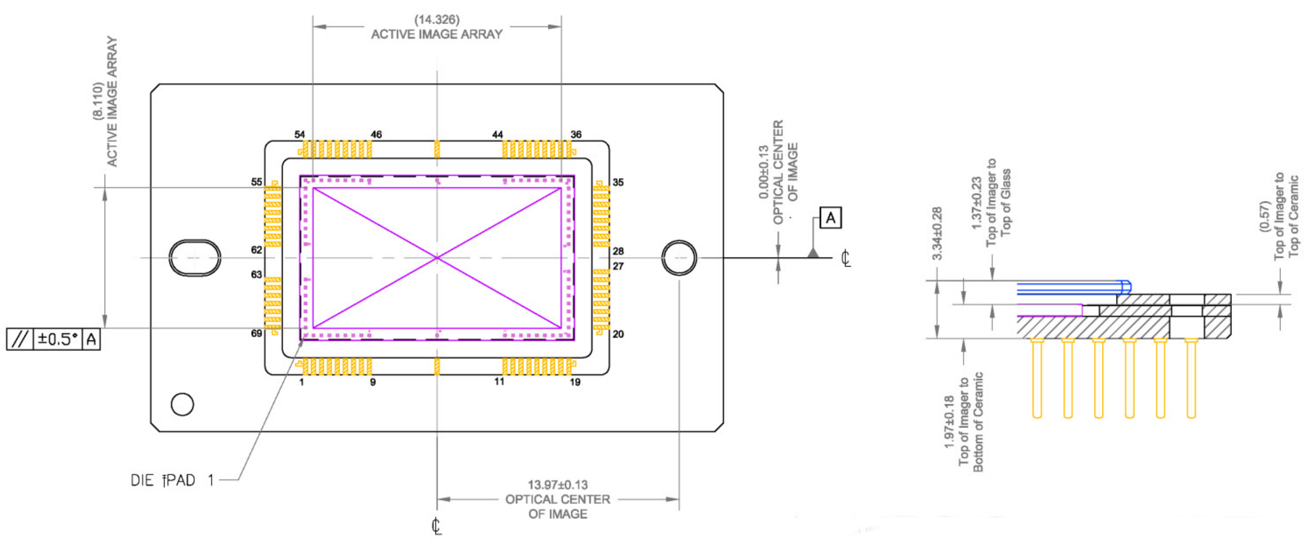
Completed Assembly



Notes:

1. See Ordering Information for marking code.
2. No materials to interfere with clearance through guide holes.
3. Units: mm.

Figure 48. Completed Assembly (1 of 2)

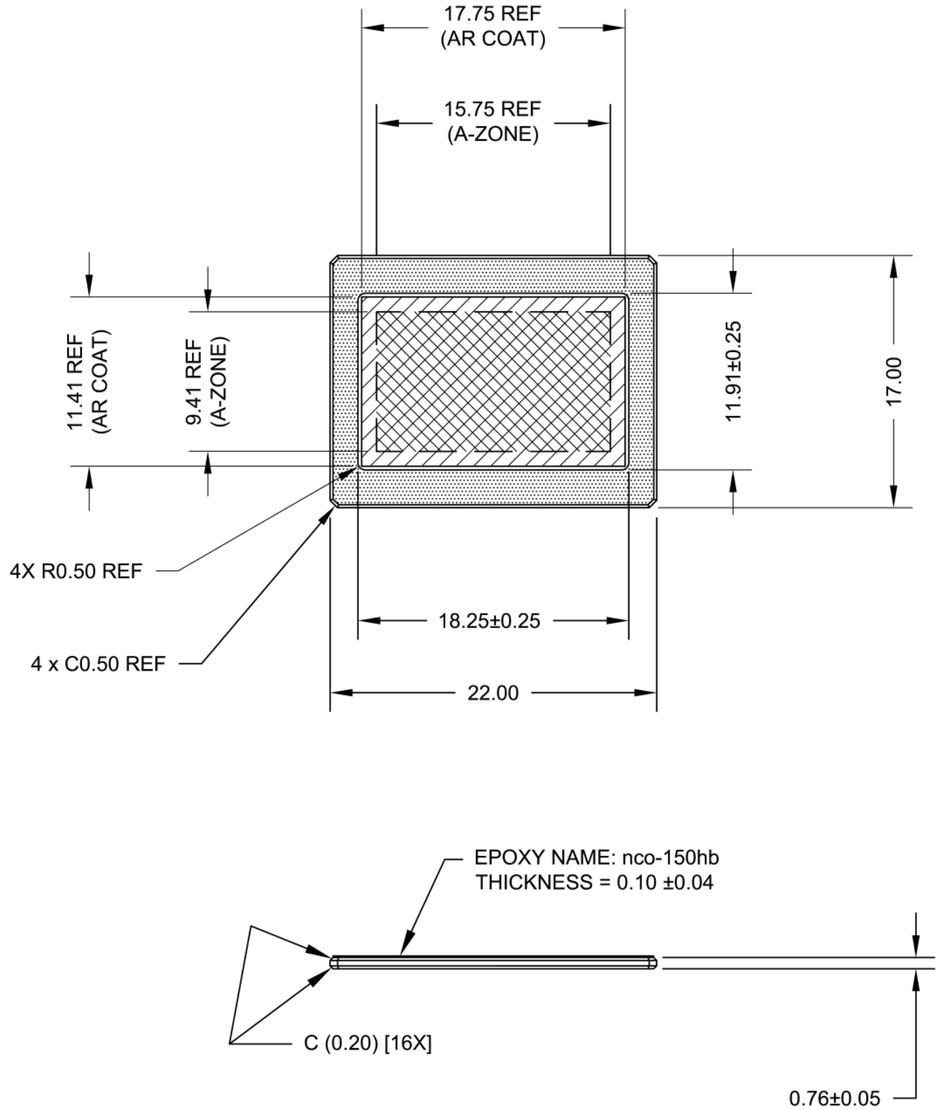


Notes:

1. Optical center of image is nominally at the package center.
2. Units: mm.

Figure 49. Completed Assembly (2 of 2)

Cover Glass



Notes:

1. Substrate = Schott D263T eco.
2. Dust, Scratch, Inclusion Specification: 10 μm maximum size in Zone A.
3. MAR coated both sides.
4. Spectral Transmission:
    a. T > 98.0% 420−435 nm
    b. T > 99.2% 435−630 nm
    c. T > 98.0% 630−680 nm
5. Units: mm.

Figure 50. Cover Glass

Cover Glass Transmission

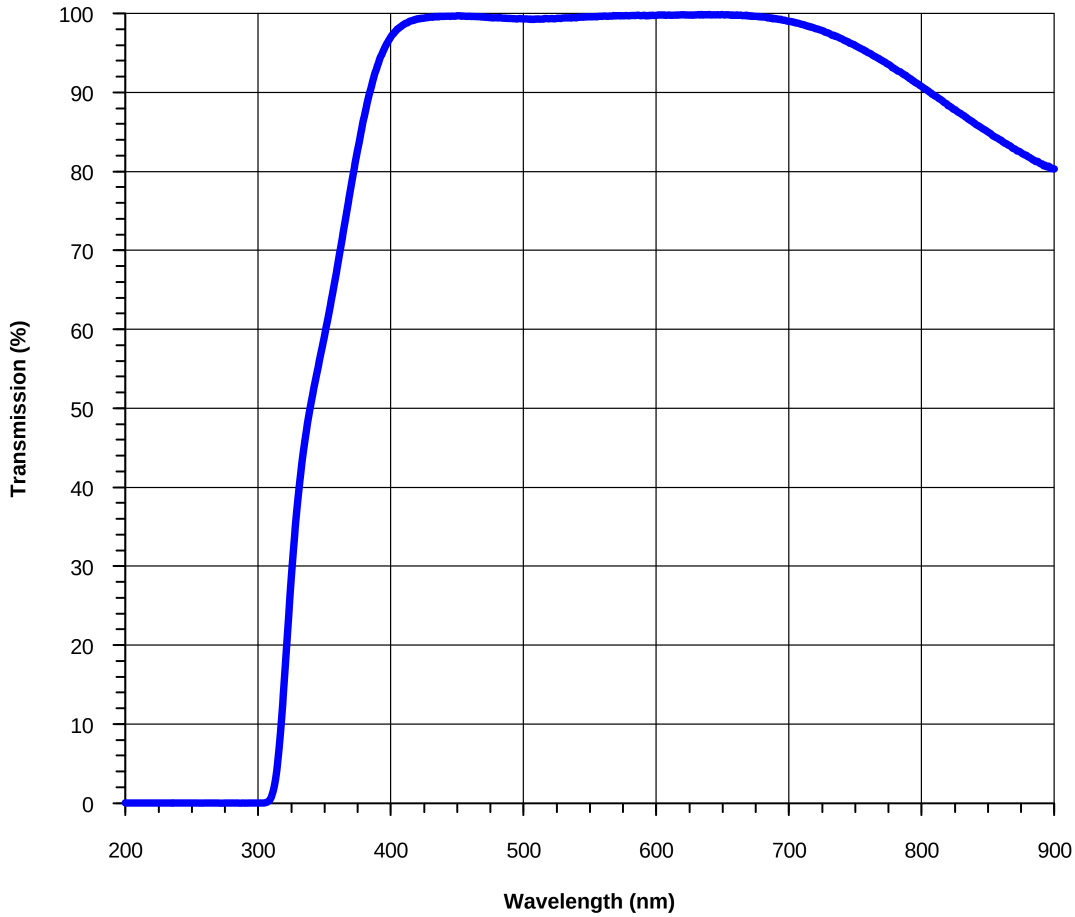


Figure 51. Cover Glass Transmission

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ООО «ЛайфЭлектроникс» "LifeElectronics" LLC

ИНН 7805602321 КПП 780501001 Р/С 40702810122510004610 ФАКБ "АБСОЛЮТ БАНК" (ЗАО) в г.Санкт-Петербурге К/С 30101810900000000703 БИК 044030703

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- *Конкурентоспособные цены и скидки постоянным клиентам.*
- *Специальные условия для постоянных клиентов.*
- *Подбор аналогов.*
- *Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.*

- *Приемлемые сроки поставки, возможна ускоренная поставка.*
- *Доставку товара в любую точку России и стран СНГ.*
- *Комплексную поставку.*
- *Работу по проектам и поставку образцов.*
- *Формирование склада под заказчика.*

- *Сертификаты соответствия на поставляемую продукцию (по желанию клиента).*
- *Тестирование поставляемой продукции.*
- *Поставку компонентов, требующих военную и космическую приемку.*
- *Входной контроль качества.*
- *Наличие сертификата ISO.*

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- *Регистрацию проекта у производителя компонентов.*
- *Техническую поддержку проекта.*
- *Защиту от снятия компонента с производства.*
- *Оценку стоимости проекта по компонентам.*
- *Изготовление тестовой платы монтаж и пусконаладочные работы.*

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