Features

- Core
  - ARM926EJ-S™ ARM® Thumb® Processor running at up to 400 MHz @ 1.0V +/- 10%
  - 16 Kbytes Data Cache, 16 Kbytes Instruction Cache, Memory Management Unit
- Memories
  - One 64-Kbyte internal ROM embedding bootstrap routine: Boot on NAND Flash, SDCard, DataFlash® or serial DataFlash. Programmable order.
  - One 32-Kbyte internal SRAM, single-cycle access at system speed
  - High Bandwidth Multi-port DDR2 Controller
  - 32-bit External Bus Interface supporting 8-bank DDR2/LPDDR, SDR/LPSDR, Static Memories
  - MLC/SLC NAND Controller, with up to 24-bit Programmable Multi-bit Error Correcting Code (PMECC)
- System running at up to 133 MHz
  - Power-on Reset Cells, Reset Controller, Shut Down Controller, Periodic Interval Timer, Watchdog Timer and Real Time Clock
  - Boot Mode Select Option, Remap Command
  - Internal Low Power 32 kHz RC and Fast 12 MHz RC Oscillators
  - Selectable 32768 Hz Low-power Oscillator and 12 MHz Oscillator
  - One PLL for the system and one PLL at 480 MHz optimized for USB High Speed
  - Twelve 32-bit-layer AHB Bus Matrix for large Bandwidth transfers
  - Dual Peripheral Bridge with dedicated programmable clock for best performance
  - Two dual port 8-channel DMA Controllers
  - Advanced Interrupt Controller and Debug Unit
  - Two Programmable External Clock Signals
- Low Power Mode
  - Shut Down Controller with four 32-bit Battery Backup Registers
  - Clock Generator and Power Management Controller
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
- Peripherals
  - LCD Controller with overlay, alpha-blending, rotation, scaling and color conversion
  - USB Device High Speed, USB Host High Speed and USB Host Full Speed with dedicated On-Chip Transceiver
  - One 10/100 Mbps Ethernet MAC Controller
  - Two High Speed Memory Card Hosts
  - Two CAN Controllers
  - Two Master/Slave Serial Peripheral Interface
  - Two Three-channel 32-bit Timer/Counters
  - One Synchronous Serial Controller
  - One Four-channel 16-bit PWM Controller
  - Three Two-wire Interfaces
  - Three USARTs, two UARTs
  - One 12-channel 10-bit Touch-Screen Analog-to-Digital Converter
  - Soft Modem
- I/O
  - Four 32-bit Parallel Input/Output Controllers
  - 105 Programmable I/O Lines Multiplexed with up to Three Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line, optional Schmitt trigger input
  - Individually Programmable Open-drain, Pull-up and pull-down resistor, Synchronous Output
- Package
  - 217-ball BGA, pitch 0.8 mm

AT91SAM ARM-based Embedded MPU

SAM9X35 Summary

NOTE: This is a summary document. The complete document is available on the Atmel website at www.atmel.com.

11055AS–ATARM–27-Jul-11

1. Description

The SAM9X35 is a highly-integrated 400 MHz ARM926 embedded MPU, featuring an extensive peripheral set and high bandwidth architecture for industrial applications that require refined user interfaces and high-speed communication.

The SAM9X35 features a graphics LCD controller with 4-layer overlay and 2D acceleration (picture-in-picture, alpha-blending, scaling, rotation, color conversion), and a 10-bit ADC that supports 4- or 5-wire resistive touchscreen panels. Networking/connectivity peripherals include two 2.0A/B compatible Controller Area Network (CAN) interfaces and an IEEE Std 802.3-compatible 10/100Mbps Ethernet MAC. Multiple communication interfaces include a soft modem supporting exclusively the Conexant SmartDAA line driver, HS USB Device and Host, FS USB Host, two HS SDCard/SDIO/MMC interfaces, USARTs, SPIs, I2S, TWIs and 10-bit ADC.

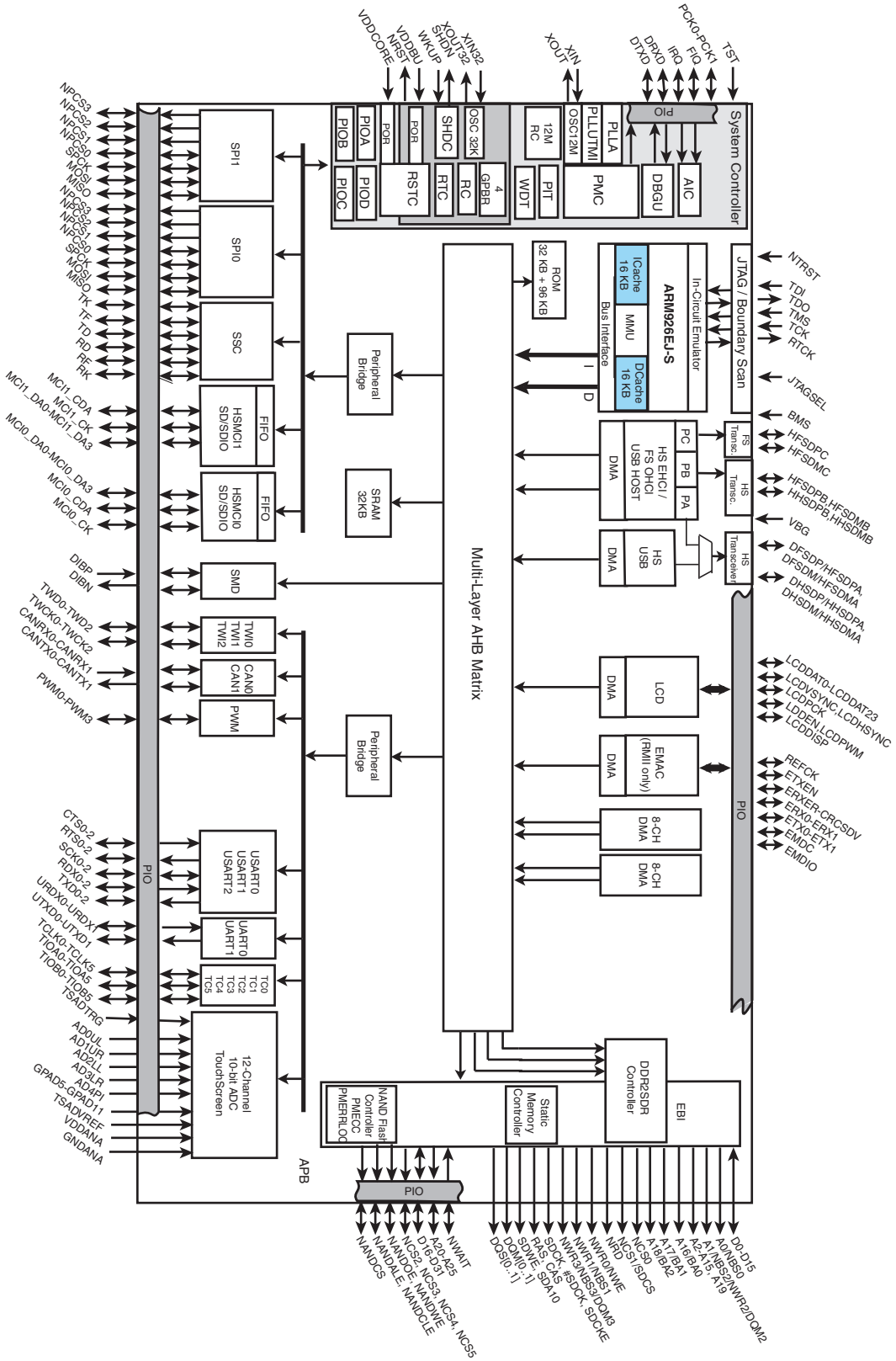
The 10-layer bus matrix associated with 2 x 8 central DMA channels as well as dedicated DMAs to support the high-speed connectivity peripherals ensure uninterrupted data transfer with minimum processor overhead.

The External Bus Interface incorporates controllers for 8-bank DDR2/LPDDR, SDRAM/LPSDRAM, static memories, and specific circuitry for MLC/SLC NAND Flash with integrated ECC.

The SAM9X35 is available in a 217-ball BGA package with 0.8mm ball pitch.

2. Block Diagram

Figure 2-1. SAM9X35 Block Diagram



3. Signal Description

Table 3-1 gives details on the signal names classified by peripheral.

Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level
Clocks, Oscillators and PLLs			
XIN	Main Oscillator Input	Input	
XOUT	Main Oscillator Output	Output	
XIN32	Slow Clock Oscillator Input	Input	
XOUT32	Slow Clock Oscillator Output	Output	
VBG	Bias Voltage Reference for USB	Analog	
PCK0-PCK1	Programmable Clock Output	Output	
Shutdown, Wakeup Logic			
SHDN	Shut-Down Control	Output	
WKUP	Wake-Up Input	Input	
ICE and JTAG			
TCK	Test Clock	Input	
TDI	Test Data In	Input	
TDO	Test Data Out	Output	
TMS	Test Mode Select	Input	
JTAGSEL	JTAG Selection	Input	
RTCK	Return Test Clock	Output	
Reset/Test			
NRST	Microcontroller Reset	I/O	Low
TST	Test Mode Select	Input	
NTRST	Test Reset Signal	Input	
BMS	Boot Mode Select	Input	
Debug Unit - DBGU			
DRXD	Debug Receive Data	Input	
DTXD	Debug Transmit Data	Output	
Advanced Interrupt Controller - AIC			
IRQ	External Interrupt Input	Input	
FIQ	Fast Interrupt Input	Input	
PIO Controller - PIOA - PIOB - PIOC - PIOD			
PA0-PA31	Parallel IO Controller A	I/O	
PB0-PB18	Parallel IO Controller B	I/O	
PC0-PC31	Parallel IO Controller C	I/O	
PD0-PD21	Parallel IO Controller D	I/O	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
External Bus Interface - EBI			
D0-D15	Data Bus	I/O	
D16-D31	Data Bus	I/O	
A0-A25	Address Bus	Output	
NWAIT	External Wait Signal	Input	Low
Static Memory Controller - SMC			
NCS0-NCS5	Chip Select Lines	Output	Low
NWR0-NWR3	Write Signal	Output	Low
NRD	Read Signal	Output	Low
NWE	Write Enable	Output	Low
NBS0-NBS3	Byte Mask Signal	Output	Low
NAND Flash Support			
NFD0-NFD16	NAND Flash I/O	I/O	
NANDCS	NAND Flash Chip Select	Output	Low
NANDOE	NAND Flash Output Enable	Output	Low
NANDWE	NAND Flash Write Enable	Output	Low
DDR2/SDRAM/LPDDR Controller			
SDCK,#SDCK	DDR2/SDRAM Differential Clock	Output	
SDCKE	DDR2/SDRAM Clock Enable	Output	High
SDCS	DDR2/SDRAM Controller Chip Select	Output	Low
BA[0..2]	Bank Select	Output	Low
SDWE	DDR2/SDRAM Write Enable	Output	Low
RAS-CAS	Row and Column Signal	Output	Low
SDA10	SDRAM Address 10 Line	Output	
DQS[0..1]	Data Strobe	I/O	
DQM[0..3]	Write Data Mask	Output	
High Speed MultiMedia Card Interface - HSMCI0-1			
MCI0_CK, MCI1_CK	Multimedia Card Clock	I/O	
MCI0_CDA, MCI1_CDA	Multimedia Card Slot Command	I/O	
MCI0_DA0-MCI0_DA3	Multimedia Card 0 Slot A Data	I/O	
MCI1_DA0-MCI1_DA3	Multimedia Card 1 Slot A Data	I/O	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
Universal Synchronous Asynchronous Receiver Transmitter - USARTx			
SCKx	USARTx Serial Clock	I/O	
TXDx	USARTx Transmit Data	Output	
RXDx	USARTx Receive Data	Input	
RTSx	USARTx Request To Send	Output	
CTSx	USARTx Clear To Send	Input	
Universal Asynchronous Receiver Transmitter - UARTx			
UTXDx	UARTx Transmit Data	Output	
URXDx	UARTx Receive Data	Input	
Synchronous Serial Controller - SSC			
TD	SSC Transmit Data	Output	
RD	SSC Receive Data	Input	
TK	SSC Transmit Clock	I/O	
RK	SSC Receive Clock	I/O	
TF	SSC Transmit Frame Sync	I/O	
RF	SSC Receive Frame Sync	I/O	
Timer/Counter - TCx x=0..5			
TCLKx	TC Channel x External Clock Input	Input	
TIOAx	TC Channel x I/O Line A	I/O	
TIOBx	TC Channel x I/O Line B	I/O	
Serial Peripheral Interface - SPIx			
SPIx_MISO	Master In Slave Out	I/O	
SPIx_MOSI	Master Out Slave In	I/O	
SPIx_SPCK	SPI Serial Clock	I/O	
SPIx_NPCS0	SPI Peripheral Chip Select 0	I/O	Low
SPIx_NPCS1-SPIx_NPCS3	SPI Peripheral Chip Select	Output	Low
Two-Wire Interface -TWIx			
TWDx	Two-wire Serial Data	I/O	
TWCKx	Two-wire Serial Clock	I/O	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
Pulse Width Modulation Controller- PWMC			
PWM0-PWM3	Pulse Width Modulation Output	Output	
USB Host High Speed Port - UHPHS			
HFSDPA	USB Host Port A Full Speed Data +	Analog	
HFSDMA	USB Host Port A Full Speed Data -	Analog	
HHSDPA	USB Host Port A High Speed Data +	Analog	
HHSDMA	USB Host Port A High Speed Data -	Analog	
HFSDPB	USB Host Port B Full Speed Data +	Analog	
HFSDMB	USB Host Port B Full Speed Data -	Analog	
HHSDPB	USB Host Port B High Speed Data +	Analog	
HHSDMB	USB Host Port B High Speed Data -	Analog	
HFSDMC	USB Host Port C Full Speed Data -	Analog	
HFSDPC	USB Host Port C Full Speed Data +	Analog	
USB Device High Speed Port - UDPHS			
DFSDM	USB Device Full Speed Data -	Analog	
DFSDP	USB Device Full Speed Data +	Analog	
DHSDM	USB Device High Speed Data -	Analog	
DHSDP	USB Device High Speed Data +	Analog	
RMII Ethernet 10/100 - EMAC			
REFCK	Transmit Clock or Reference Clock	Input	
ETXEN	Transmit Enable	Output	
ETX0-ETX1	Transmit Data	Output	
CRSDV	Receive Data Valid	Input	
ERX0-ERX1	Receive Data	Input	
ERXER	Receive Error	Input	
EMDC	Management Data Clock	Output	
EMDIO	Management Data Input/Output	I/O	
LCD Controller - LCDC			
LCDDAT 0-23	LCD Data Bus	Output	
LCDVSYNC	LCD Vertical Synchronization	Output	
LCDHSYNC	LCD Horizontal Synchronization	Output	
LCDPCK	LCD Pixel Clock	Output	
LCDDEN	LCD Data Enable	Output	
LCDPWM	LCD Contrast Control	Output	
LCDDISP	LCD Display Enable	Output	

Table 3-1. Signal Description List (Continued)

Signal Name	Function	Type	Active Level
Analog-to-Digital Converter - ADC			
$AD0_{XP\_UL}$	Top/Upper Left Channel	Analog	
$AD1_{XM\_UR}$	Bottom/Upper Right Channel	Analog	
$AD2_{YP\_LL}$	Right/Lower Left Channel	Analog	
$AD3_{YM\_SENSE}$	Left/Sense Channel	Analog	
$AD4_{LR}$	Lower Right Channel	Analog	
AD5-AD11	7 Analog Inputs	Analog	
ADTRG	ADC Trigger	Input	
ADVREF	ADC Reference	Analog	
CAN Controller - CANx			
CANRXx	CAN input	Input	
CANTXx	CAN output	Output	
Soft Modem - SMD			
DIBN	Soft Modem Signal	I/O	
DIBP	Soft Modem Signal	I/O	

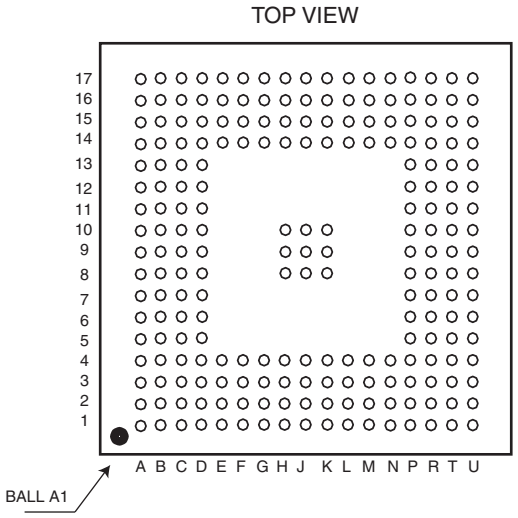
4. Package and Pinout

The SAM9X35 is available in 217-ball BGA package.

4.1 Overview of the 217-ball BGA Package

Figure 4-1 shows the orientation of the 217-ball BGA Package.

Figure 4-1. Orientation of the 217-ball BGA Package



4.2 I/O Description

Table 4-1. SAM9X35 I/O Type Description

I/O Type	Voltage Range	Analog	Pull-up	Pull-down	Schmitt Trigger
GPIO	1.65-3.6V		switchable	switchable	switchable
GPIO_CLK	1.65-3.6V		switchable	switchable	switchable
GPIO_CLK2	1.65-3.6V		switchable	switchable	switchable
GPIO_ANA	3.0-3.6V	I	switchable		switchable
EBI	1.65-1.95V, 3.0-3.6V		switchable	switchable	
EBI_O	1.65-1.95V, 3.0-3.6V		Reset State	Reset State	
EBI_CLK	1.65-1.95V, 3.0-3.6V				
RSTJTAG	3.0-3.6V		Reset State	Reset State	Reset State
SYSC	1.65-3.6V		Reset State	Reset State	Reset State
VBG	0.9-1.1V	I			
USBFS	3.0-3.6V	I/O			
USBHS	3.0-3.6V	I/O			
CLOCK	1.65-3.6V	I/O			
DIB	3.0-3.6V	I/O			

When “Reset State” is mentioned, the configuration is defined by the “Reset State” column of the Pin Description table.

Table 4-2. SAM9X35 I/O Type Assignment and Frequency

I/O Type	I/O Frequency (MHz)	Charge Load (pF)	Output Current	Signal Name
GPIO	40	10		all PIO lines except the following
GPIO_CLK	54	10		MCI0CK, MCI1CK, SPI0SPCK, SPI1SPCK, EMACx_ETXCK
GPIO_CLK2	75	10		
GPIO_ANA	25	10	16mA, 40mA (peak)	ADx, GPADx
EBI	133	50 (3.3V) 30 (1.8V)		all Data lines (Input/output) except the following
EBI_O	66	50 (3.3V) 30 (1.8V)		all Address and control lines (output only) except the following
EBI_CLK	133	10		CK, #CK
RSTJTAG	10	10		NRST, NTRST, BMS, TCK, TDI, TMS, TDO, RTCK
SYSC	0.25	10		WKUP, SHDN, JTAGSEL, TST, SHDN
VBG	0.25	10		VBG
USBFS	12	10		HFSDPA, HFSDPB/DFSDP, HFSDPC, HFSDMA, HFSDMB/DFSDM, HFSDMC
USBHS	480	10		HHSDPA, HHSDPB/DHSDP, HHSDMA, HHSDMB/DHSDM
CLOCK	50	50		XIN, XOUT, XIN32, XOUT32
DIB	25	25		DIBN, DIBP

4.2.1 Reset State

In the tables that follow, the column “Reset State” indicates the reset state of the line with mnemonics.

- “PIO” “/” signal

Indicates whether the PIO Line resets in I/O mode or in peripheral mode. If “PIO” is mentioned, the PIO Line is maintained in a static state as soon as the reset is released. As a result, the bit corresponding to the PIO Line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is mentioned in the “Reset State” column, the PIO Line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case of pins controlling memories, in particular the address lines, which require the pin to be driven as soon as the reset is released.

- “I”/”O”

Indicates whether the signal is input or output state.

- “PU”/”PD”

Indicates whether Pull-Up, Pull-Down or nothing is enabled.

- "ST"

Indicates if Schmitt Trigger is enabled.

Note: Example: The PB18 "Reset State" column shows "PIO, I, PU, ST". That means the line PIO18 is configured as an Input with Pull-Up and Schmitt Trigger enabled. PD14 reset state is "PIO, I, PU". That means PIO Input with Pull-Up. PD15 reset state is "A20, O, PD" which means output address line 20 with Pull-Down.

4.3 217-ball BGA Package Pinout

Table 4-3. Pin Description BGA217

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
L3	VDDIOP0	GPIO	PA0	I/O			TXD0	O	SPI1_NPCS1	O			PIO, I, PU, ST
P1	VDDIOP0	GPIO	PA1	I/O			RXD0	I	SPI0_NPCS2	O			PIO, I, PU, ST
L4	VDDIOP0	GPIO	PA2	I/O			RTS0	O	MCI1_DA1	I/O	ETX0	O	PIO, I, PU, ST
N4	VDDIOP0	GPIO	PA3	I/O			CTS0	I	MCI1_DA2	I/O	ETX1	O	PIO, I, PU, ST
T3	VDDIOP0	GPIO	PA4	I/O			SCK0	I/O	MCI1_DA3	I/O			PIO, I, PU, ST
R1	VDDIOP0	GPIO	PA5	I/O			TXD1	O	CANTX1	O			PIO, I, PU, ST
R4	VDDIOP0	GPIO	PA6	I/O			RXD1	I	CANRX1	I			PIO, I, PU, ST
R3	VDDIOP0	GPIO	PA7	I/O			TXD2	O	SPI0_NPCS1	O			PIO, I, PU, ST
P4	VDDIOP0	GPIO	PA8	I/O			RXD2	I	SPI1_NPCS0	I/O			PIO, I, PU, ST
U3	VDDIOP0	GPIO	PA9	I/O			DRXD	I	CANRX0	I			PIO, I, PU, ST
T1	VDDIOP0	GPIO	PA10	I/O			DTXD	O	CANTX0	O			PIO, I, PU, ST
U1	VDDIOP0	GPIO	PA11	I/O			SPI0_MISO	I/O	MCI1_DA0	I/O			PIO, I, PU, ST
T2	VDDIOP0	GPIO	PA12	I/O			SPI0_MOSI	I/O	MCI1_CDA	I/O			PIO, I, PU, ST
T4	VDDIOP0	GPIO_CLK	PA13	I/O			SPI0_SPCK	I/O	MCI1_CK	I/O			PIO, I, PU, ST
U2	VDDIOP0	GPIO	PA14	I/O			SPI0_NPCS0	I/O					PIO, I, PU, ST
U4	VDDIOP0	GPIO	PA15	I/O			MCI0_DA0	I/O					PIO, I, PU, ST
P5	VDDIOP0	GPIO	PA16	I/O			MCI0_CDA	I/O					PIO, I, PU, ST
R5	VDDIOP0	GPIO_CLK	PA17	I/O			MCI0_CK	I/O					PIO, I, PU, ST
U5	VDDIOP0	GPIO	PA18	I/O			MCI0_DA1	I/O					PIO, I, PU, ST
T5	VDDIOP0	GPIO	PA19	I/O			MCI0_DA2	I/O					PIO, I, PU, ST
U6	VDDIOP0	GPIO	PA20	I/O			MCI0_DA3	I/O					PIO, I, PU, ST
T6	VDDIOP0	GPIO	PA21	I/O			TIOA0	I/O	SPI1_MISO	I/O			PIO, I, PU, ST
R6	VDDIOP0	GPIO	PA22	I/O			TIOA1	I/O	SPI1_MOSI	I/O			PIO, I, PU, ST
U7	VDDIOP0	GPIO_CLK	PA23	I/O			TIOA2	I/O	SPI1_SPCK	I/O			PIO, I, PU, ST
T7	VDDIOP0	GPIO	PA24	I/O			TCLK0	I	TK	I/O			PIO, I, PU, ST
T8	VDDIOP0	GPIO	PA25	I/O			TCLK1	I	TF	I/O			PIO, I, PU, ST
R7	VDDIOP0	GPIO	PA26	I/O			TCLK2	I	TD	O			PIO, I, PU, ST
P8	VDDIOP0	GPIO	PA27	I/O			TIOB0	I/O	RD	I			PIO, I, PU, ST
U8	VDDIOP0	GPIO	PA28	I/O			TIOB1	I/O	RK	I/O			PIO, I, PU, ST
R9	VDDIOP0	GPIO	PA29	I/O			TIOB2	I/O	RF	I/O			PIO, I, PU, ST
R8	VDDIOP0	GPIO	PA30	I/O			TWD0	I/O	SPI1_NPCS3	O	EMDC	O	PIO, I, PU, ST
U9	VDDIOP0	GPIO	PA31	I/O			TWCK0	O	SPI1_NPCS2	O	ETXEN	O	PIO, I, PU, ST
D3	VDDANA	GPIO	PB0	I/O			ERX0	I	RTS2	O			PIO, I, PU, ST
D4	VDDANA	GPIO	PB1	I/O			ERX1	I	CTS2	I			PIO, I, PU, ST

Table 4-3. Pin Description BGA217 (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
D2	VDDANA	GPIO	PB2	I/O			ERXER	I	SCK2	I/O			PIO, I, PU, ST
E4	VDDANA	GPIO	PB3	I/O			ERXDV	I	SPI0_NPCS3	O			PIO, I, PU, ST
D1	VDDANA	GPIO_CLK	PB4	I/O			ETXCK	I	TWD2	I/O			PIO, I, PU, ST
E3	VDDANA	GPIO	PB5	I/O			EMDIO	I/O	TWCK2	O			PIO, I, PU, ST
B3	VDDANA	GPIO_ANA	PB6	I/O	AD7	I	EMDC	O					PIO, I, PU, ST
C2	VDDANA	GPIO_ANA	PB7	I/O	AD8	I	ETXEN	O					PIO, I, PU, ST
C5	VDDANA	GPIO_ANA	PB8	I/O	AD9	I							PIO, I, PU, ST
C1	VDDANA	GPIO_ANA	PB9	I/O	AD10	I	ETX0	O	PCK1	O			PIO, I, PU, ST
B2	VDDANA	GPIO_ANA	PB10	I/O	AD11	I	ETX1	O	PCK0	O			PIO, I, PU, ST
A3	VDDANA	GPIO_ANA	PB11	I/O	AD0	II			PWM0	O			PIO, I, PU, ST
B4	VDDANA	GPIO_ANA	PB12	I/O	AD1	II			PWM1	O			PIO, I, PU, ST
A2	VDDANA	GPIO_ANA	PB13	I/O	AD2	II			PWM2	O			PIO, I, PU, ST
C4	VDDANA	GPIO_ANA	PB14	I/O	AD3	II			PWM3	O			PIO, I, PU, ST
C3	VDDANA	GPIO_ANA	PB15	I/O	AD4	II							PIO, I, PU, ST
A1	VDDANA	GPIO_ANA	PB16	I/O	AD5	I				I			PIO, I, PU, ST
B1	VDDANA	GPIO_ANA	PB17	I/O	AD6	I				I			PIO, I, PU, ST
D5	VDDANA	GPIO	PB18	I/O			IRQ	I	ADTRG	I			PIO, I, PU, ST
E2	VDDIOP1	GPIO	PC0	I/O			LCDDAT0	O			TWD1	I/O	PIO, I, PU, ST
F4	VDDIOP1	GPIO	PC1	I/O			LCDDAT1	O			TWCK1	O	PIO, I, PU, ST
F3	VDDIOP1	GPIO	PC2	I/O			LCDDAT2	O			TIOA3	I/O	PIO, I, PU, ST
H2	VDDIOP1	GPIO	PC3	I/O			LCDDAT3	O			TIOB3	I/O	PIO, I, PU, ST
E1	VDDIOP1	GPIO	PC4	I/O			LCDDAT4	O			TCLK3	I	PIO, I, PU, ST
G4	VDDIOP1	GPIO	PC5	I/O			LCDDAT5	O			TIOA4	I/O	PIO, I, PU, ST
F2	VDDIOP1	GPIO	PC6	I/O			LCDDAT6	O			TIOB4	I/O	PIO, I, PU, ST
F1	VDDIOP1	GPIO	PC7	I/O			LCDDAT7	O			TCLK4	I	PIO, I, PU, ST
G1	VDDIOP1	GPIO	PC8	I/O			LCDDAT8	O			UTXD0	O	PIO, I, PU, ST
G3	VDDIOP1	GPIO	PC9	I/O			LCDDAT9	O			URXD0	I	PIO, I, PU, ST
G2	VDDIOP1	GPIO	PC10	I/O			LCDDAT10	O			PWM0	O	PIO, I, PU, ST
H3	VDDIOP1	GPIO	PC11	I/O			LCDDAT11	O			PWM1	O	PIO, I, PU, ST
J3	VDDIOP1	GPIO	PC12	I/O			LCDDAT12	O			TIOA5	I/O	PIO, I, PU, ST
L2	VDDIOP1	GPIO	PC13	I/O			LCDDAT13	O			TIOB5	I/O	PIO, I, PU, ST
H1	VDDIOP1	GPIO	PC14	I/O			LCDDAT14	O			TCLK5	I	PIO, I, PU, ST
J2	VDDIOP1	GPIO_CLK	PC15	I/O			LCDDAT15	O			PCK0	O	PIO, I, PU, ST
J1	VDDIOP1	GPIO	PC16	I/O			LCDDAT16	O			UTXD1	O	PIO, I, PU, ST
L1	VDDIOP1	GPIO	PC17	I/O			LCDDAT17	O			URXD1	I	PIO, I, PU, ST
K2	VDDIOP1	GPIO	PC18	I/O			LCDDAT18	O			PWM0	O	PIO, I, PU, ST
N3	VDDIOP1	GPIO	PC19	I/O			LCDDAT19	O			PWM1	O	PIO, I, PU, ST
K1	VDDIOP1	GPIO	PC20	I/O			LCDDAT20	O			PWM2	O	PIO, I, PU, ST
M3	VDDIOP1	GPIO	PC21	I/O			LCDDAT21	O			PWM3	O	PIO, I, PU, ST
P3	VDDIOP1	GPIO	PC22	I/O			LCDDAT22	O					PIO, I, PU, ST
J4	VDDIOP1	GPIO	PC23	I/O			LCDDAT23	O					PIO, I, PU, ST
K3	VDDIOP1	GPIO	PC24	I/O			LCDDISP	O					PIO, I, PU, ST
M2	VDDIOP1	GPIO	PC25	I/O									PIO, I, PU, ST

Table 4-3. Pin Description BGA217 (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
P2	VDDIOP1	GPIO	PC26	I/O			LCDPWM	O					PIO, I, PU, ST
M1	VDDIOP1	GPIO	PC27	I/O			LCDVSYNC	O			RTS1	O	PIO, I, PU, ST
K4	VDDIOP1	GPIO	PC28	I/O			LCDHSYNC	O			CTS1	I	PIO, I, PU, ST
N1	VDDIOP1	GPIO_CLK	PC29	I/O			LCDDEN	O			SCK1	I/O	PIO, I, PU, ST
R2	VDDIOP1	GPIO_CLK2	PC30	I/O			LCDPCK	O					PIO, I, PU, ST
N2	VDDIOP1	GPIO	PC31	I/O			FIQ	I			PCK1	O	PIO, I, PU, ST
P13	VDDNF	EBI	PD0	I/O			NANDOE	O					PIO, I, PU
R14	VDDNF	EBI	PD1	I/O			NANDWE	O					PIO, I, PU
R13	VDDNF	EBI	PD2	I/O			A21/NANDALE	O					A21,O, PD
P15	VDDNF	EBI	PD3	I/O			A22/NANDCLE	O					A22,O, PD
P12	VDDNF	EBI	PD4	I/O			NCS3	O					PIO, I, PU
P14	VDDNF	EBI	PD5	I/O			NWAIT	I					PIO, I, PU
N14	VDDNF	EBI	PD6	I/O			D16	O					PIO, I, PU
R15	VDDNF	EBI	PD7	I/O			D17	O					PIO, I, PU
M14	VDDNF	EBI	PD8	I/O			D18	O					PIO, I, PU
N16	VDDNF	EBI	PD9	I/O			D19	O					PIO, I, PU
N17	VDDNF	EBI	PD10	I/O			D20	O					PIO, I, PU
N15	VDDNF	EBI	PD11	I/O			D21	O					PIO, I, PU
K15	VDDNF	EBI	PD12	I/O			D22	O					PIO, I, PU
M15	VDDNF	EBI	PD13	I/O			D23	O					PIO, I, PU
L14	VDDNF	EBI	PD14	I/O			D24	O					PIO, I, PU
M16	VDDNF	EBI	PD15	I/O			D25	O	A20	O			A20, O, PD
L16	VDDNF	EBI	PD16	I/O			D26	O	A23	O			A23, O, PD
L15	VDDNF	EBI	PD17	I/O			D27	O	A24	O			A24, O, PD
K17	VDDNF	EBI	PD18	I/O			D28	O	A25	O			A25, O, PD
J17	VDDNF	EBI	PD19	I/O			D29	O	NCS2	O			PIO, I, PU
K16	VDDNF	EBI	PD20	I/O			D30	O	NCS4	O			PIO, I, PU
J16	VDDNF	EBI	PD21	I/O			D31	O	NCS5	O			PIO, I, PU
D10, D13, F14	VDDIOM	POWER	VDDIOM	I									I
J14, K14	VDDNF	POWER	VDDNF	I									I
H9, H10, J9, J10	GNDIOM	GND	GNDIOM	I									I
P7	VDDIOP0	POWER	VDDIOP0	I									I
H4	VDDIOP1	POWER	VDDIOP1	I									I
M4, P6	GNDIOP	GND	GNDIOP	I									I
B5	VDDBU	POWER	VDDBU	I									I
B6	GNDBU	GND	GNDBU	I									I
C6	VDDANA	POWER	VDDANA	I									I
D6	GNDANA	GND	GNDANA	I									I
R12	VDDPLLA	POWER	VDDPLLA	I									I
T13	VDDOSC	POWER	VDDOSC	I									I

Table 4-3. Pin Description BGA217 (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
U13	GNDOSC	GND	GNDOSC	I									I
H14, K8, K9	VDDCORE	POWER	VDDCORE	I									I
H8, J8, K10	GNDCORE	GND	GNDCORE	I									I
U16	VDDUTMII	POWER	VDDUTMII	I									I
T17	VDDUTMIC	POWER	VDDUTMIC	I									I
T16	GNDUTMI	GND	GNDUTMI	I									I
D14	VDDIOM	EBI	D0	I/O									O, PD
D15	VDDIOM	EBI	D1	I/O									O, PD
A16	VDDIOM	EBI	D2	I/O									O, PD
B16	VDDIOM	EBI	D3	I/O									O, PD
A17	VDDIOM	EBI	D4	I/O									O, PD
B15	VDDIOM	EBI	D5	I/O									O, PD
C14	VDDIOM	EBI	D6	I/O									O, PD
B14	VDDIOM	EBI	D7	I/O									O, PD
A15	VDDIOM	EBI	D8	I/O									O, PD
C15	VDDIOM	EBI	D9	I/O									O, PD
D12	VDDIOM	EBI	D10	I/O									O, PD
C13	VDDIOM	EBI	D11	I/O									O, PD
A14	VDDIOM	EBI	D12	I/O									O, PD
B13	VDDIOM	EBI	D13	I/O									O, PD
A13	VDDIOM	EBI	D14	I/O									O, PD
C12	VDDIOM	EBI	D15	I/O									O, PD
J15	VDDIOM	EBI_O	A0	O	NBS0	O							O, PD
H16	VDDIOM	EBI_O	A1	O	NBS2/DQM/ NWR2	O							O, PD
H15	VDDIOM	EBI_O	A2	O									O, PD
H17	VDDIOM	EBI_O	A3	O									O, PD
G17	VDDIOM	EBI_O	A4	O									O, PD
G16	VDDIOM	EBI_O	A5	O									O, PD
F17	VDDIOM	EBI_O	A6	O									O, PD
E17	VDDIOM	EBI_O	A7	O									O, PD
F16	VDDIOM	EBI_O	A8	O									O, PD
G15	VDDIOM	EBI_O	A9	O									O, PD
G14	VDDIOM	EBI_O	A10	O									O, PD
F15	VDDIOM	EBI_O	A11	O									O, PD
D17	VDDIOM	EBI_O	A12	O									O, PD
C17	VDDIOM	EBI_O	A13	O									O, PD
E16	VDDIOM	EBI_O	A14	O									O, PD
D16	VDDIOM	EBI_O	A15	O									O, PD
C16	VDDIOM	EBI_O	A16	O	BA0	O							O, PD
B17	VDDIOM	EBI_O	A17	O	BA1	O							O, PD
E15	VDDIOM	EBI_O	A18	O	BA2	O							O, PD

Table 4-3. Pin Description BGA217 (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
E14	VDDIOM	EBI_O	A19	O									O, PD
B9	VDDIOM	EBI_O	NCS0	O									O, PU
B8	VDDIOM	EBI_O	NCS1	O	SDCS	O							O, PU
D9	VDDIOM	EBI_O	NRD	O									O, PU
C9	VDDIOM	EBI_O	NWR0	O	NWRE	O							O, PU
C7	VDDIOM	EBI_O	NWR1	O	NBS1	O							O, PU
A8	VDDIOM	EBI_O	NWR3	O	NBS3/ DQM3	O							O, PU
D11	VDDIOM	EBI_CLK	SDCK	O									O
C11	VDDIOM	EBI_CLK	#SDCK	O									O
B12	VDDIOM	EBI_O	SDCKE	O									O, PU
B11	VDDIOM	EBI_O	RAS	O									O, PU
C10	VDDIOM	EBI_O	CAS	O									O, PU
A12	VDDIOM	EBI_O	SDWE	O									O, PU
C8	VDDIOM	EBI_O	SDA10	O									O, PU
A10	VDDIOM	EBI_O	DQM0	O									O, PU
B10	VDDIOM	EBI_O	DQM1	O									O, PU
A11	VDDIOM	EBI	DQS0	I/O									O, PD
A9	VDDIOM	EBI	DQS1	I/O									O, PD
A4	VDDANA	POWER	ADVREF	I									I
U17	VDDUTMIC	VBG	VBG	I									I
T14	VDDUTMII	USBFS	HFSDPA	I/O	DFSDP	I/O							O, PD
T15	VDDUTMII	USBFS	HFSDMA	I/O	DFSDM	I/O							O, PD
U14	VDDUTMII	USBHS	HHSDPA	I/O	DHSDP	I/O							O, PD
U15	VDDUTMII	USBHS	HHSDMA	I/O	DHSDM	I/O							O, PD
R16	VDDUTMII	USBFS	HFSDPB	I/O									O, PD
P16	VDDUTMII	USBFS	HFSDMB	I/O									O, PD
R17	VDDUTMII	USBHS	HHSDPB	I/O									O, PD
P17	VDDUTMII	USBHS	HHSDMB	I/O									O, PD
L17	VDDUTMII	USBFS	HFSDPC	I/O									O, PD
M17	VDDUTMII	USBFS	HFSDMC	I/O									O, PD
R11	VDDIOP0	DIB	DIBN	I/O									O, PU
P11	VDDIOP0	DIB	DIBP	I/O									O, PU
A7	VDDBU	SYSC	WKUP	I									I, ST
D8	VDDBU	SYSC	SHDN	O									O, PU
P9	VDDIOP0	RSTJTAG	BMS	I									I, PD, ST
D7	VDDBU	SYSC	JTAGSEL	I									I, PD
B7	VDDBU	SYSC	TST	I									I, PD, ST
U10	VDDIOP0	RSTJTAG	TCK	I									I, ST
T9	VDDIOP0	RSTJTAG	TDI	I									I, ST
T10	VDDIOP0	RSTJTAG	TDO	O									O
U11	VDDIOP0	RSTJTAG	TMS	I									I, ST
R10	VDDIOP0	RSTJTAG	RTCK	O									O

Table 4-3. Pin Description BGA217 (Continued)

			Primary		Alternate		PIO Peripheral A		PIO Peripheral B		PIO Peripheral C		Reset State
Ball	Power Rail	I/O Type	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir	Signal, Dir, PU, PD, ST
P10	VDDIOP0	RSTJTAG	NRST	I/O									I, PU, ST
T11	VDDIOP0	RSTJTAG	NTRST	I									I, PU, ST
A6	VDDBU	CLOCK	XIN32	I									I
A5	VDDBU	CLOCK	XOUT32	O									O
T12	VDDOSC	CLOCK	XIN	I									I
U12	VDDOSC	CLOCK	XOUT	O									O

5. Power Considerations

5.1 Power Supplies

The SAM9X35 has several types of power supply pins.

Table 5-1. SAM9X35 Power Supplies

Name	Voltage Range, nominal	Powers	Associated Ground
VDDCORE	0.9-1.1V, 1.0V	ARM core, internal memories, internal peripherals and part of the system controller.	GNDCORE
VDDIOM	1.65-1.95V, 1.8V 3.0-3.6V, 3.3V	External Memory Interface I/O lines	GNDIOM
VDDNF	1.65-1.95V, 1.8V 3.0-3.6V, 3.3V	NAND Flash I/O and control, D16-D32 and multiplexed SMC lines	GNDIOM
VDDIOP0	1.65-3.6V	a part of Peripheral I/O lines(1)	GNDIOP
VDDIOP1	1.65-3.6V	a part of Peripheral I/O lines (1)	GNDIOP
VDDBU	1.65-3.6V	the Slow Clock oscillator, the internal 32 kHz RC oscillator and backup part of the System Controller	GNDBU
VDDUTMIC	0.9-1.1V, 1.0V	the USB transceiver core logic	GNDUTMI
VDDUTMII	3.0-3.6V, 3.3V	the USB transceiver interface	GNDUTMI
VDDPLLA	0.9-1.1V, 1.0V	the PLLA cell	GNDOSC
VDDOSC	1.65-3.6V	the Main Oscillator cells	GNDOSC
VDDANA	3.0-3.6V, 3.3V	the Analog to Digital Converter	GNDANA

Note: 1. Refer to Table 4-2 for more details.

6. Processor and Architecture

6.1 ARM926EJ-S Processor

- RISC Processor Based on ARM v5TEJ Architecture with Jazelle technology for Java acceleration
- Two Instruction Sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- DSP Instruction Extensions
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 16 KB Data Cache, 16 KB Instruction Cache
  - Virtually-addressed 4-way Associative Cache
  - Eight words per line
  - Write-through and Write-back Operation
  - Pseudo-random or Round-robin Replacement
- Write Buffer
  - Main Write Buffer with 16-word Data Buffer and 4-address Buffer
  - DCache Write-back Buffer with 8-word Entries and a Single Address Entry
  - Software Control Drain
- Standard ARM v4 and v5 Memory Management Unit (MMU)
  - Access Permission for Sections
  - Access Permission for large pages and small pages can be specified separately for each quarter of the page
  - 16 embedded domains
- Bus Interface Unit (BIU)
  - Arbitrates and Schedules AHB Requests
  - Separate Masters for both instruction and data access providing complete Matrix system flexibility
  - Separate Address and Data Buses for both the 32-bit instruction interface and the 32-bit data interface
  - On Address and Data Buses, data can be 8-bit (Bytes), 16-bit (Half-words) or 32-bit (Words)

6.2 APB/AHB Bridge

The SAM9X35 product embeds two separated APB/AHB bridges.

This architecture enables to make concurrent access on both bridge.

Each peripheral can be clocked at a lower speed (MCK divided clock) in order to decrease the current consumption.

6.3 Bus Matrix

- 12-layer Matrix, handling requests from 11 masters
- Programmable Arbitration strategy
  - Fixed-priority Arbitration
  - Round-Robin Arbitration, either with no default master, last accessed default master or fixed default master
- Burst Management
  - Breaking with Slot Cycle Limit Support
  - Undefined Burst Length Support
- One Address Decoder provided per Master
  - Three different slaves may be assigned to each decoded memory area: one for internal ROM boot, one for internal flash boot, one after remap
- Boot Mode Select
  - Non-volatile Boot Memory can be internal ROM or external memory on EBI_NCS0
  - Selection is made by General purpose NVM bit sampled at reset
- Remap Command
  - Allows Remapping of an Internal SRAM in Place of the Boot Non-Volatile Memory (ROM or External Flash)
  - Allows Handling of Dynamic Exception Vectors

6.4 Matrix Masters

The Bus Matrix of the SAM9X35 product manages 12 masters, which means that each master can perform an access concurrently with others, to an available slave.

Each master has its own decoder, which is defined specifically for each master. In order to simplify the addressing, all the masters have the same decodings.

Table 6-1. List of Bus Matrix Masters

Master 0	ARM926 Instruction
Master 1	ARM926 Data
Master 2&3	DMA Controller 0
Master 4&5	DMA Controller 1
Master 6	UDP HS DMA
Master 7	UHP EHCI DMA
Master 8	UHP OHCI DMA
Master 9	LCD DMA
Master 10	EMAC DMA

6.5 Matrix Slaves

The Bus Matrix of the SAM9X35 product manages 9 slaves. Each slave has its own arbiter, allowing a different arbitration per slave.

Table 6-2. List of Bus Matrix Slaves

Slave 0	Internal SRAM
Slave 1	Internal ROM
Slave 2	Soft Modem (SMD)
Slave 3	USB Device High Speed Dual Port RAM (DPR)
	USB Host EHCI registers
	USB Host OHCI registers
Slave 4	External Bus Interface
Slave 5	DDR2 port 1
Slave 6	DDR2 port 2
Slave 7	DDR2 port 3
Slave 8	Peripheral Bridge 0
Slave 9	Peripheral Bridge 1

6.6 Master to Slave Access

All the Masters can normally access all the Slaves. However, some paths do not make sense, for example allowing access from the USB Device High speed DMA to the Internal Peripherals. Thus, these paths are forbidden or simply not wired, and shown as “-” in the following table.

Table 1. SAM9X35 Master to Slave Access

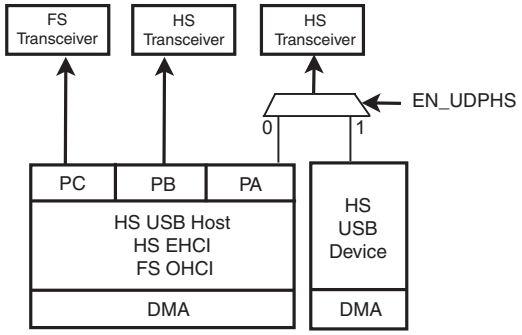
Masters		0	1	2&3	4&5	6	7	8	9	10
Slaves		ARM926 Instr.	ARM926 Data	DMA 0	DMA 1	USB Device HS DMA	USB Host HS EHCI	USB Host HS OHCI	LCD DMA	EMAC DMA
0	Internal SRAM	X	X	X	X	X	X	X	X	X
1	Internal ROM	X	X	X	X	-	-	-	-	-
2	SMD	X	X	-	X	-	-	-	-	-
3	USB Device High Speed DPR USB Host EHCI registers USB Host OHCI registers	X	X	-	-	-	-	-	-	-
4	External Bus Interface	X	X	X	X	X	X	X	X	X
5	DDR2 Port 1	X	-	X	-	-	-	-	-	-
6	DDR2 Port 2	-	X	-	X	-	-	-	-	-
7	DDR2 Port 3	-	-	-	-	-	-	-	X	-
8	Peripheral Bridge 0	X	X	X	X	-	-	-	-	-
9	Peripheral Bridge 1	X	X	X	X	-	-	-	-	-

6.7 USB

The SAM9X35 features the following USB communication ports:

- 2 Host (A and B) High Speed (EHCI) and Full Speed (OHCI)
- 1 Host (C) Full Speed only (OHCI)
- 1 Device High Speed

The High Speed USB Host Port A is shared with the High Speed USB Device port and connected to the second UTMI transceiver. The selection between Host Port A and USB Device is controlled by the UDPHS enable bit (EN_UDPHS) located in the UDPHS_CTRL control register.



6.8 DMA Controller 0

- Two Masters
- Embeds 8 channels
- 64-byte FIFO for channel 0, 16-byte FIFO for Channel 1 to 7
- features:
  - Linked List support with Status Write Back operation at End of Transfer
  - Word, HalfWord, Byte transfer support.
  - memory to memory transfer
  - Peripheral to memory
  - Memory to peripheral

The DMA controller can handle the transfer between peripherals and memory and so receives the triggers from the peripherals below. The hardware interface numbers are also given in Table 6-3

Table 6-3. DMA Channel Definition

Instance name	T/R	DMA Channel HW interface Number
HSMCI0	RX/TX	0
SPI0	TX	1
SPI0	RX	2
USART0	TX	3
USART0	RX	4
USART1	TX	5
USART1	RX	6
TWI0	TX	7
TWI0	RX	8
TWI2	TX	9
TWI2	RX	10
UART0	TX	11
UART0	RX	12
SSC	TX	13
SSC	RX	14

6.9 DMA Controller 1

- Two Masters
- Embeds 8 channels
- 16-bytes FIFO per Channel
- features:
  - Linked List support with Status Write Back operation at End of Transfer
  - Word, HalfWord, Byte transfer support.
  - Peripheral to memory
  - Memory to peripheral

The DMA controller can handle the transfer between peripherals and memory and so receives the triggers from the peripherals below. The hardware interface numbers are also given in Table 6-4

Table 6-4. DMA Channel Definition

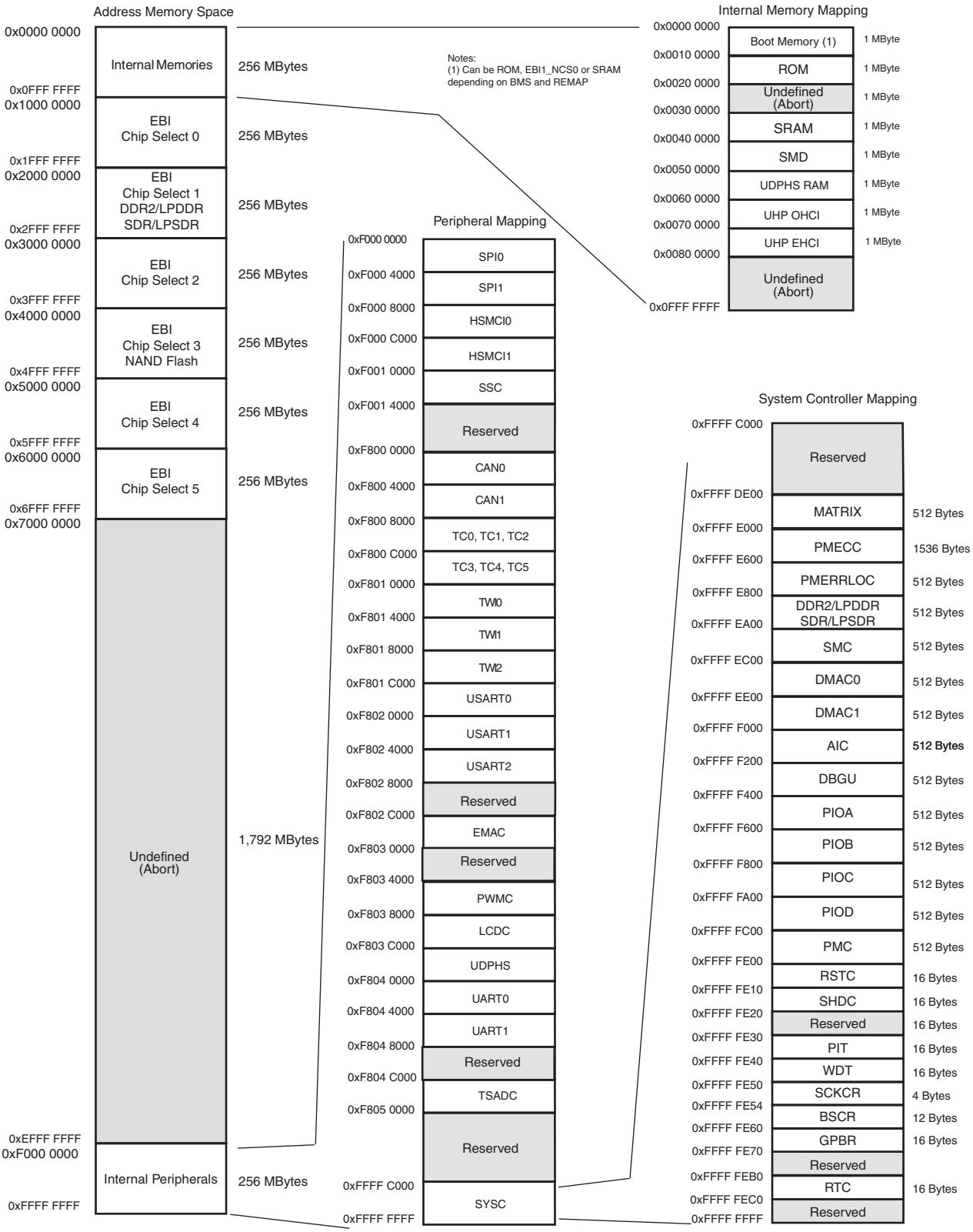
Instance name	T/R	DMA Channel HW interface Number
HSMCI1	RX/TX	0
SPI1	TX	1
SPI1	RX	2
SMD	TX	3
SMD	RX	4
TWI1	TX	5
TWI1	RX	6
ADC	RX	7
DBGU	TX	8
DBGU	RX	9
UART1	TX	10
UART1	RX	11
USART2	TX	12
USART2	RX	13

6.10 Debug and Test Features

- ARM926 Real-time In-circuit Emulator
  - Two real-time Watchpoint Units
  - Two Independent Registers: Debug Control Register and Debug Status Register
  - Test Access Port Accessible through JTAG Protocol
  - Debug Communications Channel
- Debug Unit
  - Two-pin UART
  - Debug Communication Channel Interrupt Handling
  - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on All Digital Pins.

7. Memories

Figure 7-1. SAM9X35 Memory Mapping



7.1 Memory Mapping

A first level of address decoding is performed by the AHB Bus Matrix, i.e., the implementation of the Advanced High performance Bus (AHB) for its Master and Slave interfaces with additional features.

Decoding breaks up the 4 Gbytes of address space into 16 banks of 256 Mbytes. Banks 1 to 6 are directed to the EBI that associates these banks to the external chip selects, EBI_NCS0 to EBI_NCS5. Bank 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1 Mbyte of internal memory area. Bank 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

7.2 Embedded Memories

7.2.1 Internal SRAM

The SAM9X35 embeds a total of 32 Kbytes of high-speed SRAM.

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0030 0000.

After Remap, the SRAM also becomes available at address 0x0.

7.2.2 Internal ROM

The SAM9X35 embeds an Internal ROM, which contains the SAM-BA program.

At any time, the ROM is mapped at address 0x0010 0000. It is also accessible at address 0x0 (BMS = 1) after the reset and before the Remap Command.

7.3 External Memories

7.3.1 External Bus Interface

- Integrates three External Memory Controllers:
  - Static Memory Controller
  - DDR2/SDRAM Controller
  - MLC NAND Flash ECC Controller
- Additional logic for NAND Flash and CompactFlash®
- Up to 26-bit Address Bus (up to 64 MBytes linear per chip select)
- Up to 6 chips selects, Configurable Assignment:
  - Static Memory Controller on NCS0, NCS1, NCS2, NCS3, NCS4, NCS5
  - DDR2/SDRAM Controller (SDCS) or Static Memory Controller on NCS1
  - Optional NAND Flash support on NCS3

7.3.2 Static Memory Controller

- 8- or 16-bit Data Bus
- Multiple Access Modes supported
  - Byte Write or Byte Select Lines
  - Asynchronous read in Page Mode supported (4- up to 16-byte page size)

- Multiple device adaptability
  - Control signals programmable setup, pulse and hold time for each Memory Bank
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time
- Slow Clock mode supported

7.3.3 DDR2SDR Controller

- Supports 8-bank DDR2, LPDDR2, SDR and LPSDR
- Numerous Configurations Supported
  - 2K, 4K, 8K, 16K Row Address Memory Parts
  - SDRAM with 8 Internal Banks
  - SDR-SDRAM with 32-bit Data Path
  - DDR2/LPDDR with 16-bit Data Path
  - One Chip Select for SDRAM Device (256 Mbyte Address Space)
- Programming Facilities
  - Multibank Ping-pong Access (Up to 8 Banks Opened at Same Time = Reduces Average Latency of Transactions)
  - Timing Parameters Specified by Software
  - Automatic Refresh Operation, Refresh Rate is Programmable
  - Automatic Update of DS, TCR and PASR Parameters (LPSDR)
- Energy-saving Capabilities
  - Self-refresh, Power-down and Deep Power Modes Supported
- SDRAM Power-up Initialization by Software
- CAS Latency of 2, 3 Supported
- Auto Precharge Command Not Used
- SDR-SDRAM with 16-bit Datapath and Eight Columns Not Supported
  - Clock Frequency Change in Precharge Power-down Mode Not Supported

8. System Controller

The System Controller is a set of peripherals that allows handling of key elements of the system, such as power, resets, clocks, time, interrupts, watchdog, etc.

The System Controller User Interface also embeds the registers that configure the Matrix and a set of registers for the chip configuration. The chip configuration registers configure the EBI chip select assignment and voltage range for external memories.

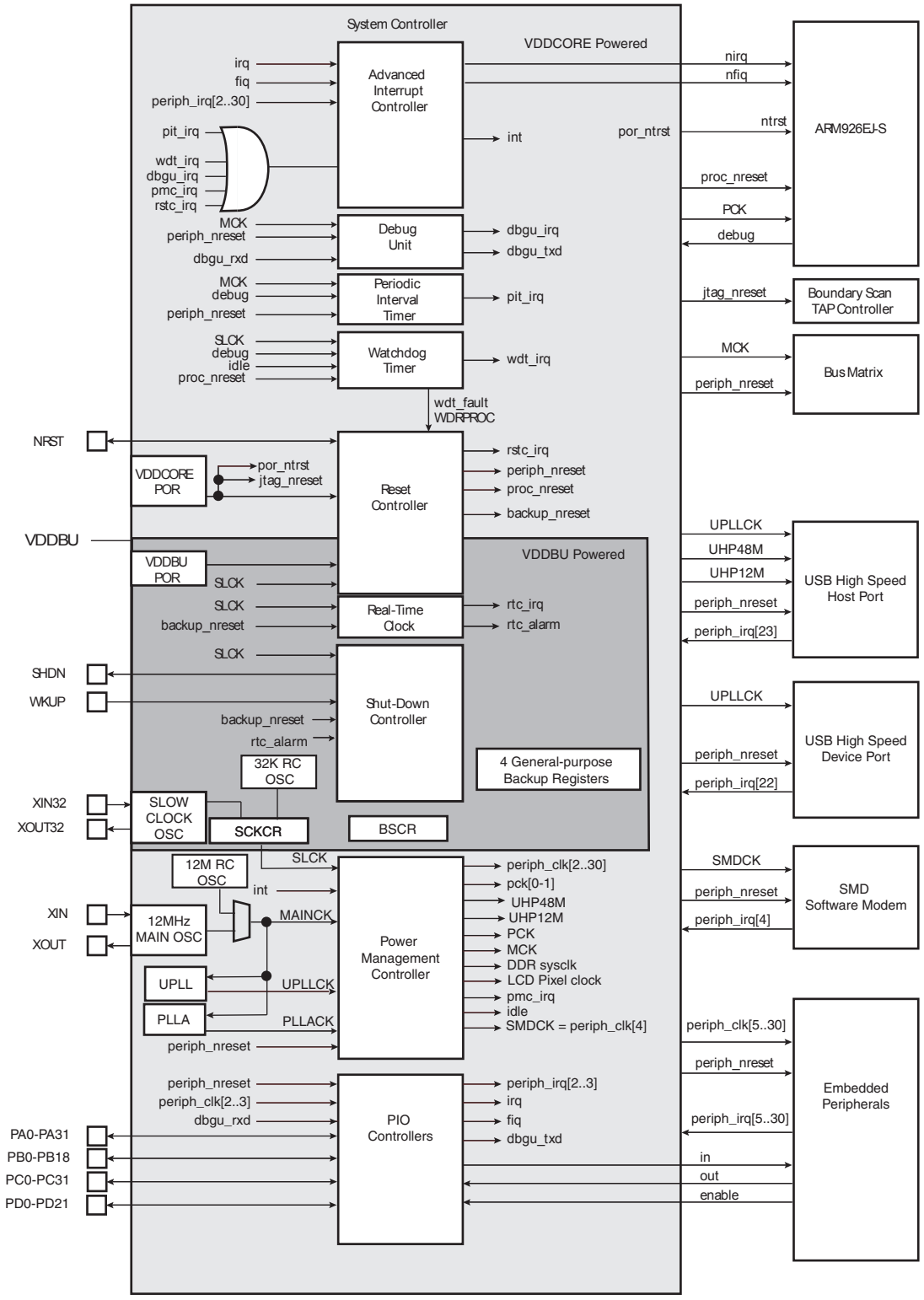
The System Controller's peripherals are all mapped within the highest 16 KBytes of address space, between addresses 0xFFFF C000 and 0xFFFF FFFF.

However, all the registers of System Controller are mapped on the top of the address space. All the registers of the System Controller can be addressed from a single pointer by using the standard ARM instruction set, as the Load/Store instruction have an indexing mode of ±4 KBytes.

Figure 8-1 shows the System Controller block diagram.

Figure 7-1 shows the mapping of the User Interface of the System Controller peripherals.

Figure 8-1. SAM9X35 System Controller Block Diagram



8.1 Chip Identification

- Chip ID: 0x819A_05A1
- Chip ID Extension: 2
- JTAG ID: 0x05B2_F03F
- ARM926 TAP ID: 0x0792_603F

8.2 Backup Section

The SAM9X35 features a Backup Section that embeds:

- RC Oscillator
- Slow Clock Oscillator
- Real Time Counter (RTC)
- Shutdown Controller
- 4 Backup Registers
- Slow Clock Control Register (SCKCR)
- Boot Sequence Configuration Register (BSCR)
- A part of the Reset Controller (RSTC)

This section is powered by the VDDBU rail.

9. Peripherals

9.1 Peripheral Mapping

As shown in Figure 7-1, the Peripherals are mapped in the upper 256 Mbytes of the address space between the addresses 0xF000 0000 and 0xFFFF C000.

Each User Peripheral is allocated 16 Kbytes of address space.

9.2 Peripheral Identifiers

Table 9-1 defines the Peripheral Identifiers of the SAM9X35. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 9-1. Peripheral Identifiers

Instance ID	Instance Name	Instance Description	External interrupt	Wired-OR interrupt
0	AIC	Advanced Interrupt Controller	FIQ	
1	SYS	System Controller Interrupt		DBGU, PMC, SYSC, PMECC, PMERRLOC
2	PIOA,PIOB	Parallel I/O Controller A and B		
3	PIOC,PIOD	Parallel I/O Controller C and D		
4	SMD	SMD Soft Modem		
5	USART0	USART 0		
6	USART1	USART 1		
7	USART2	USART 2		
9	TWI0	Two-Wire Interface 0		
10	TWI1	Two-Wire Interface 1		
11	TWI2	Two-Wire Interface 2		
12	HSMCI0	High Speed Multimedia Card Interface 0		
13	SPI0	Serial Peripheral Interface 0		
14	SPI1	Serial Peripheral Interface 1		
15	UART0	UART 0		
16	UART1	UART 1		
17	TC0,TC1	Timer Counter 0,1,2,3,4,5		
18	PWM	Pulse Width Modulation Controller		
19	ADC	ADC Controller		
20	DMAC0	DMA Controller 0		
21	DMAC1	DMA Controller 1		
22	UHPHS	USB Host High Speed		
23	UDPHS	USB Device High Speed		

Table 9-1. Peripheral Identifiers (Continued)

Instance ID	Instance Name	Instance Description	External interrupt	Wired-OR interrupt
24	**EMAC**	Ethernet MAC		
25	**LCDC**	LCD Controller		
26	**HSMCI1**	High Speed Multimedia Card Interface 1		
28	**SSC**	Synchronous Serial Controller		
29	**CAN0**	CAN Controller 0		
30	**CAN1**	CAN Controller 1		
31	**AIC**	Advanced Interrupt Controller	IRQ	

9.3 Peripheral Signal Multiplexing on I/O Lines

The SAM9X35 features 4 PIO Controllers, PIOA, PIOB, PIOC and PIOD, which multiplex the I/O lines of the peripheral set.

Each PIO Controller controls 32 lines, 19 lines, 32 lines and 22 lines respectively for PIOA, PIOB, PIOC and PIOD. Each line can be assigned to one of three peripheral functions, A, B or C. Refer to Section 4. “Package and Pinout”, Table 4-3 to see the PIO assignments.

10. Embedded Peripherals Overview

10.1 Serial Peripheral Interface (SPI)

- Two SPIs
- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Very fast transfers supported
  - Transfers with baud rates up to MCK
  - The chip select line may be left active to speed up transfers on the same device

10.2 Two Wire Interface (TWI)

- Two TWIs
- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential read/write operations
- Supports either master or slave modes
- Compatible with Standard Two-wire Serial Memories
- Master, Multi-master and Slave Mode Operation
- Bit Rate: Up to 400 Kbits
- General Call Supported in Slave mode

10.3 Universal Synchronous/Asynchronous Receiver Transmitters (USART)

- Three USARTs
- Manchester Encoding/Decoding
- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection

  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Hardware handshaking RTS-CTS
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
  - Optional Manchester Encoding
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- SPI Mode
  - Master or Slave
  - Serial Clock Programmable Phase and Polarity
  - SPI Serial Clock (SCK) Frequency up to Internal Clock Frequency MCK/4
- LIN Mode
  - Compliant with LIN 1.3 and LIN 2.0 specifications
  - Master or Slave
  - Processing of frames with up to 256 data bytes
  - Response Data length can be configurable or defined automatically by the Identifier
  - Self synchronization in Slave node configuration
  - Automatic processing and verification of the “Synch Break” and the “Synch Field”
  - The “Synch Break” is detected even if it is partially superimposed with a data byte
  - Automatic Identifier parity calculation/sending and verification
  - Parity sending and verification can be disabled
  - Automatic Checksum calculation/sending and verification
  - Checksum sending and verification can be disabled
  - Support both “Classic” and “Enhanced” checksum types
  - Full LIN error checking and reporting
  - Frame Slot Mode: the Master allocates slots to the scheduled frames automatically.
  - Generation of the Wakeup signal
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo

10.4 Universal Asynchronous Receiver Transmitters (UART)

- Two UARTs
- Independent receiver and transmitter with a common programmable Baud Rate Generator
- Even, Odd, Mark or Space Parity Generation
- Parity, Framing and Overrun Error Detection
- Automatic Echo, Local Loopback and Remote Loopback Channel Modes

10.5 Serial Synchronous Controller (SSC)

- One SSC
- Provides serial synchronous communication links used in audio and telecom applications (with CODECs in Master or Slave Modes, I^2S, TDM Buses, Magnetic Card Reader, ...)
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.6 Timer Counter (TC)

- Dual three 32-bit Timer Counter Channels
- Double PWM generation
- Capture/Waveform mode
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting
  - Interval Measurement
  - Pulse Generation
  - Delay Timing
  - Pulse Width Modulation
  - Up/down Capabilities
- Each channel is user-configurable and contains:
  - Three external clock inputs
  - Five internal clock inputs
  - Two multi-purpose input/output signals
- Two global registers that act on all three TC Channels

10.7 High Speed Multimedia Card Interface (HSMCI)

- Two 4-bit HSMCI controllers
- Compatibility with MMC Plus Specification Version 4.3
- Compatibility with MultiMedia Card Specification Version 4.1
- Compatibility with SD Memory Card Specification Version 2.0
- Compatibility with SDIO Specification Version V2.0.
- Compatibility with CE ATA

10.8 High Speed USB Host Port (UHPHS)

- Compliant with EnhancedHCI Rev 1.0 Specification
  - Compliant with USB V2.0 High-speed and Full-speed Specification
  - Supports Both High-speed 480Mbps and Full-speed 12 Mbps USB devices
- Compliant with OpenHCI Rev 1.0 Specification
  - Compliant with USB V2.0 Full-speed and Low-speed Specification
  - Supports Both Low-speed 1.5 Mbps and Full-speed 12 Mbps USB devices
- Root Hub Integrated with 3 Downstream USB Ports
- Shared Embedded USB Transceivers
- Embedded one additional USB Full Speed Transceiver

10.9 USB High Speed Device Port (UDPHS)

- USB V2.0 high-speed compliant, 480 Mbits per second
- Embedded USB V2.0 UTMI+ high-speed transceiver shared with UHP HS.
- Embedded 4K-byte dual-port RAM for endpoints
- Embedded 6 channels DMA controller
- Suspend/Resume logic
- Up to 2 or 3 banks for isochronous and bulk endpoints
- Seven endpoints:
  - Endpoint 0: 64 bytes, 1 bank mode
  - Endpoint 1 & 2: 1024 bytes, DMA, 2 banks mode, HS isochronous capable
  - Endpoint 3 & 4:1024 bytes, DMA, 3 banks mode
  - Endpoint 5 & 6: 1024 bytes, DMA, 3 banks mode, HS isochronous capable

10.10 Analog-to-Digital Converter (ADC)

- 7-channel ADC
- 5-channel to support 4wire and 5-wire resistive Touch Screen
- 10-bit 384 Ksamples/sec. Successive Approximation Register ADC
- -3/+3 LSB Integral Non Linearity, -2/+2 LSB Differential Non Linearity
- Integrated 12-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger sources
  - Hardware or software trigger
  - External trigger pin
  - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
  - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Compare level interrupt for background signal surveillance

10.11 LCD Controller (LCDC)

- One Master
- Up to 266 MHz input clock
- 384-byte Asynchronous Output FIFO
- One Background Layer
- One High End Overlay Layer, YUV Full planar, 4.2.0, 4.2.2 packed
- One Overlay RGB
- One Hardware cursor with user-defined size
- Up to 24 bits per Pixel in TFT Mode
- Dithering for 12bpp, 16bpp and 18bpp modes
- LUT for 1bpp, 2bpp, 4bpp and 8bpp
- Resolution Up to 2048x2048 pixels
- Supported formats:
  - RGB: 444 (12bpp), 565 (16bpp), 666 (18bpp), 888 (24bpp and packed 24bpp)
  - Transparency + RGB: 1555 (16bpp), 1666 (19bpp and packed 19bpp), 1888 (25bpp)
  - Alpha + RGB or RGB + Alpha: 4444 (16bpp), 8888 (32bpp)
- alpha blending, color conversion, rotation
- scaling up to 800x600 pixels

10.12 Ethernet 10/100 MAC (EMAC)

- supports RMII Mode only
- Compatibility with IEEE Standard 802.3
- 10 and 100 Mbits per second data throughput capability
- Full- and half-duplex operations
- Register Interface to address, data, status and control registers
- DMA Interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 128-byte transmit and 128-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Support promiscuous mode where all valid frames are copied to memory
- Support physical layer management through MDIO interface
- Support Wake On Lan: The receiver supports Wake on LAN by detecting the following events on incoming receive frames:
  - Magic packet
  - ARP request to the device IP address
  - Specific address 1 filter match
  - Multicast hash filter match

10.13 8-channel DMA (DMAC)

- Two DMACs
- DMAC0 is full featured and optimized for memory-to-memory transfers thanks to the 64-word FIFO on channel 0
- DMAC1 is optimized for peripheral-to-memory transfers, without PIP support
- Acting as Two Matrix Masters
- Embeds 8 unidirectional channels with programmable priority
- Address Generation
  - Source / destination address programming
  - Address increment, decrement or no change
  - DMA chaining support for multiple non-contiguous data blocks through use of linked lists
  - Scatter support for placing fields into a system memory area from a contiguous transfer. Writing a stream of data into non-contiguous fields in system memory
  - Gather support for extracting fields from a system memory area into a contiguous transfer
  - User enabled auto-reloading of source, destination and control registers from initially programmed values at the end of a block transfer
  - Auto-loading of source, destination and control registers from system memory at end of block transfer in block chaining mode
  - Unaligned system address to data transfer width supported in hardware
  - Picture-In-Picture Mode (on DMAC0 only)
- Channel Buffering
  - 16-word FIFO (64-word for channel 0 of DMAC0)
  - Automatic packing/unpacking of data to fit FIFO width
- Channel Control
  - Programmable multiple transaction size for each channel
  - Support for cleanly disabling a channel without data loss
  - Suspend DMA operation
  - Programmable DMA lock transfer support
- Transfer Initiation
  - Support for Software handshaking interface. Memory mapped registers can be used to control the flow of a DMA transfer in place of a hardware handshaking interface
- Interrupt
  - Programmable Interrupt generation on DMA Transfer completion Block Transfer completion, Single/Multiple transaction completion or Error condition

10.14 CAN Controller (CAN)

- Fully Compliant with CAN 2.0 Part A and 2.0 Part B
- Bit Rates up to 1Mbit/s
- 8 Object Oriented Mailboxes with the Following Properties:
  - CAN Specification 2.0 Part A or 2.0 Part B Programmable for Each Message
  - Object Configurable in Receive (with Overwrite or Not) or Transmit Modes
  - Independent 29-bit Identifier and Mask Defined for Each Mailbox
  - 32-bit Access to Data Registers for Each Mailbox Data Object
  - Uses a 16-bit Timestamp on Receive and Transmit Messages
  - Hardware Concatenation of ID Masked Bitfields To Speed Up Family ID Processing
- 16-bit Internal Timer for Timestamping and Network Synchronization
- Programmable Reception Buffer Length up to 8 Mailbox Objects
- Priority Management between Transmission Mailboxes
- Autobaud and Listening Mode
- Low Power Mode and Programmable Wake-up on Bus Activity or by the Application
- Data, Remote, Error and Overload Frame Handling

10.15 Pulse Width Modulation Controller (PWM)

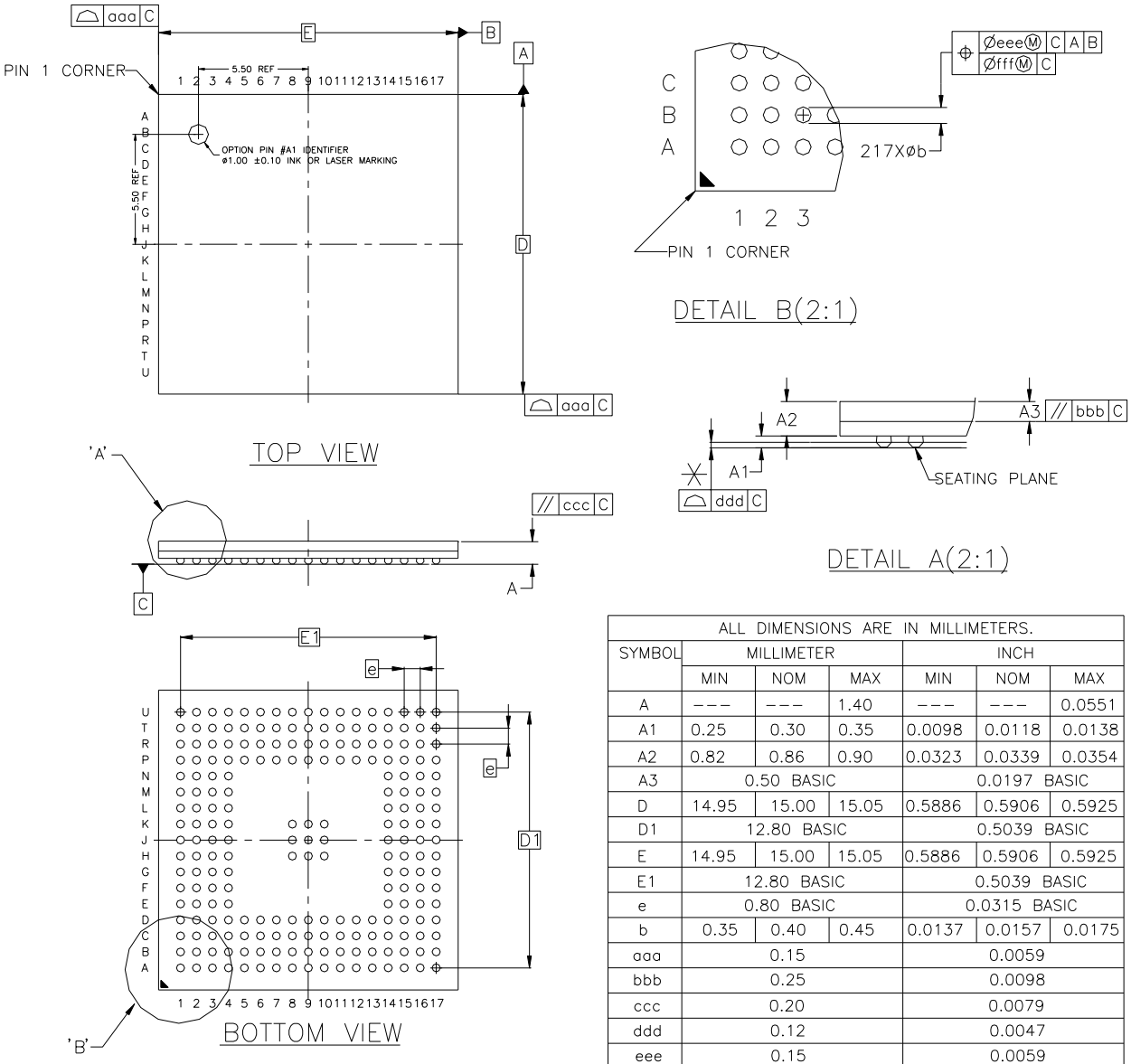
- 4 channels, one 32-bit counter per channel
- Common clock generator, providing Thirteen Different Clocks
  - A Modulo n counter providing eleven clocks
  - Two independent Linear Dividers working on modulo n counter outputs
- Independent channel programming
  - Independent Enable Disable Commands
  - Independent Clock Selection
  - Independent Period and Duty Cycle, with Double Bufferization
  - Programmable selection of the output waveform polarity
  - Programmable center or left aligned output waveform

10.16 Soft Modem (SMD)

- Modulations and protocols
  - V.90
  - V.34
  - V.32bis, V.32, V.22bis, V.22, V.23, V.21
  - V.23 reverse, V.23 half-duplex
  - Bell 212A/Bell 103
  - V.29 FastPOS
  - V.22bis fast connect
  - V.80 Synchronous Access Mode
- Data compression and error correction
  - V.44 data compression (V.92 model)
  - V.42bis and MNP 5 data compression
  - V.42 LAPM and MNP 2-4 error correction
  - EIA/TIA 578 Class 1 and T.31 Class 1.0
  - Call Waiting (CW) detection and Type II Caller ID decoding during data mode
- Type I Caller ID (CID) decoding
- Sixty-three embedded and upgradeable country profiles
- Embedded AT commands
- SmartDAA
  - Extension pick-up detection
  - Digital line protection
  - Line reversal detection
  - Line-in-use detection
  - Remote hang-up detection
  - Worldwide compliance

11. Mechanical Overview

Figure 11-1. 217-ball BGA Package Drawing



ALL DIMENSIONS ARE IN MILLIMETERS.						
SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.0551
A1	0.25	0.30	0.35	0.0098	0.0118	0.0138
A2	0.82	0.86	0.90	0.0323	0.0339	0.0354
A3	0.50 BASIC			0.0197 BASIC		
D	14.95	15.00	15.05	0.5886	0.5906	0.5925
D1	12.80 BASIC			0.5039 BASIC		
E	14.95	15.00	15.05	0.5886	0.5906	0.5925
E1	12.80 BASIC			0.5039 BASIC		
e	0.80 BASIC			0.0315 BASIC		
b	0.35	0.40	0.45	0.0137	0.0157	0.0175
aaa	0.15			0.0059		
bbb	0.25			0.0098		
ccc	0.20			0.0079		
ddd	0.12			0.0047		
eee	0.15			0.0059		
fff	0.08			0.0031		

Table 11-1. Device and 217-ball BGA Package Maximum Weight

450	mg

Table 11-2. 217-ball BGA Package Characteristics

Moisture Sensitivity Level	3

Table 11-3. Package Reference

JEDEC Drawing Reference	MO-205
JESD97 Classification	e1

Table 11-4. Soldering Information

Ball Land	0.43 mm ± 0.05
Solder Mask Opening	0.30 mm ± 0.05

12. SAM9X35 Ordering Information

Table 12-1. SAM9X35 Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT91SAM9X35-CU	BGA217	Green	Industrial -40°C to 85°C

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Product Contact

Web Site
www.atmel.com
www.atmel.com/AT91SAM

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AT91SAM Support
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