CYUSB3610

EZ-USB GX3: SuperSpeed USB to Gigabit Ethernet Bridge Controller

Features

- Low-power single chip USB 3.0 to 10/100/1000M Gigabit Ethernet Bridge Controller with Energy Efficient Ethernet (EEE)
- Gigabit Ethernet Controller
  - Supports IEEE 802.3az (Energy Efficient Ethernet)
  - IEEE 802.3, 802.3u, and 802.3ab compatible
  - Integrates 10/100/1000Mbps Gigabit Ethernet MAC/PHY
  - Supports dynamic cable length detection and dynamic power adjustment Green Ethernet (Gigabit mode only)
  - Supports parallel detection and automatic polarity correction
  - Supports crossover detection and auto-correction
  - Supports IPv4/IPv6 packet Checksum Offload Engine (COE) to reduce CPU loading, including IPv4 IP/TCP/UDP/ICMP/IGMP & IPv6 TCP/UDP/ICMPv6 checksum check & generation
  - Supports TCP Large Send Offload V1
  - Supports full duplex operation with IEEE 802.3x flow control and half duplex operation with back-pressure flow control.
  - Supports IEEE 802.1P Layer 2 Priority Encoding and Decoding
  - Supports IEEE 802.1Q VLAN tagging and 2 VLAN ID filtering; received VLAN Tag (4 bytes) can be stripped off or preserved
  - Supports Jumbo frame
  - PHY loop-back diagnostic capability
- USB Device Controller
  - Integrates on-chip USB 3.0 PHY and controller
  - Supports USB 3.0 power saving modes (U0, U1, U2, and U3)
  - High performance packet transfer rate over USB bus using burst transfer mechanism
- Advanced Power Management Features
  - Supports power management offload (ARP & NS)
  - Supports dynamic power management to reduce power dissipation during idle or light traffic
  - Supports AutoDetach power saving. Soft-disconnect from USB host when Ethernet cable is unplugged
  - Supports advanced link down power saving when Ethernet cable is unplugged
- Wake-on-LAN Feature
  - Supports suspend mode and remote wakeup via link-change, Magic Packet, Microsoft wakeup frame and external wakeup pin
  - Supports Bonjour wake-on-demand
- Supports serial EEPROM (93C56/66) for storing USB Descriptors, Node-ID, etc
- Supports automatic loading of USB Device Descriptors, Node-ID, etc. from internal memory or external EEPROM after power-on initialization
- Single 25 MHz clock input from crystal or oscillator source
- Integrates on-chip power-on reset circuit
- Integrates pipelined RISC SoC (System on Chip) for handling protocol and control functions
- 68-pin QFN 8 mm × 8 mm RoHS/REACH compliant package
- Operating temperature: 0 °C to 70 °C

Target Applications

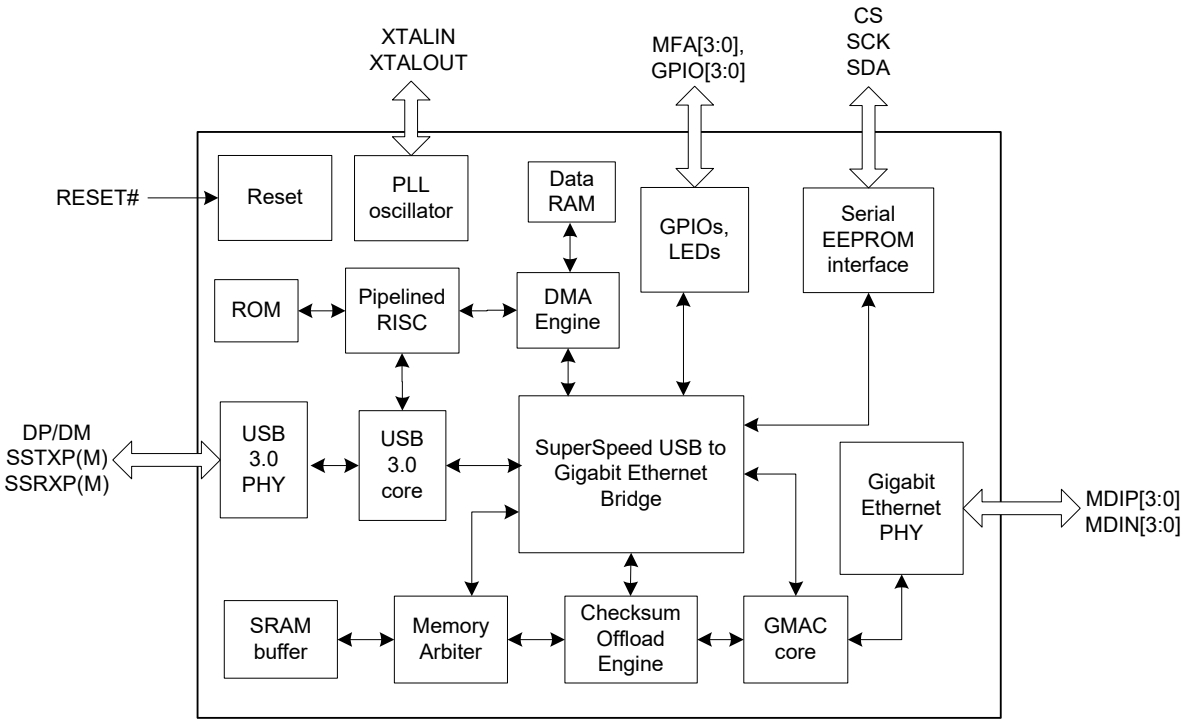
- Docking Station
- USB Dongle
- Embedded systems
- Network Printer
- USB Port Replicator
- POS, Card Reader
- Netbook, UMPC, MID
- Ultrabook
- IP STB, IP TV
- Gaming Console

Functional Description

The GX3 SuperSpeed USB to 10/100/1000M Gigabit Ethernet Bridge Controller is a high-performance and highly integrated controller that enables low-cost design, small form-factor, and simple plug-and-play Gigabit Ethernet network connection capability for docking stations, desktops, notebook PCs, Ultrabooks, gaming consoles, digital-home appliances, and any embedded system using a standard USB port.

GX3 implements a 10/100/1000Mbps Ethernet LAN function based on IEEE802.3, IEEE802.3u, and IEEE802.3ab standards with embedded SRAMs for packet buffering. It also integrates an on-chip 10/100/1000Mbps EEE-compliant Ethernet PHY to simplify system design. It features a USB interface to communicate with a USB Host Controller and is compliant with USB specification v3.0.

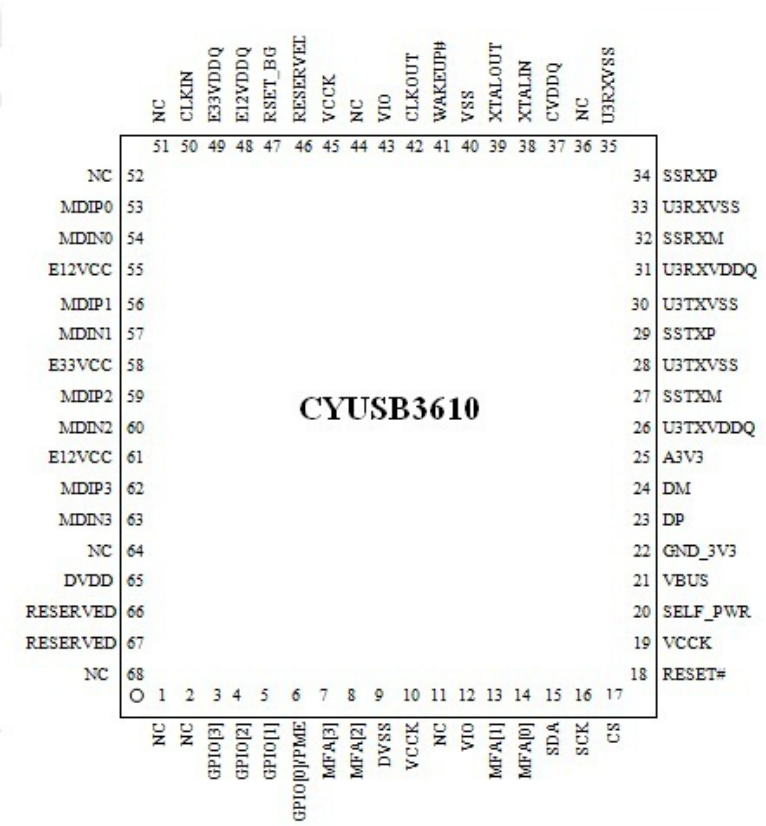
Block Diagram



Contents

Pin Configurations

Figure 1. 68-pin QFN pinout



Signal Description

The following abbreviations apply to the following pin description table.

Signal Name	Signal Description	Signal Name	Signal Description
I12	Input, 1.2 V	AI	Analog Input
I3	Input, 3.3 V	AO	Analog Output
I5	Input, 3.3 V with 5 V tolerance	AB	Analog Bi-directional I/O
O3	Output, 3.3 V	PU	Internal Pull Up (75 kΩ)
B5	Bi-directional I/O, 3.3 V with 5 V tolerance	PD	Internal Pull Down (75 kΩ)
B3	Bi-directional I/O, 3.3 V	S	Schmitt Trigger
P	Power/GND	T	Tri-stateable

Pin Description

Pin Name	Type	Pin No.	Pin Description
USB Interface			
DP	AB	23	USB 2.0 D+ pin.
DM	AB	24	USB 2.0 D– pin.
SSTXP	AB	29	USB 3.0 SSTX+ pin.
SSTXM	AB	27	USB 3.0 SSTX– pin.
SSRXP	AB	34	USB 3.0 SSRX+ pin.
SSRXM	AB	32	USB 3.0 SSRX– pin.
VBUS	I5/PD/S	21	VBUS pin input. Please connect to USB bus power.
Gigabit EEE Ethernet PHY Interface			
RSET_BG	AO	47	For Ethernet PHY's internal biasing. Please connect to GND through a 2.49 kΩ ±1% resistor.
MDIP0	AB	53	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN0	AB	54	
MDIP1	AB	56	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN1	AB	57	
MDIP2	AB	59	In MDI mode, this is the third pair in 1000Base-T, i.e., the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
MDIN2	AB	60	
MDIP3	AB	62	In MDI mode, this is the fourth pair in 1000Base-T, i.e., the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
MDIN3	AB	63	
Clock Pins			
XTALIN	I3	38	25 MHz ± 0.005% crystal or oscillator clock input.
XTALOUT	O3	39	25 MHz crystal or oscillator clock output.
CLKOUT	O3	42	A controllable 25MHz clock output. Please connect it to CLKIN pin with a 22 Ohm termination resistor near to CLKOUT pin.
CLKIN	I3	50	25 MHz clock input. Please connect it to CLKOUT pin with a 22 Ohm termination resistor.

Pin Description *(continued)*

Pin Name	Type	Pin No.	Pin Description
Serial EEPROM Interface			
SCK	B5/PD/T	16	EEPROM Clock. SCK is an output clock to EEPROM to provide timing reference for the transfer of CS, and SDA signals. SCK only drive high / low only while accessing EEPROM otherwise it is tri-stated and internally pulled down.
CS	B5/PD/T	17	EEPROM Chip Select. CS is asserted high synchronously with respect to rising edge of SCK as chip select signal. CS drives high / low only while accessing EEPROM otherwise it is tri-stated and internally pulled down.
SDA	B5/PU/T	15	EEPROM Data. SDA is the serial output data to EEPROM's data input pin and is synchronous with respect to the rising edge of SCK. SDA drives high / low only while accessing EEPROM otherwise it is tri-stated and internally pulled up.
Misc. Pins			
RESET#	I5/PU/S	18	Extrernal chip reset input. Active low. This input feeds to the internal power-on reset circuitry, which provides the main reset source of this chip.
WAKEUP#	I3/PU/S	41	Remote-wakeup trigger from external pin. WAKEUP# should be asserted low for more than 2 cycles of 25 MHz clock to be effective.
SLF_PWR	I5/PD/S	20	Self_power Indication Input. 0: will indicate to Host that this device is a bus-powered device. 1: will indicate to Host that this device is a self-powered device.
GPIO[3]	B3/PD	3	General Purpose Input/Output Pin 3.
GPIO[2]	B3/PD	4	General Purpose Input/Output Pin 2.
GPIO[1]	B3/PD	5	General Purpose Input/Output Pin 1.
GPIO[0]/PME	B3/PD	6	General Purpose Input/Output Pin 0 or PME (Power Management Event). This pin is an input pin by default after power-on reset. GPIO[0] also can be defined as PME output to indicate wake up event detected.
MFA[3]	B3	7	It is a multi-function pin. It acts as a USB SuperSpeed indicator on power up. It can be defined as a GPIO pin. Please refer to Table 3 on page 8.
MFA[2]	B3	8	It is a multi-function pin. It acts as an Ethernet PHY LED indicator (Link 10/100/1000+Active) by default. It can be defined as a GPIO pin. Please refer to Table 3 on page 8.
MFA[1]	B3	13	It is a multi-function pin. It acts as an Ethernet PHY LED indicator (Link 10/100/1000) by default and can be a GPIO pin. Please refer to Table 3 on page 8.
MFA[0]	B3	14	It is a multi-function pin. It acts as an Ethernet PHY LED indicator (Active) and can be a GPIO pin. Please refer to Table 3 on page 8.
NC	I3/PD/S	68	Test pin. User can keep this pin NC.
NC	I3/PD	1	Test pin. User can keep this pin NC.
NC	I3/PD	2	Test pin. User can keep this pin NC.
RESERVED	I3/S	66	Test pin. User should pull down this pin.
RESERVED	I3/S	67	Test pin. User should pull down this pin.
RESERVED	I3	46	Test pin. User should pull down this pin.
NC	O3	11, 36, 44, 51, 52, 64	Test pin. NC.
Power and Ground Pins			
A3V3	P	25	Analog Power for USB 3.0 transceiver. 3.3 V.
GND_3V3	P	22	Analog Ground for USB 3.0 transceiver.
U3TXVDDQ	P	26	Analog Power for USB 3.0 transceiver. 1.2 V.
U3TXVSS	P	28, 30	Analog Ground for USB 3.0 transceiver.

Pin Description *(continued)*

Pin Name	Type	Pin No.	Pin Description
U3RXVDDQ	P	31	Analog Power for USB 3.0 transceiver. 1.2 V.
U3RXVSS	P	33, 35	Analog Ground for USB 3.0 transceiver.
E12VDDQ	P	48	Analog Power for Ethernet PHY. 1.2 V.
E33VDDQ	P	49	Analog Power for Ethernet PHY. 3.3 V.
E12VCC	P	55, 61	Analog Power for Ethernet PHY. 1.2 V.
E33VCC	P	58	Analog Power for Ethernet PHY. 3.3 V.
CVDDQ	P	37	Digital I/O Power for Clock pins. 3.3 V.
VSS	P	40	Digital Ground for clock pins.
DVDD	P	10, 19, 45, 65	Digital Core Power. 1.2 V.
DVSS	P	9	Digital Ground to E-pad
VIO	P	12, 43	Digital I/O Power. 3.3 V.

Settings

Hardware Setting for Operation Mode and Multi-Function Pins

The following hardware settings define the desired operation mode and some multi-function pin configurations. The logic levels shown on setting the pins below are sampled from the chip I/O pins during power on reset based on the setting of the pin's pull-up or pull-down resistor in the schematic.

- EEPROM Offset 05h, Flag[4]: Defines the multi-function pin GPIO[0] / PME

  GPIO[0] is a general purpose I/O normally controlled by vendor commands. User can change this pin to operate as a PME (Power Management Event) for remote wake up. Please refer to Flag (EEPROM: 05h) on page 15 for detailed description of "Flag" of bit 4 (PME_PIN).

- GPIO[1] pin: Determines whether this chip will go to Default WOL (Wake-On-LAN) Ready Mode after power on reset.

Table 1. GPIO[1] Description

GPIO[1]	Description
0	Normal operation mode. By default, internal pull-up resistor (4.7 KΩ) is enabled.
1	Enable Default WOL Ready Mode. Notice that the external pulled-up resistor must be 4.7 KΩ. For more details, please refer to Default Wake-On-LAN (DWOL) Ready Mode on page 11.

- GPIO[2] pin: Determines whether SSTXP swaps with SSTXM and SSRXP swaps with SSRXM for USB3.0 PHY.

Table 2. GPIO[2] Description

GPIO[2]	Description
0	Disable swapping. By default, internal pull-up resistor (4.7 KΩ) is enabled.
1	Enable swapping. Notice that the external pulled-up resistor must be 4.7 KΩ.

- MFA[3] ~ MFA[0] pins: There are 4 multi-function pins. They can be used either for driving indicator LEDs or as normal GPIOs controlled by vendor command PIN Control Register MFA_EN.

Table 3. MFA_3 ~ MFA_0 pin configuration

PIN Name	Default Definition	Section LED Mode (EEPROM: 42h) on page 16	MFA Control Register
MFA[3]	LED_USB indicator (Super-speed)	LED_3	MFAIO_3
MFA[2]	Programmable LED (Link 10/100/1000+Active)	LED_2	MFAIO_2
MFA[1]	Programmable LED (Link 10/100/1000)	LED_1	MFAIO_1
MFA[0]	Programmable LED (Active)	LED_0	MFAIO_0

Functional Overview

USB Core and Interfaces

The USB core is made up of USB 3.0 PHY and Device Controller. The USB 3.0 PHY processes USB Physical layer signals. The USB 3.0 Device Controller is interfaced with USB 3.0 PHY by PIPE/UTMI buses and it processes packets of link layer and protocol layer. The USB 3.0 Device Controller supports Bulk IN, Bulk OUT and Interrupt IN transfers for data transactions.

Energy Efficient Ethernet (EEE)

GX3 supports IEEE 802.3az, also known as Energy Efficient Ethernet (EEE) at 10Mbps, 100Mbps and 1000Mbps. It also supports EEE specified negotiation method to enable link partner to determine whether EEE is supported and to select the best set of parameters common to both devices. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and starts transmitting packets without changing the link status and without dropping/corrupting frames.

During the Low Power Idle mode, most of the circuits are disabled to save power. However, the transition time to/from Low Power Idle mode is kept small enough to be transparent to the upper layer protocols and applications.

10/100/1000M Ethernet PHY

The 10/100/1000M Ethernet PHY is compliant with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. It provides all the necessary physical layer functions to transmit and receive Ethernet packets over CAT 5 UTP cable or CAT 3 UTP (10 Mbps only) cable. It uses state-of-the-art DSP technology and an Analog Front End (AFE) to enable high-speed data transmission and reception over UTP cable. Crossover Detection & Auto-Correction, polarity correction, adaptive equalization, cross-talk cancellation, echo cancellation, timing recovery, and error correction functions are also implemented.

MAC Core

The MAC core supports IEEE 802.3, IEEE 802.3u and IEEE 802.3ab MAC sub-layer functions, such as basic MAC frame receive and transmit, CRC checking and generation, filtering, forwarding, flow-control in full-duplex mode, and collision-detection and handling in half-duplex mode, etc. It supports virtual local area network (VLAN)-tagged frames according to IEEE 802.1Q specification in both transmit and receive functions. The MAC core also implements CRC-32 checking at full-speed using a multi-stage, cyclic redundancy code (CRC) calculation architecture with optional forwarding of the frame check sequence (FCS) field to the user application CRC-32 generation and append on transmit.

Checksum Offload Engine (COE)

The Checksum Offload Engine (COE) supports IPv4, IPv6, layer 4 (TCP, UDP, ICMP, ICMPv6 and IGMP) header processing functions and real time checksum calculation in the hardware.

The COE supports the following features in layer 3:

- IP header parsing, including IPv4 and IPv6
- IPv6 routing header type 0 supported
- IPv4 header checksum check and generation (There is no checksum field in IPv6 header)
- Detecting on RX direction for IP packets with error header checksum

The COE supports the following features in layer 4:

- TCP and UDP checksum check and generation for non-fragmented packet
- TCP Large Send Offload V1
- ICMP, ICMPv6 and IGMP message checksum check and generation for non-fragmented packet

Memory Arbiter

The memory arbiter block stores received MAC frames into on-chip SRAM (packet buffer) and then forward it to the USB bus upon request from the USB host via Bulk IN transfer. It also monitors the packet buffer usage in full-duplex mode for triggering PAUSE frame (or in half-duplex mode to activate Back pressure jam signal) transmission out on transmit (TX) direction. The memory arbiter block is also responsible for storing MAC frames received from the USB host via Bulk OUT transfer and scheduling transmission out towards Ethernet network.

USB to Ethernet Bridge

The USB to Ethernet bridge block converts Ethernet MAC frames into USB packets or vice-versa. This block supports burst transfer mechanism to offload software burden and to offer very high packet transfer throughput over USB bus.

SEEPROM Loader Interface

The SEEPROM loader interface is responsible for reading configuration data automatically from the external serial EEPROM after power-on reset.

If the content of EEPROM offset 05h (low byte) is equal to (0xFF - SUM [EEPROM offset 03h ~ 04h]), the EEPROM is the first candidate for SEEEPROM loader.

GPIOs and LED

There are 4 GPIO pins (GPIO[0/1/2/3]) and 4 multi-function pins group A (MFA[0/1/2/3]) provided by this chip. The MFA[0/1/2/3] pins are also used for LED indication. Please refer to LED Mode (EEPROM: 42h) on page 16 for details.

PLL Clock Generator

GX3 includes an on-chip internal oscillator circuit for 25 MHz which allows the chip to operate cost effectively with just external 25 MHz crystals.

The external 25 MHz crystal or oscillator, via pins XTALIN/XTALOUT, provides the reference clock to internal oscillator circuit to generate clock for the embedded Ethernet PHY, embedded USB PHY, and base clock for the ASIC.

The external 25 MHz Crystal spec is listed in below table. For more details on crystal timing, please refer to Clock Timing on page 28 and CYUSB3610 demo board reference schematic.

Table 4. External 25 MHz Crystal Units specifications

Parameter	Symbol	Typical Value
Nominal Frequency	f_O	25.000000 MHz
Oscillation Mode		Fundamental
Frequency Tolerance (@25 °C)		±30 ppm
Frequency Stability Over Operating Temperature Range		±30 ppm
Equivalent Series Resistance	ESR	70 Ω max.
Load Capacitance	CL	12 pF
Drive Level		350 µW
Operation Temperature Range		0 °C ~ +70 °C
Aging		±3 ppm/year

Reset Generation

GX3 integrates an on-chip power-on-reset circuit, which simplifies the external reset circuitry on the board. The power-on-reset circuit generates a reset pulse after 1.2 V core power ramps up to 0.72 V (typical threshold). The external reset pin, RESET#, can be directly connected to the input of the power-on-reset circuit and can also be used as an additional hardware reset source. For more details on RESET# timing, please refer to Reset Timing on page 28.

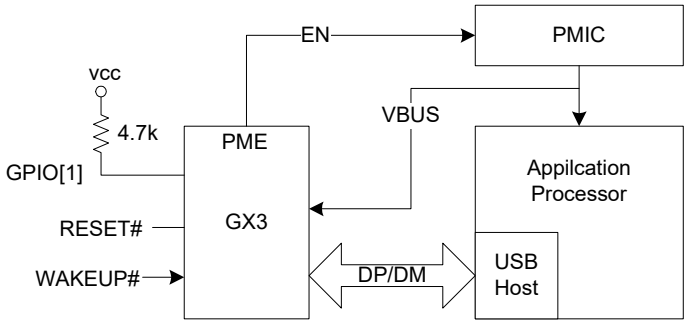
Default Wake-On-LAN (DWOL) Ready Mode

This Default WOL Ready Mode application is different from normal operation where GX3 Suspend/Resume state usually has to be configured by software driver during normal system operation. This application applies to a system that uses a predefined remote wakeup event to turn on the system power supply and its peripheral circuits without having any system software running in the beginning. This is quite useful when a system has been powered down already and a user needs to power on the system remotely.

GX3 can be configured to support Default WOL Ready Mode, where no system driver is required to configure its WOL related settings after power on reset. A system design usually partitions its power supply into two or more groups and the GX3 is supplied with an independent power separated from the system processor. The power supply of GX3 is usually available as soon as power plug is connected. The power supply of system processor remains off initially when power plug is connected and is controlled by GX3's PME pin, which can be activated whenever GX3 detects a pre-defined wakeup event such as valid Magic Packet reception or the WAKEUP# pin trigger. To reduce power consumption, initially the USB host controller communicating with GX3 can also be unpowered as the system processor.

The PME pin of GX3 can control the power management IC (PMIC) to power up the system processor along with the USB host controller, which will perform USB transactions with GX3 after both have been initialized. The pin polarity of PME is configured as high active when enabling Default WOL Ready Mode. Note that the GX3 must be in self-power (via setting EEPROM Flag [0]) mode for this function.

Procedure to Enable Default WOL Ready Mode



To enable Default WOL Ready Mode, configure GPIO[0] pin as PME (via setting EEPROM Flag [12]) and have GPIO[1] pulled-up with a 4.7K resistor. After power on reset, GX3 will disable most functions including USB transceiver (see Note 2) but enable Magic Packet detector logic, internal Ethernet PHY and its auto-negotiation function to be ready to

receive Magic Packet. When a valid Magic Packet is received, GX3 will assert the PME pin to indicate to system processor the wakeup event. The PME pin, when being configured as static level output signal (via setting EEPROM Flag [15], see Note 3), can be used to control the power management IC to enable system power supply. After asserting the PME pin, GX3 will also exit from the Default WOL Ready Mode and revert back to normal operation mode to start normal USB device detection, handshaking, and enumeration.

The PME pin, when being configured as static level output signal, maintains its signal level until RESET# is asserted again. If RESET# to GX3 is asserted with GPIO[1] pulled-up, the Default WOL Ready Mode will be re-entered. Otherwise (GPIO[1] being pulled-down), it will enter into normal operation mode and the normal USB device detection, handshaking and enumeration process should take place right after RESET# negation.

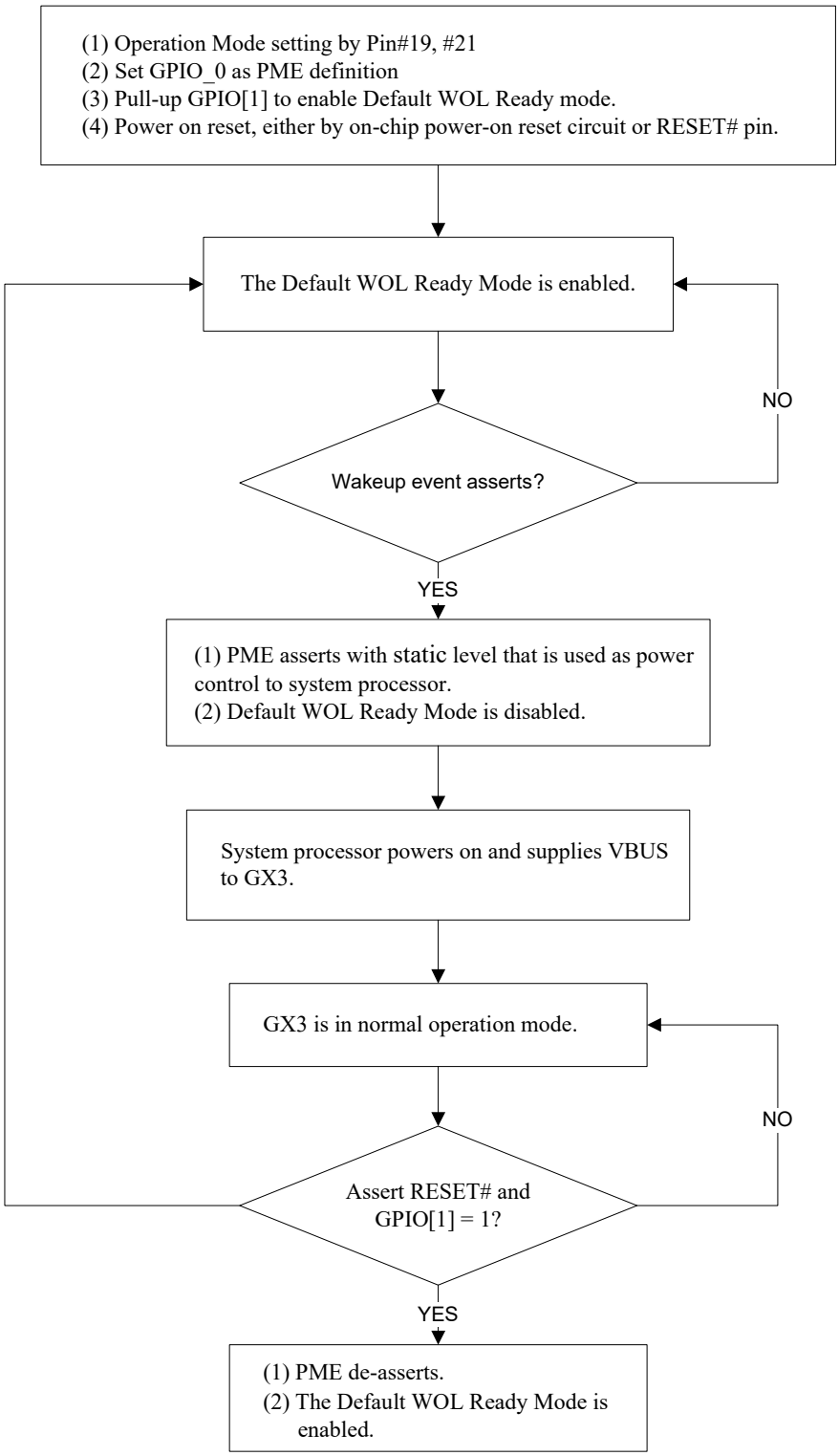
Notes
1. For complete truth table of wakeup events supported, please refer to below on the "GPIO[1] = 1" setting.
2. When the Default WOL Ready Mode is enabled, the DP/DM pins of GX3 will be in tri-state.
3. Please refer to Flag (EEPROM: 05h) on page 15. The bit [15:12] of Flag (PME_IND, PME_TYP, PME_POL, PME_PIN) = 0111.
4. It is recommended that VBUS pin be connected to system power group directly. This way the VBUS will become HIGH when power management IC enables the system power supply.

Table 5. Remote Wakeup Truth Table

Waken Up by	Setting						Wakeup Event					Device wakes up
	RWU bit of Flag byte in EEPROM	Set_Feature standard command	RWWF	RWMP	RWLC	GPIO_1 [5]	Host sends resume signal	Receiving a Wakeup Frame	Receiving a Magic Packet	Link status change detected On PHY	EX-TWAKE_N pin	
USB Host	X	X	X	X	X	0	J -> K					Yes
Device	0	0	X	X	X	0		X	X	X	X	No
Device	1	1	1	0	0	0		Yes				Yes
Device	1	1	0	1	0	0			Yes			Yes
Device	1	1	0	0	1	0				Yes		Yes
Device	1	1	0	0	1	0						Yes
Device	1	1	X	X	X	0					Low-pulse	Yes
Device	X	0	0	0	0	1			Yes		Low-pulse	Yes

Note
5. About Default WOL Ready Mode, please refer to GPIOs and LED on page 10.

Flow Chart of Default WOL Ready Mode



Serial EEPROM Memory Map

Table 6. Serial EEPROM Memory Map

EEPROM OFFSET	HIGH BYTE	LOW BYTE
00h	Node ID 1	Node ID 0 (Note 6)
01h	Node ID 3	Node ID 2
02h	Node ID 5	Node ID 4
03h	PID_HB	PID_LB
04h	VID_HB	VID_LB
05h	Flag	EEPROM Checksum (Note 7)
06h	Reserved	Reserved
07h	Max. Power for Self Power	Max. Power for Bus Power
08h	EndPoint1 for SS/HS	EndPoint1 for FS
09h	Language ID High Byte	Language ID Low Byte
0Ah	Length of Product String (bytes)	Offset of Product String (0Eh)
0Bh	Length of Manufacturer String (bytes)	Offset of Manufacturer String (1Ah)
0Ch	Length of Serial Number String (bytes)	Offset of Serial Number String (26h)
0Dh	Length of BOS-type Descriptor (bytes)	Offset of BOS-type Descriptor (2Dh)
19~0Eh	Product String: (Max.) 24 bytes	
25~1Ah	Manufacturer String: (Max.) 24 bytes	
2C~26h	Serial Number String: (Max.) 14 bytes	
3B~2Dh	BOS-type Descriptor: (Max.) 30 bytes	
3Ch	Reserved	Max. Burst: [7:4] for EP3, [3:0] for EP2
41~3Dh	Fixed_pattern (10 bytes)	
42h	LED_Mode_HB	LED_Mode_LB

Notes
6. The Node ID 0 value cannot be set to 0xFF and 1st bit of Node ID 0 cannot be set to “1” (i.e. cannot be set to multicast MAC address).
7. The value of EEPROM Checksum field located at EEPROM offset 05h (low byte). The correct value must be equal to (0xFF - SUM [EEPROM offset 03h ~ 04h]). If SUM [EEPROM offset 03h ~ 04h] has carry, please add ‘1’ to its result.
8. Total usage is about 134 bytes.

Detailed Description

The following sections provide detailed descriptions for some of the fields in memory maps of serial EEPROM.

Node ID (00~02h)

The Node ID 0 to 5 bytes represent the MAC address of the device, for example, if MAC address = 04-23-45-67-89-AB, then Node ID 0 = 04h, Node ID 1 = 23h, Node ID 2 = 45h, Node ID 3 = 67h, Node ID 4 = 89h, and Node ID 5 = ABh.

Default values: Node ID {0, 1, 2, 3, 4, 5} = 00-0E-C6-F9-D0-00.

Flag (EEPROM: 05h)

Table 7. Flag (EEPROM: 05h)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PME_IND	PME_TYPE	PME_POL	PME_PIN	0	0	WOLLP	RWU

RWU: Remote Wakeup support.

1: Indicate that this device supports Remote Wakeup (default).

0: Not supported.

WOLLP: Wake-On-LAN Low Power function.

1: Enabled (default).

0: Disabled.

PME_PIN: PME / GPIO[0].

1: Set GPIO[0] pin as PME (default).

0: GPIO[0] pin is controlled by vendor command.

PME_POL: PME pin active Polarity.

1: PME active high (default).

0: PME active low.

PME_TYP: PME I/O Type.

1: PME output is a Push-Pull driver (default).

0: PME output to function as an open-drain buffer.

PME_IND: PME indication.

1: A 1.363 ms pulse active when detecting wake-up event.

0: A static signal active when detecting wake-up event (default).

Max. Power for Self/Bus Power (07h)

They are Max power values' setting of powered device for EEPROM at offset 07h.

The default value of Bus Power is 3Eh.

For USB 3.0, the power value is 496 mA (Unit = 8 mA).

For USB 2.0, the power value is 248mA (Unit = 4 mA).

Self power setting follows conversion above.

EndPoint1 for SS/HS/FS (EEPROM:08h)

The time interval (named “bInterval”) for polling Interrupt IN endpoint 1 for data transfers of SuperSpeed/High-Speed/Full-Speed is stored at EEPROM offset 08h. It is expressed in frames or microframes depending on the device operating speed (i.e. either 1 millisecond or 125 µs units).

The default “bInterval” value is 0Bh for Super-Speed/High-Speed (the polling time of endpoint 1 = $2^{(11-1)}$ × 125 µs =128 ms) and is 80h for Full-Speed (the polling time of endpoint 1 = 128 × 1 ms = 128 ms).

Max. Burst for EP3/EP2 (EEPROM: 3Ch)

This value is bMaxBurst field in SS endpoint companion descriptor.

LED Mode (EEPROM: 42h)

LED Mode defines the indication setting for LED_0/1/2/3 function of MFA[0/1/2/3] pins.

Table 8. Bit 7~Bit 0: LED_Mode_LB

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LED1_100	LED1_10	LED1_Active	LED0_Duplex	LED0_1000	LED0_100	LED0_10	LED0_Active

Table 9. Bit 15~Bit 8: LED_Mode_HB

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8
1	LED2_Duplex	LED2_1000	LED2_100	LED2_10	LED2_Active	LED1_Duplex	LED1_1000

Note: Bit 15 must be ‘1’ to enable the LED_mode setting; otherwise, it will work at default LED mode.

The LED mode table is as below:

Table 10. LED Mode Setting Table

	Full duplex	Link speed (Mbps)			Active (TX/RX)	Description of Indication
		1000	100	10		
Bit	**4**	**3**	**2**	**1**	**0**	
LED_0	0	0	0	0	0	USB3.0 Super Speed: It turns ON when device operates at USB3.0 Super Speed.
	0	0	0	0	1	Active (Default for LED0)
	0	0	0	1	0	Link 10
	0	0	0	1	1	Link 10+Active
	0	0	1	0	0	Link 100
	0	0	1	0	1	Link 100+Active
	0	0	1	1	0	Link 100/10
	0	0	1	1	1	Link 100/10+Active
	0	1	0	0	0	Link 1000
	0	1	0	0	1	Link 1000+Active
	0	1	0	1	0	Link 1000/10
	0	1	0	1	1	Link 1000/10+Active
	0	1	1	0	0	Link 1000/100
	0	1	1	0	1	Link 1000/100+Active
	0	1	1	1	0	Link 1000/100/10
	0	1	1	1	1	Link 1000/100/10+Active
	1	0	0	0	0	Full duplex
Bit	**9**	**8**	**7**	**6**	**5**	
LED_1	0	0	0	0	0	USB3.0 Super Speed: It turns ON when device operates at USB3.0 Super Speed.
	0	0	0	0	1	Active
	0	0	0	1	0	Link 10
	0	0	0	1	1	Link 10+Active
	0	0	1	0	0	Link 100
	0	0	1	0	1	Link 100+Active
	0	0	1	1	0	Link 100/10
	0	0	1	1	1	Link 100/10+Active
	0	1	0	0	0	Link 1000
	0	1	0	0	1	Link 1000+Active
	0	1	0	1	0	Link 1000/10
	0	1	0	1	1	Link 1000/10+Active
	0	1	1	0	0	Link 1000/100
	0	1	1	0	1	Link 1000/100+Active
	0	1	1	1	0	Link 1000/100/10
	0	1	1	1	1	Link 1000/100/10+Active
	1	0	0	0	0	Full duplex

Table 10. LED Mode Setting Table *(continued)*

	Full duplex	Link speed (Mbps)			Active (TX/RX)	Description of Indication
		1000	100	10		
Bit	**14**	**13**	**12**	**11**	**10**	
LED_2	0	0	0	0	0	USB3.0 Super Speed: It turns ON when device operates at USB3.0 Super Speed.
	0	0	0	0	1	Active
	0	0	0	1	0	Link 10
	0	0	0	1	1	Link 10+Active
	0	0	1	0	0	Link 100
	0	0	1	0	1	Link 100+Active
	0	0	1	1	0	Link 100/10
	0	0	1	1	1	Link 100/10+Active
	0	1	0	0	0	Link 1000
	0	1	0	0	1	Link 1000+Active
	0	1	0	1	0	Link 1000/10
	0	1	0	1	1	Link 1000/10+Active
	0	1	1	0	0	Link 1000/100
	0	1	1	0	1	Link 1000/100+Active
	0	1	1	1	0	Link 1000/100/10
	0	1	1	1	1	Link 1000/100/10+Active
	1	0	0	0	0	Full duplex
Bit	**4**	**3**	**2**	**1**	**0**	
LED_3	0	0	0	0	1	USB3.0 Super Speed: The LED_0 mode MUST be set to “Active” only when the LED_3 is used. It will be ON when device operates at USB3.0 and keep flashing when device is receiving/transmitting packets.

Fixed_pattern (EEPROM: 41~3Dh)

Please write these 10 bytes of fixed_pattern with hexadecimal (from low bytes to high bytes) = “40 4A 40 00 40 30 0D 49 90 41”.

Internal Memory Description

The internal Memory data is a fixed value. User can't modify it.

Table 11. Internal Memory Description

Field Definition	Default Values	Description
Node ID	00 0E C6 F9 D0 00	Node ID 0 ~ 5
Product ID (PID)	10 36	PID of GX3
Vender ID (VID)	B4 04	Cypress VID
Flag - Remote Wakeup and PME setting, etc.	73	Enable the "remote wakeup" and Low Power WOL function (Note 9)
Max Power for Bus Power	3E	496 mA for USB 3.0 248 mA for USB 2.0 (Note 10)
Max Power for Self Power	01	8 mA for USB 3.0 4 mA for USB 2.0 (Note 10)
Length of Product String	03	Product String Length (Note 11)
Length of Manufacturer String	07	Manufacturer String Length (Note 11)
Product String (Max. 12 bytes)	41 58 33 00 00 00 00 00 00 00 00 00	"GX3"
Manufacture String (Max. 10 bytes)	43 79 70 72 65 73 73 00 00 00	"Cypress"
Fixed Pattern	40 4A 40 00 40 30 0D 49 90 41	Fixed pattern to be written

External EEPROM Description

User can assign the specific VID/PID, Serial Number, Manufacture String, Product String, etc. user defined fields by external EEPROM. Please refer to GX3 EEPROM User Guide document for more details about how to configure GX3 EEPROM content.

Note the EEPROM checksum field should be changed together with the VID/PID fields.

Notes

9. Remote Wakeup/PME Settings
   The offset 05h field of GX3 EEPROM is used to configure the Remote Wakeup and PME functions. Please refer to Serial EEPROM Memory Map on page 14 for the detailed description of EEPROM offset 05h.
   The RWU bit of GX3 EEPROM offset 05h is used to configure the "bmAttributes" field of Standard Configuration Descriptor that will be reported to the USB host controller when the GET_DESCRIPTOR command with CONFIGURATION type is issued. Please refer to "Section 9.6.3 Configuration" of Universal Serial Bus 3.0 Spec for the detailed description of the "bmAttributes" field of Standard Configuration Descriptor.
   The power mode about Bus-powered or Self-powered is decided by the SELF_PWR pin when chip powers on. This will be updated to the "bmAttributes" field of Standard Configuration Descriptor.
10. Max Power Setting
    The low byte of GX3 EEPROM offset 07h (for bus-powered) field and high byte of GX3 EEPROM offset 07h (for self-powered) field are used to configure the "bMaxPower" field of Standard Configuration Descriptor that will be reported to the USB host controller when the GET_DESCRIPTOR command with CONFIGURATION type is issued. Please refer to "Section 9.6.3 Configuration" of Universal Serial Bus 3.0 Spec for the detailed description of the "bMaxPower" field of Standard Configuration Descriptor. These fields are used to define the Maximum power consumption of the USB device drawn from the USB bus in this specific configuration when the device is fully operational.
11. Product/Manufacturer/Serial Number String Settings
    The "Offset" fields of Product/Manufacturer/Serial Number String are fixed in GX3 EEPROM memory map. Please DO NOT change the recommended values of these fields.
    If you need to change the Product/Manufacturer/Serial Number strings on your GX3 EEPROM, please modify the "Length" fields of Product/Manufacturer/Serial Number String to meet the exact string length of your Product/Manufacturer/Serial Number strings.

USB Configuration Structure

GX3 supports only one USB configuration, one interface and four USB endpoints. The four endpoints are defined as below:

- Endpoint 0: Control endpoint. It is used for configuring the device.
- Endpoint 1: Interrupt endpoint. It is used for reporting network Link status.
- Endpoint 2: Bulk IN endpoint. It is used for receiving Ethernet Packet.
- Endpoint 3: Bulk OUT endpoint. It is used for transmitting Ethernet Packet.

Electrical Specifications

DC Characteristics

Absolute Maximum Ratings

Table 12. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VCCK	Digital core power supply	–0.5 to 1.44	V
U3TXVDDQ	Analog Power for USB Transceiver. 1.2 V	–0.5 to 1.6	V
U3RXVDDQ	Analog Power for USB Transceiver. 1.2 V	–0.5 to 1.6	V
E12VDDQ	Analog Power for Ethernet PHY. 1.2 V	–0.1 to 1.26	V
E12VCC	Analog Power for Ethernet PHY. 1.2 V	–0.1 to 1.26	V
VIO33	Power supply of 3.3 V I/O	–0.5 to 4.2	V
CVDDQ	Power supply of 3.3 V for clock pin.	–0.5 to 4.6	V
A3V3	Analog Power 3.3 V for USB Transceiver.	–0.5 to 4.6	V
E33VDDQ	Analog Power for Ethernet PHY. 3.3 V	–0.4 to 3.7	V
E33VCC	Analog Power for Ethernet PHY. 3.3 V	–0.4 to 3.7	V
V_{IN3}	Input voltage of 3.3 V I/O	–0.5 to 4.2	V
	Input voltage of 3.3 V I/O with 5 V tolerant	–0.5 to 5.8	V
TSTG	Storage temperature	–65 to 150	°C
I_{IN}	DC input current	50	mA
I_{OUT}	Output short circuit current	50	mA

Notes:

1.Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the optional sections of this datasheet. Exposure to absolute maximum rating condition for extended periods may affect device reliability.

2. The input and output negative voltage ratings may be exceeded if the input and output currents under ratings are observed.

Recommended Operating Conditions

Table 13. Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VCCK	Digital core power supply	1.14	1.2	1.26	V
U3TXVDDQ	Analog Power for USB Transceiver. 1.2 V	1.14	1.2	1.26	V
U3RXVDDQ	Analog Power for USB Transceiver. 1.2 V	1.14	1.2	1.26	V
E12VDDQ	Analog Power for Ethernet PHY. 1.2 V	1.14	1.2	1.26	V
E12VCC	Analog Power for Ethernet PHY. 1.2 V	1.14	1.2	1.26	V
VIO	Power supply of 3.3 V I/O	3.13	3.3	3.47	V
CVDDQ	Power supply of 3.3 V for clock pin.	3.13	3.3	3.47	V
A3V3	Analog Power 3.3 V for USB Transceiver.	3.13	3.3	3.47	V
E33VDDQ	Analog Power for Ethernet PHY. 3.3 V	2.97	3.3	3.63	V
E33VCC	Analog Power for Ethernet PHY. 3.3 V	2.97	3.3	3.63	V
V_{IN3}	Input voltage of 3.3 V I/O	3.13	3.3	3.47	V
	Input voltage of 3.3 V I/O with 5 V tolerance	3.13	3.3	5.25	V
T_j	Maximum junction operating temperature	–	–	125	°C
T_a	Ambient operating temperature	0	–	70	°C

Leakage Current and Capacitance

Table 14. Leakage Current and Capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IN}	True 3.3 V I/O input leakage current	V_{IN} = 3.3 V or 0 V	–	≤±1	–	µA
	3.3 V with 5 V tolerance I/O input leakage current	V_{IN} = 5 V or 0 V	–	<±1	–	pF
C_{IN}	Input capacitance	3.3 V I/O cells	–	2.25	–	pF
		3.3 V with 5 V tolerant I/O cells	–	3.6	–	pF

Note: C_{IN} includes the cell layout capacitance and pad capacitance (Estimated to be 0.5 pF).

DC Characteristics of 3.3 V I/O Pins

Table 15. DC Characteristics of 3.3 V I/O Pins

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vil	Input low voltage	LVTTL	–	–	0.8	V
Vih	Input high voltage		2.0	–	–	V
Vt-	Schmitt trigger negative going threshold voltage	LVTTL	0.8	1.1	–	V
Vt+	Schmitt trigger positive going threshold voltage		–	1.6	2.0	V
Vol	Output low voltage	|Iol| = 4~8mA	–	–	0.4	V
Voh	Output high voltage	|Ioh| = 4~8mA	2.4	–	–	V
Vopu [12]	Output pull-up voltage for 5 V tolerance I/O cells	PU = High, PD = Low E = 0, |Ipu| = 1 µA	V_{IO} – 0.9	–	–	V
Rpu	Input pull-up resistance	PU = High, PD = Low	40	75	190	KΩ
Rpd	Input pull-down resistance	PU = Low, PD = High	40	75	190	KΩ

Note
12. This parameter indicates that the pull-up resistor for the 5 V tolerance I/O cells cannot reach the V_{IO} DC level even without the DC loading current.

Thermal Characteristics

Table 16. Thermal Characteristics

Description	Symbol	Rating	Units
Thermal resistance of junction to case	Θ_{JC}	8.3	°C/W
Thermal resistance of junction to ambient	Θ_{JA}	21.4	°C/W

Note: Θ_{JA}, Θ_{JC} defined as below

$\Theta_{JA} = (T_J - T_A) / P$

$\Theta_{JC} = (T_J - T_C) / P$

T_J: maximum junction temperature (°C)
T_A: ambient or environment temperature (°C)
T_C: the top centre of compound surface temperature (°C)
P: input power (watts)

Power Consumption

Table 17. Power Consumption

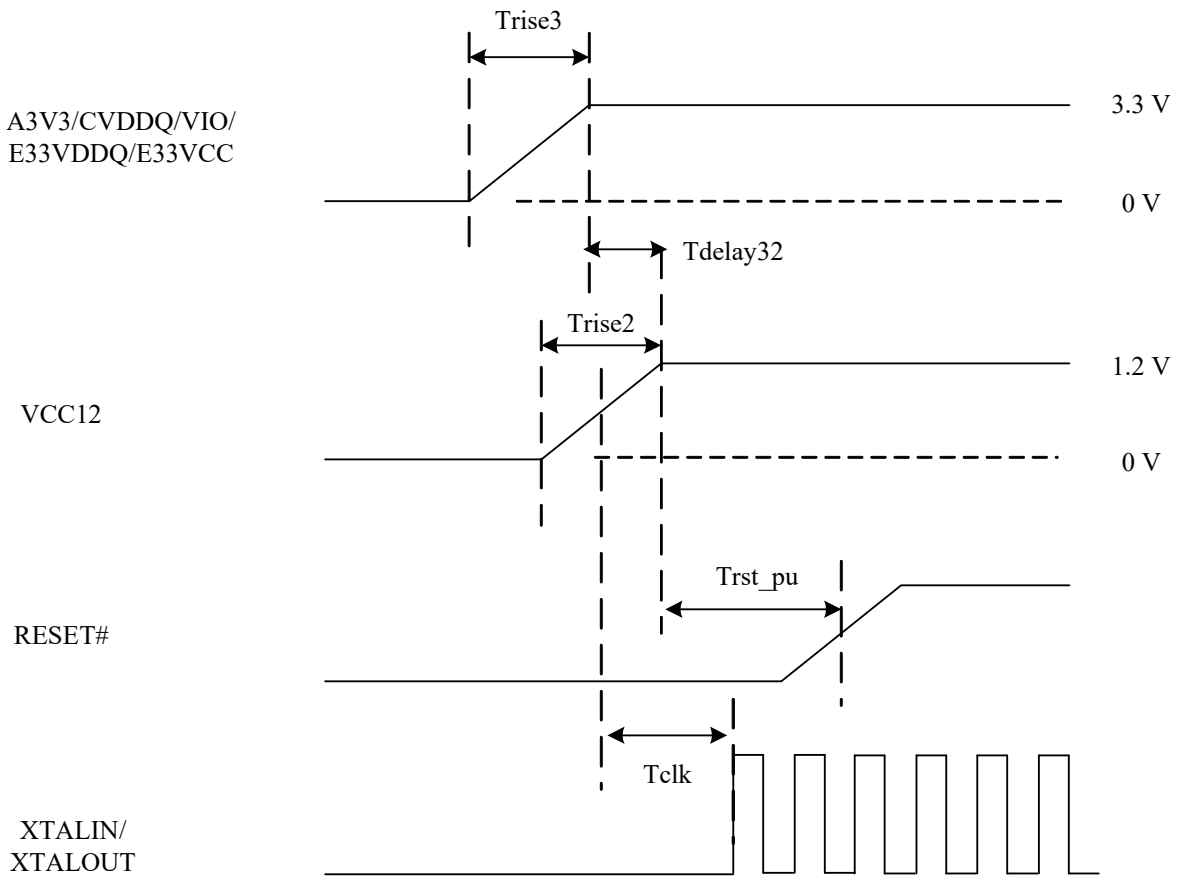
Symbol	Description	Conditions	Min	Typ	Max	Unit
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 1 Gbps (full duplex) mode and USB Super Speed mode	–	335	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	67	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 100 Mbps full duplex mode and USB Super Speed mode	–	189	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	41	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 10 Mbps half duplex mode and USB Super Speed mode	–	151	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	48	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 1 Gbps (full duplex) mode and USB High Speed mode	–	228	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	79	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 100 Mbps full duplex mode and USB High Speed mode	–	85	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	50	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 10 Mbps half duplex mode and USB High Speed mode	–	48	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	53	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 1 Gbps (full duplex) mode and USB Full Speed mode	–	216	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	63	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 100 Mbps full duplex mode and USB Full Speed mode	–	77	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	40	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 10 Mbps half duplex mode and USB Full Speed mode	–	42	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	46	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Ethernet unlink (Disable AutoDetach) and USB Super Speed mode	–	151	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	29	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Ethernet unlink (Enable AutoDetach)	–	23	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	12	–	mA
I_{VCC12}	Current Consumption at 1.2 V	USB Suspend and Ethernet is 1 Gbps: enable Remote WakeUp and disable WOLLP (WOL Low Power)	–	200	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	47	–	mA
I_{VCC12}	Current Consumption at 1.2 V	USB Suspend and enable Remote WakeUp and enable WOLLP to 10Mbps	–	25	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	13	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Suspend and disable Remote WakeUp (Refer to below $I_{SYSTEM(Suspend)}$ item for total power consumption at Suspend mode)	–	1.5	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	1.7	–	mA
IDLE Power Consumption for Etherent Linked in EEE / non-EEE						
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 1 Gbps mode and USB Super Speed mode (Ethernet linked in EEE)	–	177	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	32	–	mA

Table 17. Power Consumption *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 1 Gbps mode and USB Super Speed mode (Ethernet linked in non-EEE)	–	320	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	66	–	mA
I_{VCC12}	Current Consumption at 1.2 V	USB Suspend and enable Remote WakeUp (Ethernet linked in EEE 1Gbps mode)	–	56	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	0.4	–	mA
Green Ethernet Cable-Length Power Saving (GEPS)						
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 1 Gbps mode @ 1.5 meters and USB Super Speed mode (Enable GEPS)	–	320	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	66	–	mA
I_{VCC12}	Current Consumption at 1.2 V	Operating at Ethernet 1 Gbps mode @ 1.5 meters and USB Super Speed mode (Disable GEPS)	–	328	–	mA
I_{VCC33}	Current Consumption at 3.3 V		–	69	–	mA
I_{DEVICE}	1.2 V/3.3 V power consumption at full loading (chip only)	1.2 V (Operating at Super Speed/1 Gbps mode)	–	335	–	mA
		3.3 V (Operating at Super Speed/1 Gbps mode)	–	67	–	mA
I_{SYSTEM}	Total power consumption at full loading (demo board)	VBUS of 5.0 V ((Operating at Super Speed/1 Gbps mode), (Using Switching regulator with dual VOUT 3.3/1.2 V))	–	161	–	mA
$I_{SYSTEM(Suspend)}$	Total power consumption at Suspend mode (demo board)	VBUS of 5.0 V ((Disable Remote WakeUp), (Using Switching regulator with dual VOUT 3.3/1.2 V))	–	1.92	–	mA

Power-up Sequence

At power-up, the GX3 requires the A3V3/CVDDQ/VIO/E33VDDQ/E33VCC power supply to rise to nominal operating voltage within Trise3 and the VCC12 (Note) power supply to rise to nominal operating voltage within Trise2.



Note: The VCC12 includes VCCK, E12VCC, and E12VDDQ/TX/RX.

Table 18. Power-up Sequence Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{rise3}	3.3 V power supply rise time	From 0 V to 3.3 V	–	–	10	ms
T_{rise2}	1.2 V power supply rise time	From 0 V to 1.2 V	–	–	10	ms
$T_{delay32}$	3.3 V rise to 1.2 V rise time delay		–5	–	5	ms
T_{clk}	25 MHz crystal oscillator stable time	From VCC3IO = 3.3V to stable clock period of XTALIN or XTALOUT	–	1 [14]	–	ms
T_{rst_pu}	RESET# low level interval time from power-up	From VCC12 = 1.2 V and VCC3IO = 3.3 V to RESET# going high	0 [13]	–	10	ms

Notes

13. When the VCC12 power-up, the internal power-on-reset circuit will generate a few us (micro second) of hardware reset to chip and will start operation after the XTALIN/N 25 MHz clock signals are stable.
14. The Tclk timing is depended on the 25 MHz crystal circuit. The 1 ms Tclk timing is reference timing based on the GX3 reference 25 MHz crystal circuit. Please refer to GX3 reference schematic for details.

AC Timing Characteristics

Notice that the following AC timing specifications for output pins are based on CL (Output load) equal to 50 pF.

Clock Timing

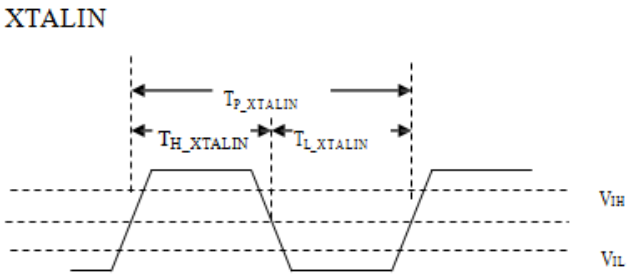


Table 19. Clock Timing Parameters

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_XTALIN}	XTALIN clock cycle time		–	40.0	–	ns
T_{H_XTALIN}	XTALIN clock high time		–	20.0	–	ns
T_{L_XTALIN}	XTALIN clock low time		–	20.0	–	ns

Reset Timing

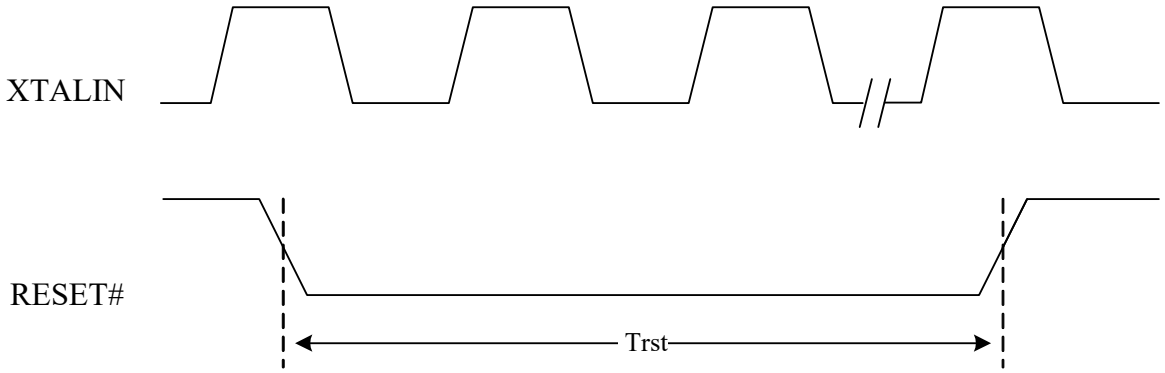


Table 20. Reset Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
Trst	Reset pulse width after XTALIN is running	125	–	250000	XTALIN clock cycle [15]

Note

15. If the system applications require using hardware reset pin, RESET#, to reset GX3 during device initialization or normal operation after VBUS pin is asserted, the above timing spec (Min = 5 µs, Max =10 ms) of RESET# should be met.

Serial EEPROM Timing

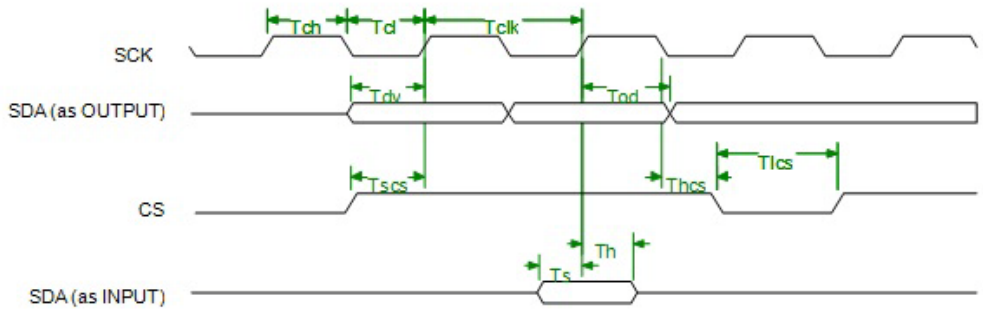


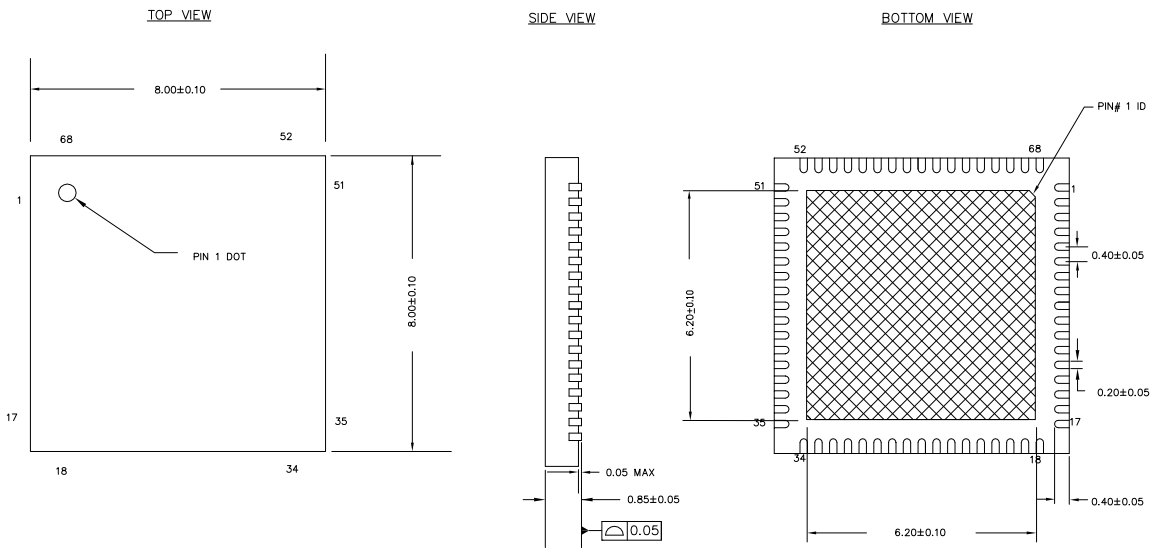
Table 21. Serial EEPROM Timing Parameters

Symbol	Description	Min	Typ	Max	Unit
Tclk	SCK clock cycle time	–	5120	–	ns
Tch	SCK clock high time	–	2560	–	ns
Tcl	SCK clock low time	–	2560	–	ns
Tdv	SDA output valid to SCK rising edge time	2560	–	–	ns
Tod	SCK rising edge to SDA output delay time	2562	–	–	ns
Tscs	CS output valid to SCK rising edge time	2560	–	–	ns
Thcs	SCK falling edge to CS invalid time	7680	–	–	ns
Tlcs	Minimum CS low time	23039	–	–	ns
Ts	SDA input setup time	20	–	–	ns
Th	SDA input hold time	0	–	–	ns

Package Information

68-pin QFN 8 × 8 package

Figure 2. 68-pin QFN (8 × 8 × 0.85 mm) LT68D 6.2 × 6.2 mm E-Pad (Sawn Type) Package Outline, 001-96836



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. ALL DIMENSIONS ARE IN MILLIMETERS

001-96836 **

Recommended PCB Footprint for 68-pin QFN 8x8 package

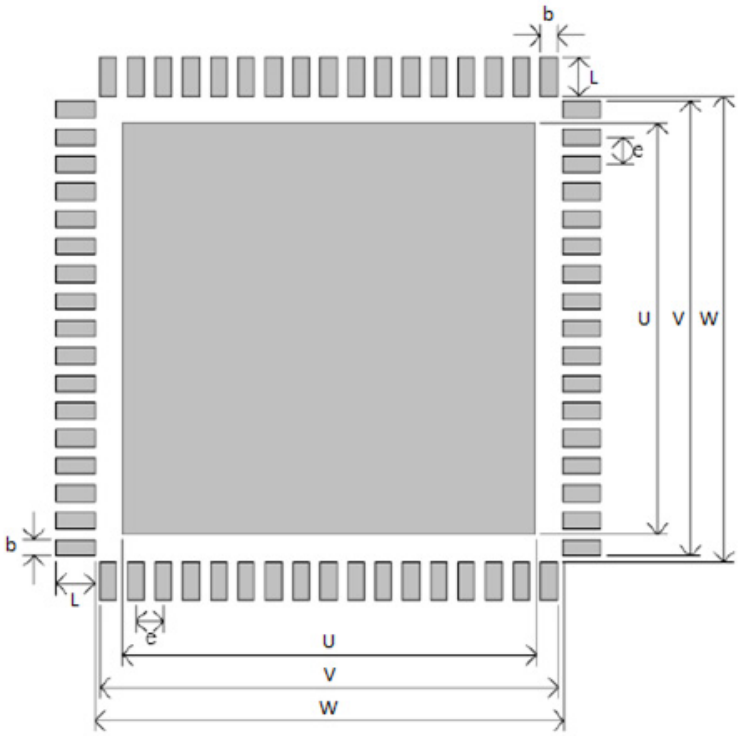


Table 22. Details

Symbol	Description	Typical Dimension
e	Lead pitch	0.40 mm
b	Pad width	0.23 mm
L	Pad length	0.80 mm
U	–	6.30 mm
V	–	6.63 mm
W	–	7.20 mm

Ordering Information

Table 23. Ordering Information

Part Number	Description
CYUSB3610-68LTXC	68 PIN, QFN Package, Commercial Grade Temperature Range 0 ℃ to +70 ℃ (Green, Lead-Free)

Acronyms

Acronym	Description
COE	Checksum Offload Engine
EEE	Energy Efficient Ethernet
GPIO	General Purpose Input Output
MDI	Medium Dependent Interface
NC	No Connection
RISC	Reduced Instruction Set Computer
USB	Universal Serial Bus
UTP	Unshielded Twisted Pair
VLAN	Virtual Local Area Network
W-LAN	Wake-On LAN

Document Conventions

Units of measure

Symbol	Unit of measure
°C	degree Celsius
Gbps	gigabits per second
kΩ	kilohm
Mbps	megabits per second
MHz	megahertz
µW	microwatt
mA	milliampere
mm	millimeter
ms	millisecond
ns	nanosecond
pF	picofarad
ppm	parts per million
V	volt

Document History Page

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4703075	RAJV	05/29/2015	New data sheet.
*A	4870097	MDDD	08/03/2015	Changed status from Preliminary to Final.
*B	5713474	AESATMP8	04/26/2017	Updated logo and Copyright.
*C	6192311	MDDD	05/31/2018	Updated to new template. Completing Sunset Review.

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