

RoHS Compliant

Serial ATA Flash Drive

SS210-297 High-Speed Product Specifications

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Version 1.1



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Features:

- **Compliance with SATA Revision 3.1**
 - SATA 6.0 Gbps interface
 - Backward compatible with SATA 1.5 and 3.0 Gbps interfaces
 - ATA-8 command set
- **Capacity**
 - 4, 8, 16, 32, 64, 128 GB
- **Performance***
 - Burst read/write: 600 MB/sec
 - Sequential read: up to 525 MB/sec
 - Sequential write: up to 435 MB/sec
 - Seq. read QD32: Up to 555 MB/sec
 - Seq. write QD32: Up to 435 MB/sec
 - Random read (4K): up to 86,000 IOPS
 - Random write (4K): up to 76,000 IOPS
- **Flash Management**
 - Built-in hardware ECC
 - Global Wear Leveling
 - Flash bad-block management
 - S.M.A.R.T.
 - Power Failure Management
 - ATA Secure Erase
 - TRIM
- **SATA Power Management**
- **NAND Flash Type: SLC**
- **MTBF: >2,000,000 hours**
- **Temperature Range**
 - Operating:
 - Standard: 0°C to 70°C
 - Extended: -40°C to 85°C
 - Storage: -40°C to 100°C
- **Supply Voltage**
 - 5.0 V ± 5%
- **Power Consumption***
 - Active mode: 470 mA
 - Idle mode: 85 mA
- **Connector Type**
 - 7-pin SATA signal connector
 - 15-pin SATA power connector
- **Form Factor**
 - JEDEC MO-297
 - Dimensions (54.0 x 39.8 x 4.0, unit: mm)
- **Shock & Vibration****
 - Shock: 1,500 G
 - Vibration: 15 G
- **DRAM Cache for Enhanced Random Performance**
- **Thermal Sensor**
- **Device Sleep**
- **RoHS Compliant**

*Varies from capacities. The values for performances and power consumptions presented are typical and may vary depending on flash configurations or platform settings. Power consumption results of 128/256GB were based on experimental estimations.

**Non-operating

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1. General Descriptions

1.1 Introduction

Apacer's SS210-297 is a well-balanced solid-state disk (SSD) drive with compact form factor and great performance. Designed in SATA 6.0 Gbps interface, the SSD is able to deliver exceptional read/write speed, making it the ideal companion for heavy-loading industrial or server operations.

For data efficiency, the internal controlling unit of the SSD is engineered with DRAM for enhanced random performance. In regard of reliability, the drive comes with various implementations including powerful hardware ECC engine, power saving modes, wear leveling, flash block management, S.M.A.R.T., TRIM, and power failure management.

1.2 Capacity

Capacity specifications of SS210-297 are available as shown in Table 1-1. It lists the specific capacity and the default numbers of heads, sectors and cylinders for each product line.

Table 1-1 Capacity Specifications

| Capacity | Total bytes* | Cylinders | Heads | Sectors | Max LBA |
|----------|-----------------|-----------|-------|---------|-------------|
| 4 GB | 4,011,614,208 | 7,773 | 16 | 63 | 7,835,184 |
| 8 GB | 8,012,390,400 | 15,525 | 16 | 63 | 15,649,200 |
| 16 GB | 16,013,942,784 | 16,383 | 16 | 63 | 31,277,232 |
| 32 GB | 32,017,047,552 | 16,383 | 16 | 63 | 62,533,296 |
| 64 GB | 64,023,257,088 | 16,383 | 16 | 63 | 125,045,424 |
| 128 GB | 128,035,676,160 | 16,383 | 16 | 63 | 250,069,680 |

*Display of total bytes varies from file systems, which means not all of the bytes can be used for storage.

**Notes: 1 GB = 1,000,000,000 bytes; 1 sector = 512 bytes.

LBA count addressed in the table above indicates total user storage capacity and will remain the same throughout the lifespan of the device. However, the total usable capacity of the SSD is most likely to be less than the total physical capacity because a small portion of the capacity is reserved for device maintenance usages.

1.3 Performance

Performance of SS210-297 is listed below in Table 1-2.

Table 1-2 Performance Specifications

| Capacity | 4 GB | 8 GB | 16 GB | 32 GB | 64 GB | 128 GB |
|---------------------------------|--------|--------|--------|--------|--------|--------|
| Performance | | | | | | |
| Sequential Read* (MB/s) | 120 | 135 | 110 | 525 | 525 | 515 |
| Sequential Write* (MB/s) | 55 | 110 | 75 | 250 | 425 | 435 |
| Seq. Read QD32* (MB/s) | 125 | 135 | 110 | 555 | 555 | 545 |
| Seq. Write QD32* (MB/s) | 55 | 110 | 75 | 250 | 430 | 435 |
| Random Read IOPS** (4K) | 25,000 | 25,000 | 24,000 | 79,000 | 81,000 | 86,000 |
| Random Write IOPS** (4K) | 3,000 | 6,000 | 14,000 | 58,000 | 72,000 | 76,000 |

Note:

Results may differ from various flash configurations or host system setting.

*Sequential performance is based on CrystalDiskMark 5.2.1 with file size 1,000MB.

**Random performance measured using IOMeter with Queue Depth 32.

1.4 Pin Assignments

Table 1-4 describes the SFD signal segment and Table1-5 for power segment.

Figure 1-1 SATA Connectors

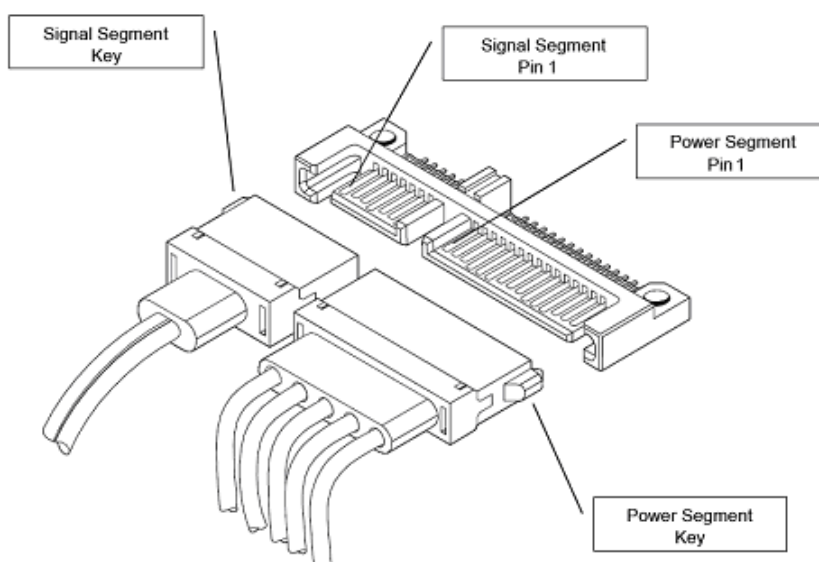


Table 1-3 Signal Segment

| Pin | Type | Description |
|-----|------|-------------------------|
| S1 | GND | |
| S2 | RxP | + Differential Receive |
| S3 | RxN | - Differential Receive |
| S4 | GND | |
| S5 | TxN | - Differential Transmit |
| S6 | TxP | + Differential Transmit |
| S7 | GND | |

Table 1-4 Power Segment

| Pin | Signal/Description |
|-------|--------------------|
| Pin1 | Unused (3.3V) |
| Pin2 | Unused (3.3V) |
| Pin3 | Device Sleep |
| Pin4 | Ground |
| Pin5 | Ground |
| Pin6 | Ground |
| Pin7 | 5V |
| Pin8 | 5V |
| Pin9 | 5V |
| Pin10 | Ground |
| Pin11 | DAS |
| Pin12 | Ground |
| Pin13 | Unused (12V) |
| Pin14 | Unused (12V) |
| Pin15 | Unused (12V) |



Figure 1-2 SATA Cable/Connector Connection Diagram

The connector on the left represents the Host with TX/RX differential pairs connected to a cable. The connector on the right shows the Device with TX/RX differential pairs also connected to the cable. Notice also the ground path connecting the shielding of the cable to the Cable Receptacle.

2. Software Interface

2.1 Command Set

Table 2-1 summarizes the ATA commands supported by SS210-297.

Table 2-1 Command Set

| Code | Command | Code | Command |
|-----------|------------------------------|------------|---------------------------|
| E5h | Check Power Mode | F6h | Security Disable Password |
| 90h | Execute Diagnostics | F3h | Security Erase Prepare |
| E7h | Flush Cache | F4h | Security Erase Unit |
| ECh | Identify Device | F5h | Security Freeze Lock |
| E3h | Idle | F1h | Security Set Password |
| E1h | Idle Immediate | F2h | Security Unlock |
| 91h | Initialize Device Parameters | 7Xh | Seek |
| C8h | Read DMA | EFh | Set Features |
| 25h | Read DMA EXT | C6h | Set Multiple Mode |
| 60h | Read FPDMA Queued | E6h | Sleep |
| 47h | Read Log DMA EXT | B0h | S.M.A.R.T. |
| 2Fh | Read Log EXT | E2h | Standby |
| C4h | Read Multiple | E0h | Standby Immediate |
| 20 or 21h | Read Sector(s) | CAh | Write DMA |
| 40 or 41h | Read Verify Sector(s) | 35h | Write DMA EXT |
| 10h | Recalibrate | 61h | Write FPDMA Queued |
| 57h | Write Log DMA EXT | 3Fh | Write Log EXT |
| C5h | Write Multiple | 30h or 31h | Write Sector(s) |

2.2 S.M.A.R.T.

S.M.A.R.T. is an abbreviation for Self-Monitoring, Analysis and Reporting Technology, a self-monitoring system that provides indicators of drive health as well as potential disk problems. It serves as a warning for users from unscheduled downtime by monitoring and displaying critical drive information. Ideally, this should allow taking proactive actions to prevent drive failure and make use of S.M.A.R.T. information for future product development reference.

Apacer devices use the standard SMART command B0h to read data out from the drive to activate our S.M.A.R.T. feature that complies with the ATA/ATAPI specifications. S.M.A.R.T. Attribute IDs shall include initial bad block count, total later bad block count, maximum erase count, average erase count, power on hours and power cycle. When the S.M.A.R.T. Utility running on the host, it analyzes and reports the disk status to the host before the device reaches in critical condition.

Note: Attribute IDs may vary from product models due to various solution design and supporting capabilities.

Apacer memory products come with S.M.A.R.T. commands and subcommands for users to obtain information of drive status and to predict potential drive failures. Users can take advantage of the following commands/subcommands to monitor the health of the drive.

| Code | SMART Subcommand |
|------|-----------------------------------|
| D0h | READ DATA |
| D1h | READ ATTRIBUTE THRESHOLDS |
| D2h | Enable/Disable Attribute Autosave |
| D4h | Execute Off-line Immediate |
| D5h | Read Log (optional) |
| D6h | Write Log (optional) |
| D8h | Enable Operations |
| D9h | Disable operations |
| DAh | Return Status |

General SMART attribute structure

| Byte | Description |
|-------|-------------|
| 0 | ID (Hex) |
| 1 – 2 | Status flag |
| 3 | Value |
| 4 | Worst |
| 5*-11 | Raw Data |

*Byte 5: LSB

SMART attribute ID list

| ID (Hex) | Attribute Name |
|------------|------------------------------------|
| 9 (0x09) | Power-on hours |
| 12 (0x0C) | Power cycle count |
| 163 (0xA3) | Max. erase count |
| 164 (0xA4) | Avg. erase count |
| 166 (0xA6) | Total later bad block count |
| 167 (0xA7) | SSD Protect Mode (vendor specific) |
| 168 (0xA8) | SATA PHY Error Count |
| 175 (0xAF) | Bad Cluster Table Count |
| 192 (0xC0) | Unexpected Power Loss Count |
| 194 (0xC2) | Temperature |
| 241 (0xF1) | Total sectors of write |

3. Flash Management

3.1 Error Correction/Detection

SS210-297 implements a hardware ECC scheme, based on the BCH algorithm. It can detect and correct up to 40 bits error in 1K bytes.

3.2 Flash Block Management

Current production technology is unable to guarantee total reliability of NAND flash memory array. When a flash memory device leaves factory, it comes with a minimal number of initial bad blocks during production or out-of-factory as there is no currently known technology that produce flash chips free of bad blocks. In addition, bad blocks may develop during program/erase cycles. When host performs program/erase command on a block, bad block may appear in Status Register. Since bad blocks are inevitable, the solution is to keep them in control. Apacer flash devices are programmed with ECC, block mapping technique and S.M.A.R.T to reduce invalidity or error. Once bad blocks are detected, data in those blocks will be transferred to free blocks and error will be corrected by designated algorithms.

3.3 Global Wear Leveling

Flash memory devices differ from Hard Disk Drives (HDDs) in terms of how blocks are utilized. For HDDs, when a change is made to stored data, like erase or update, the controller mechanism on HDDs will perform overwrites on blocks. Unlike HDDs, flash blocks cannot be overwritten and each P/E cycle wears down the lifespan of blocks gradually. Repeatedly program/erase cycles performed on the same memory cells will eventually cause some blocks to age faster than others. This would bring flash storages to their end of service term sooner. Global wear leveling is an important mechanism that levels out the wearing of all blocks so that the wearing-down of all blocks can be almost evenly distributed. This will increase the lifespan of SSDs.

3.4 Power Failure Management

Power Failure Management plays a crucial role when experiencing unstable power supply. Power disruption may occur when users are storing data into the SSD. In this urgent situation, the controller would run multiple write-to-flash cycles to store the metadata for later block rebuilding. This urgent operation requires about several milliseconds to get it done. At the next power up, the firmware will perform a status tracking to retrieve the mapping table and resume previously programmed NAND blocks to check if there is any incompleteness of transmission.

Note: The controller unit of this product model is designed with a DRAM as a write cache for improved performance and data efficiency. Though unlikely to happen in most cases, the data cached in the volatile DRAM might be potentially affected if a sudden power loss takes place before the cached data is flushed into non-volatile NAND flash memory.

3.5 ATA Secure Erase

ATA Secure Erase is an ATA disk purging command currently embedded in most of the storage drives. Defined in ATA specifications, (ATA) Secure Erase is part of Security Feature Set that allows storage drives to erase all user data areas. The erase process usually runs on the firmware level as most of the ATA-based storage media currently in the market are built-in with this command. ATA Secure Erase can securely wipe out the user data in the drive and protects it from malicious attack.

3.6 TRIM

TRIM is a SATA command that helps improve the read/write performance and efficiency of solid-state drives (SSD). The command enables the host operating system to inform SSD controller which blocks contain invalid data, mostly because of the erase commands from host. The invalid will be discarded permanently and the SSD will retain more space for itself.

3.7 SATA Power Management

By complying with SATA 6.0 Gb/s specifications, the SSD supports the following SATA power saving modes:

- ACTIVE: PHY ready, full power, Tx & Rx operational
- PARTIAL: Reduces power, resumes in under 10 μ s (microseconds)
- SLUMBER: Reduces power, resumes in under 10 ms (milliseconds)
- HIPM: Host-Initiated Power Management
- DIPM: Device-Initiated Power Management
- AUTO-SLUMBER: Automatic transition from partial to slumber.
- Device Sleep (DevSleep or DEVSLP): PHY powered down; power consumption \leq 5 mW; host assertion time \leq 10 ms; exit timeout from this state \leq 20 ms (unless specified otherwise in SATA Identify Device Log).

Note: The behaviors of power management features would depend on host/device settings.

3.8 Thermal Sensor

Apacer Thermal Sensor is a digital temperature sensor with serial interface. By using designated pins for transmission, storage device owners are able to read temperature data.

4. Environmental Specifications

4.1 Environmental Specifications

SS210-297 environmental specifications follow the US military standards, shown in the table below.

Table 4-1 Environmental Specifications

| Environment | Specifications |
|-------------|---|
| Temperature | 0°C to 70°C (Standard); -40°C to 85°C (Extended) |
| | -40°C to 100°C (Non-operating) |
| Vibration | Non-operating: Sine wave, 15(G), 10~2000(Hz), Operating: Random, 7.69(Grms), 20~2000(Hz) |
| Shock | Non-operating: Acceleration, 1,500 G, 0.5 ms Operating: Peak acceleration, 50 G, 11 ms |

4.2 Mean Time Between Failures (MTBF)

Mean Time Between Failures (MTBF) is predicted based on reliability data for the individual components in SS210-297. The prediction result for SS210-297 is more than 2,000,000 hours.

Note: The MTBF is predicated and calculated based on “Telcordia Technologies Special Report, SR-332, Issue 2” method.

4.3 Certification and Compliance

SS210-297 complies with the following standards:

- CE
- FCC
- RoHS
- MIL-STD-810F

5. Electrical Specifications

5.1 Operating Voltage

Table 5-1 lists the supply voltage for SS210-297.

Table 5-1 Operating Range

| Item | Range |
|----------------|--------------------------|
| Supply Voltage | 5V \pm 5% (4.75-5.25V) |

5.2 Power Consumption

Table 5-2 lists the power consumption for SS210-297.

Table 5-2 Power Consumption

| Capacity | 4 GB | 8 GB | 16 GB | 32 GB | 64 GB | 128 GB |
|--------------------|------|------|-------|-------|-------|--------|
| Mode | | | | | | |
| Active (mA) | 205 | 280 | 200 | 310 | 455 | 470 |
| Idle (mA) | 85 | 85 | 85 | 80 | 80 | 80 |

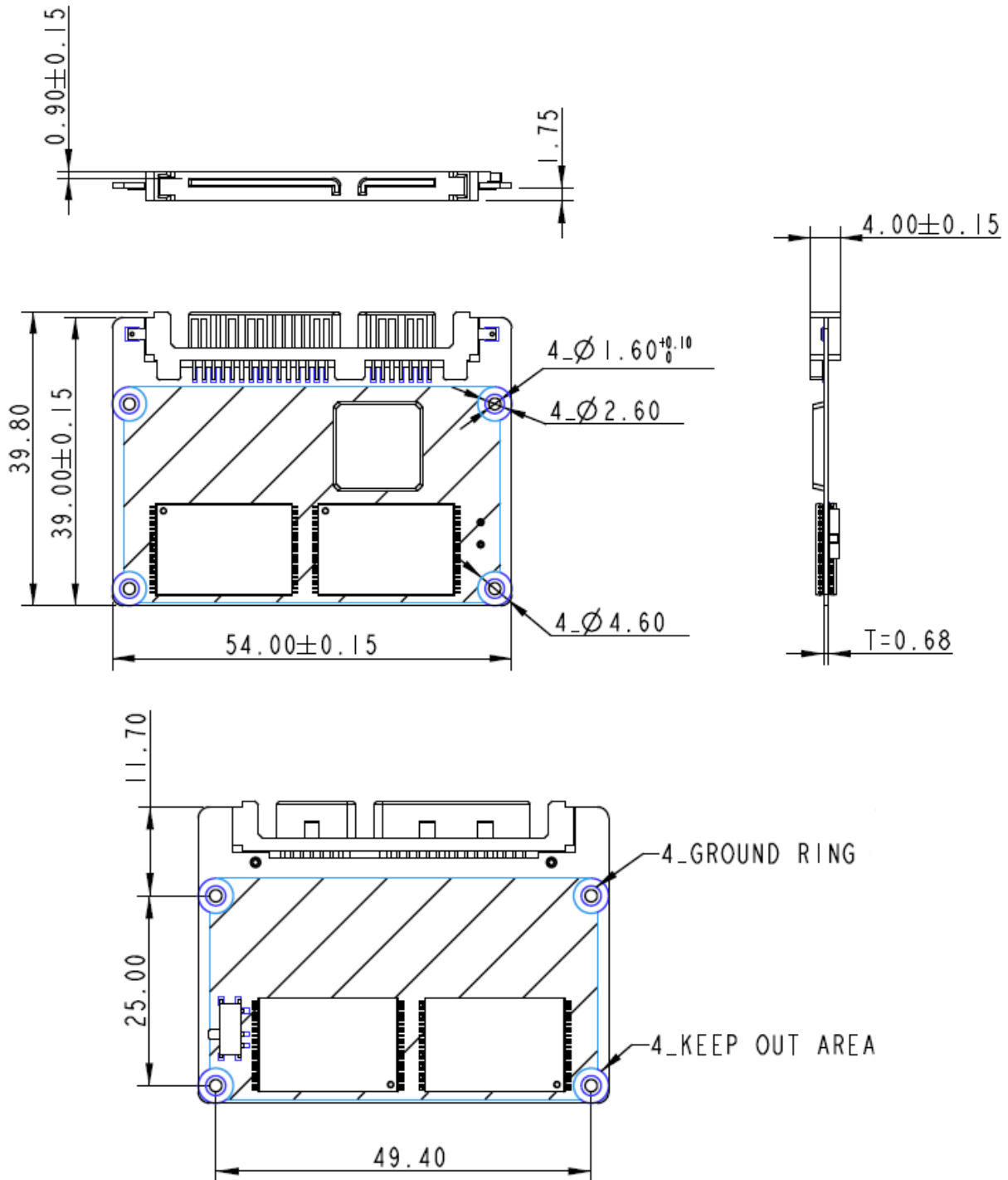
Note:

*All values are typical and may vary depending on flash configurations or host system settings.

**Active power is an average power measurement performed using CrystalDiskMark with 128KB sequential read/write transfers.

6. Physical Characteristics

6.1 Dimensions – TSOP



6.2 Dimensions – BGA



7. Product Ordering Information

7.1 Product Code Designations



7.2 Valid Combinations

| Capacity | Standard Temperature | Extended Temperature |
|----------|----------------------|----------------------|
| 4GB | APS297F004G-4BTF | APS297F004G-4BTWF |
| 8GB | APS297F008G-4BTF | APS297F008G-4BTWF |
| 16GB | APS297F016G-4BTF | APS297F016G-4BTWF |
| 32GB | APS297F032G-4BTF | APS297F032G-4BTWF |
| 64GB | APS297F064G-4BTF | APS297F064G-4BTWF |
| 128GB | APS297F128G-4BTF | APS297F128G-4BTWF |

Note: Valid combinations are those products in mass production or will be in mass production. Consult your Apacer sales representative to confirm availability of valid combinations and to determine availability of new combinations.

Revision History

| Revision | Description | Date |
|----------|-------------------------------------|------------|
| 1.0 | Official release | 8/10/2017 |
| 1.1 | Updated 6. Physical Characteristics | 10/25/2017 |

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