

## 24-bit, High Performance 192kHz Stereo DAC

### DESCRIPTION

The WM8740 is a very high performance stereo DAC designed for audio applications such as CD, DVD, home theatre systems, set top boxes and digital TV. The WM8740 supports data input word lengths from 16 to 24-bits and sampling rates up to 192kHz. The WM8740 consists of a serial interface port, digital interpolation filter, multi-bit sigma delta modulator and stereo DAC in a small 28-pin SSOP package. The WM8740 also includes a digitally controllable mute and attenuator function on each channel.

The internal digital filter has two selectable roll-off characteristics. A sharp or slow roll-off can be selected dependent on application requirements. Additionally, the internal digital filter can be by-passed and the WM8740 used with an external digital filter.

The WM8740 supports two connection schemes for audio DAC control. The SPI-compatible serial control port provides access to a wide range of features including on-chip mute, attenuation and phase reversal. A hardware controllable interface is also available.

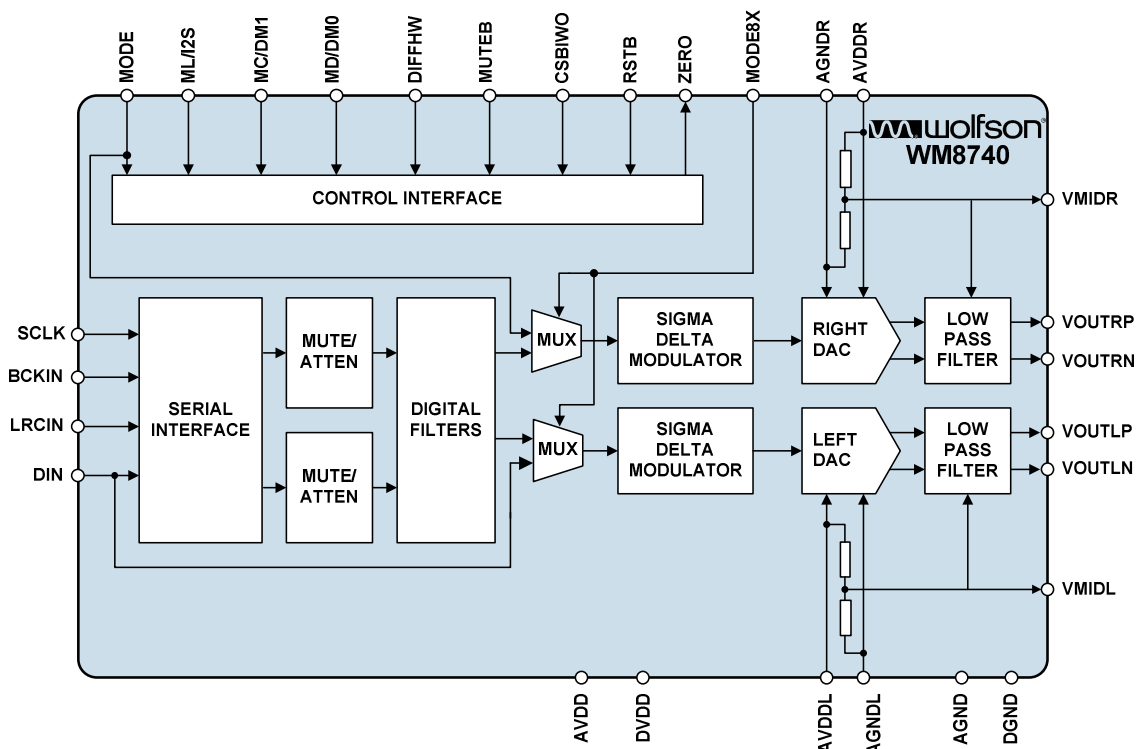
### FEATURES

- 120dB SNR ('A' weighted mono @48kHz), THD+N: -104dB @ FS
- 117dB SNR ('A' weighted stereo @48kHz), THD+N: -104dB @ FS
- Sampling frequency: 8kHz to 192kHz
- Selectable digital filter roll-off
- Optional interface to industry standard external filters
- Differential mono mode needing no glue logic
- Input data word: 16 to 24-bit
- Hardware or SPI compatible serial control modes:
  - Hardware mode: mute, de-emphasis, audio format control
  - Serial mode: mute, de-emphasis, attenuation (256 steps), phase reversal
- Fully differential voltage outputs

### APPLICATIONS

- CD, DVD audio
- Home theatre systems
- Professional audio systems

### BLOCK DIAGRAM



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## PIN CONFIGURATION

|        |                          |     |    |                          |        |
|--------|--------------------------|-----|----|--------------------------|--------|
| LRCIN  | <input type="checkbox"/> | 1 ● | 28 | <input type="checkbox"/> | ML/I2S |
| DIN    | <input type="checkbox"/> | 2   | 27 | <input type="checkbox"/> | MC/DM1 |
| BCKIN  | <input type="checkbox"/> | 3   | 26 | <input type="checkbox"/> | MD/DM0 |
| MODE8X | <input type="checkbox"/> | 4   | 25 | <input type="checkbox"/> | MUTEB  |
| SCLK   | <input type="checkbox"/> | 5   | 24 | <input type="checkbox"/> | MODE   |
| DIFFHW | <input type="checkbox"/> | 6   | 23 | <input type="checkbox"/> | CSBIWO |
| DGND   | <input type="checkbox"/> | 7   | 22 | <input type="checkbox"/> | RSTB   |
| DVDD   | <input type="checkbox"/> | 8   | 21 | <input type="checkbox"/> | ZERO   |
| AVDDR  | <input type="checkbox"/> | 9   | 20 | <input type="checkbox"/> | AVDDL  |
| AGNDR  | <input type="checkbox"/> | 10  | 19 | <input type="checkbox"/> | AGNDL  |
| VMIDR  | <input type="checkbox"/> | 11  | 18 | <input type="checkbox"/> | VMIDL  |
| VOUTRP | <input type="checkbox"/> | 12  | 17 | <input type="checkbox"/> | VOUTLP |
| VOUTRN | <input type="checkbox"/> | 13  | 16 | <input type="checkbox"/> | VOUTLN |
| AGND   | <input type="checkbox"/> | 14  | 15 | <input type="checkbox"/> | AVDD   |

## ORDERING INFORMATION

| DEVICE        | TEMPERATURE RANGE | PACKAGE     | MOISTURE SENSITIVITY LEVEL | PEAK SOLDERING TEMPERATURE |
|---------------|-------------------|-------------|----------------------------|----------------------------|
| WM8740SEDS/V  | -40° to +85°C     | 28-pin SSOP | MSL2                       | 260°C                      |
| WM8740SEDS/RV | -40° to +85°C     | 28-pin SSOP | MSL2                       | 260°C                      |

**Note:**

Reel Quantity: 2,000

**PIN DESCRIPTION**

| PIN | NAME   | TYPE            | DESCRIPTION  |
|-----|--------|-----------------|--|
| 1   | LRCIN  | Digital input   | Sample rate clock input.   |
| 2   | DIN    | Digital input   | Audio data serial input (except in 8XMODE when it is DINL).                      |
| 3   | BCKIN  | Digital input   | Audio data bit clock input .   |
| 4   | MODE8X | Digital input   | Internal pull-down, active high, 8 x fs mode.                                    |
| 5   | SCLK   | Digital input   | System clock input.  |
| 6   | DIFFHW | Digital input   | Internal pull-down, active high, differential mono mode.                         |
| 7   | DGND   | Supply          | Digital ground supply.   |
| 8   | DVDD   | Supply          | Digital positive supply.   |
| 9   | AVDDR  | Supply          | Analogue positive supply.  |
| 10  | AGNDR  | Supply          | Analogue ground supply.  |
| 11  | VMIDR  | Analogue output | Mid rail right channel.  |
| 12  | VOUTRP | Analogue output | Right channel DAC output positive.   |
| 13  | VOUTRN | Analogue output | Right channel DAC output negative.   |
| 14  | AGND   | Supply          | Analogue ground supply.  |
| 15  | AVDD   | Supply          | Analogue positive supply.  |
| 16  | VOUTLN | Analogue output | Left channel DAC output negative.  |
| 17  | VOUTLP | Analogue output | Left channel DAC output positive.  |
| 18  | VMIDL  | Analogue output | Mid rail left channel.   |
| 19  | AGNDL  | Supply          | Analogue ground supply.  |
| 20  | AVDDL  | Supply          | Analogue positive supply.  |
| 21  | ZERO   | Digital output  | Infinite zero detect – active low. Open drain type output with active pull-down. |
| 22  | RSTB   | Digital input   | Reset input – active low. Internal pull-up.                                      |

| PIN | NAME   | TYPE                                | DESCRIPTION  |  |  | Software Mode  |
|-----|--------|-------------------------------------|--|--|--|--|
|     |        |                                     | Normal Mode  | Differential Mode  | 8X Mode  |  |
| 23  | CSBIWO | Digital input<br>Internal pull-down | Wordlength:<br>Low for 16-bit data.<br>High for 20-bit<br>(normal) or 24-bit<br>I <sup>2</sup> S data. | Wordlength:<br>Low for 16-bit data.<br>High for 20-bit<br>(normal) or 24-bit<br>I <sup>2</sup> S data. | Wordlength:<br>Low for 20-bit data.<br>High for 24-bit data.           | Low for<br>serial<br>interface<br>operation.             |
| 24  | MODE   | Digital input<br>Internal pull-up   | Low for hardware<br>mode.  | Low for left<br>mono mode.<br>High for right<br>mono mode  | DINR   | High for<br>software<br>mode.                            |
| 25  | MUTEB  | Digital input<br>Internal pull-up   | Low to soft mute.<br>High for normal<br>operation.   | Low to soft mute.<br>High for normal<br>operation.   | Low to soft mute.<br>High for normal<br>operation.                     | Low to<br>soft mute.<br>High for<br>normal<br>operation. |
| 26  | MD/DM0 | Digital input<br>Internal pull-up   | De-emphasis mode<br>select bit 0.  | Low for no<br>de-emphasis.<br>High for 44.1kHz<br>de-emphasis.   | LRP – LRCLK<br>polarity select.  | Control serial<br>interface<br>data signal.              |
| 27  | MC/DM1 | Digital input<br>Internal pull-up   | De-emphasis mode<br>select bit 1.  | Low for normal filter<br>operation.<br>High for filter slow<br>roll-off.                               | Unused.<br>Leave unconnected.  | Control serial<br>interface<br>clock signal.             |
| 28  | ML/I2S | Digital input<br>Internal pull-up   | Audio serial format:<br>Low – right justified.<br>High – I <sup>2</sup> S.                             | Audio serial format:<br>Low – right justified.<br>High – I <sup>2</sup> S.                             | Input data format:<br>Low – right justified.<br>High – left justified. | Control serial<br>interface<br>load signal.              |

**Note:** Digital input pins have Schmitt trigger input buffers.

## ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

| CONDITION                                   | MIN                   | MAX        |
|---|-----------------------|------------|
| Supply voltage                              | -0.3V                 | +7.0V      |
| Input                                       | GND -0.3V             | VDD + 0.3V |
| Operating temperature range, T <sub>A</sub> | -40°C                 | +85°C      |
| Storage temperature prior to soldering      | 30°C max / 85% RH max |            |
| Storage temperature after soldering         | -65°C                 | +150°C     |

**Note:** It is strongly recommended that AVDD, AVDDL and AVDDR are tied together. AGND, AGNDL and AGND right must also be tied together.

## RECOMMENDED OPERATING CONDITIONS

| PARAMETER               | SYMBOL      | TEST CONDITIONS | MIN  | TYP      | MAX  | UNIT |
|-------------------------|-------------|-----------------|------|----------|------|------|
| Digital supply range    | DVDD        |                 | -10% | 3.3 to 5 | +10% | V    |
| Analogue supply range   | AVDD        |                 | -10% | 3.3 to 5 | +10% | V    |
| Ground                  | AGND, DGND  |                 |      | 0        |      | V    |
| Difference DGND to AGND |             |                 | -0.3 | 0        | +0.3 | V    |
| Analogue supply current | AVDD = 5V   |                 |      | 13       |      | mA   |
| Digital supply current  | DVDD = 5V   |                 |      | 19       |      | mA   |
| Analogue supply current | AVDD = 3.3V |                 |      | 12       |      | mA   |
| Digital supply current  | DVDD = 3.3V |                 |      | 12       |      | mA   |

### Note:

DVDD must be equal to, or less than the AVDD supply (i.e. DVDD = AVDD = +5V; DVDD = AVDD = +3.3V; DVDD = +3.3V AVDD = +5V).

## ELECTRICAL CHARACTERISTICS

### Test Conditions

AVDD, DVDD = 5V, AGND, DGND = 0V, T<sub>A</sub> = +25°C, f<sub>s</sub> = 48kHz, SCKI = 256fs unless otherwise stated.

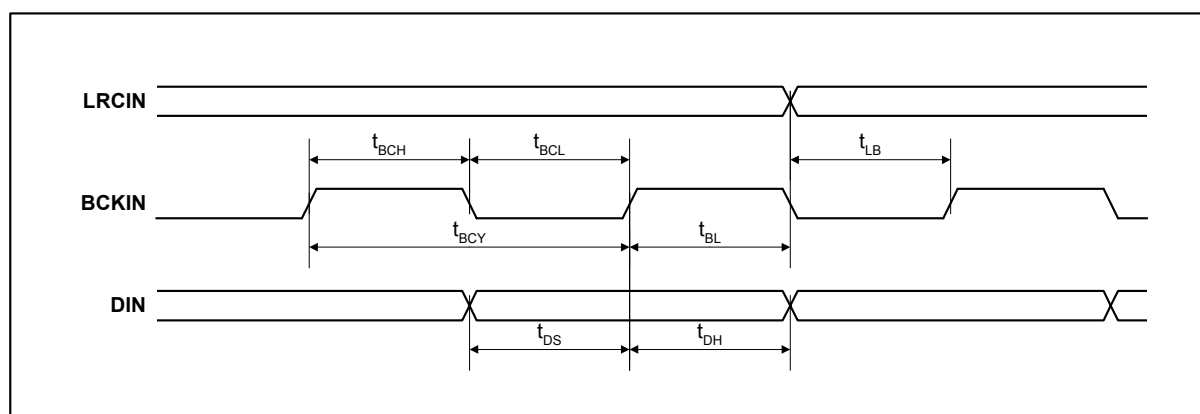
| PARAMETER                                      | SYMBOL          | TEST CONDITIONS       | MIN         | TYP     | MAX         | UNIT |
|--|-----------------|-----------------------|-------------|---------|-------------|------|
| <b>DAC Circuit Specifications</b>              |                 |                       |             |         |             |      |
| SNR<br>(See Note 1)                            |                 | Mono fs @ 48kHz       |             | 120     |             | dB   |
|  |                 | Stereo fs @ 48kHz     | 110         | 117     |             | dB   |
|  |                 | Stereo fs @ 96kHz     |             | 116     |             | dB   |
| THD (full-scale)<br>(See Note 2)               |                 | Mono 0dB              |             | -104    |             | dB   |
|  |                 | Stereo 0dB            | -95         | -104    |             | dB   |
| THD+N (Dynamic range)<br>(See Note 2)          |                 | -60dB                 |             | 117     |             | dB   |
| <b>Filter Characteristics (Sharp Roll-off)</b> |                 |                       |             |         |             |      |
| Passband                                       |                 | ±0.0012 dB            | 0.4535fs    |         |             | dB   |
| Stopband                                       |                 | -3dB                  |             | 0.491fs |             |      |
| Passband ripple                                |                 |                       |             |         | ±0.0012     | dB   |
| Stopband attenuation                           |                 | f > 0.5465fs          | -82         |         |             | dB   |
| Delay time                                     |                 |                       |             | 30/fs   |             | s    |
| <b>Filter Characteristics (Slow Roll-off)</b>  |                 |                       |             |         |             |      |
| Passband                                       |                 | ±0.001dB              | 0.274fs     |         |             |      |
| Stopband                                       |                 | -3dB                  | 0.459fs     |         |             |      |
| Passband ripple                                |                 |                       |             |         | ±0.001      | dB   |
| Stopband attenuation                           |                 | f > 0.732fs           | -82         |         |             | dB   |
| Delay time                                     |                 |                       |             | 9/fs    |             | s    |
| <b>Internal Analogue Filter</b>                |                 |                       |             |         |             |      |
| Bandwidth                                      |                 | -3dB                  |             | 195     |             | kHz  |
| Passband edge response                         |                 | 20kHz                 |             | -0.043  |             | dB   |
| <b>Digital Logic Levels</b>                    |                 |                       |             |         |             |      |
| Input LOW level                                | V <sub>IL</sub> |                       |             |         | 0.8         |      |
| Input HIGH level                               | V <sub>IH</sub> |                       | 2.0         |         |             | V    |
| Output LOW level                               | V <sub>OL</sub> | I <sub>OL</sub> = 2mA |             |         | DGND + 0.3V | V    |
| Output HIGH level                              | V <sub>OH</sub> | I <sub>OH</sub> = 2mA | DVDD - 0.3V |         |             |      |

**Test Conditions**

AVDD, DVDD = 5V, AGND, DGND = 0V,  $T_A = +25^\circ\text{C}$ ,  $f_s = 48\text{kHz}$ , SCKI = 256fs unless otherwise stated.

| PARAMETER                     | SYMBOL | TEST CONDITIONS                                   | MIN | TYP    | MAX | UNIT       |
|-------------------------------|--------|---|-----|--------|-----|------------|
| <b>Analogue Output Levels</b> |        |   |     |        |     |            |
| Output level differential     |        | Into 10k $\Omega$ , full scale 0dB, (5V supply)   |     | 2      |     | $V_{RMS}$  |
|                               |        | Into 10k $\Omega$ , full scale 0dB, (3.3V supply) |     | 1.32   |     | $V_{RMS}$  |
| Minimum resistance load       |        | To midrail or AC coupled (5V supply)              |     | 1      |     | k $\Omega$ |
|                               |        | To midrail or AC coupled (3.3V supply)            |     | 600    |     | $\Omega$   |
| Maximum capacitance load      |        | 5V or 3.3V  |     | 100    |     | pF         |
| Output DC level               |        |   |     | AVDD/2 |     | V          |
| <b>Reference Levels</b>       |        |   |     |        |     |            |
| Potential divider resistance  |        | AVDD to VMIDL/VMIDR and VMIDL/VMIDR to AGND       |     | 10     |     | k $\Omega$ |
| Voltage at VMIDL/VMIDR        |        |   |     | AVDD/2 |     |            |

- Notes:**
- Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
  - All performance measurements done with 20kHz low pass filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.



**Figure 1 Audio Data Input Timing**

**Test Conditions**

AVDD, DVDD = 5V, AGND, DGND = 0V,  $T_A = +25^\circ\text{C}$ ,  $f_s = 48\text{kHz}$ , SCKI = 256fs unless otherwise stated.

| PARAMETER                                  | SYMBOL    | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------|-----------------|-----|-----|-----|------|
| <b>Audio Data Input Timing Information</b> |           |                 |     |     |     |      |
| BCKIN pulse cycle time                     | $t_{BCY}$ |                 | 100 |     |     | ns   |
| BCKIN pulse width high                     | $t_{BCH}$ |                 | 40  |     |     | ns   |
| BCKIN pulse width low                      | $t_{BCL}$ |                 | 40  |     |     | ns   |
| BCKIN rising edge to LRCIN edge            | $t_{BL}$  |                 | 20  |     |     | ns   |
| LRCIN rising edge to BCKIN rising edge     | $t_{LB}$  |                 | 20  |     |     | ns   |
| DIN setup time                             | $t_{DS}$  |                 | 20  |     |     | ns   |
| DIN hold time                              | $t_{DH}$  |                 | 20  |     |     | ns   |

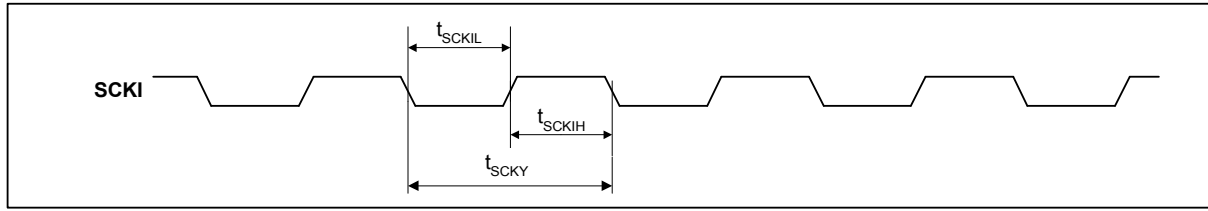


Figure 2 System Clock Timing Requirements

**Test Conditions**

AVDD, DVDD = 5V, AGND, DGND = 0V,  $T_A = +25^\circ\text{C}$ ,  $f_s = 48\text{kHz}$ , SCKI = 256fs unless otherwise stated.

| PARAMETER                              | SYMBOL      | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------|-----------------|-----|-----|-----|------|
| <b>System Clock Timing Information</b> |             |                 |     |     |     |      |
| System clock pulse width high          | $t_{SCKIH}$ |                 | 10  |     |     | ns   |
| System clock pulse width low           | $t_{SCKIL}$ |                 | 10  |     |     | ns   |
| System clock cycle time                | $t_{SCKY}$  |                 | 27  |     |     | ns   |

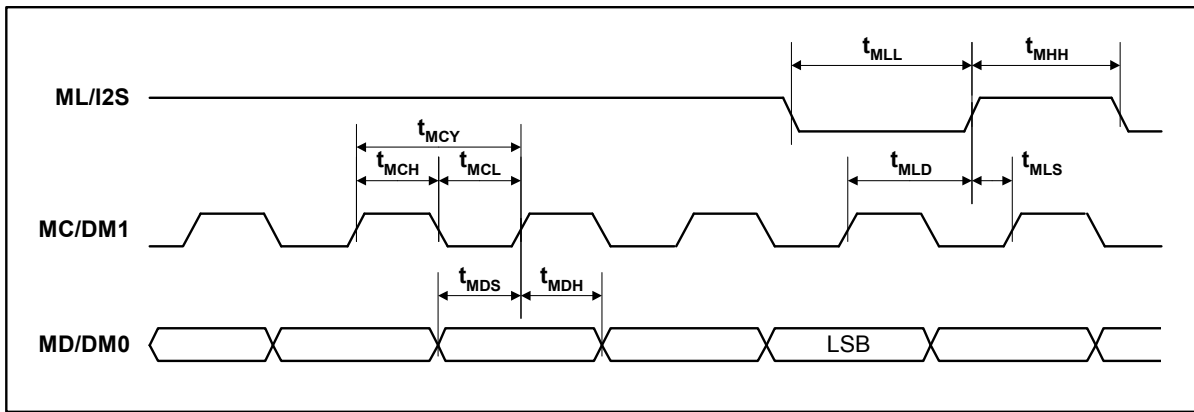


Figure 3 Program Register Input Timing – SPI Compatible Serial Control Mode

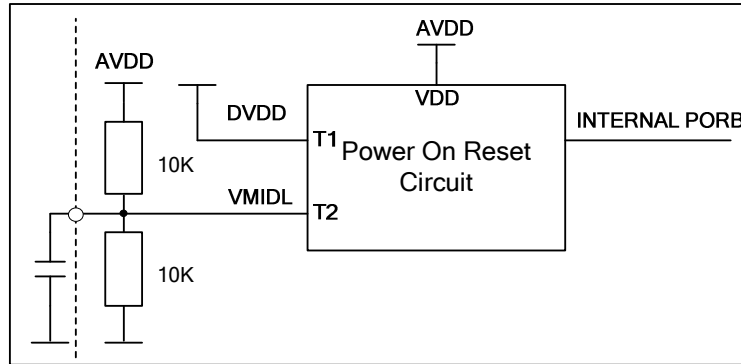
**Test Conditions**

AVDD, DVDD = 5V, AGND, DGND = 0V,  $T_A = +25^\circ\text{C}$ ,  $f_s = 48\text{kHz}$ , SCKI = 256fs unless otherwise stated.

| PARAMETER                                 | SYMBOL    | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------|-----------------|-----|-----|-----|------|
| <b>Program Register Input Information</b> |           |                 |     |     |     |      |
| MC/DM1 pulse cycle time                   | $t_{MCY}$ |                 | 80  |     |     | ns   |
| MC/DM1 pulse width low                    | $t_{MCL}$ |                 | 32  |     |     | ns   |
| MD/DM0 pulse width high                   | $t_{MCH}$ |                 | 32  |     |     | ns   |
| MD/DM0 set-up time                        | $t_{MDS}$ |                 | 10  |     |     | ns   |
| MC/DM1 hold time                          | $t_{MDH}$ |                 | 10  |     |     | ns   |
| ML/I2S pulse width low                    | $t_{MLL}$ |                 | 10  |     |     | ns   |
| ML/I2S pulse width high                   | $t_{MHH}$ |                 | 10  |     |     | ns   |
| ML/I2S set-up time                        | $t_{MLS}$ |                 | 10  |     |     | ns   |
| ML/I2S delay from MC                      | $t_{MLD}$ |                 | 10  |     |     | ns   |



**INTERNAL POWER ON RESET CIRCUIT**



**Figure 4 Internal Power On Reset Circuit Schematic**

The WM8740 includes an internal Power On Reset Circuit which is used reset the digital logic into a default state after power up.

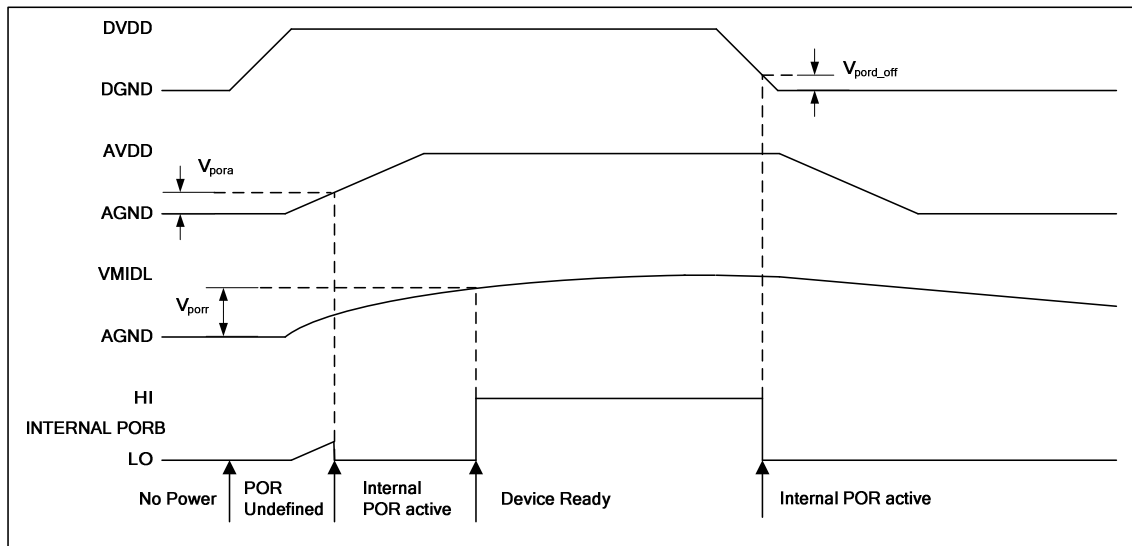
Figure 4 shows a schematic of the internal POR circuit. The POR circuit is powered from AVDD. The circuit monitors DVDD and VMIDL and asserts PORB low if DVDD or VMIDL are below the minimum threshold  $V_{por\_off}$ .

On power up, the POR circuit requires AVDD to be present to operate. PORB is asserted low until AVDD and DVDD and VMIDL are established. When AVDD, DVDD, and VMIDL have been established, PORB is released high, all registers are in their default state and writes to the digital interface may take place.

On power down, PORB is asserted low whenever DVDD or VMIDL drop below the minimum threshold  $V_{por\_off}$ .

If AVDD is removed at any time, the internal Power On Reset circuit is powered down and PORB will follow AVDD.

In most applications the time required for the device to release PORB high will be determined by the charge time of the VMIDL node.



**Figure 5 Typical Power Up Sequence where DVDD is Powered before AVDD**

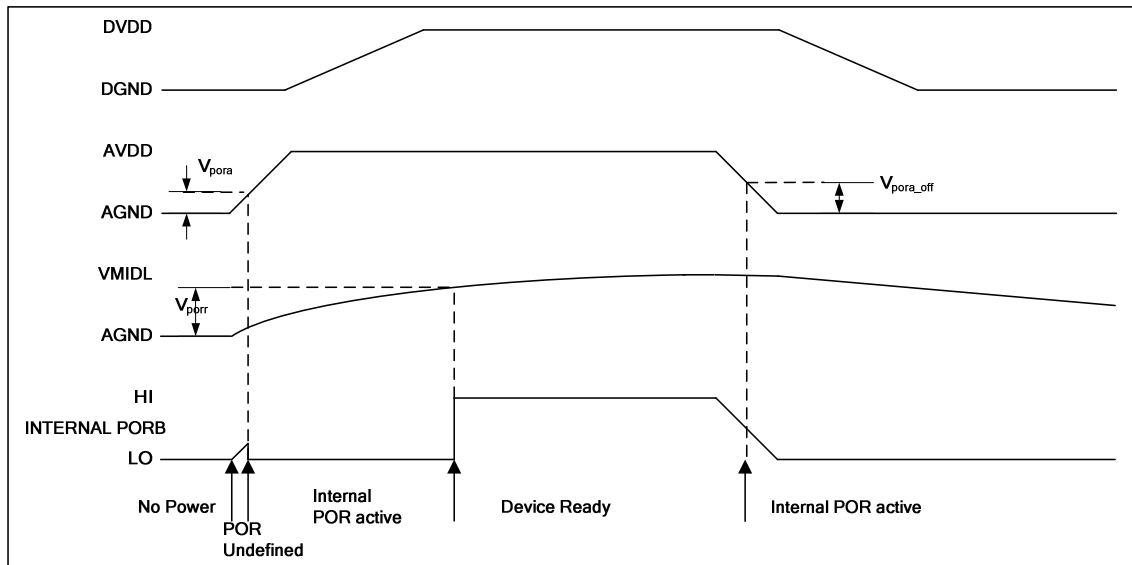


Figure 6 Typical Power Up Sequence where AVDD is Powered before DVDD

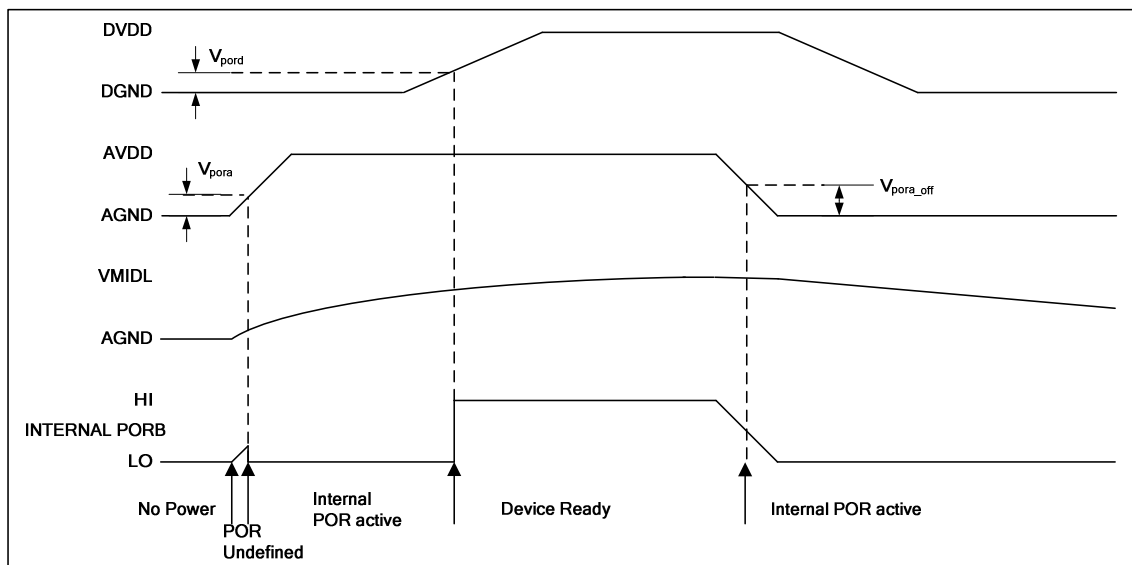


Figure 7 Typical Power Up Sequence where AVDD is Powered and VMIDL has Charged before DVDD

Typical POR Operation (typical values, not tested)

| SYMBOL          | TYP  | UNIT |
|-----------------|------|------|
| $V_{pora}$      | 0.35 | V    |
| $V_{pord}$      | 0.8  | V    |
| $V_{porr}$      | 0.85 | V    |
| $V_{pora\_off}$ | 2.6  | V    |
| $V_{pord\_off}$ | 0.8  | V    |

In a real application the designer is unlikely to have control of the relative power up sequence of AVDD and DVDD. Using the POR circuit to monitor VMIDLL ensures a reasonable delay between applying power to the device and Device Ready.

Figure 5 and Figure 6 show typical power up scenarios in a real system. Both AVDD and DVDD must be established and VMIDL must have reached the threshold  $V_{porr}$  before the device is ready and can be written to. Any writes to the device before Device Ready will be ignored.

Figure 5 shows DVDD powering up before AVDD. Figure 6 shows AVDD powering up before DVDD. In both cases, the time from applying power to Device Ready is dominated by the charge time of VMIDLL. In the case where AVDD is powered long before DVDD, thus allowing VMIDL to charge above  $V_{porr}$ , the PORB will not release until DVDD passes the  $V_{pord}$  threshold. This situation is shown in Figure 7.

## DEVICE DESCRIPTION

The WM8740 is a high performance 128fs oversampling rate stereo DAC employing a novel 64 level sigma delta DAC design which provides optimised signal-to-noise performance and clock jitter tolerance. It is ideally suited to high quality audio applications such as CD, DVD-audio, home theatre receivers and professional mixing consoles. The WM8740 supports sample rates from 8ks/s to 192ks/s.

The control functions of the WM8740 are either pin selected (hardware mode) or programmed via the serial interface (software mode). Control functions that are available include: data input word length and format selection (16-24 bits: I<sup>2</sup>S, left justified or right justified); de-emphasis sample rate selection (48kHz, 44.1kHz and 32kHz); differential output modes; a software or hardware mute and independently digitally controllable attenuation on both channels.

The digital filtering may be bypassed entirely by selecting MODE8X. Data is then input directly to the DAC, bypassing the digital filters. Left and right channels are input separately, using the MODE pin as the right channel input. This mode allows the use of alternative digital filters, such as the Pacific Microsonics PMD100 HDCD filter.

In addition to the normal stereo operating mode the WM8740 may also be used in dual differential mode with either the left or right channel (selectable) being output dual differentially. Two WM8740s can then be used in parallel to implement a stereo channel, each supporting a single channel differentially. Note that this mode uses 2 pairs of differential outputs for each channel – the benefit is SNR improved by 3dB. This mode is available in both software and hardware modes and may also be used in conjunction with MODE8X.

## SYSTEM CLOCK

Sample rates from 8ks/s up to 96ks/s are available, and automatically selected, with a system clock of 256fs or 384fs. In addition a system clock of 128fs or 192fs may be used, with sample rates up to 192ks/s. With a 128fs or 192fs system clock 64x oversampling mode operation is automatically selected and the first stage of the digital filter is bypassed.

WM8740 has an asynchronous monitor circuit, which in the event of removal of the master system clock, resets the digital filters and analogue circuits, muting the output. Re-application of the system clock re-starts the filters from an initialised state. Control registers are not reset under this condition.

The WM8740 is tolerant of asynchronous bit clock jitter. The internal signal processing resynchronises to the external LRCIN once the phase difference between bit clock and the system clock exceeds half an LRCIN period. During this re-synch period the interpolating filters will either miss or repeat an audio sample, minimising the audible effects of the operation. Table 1 shows the typical system clock frequency inputs for the WM8740.

| SAMPLING RATE (LRCIN) | SYSTEM CLOCK FREQUENCY (MHZ) |        |             |             |             |             |
|-----------------------|------------------------------|--------|-------------|-------------|-------------|-------------|
|                       | 128fs                        | 192fs  | 256fs       | 384fs       | 512fs       | 768fs       |
| 32kHz                 | 4.096                        | 6.144  | 8.192       | 12.288      | 16.384      | 24.576      |
| 44.1kHz               | 5.6448                       | 8.467  | 11.2896     | 16.9340     | 22.5792     | 33.8688     |
| 48kHz                 | 6.114                        | 9.216  | 12.288      | 18.432      | 24.576      | 36.864      |
| 96kHz                 | 12.288                       | 18.432 | 24.576      | 36.864      | Unavailable | Unavailable |
| 192kHz                | 24.576                       | 36.864 | Unavailable | Unavailable | Unavailable | Unavailable |

Table 1 System Clock Frequencies Versus Sampling Rate

## AUDIO DATA INTERFACE

Data may be input at a rate corresponding to the system clock having a rate of 256fs or 384fs, in which case an oversampling ratio of 128x is selected. Alternatively a rate of 128fs or 192fs may be used, in which case the first filter stage is bypassed and an oversampling ratio of 64x results. Finally, in MODE8X, data may be input at 8x the normal rate, in which case separate input pins are used to input the two stereo channels of data (unless DIFFHW mode and MODE8X are both selected, in which case only a mono channel is converted differentially). In MODE8X all filter stages are bypassed, prior to the sigma delta modulator, MODE8X is not supported at 192kHz sampling rate. Data is input MSB first in all modes.

**NORMAL SAMPLE RATE**

In normal mode, the data is input serially on one pin for both left and right channels.

Data can be "right justified" meaning that the last 16, 20 or 24 bits (depending on chosen PCM word length) that were clocked in prior to the transition on LRCIN are valid.

Alternatively data can be "left justified" (20 and 24-bit PCM data only), where the bits are clocked in as the first 20 or 24 bits after a transition on LRCIN.

For the three I<sup>2</sup>S modes supported (16-bit, 20-bit and 24-bit PCM data), data is clocked "left justified" except with one additional preceding clock cycle.

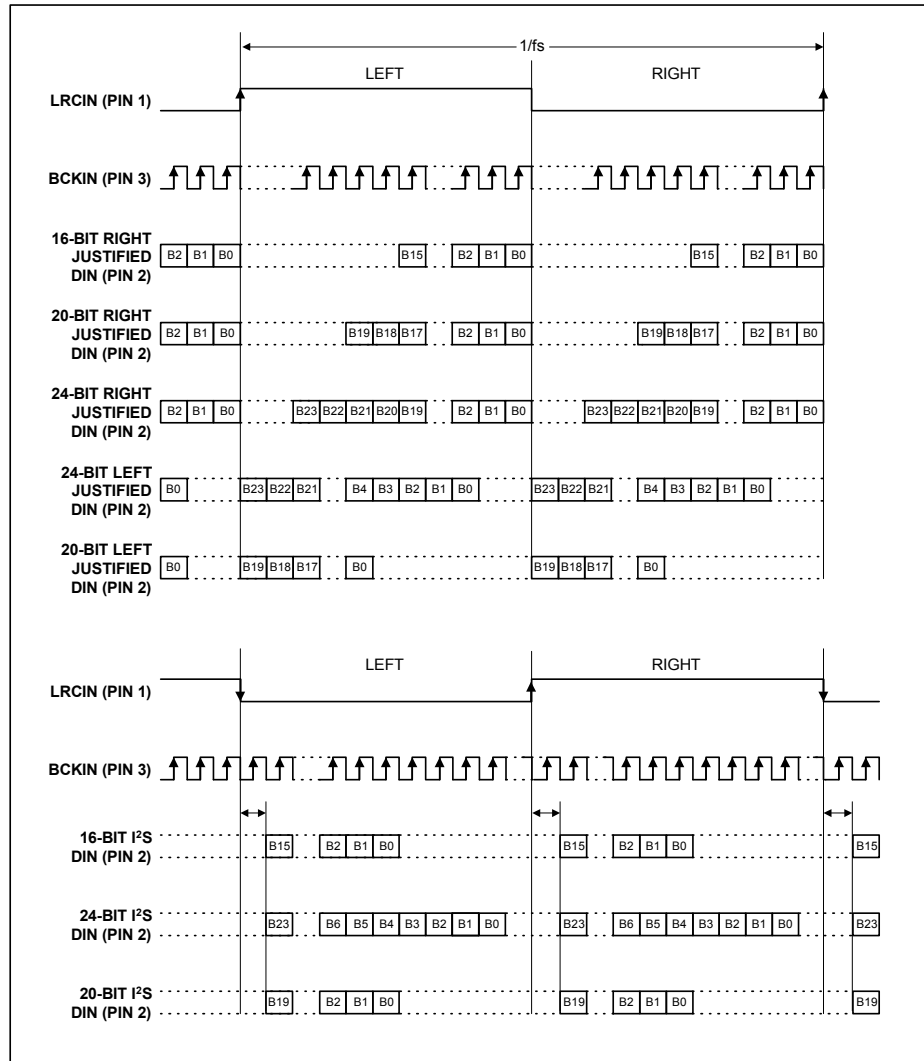


Figure 8 Audio Data Input Format

## 8 X FS INPUT SAMPLE RATE

Due to the higher speed of the interface in 8 x fs mode, audio data is input on two pins. The MODE pin (pin 24) is used as the second input for the right channel data and left data is input on DIN (pin2). In this mode, software control of the device is not available. The data can be input in two formats, left or right justified, selectable by ML/I2S and two word lengths (20 or 24 bit), selectable by CSBIWO. In both modes the data is always clocked in MSB first.

For left justified data the word start is marked by the falling edge of LRCIN. The data is clocked in on the next 20/24 BCKIN rising edges. This format is compatible with devices such as the PMD100.

For right justified the data is justified to the rising edge of LRCIN and the data is clocked in on the preceding 20/24 BCKIN rising edges before the LRCIN rising edge. This format is compatible with devices such as the DF1704 or SM5842.

In both modes the polarity of LRCIN can be switched using MD/DM0.

Differential hardware mode can be used in conjunction with 8fs mode by setting the DIFFHW pin high. In differential 8fs mode the data is input on DIN and output differentially. MODE is unused and must be tied low.

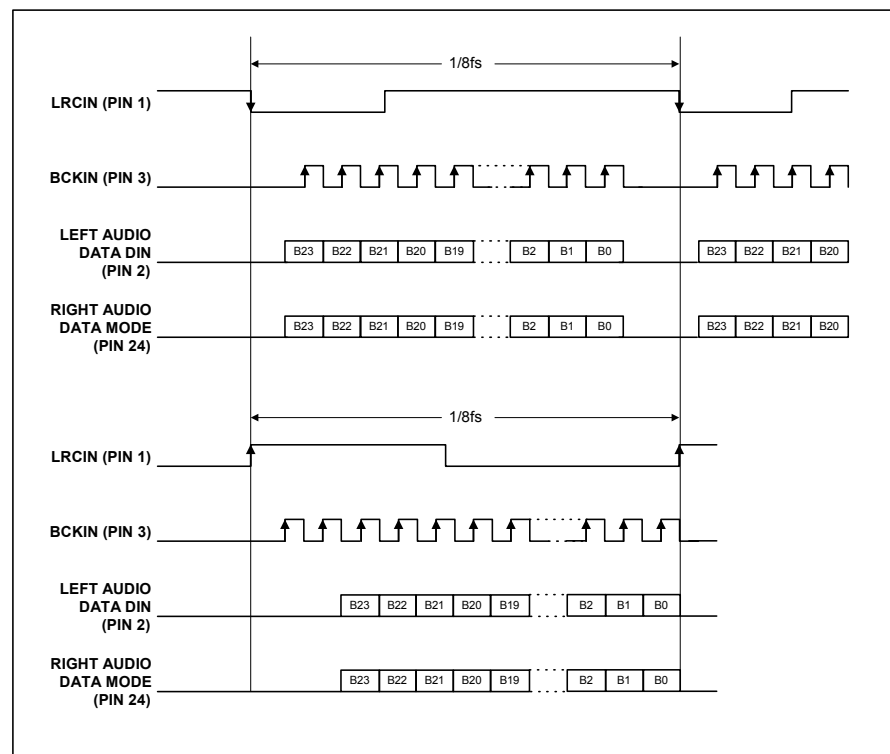


Figure 9 Audio Data Input Format (8 x fs Operation)

## MODES OF OPERATION

Control of the various modes of operation is either by software control over the serial interface, or by hard-wired pin control. Selection of software or hardware mode is via MODE pin. The following functions may be controlled either via the serial control interface or by hard wiring of the appropriate pins.

## HARDWARE CONTROL MODES

When the MODE pin is held 'low' the following hardware modes of operation are available. In Hardware differential mode or 8X mode some of these modes/control words are altered or unavailable.

**DE-EMPHASIS CONTROL**

| MDDM1<br>PIN 27 | MCDMO<br>PIN 26 | DE-EMPHASIS |
|-----------------|-----------------|-------------|
| L               | L               | Off         |
| L               | H               | 48kHz       |
| H               | L               | 44.1kHz     |
| H               | H               | 32kHz       |

Table 2 De-Emphasis Control

**AUDIO INPUT FORMAT**

| ML/I2S<br>PIN 28 | CSBIWO<br>PIN 23 | DATA FORMAT                   |
|------------------|------------------|-------------------------------|
| L                | L                | 16 bit normal right justified |
| L                | H                | 20 bit normal right justified |
| H                | L                | 16 bit I <sup>2</sup> S       |
| H                | H                | 24 bit I <sup>2</sup> S       |

Table 3 Audio Input Format

**SOFT MUTE**

| MUTE B<br>PIN 25 | FUNCTION                    |
|------------------|-----------------------------|
| L                | Mute On (no output)         |
| H                | Mute Off (normal operation) |

Table 4 Soft Mute

A logic low on the MUTE B pin will cause the attenuation to ramp to infinite attenuation at a rate of 128/fs seconds per 0.5dB step. Setting MUTE B high will cause the attenuation to ramp back to its previous value.

**SOFTWARE CONTROL INTERFACE**

The WM8740 can be controlled using a 3-wire serial interface. MD/DM0 (pin 26) is used for the program data, MC/DM1 (pin 22) is used to clock in the program data and ML/I2S (pin 28) is used to latch in the program data. The 3-wire interface protocol is shown in Figure 6. CSB/IWO (pin 23) must be low when writing.

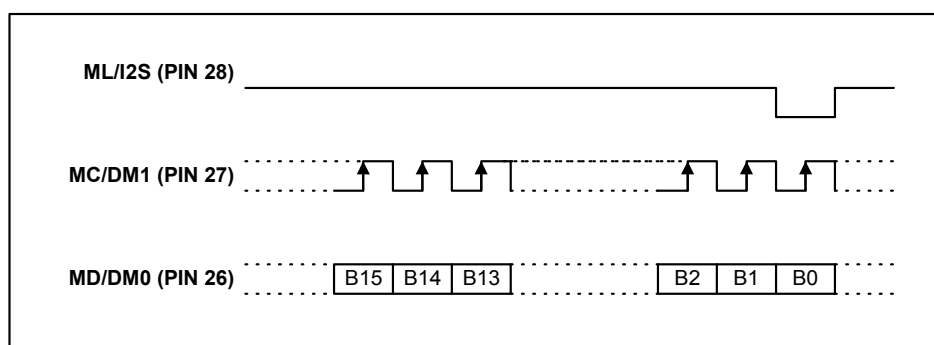


Figure 10 Three-Wire Serial Interface

## REGISTER MAP

WM8740 controls the special functions using 4 program registers, which are 16-bits long. These registers are all loaded through input pin MD/DM0. After the 16 data bits are clocked in, ML/I2S is used to latch in the data to the appropriate register. Table 5 shows the complete mapping of the 4 registers. Note that in hardware differential mode and 8X modes, software control is not available. The hardware differential mode (Diff[1:0]) clock loss detector disable (CDD) can only be accessed by writing to M2[8:5] with the pattern 1111. Register M4 is then accessible by setting A[2:0] to 110.

|           | B15 | B14 | B13 | B12 | B11   | B10   | B9    | B8  | B7  | B6  | B5    | B4    | B3  | B2  | B1  | B0               |
|-----------|-----|-----|-----|-----|-------|-------|-------|-----|-----|-----|-------|-------|-----|-----|-----|------------------|
| <b>M0</b> | -   | -   | -   | -   | A2(0) | A1(0) | A0(0) | LDL | AL7 | AL6 | AL5   | AL4   | AL3 | AL2 | AL1 | AL0              |
| <b>M1</b> | -   | -   | -   | -   | A2(0) | A1(0) | A0(1) | LDR | AR7 | AR6 | AR5   | AR4   | AR3 | AR2 | AR1 | AR0              |
| <b>M2</b> | -   | -   | -   | -   | A2(0) | A1(1) | A0(0) | -   | -   | -   | -     | IW1   | IW0 | OPE | DEM | MUT              |
| <b>M3</b> | -   | -   | -   | -   | A2(0) | A1(1) | A0(1) | IZD | SF1 | SF0 | -     | REV   | SR0 | ATC | LRP | I <sup>2</sup> S |
| <b>M4</b> | -   | -   | -   | -   | A2(1) | A1(1) | A0(0) | -   | -   | CDD | DIFF1 | DIFF0 | -   | -   | -   | -                |

Table 5 Mapping of Program Registers

| REGISTER | BITS  | NAME    | DEFAULT | DESCRIPTION                                      |
|----------|-------|---------|---------|--|
| 0        | [7:0] | AL[7:0] | FF      | Attenuation data for left channel.               |
|          | 8     | LDL     | 0       | Attenuation data load control for left channel.  |
| 1        | [7:0] | AR[7:0] | FF      | Attenuation data for right channel.              |
|          | 8     | LDR     | 0       | Attenuation data load control for right channel. |
| 2        | 0     | MUT     | 0       | Left and right DACs soft mute control.           |
|          | 1     | DEM     | 0       | De-emphasis control.                             |
|          | 2     | OPE     | 0       | Left and right DACs operation control.           |
|          | [4:3] | IW[1:0] | 0       | Input audio data bit select.                     |
| 3        | 0     | I2S     | 0       | Audio data format select.                        |
|          | 1     | LRP     | 0       | Polarity of LRCIN select.                        |
|          | 2     | ATC     | 0       | Attenuator control.                              |
|          | 3     | SR0     | 0       | Digital filter slow roll-off select.             |
|          | 4     | REV     | 0       | Output phase reverse.                            |
|          | [7:6] | SF[1:0] | 0       | Sampling rate select.                            |
|          | 8     | IZD     | 0       | Infinite zero detection circuit control.         |
| 4        | [5:4] | DIFF    | 0       | Differential output mode.                        |
|          | 6     | CDD     | 0       | Clock loss detector disable.                     |

Table 6 Register Bit Descriptions

## DAC OUTPUT ATTENUATION

The level of attenuation for eight bit code X, is given by:

$$0.5 * (X - 255) \text{ dB}, \quad 1 \leq X \leq 255$$

$$-\infty \text{ dB (mute)}, \quad X = 0$$

Bit 8 in register 0 (LDL) is used to control the loading of attenuation data in B[7:0]. When LDL is set to 0, attenuation data will be loaded into AL[7:0], but it will not affect the filter attenuation. LDR in register 1 has the same function for right channel attenuation. Only when LDL or LDR is set to '1' will the filter attenuation be updated. This permits left and right channel attenuation to be updated simultaneously.

Attenuation level is controlled by AL[7:0] (left channel) or AR[7:0] (right channel). Attenuation levels are given in Table 7.



| X[7:0]  | ATTENUATION LEVEL |
|---------|-------------------|
| 00(hex) | -∞dB (mute)       |
| 01(hex) | -127.0dB          |
| :       | :                 |
| :       | :                 |
| FD(hex) | -1.0dB            |
| FE(hex) | -0.5dB            |
| FF(hex) | 0.0dB             |

Table 7 Attenuation Control Level

Bit 2 in Reg3 is used to control the attenuator (ATC). When ATC is "high", the attenuation data loaded in program register 0 is used for both the left and the right channels. When ATC is low, the attenuation data for each register is applied separately to left and right channels.

**SOFT MUTE**

| MUT<br>(REG2, B0) |                                  |
|-------------------|----------------------------------|
| L                 | Soft Mute off (normal operation) |
| H                 | Soft Mute on (no output)         |

Table 8 Soft Mute

Setting MUT causes the attenuation to ramp from the current value down to 00. The values held in the attenuation registers are unchanged. When MUT is reset the attenuation will ramp back up to the previous value. The ramp rate is 128/fs s/0.5dB step.

**DIGITAL DE-EMPHASIS**

| DEM<br>(REG2, B1) |                 |
|-------------------|-----------------|
| L                 | De-emphasis off |
| H                 | De-emphasis on  |

Table 9 Digital De-Emphasis

**DAC OPERATION ENABLE**

| OPE<br>(REG2, B2) |  |
|-------------------|--|
| L                 | Normal operation   |
| H                 | DAC output forced to bipolar zero, irrespective of input data. |

Table 10 DAC Operation Enable

**AUDIO DATA INPUT FORMAT**

| I2S<br>(REG3, B0) | IW1<br>(REG2, B4) | IW0<br>(REG2, B3) | AUDIO INTERFACE                   |
|-------------------|-------------------|-------------------|-----------------------------------|
| 0                 | 0                 | 0                 | 16-bit standard right justified   |
| 0                 | 0                 | 1                 | 20-bit standard right justified   |
| 0                 | 1                 | 0                 | 24-bit standard right justified   |
| 0                 | 1                 | 1                 | 24-bit left justified (MSB first) |
| 1                 | 0                 | 0                 | 16-bit I <sup>2</sup> S           |
| 1                 | 0                 | 1                 | 24-bit I <sup>2</sup> S           |
| 1                 | 1                 | 0                 | 20-bit I <sup>2</sup> S           |
| 1                 | 1                 | 1                 | 20-bit left justified (MSB first) |

Table 11 Audio Data Input Format

**POLARITY OF LR INPUT CLOCK**

The left channel data for a particular sample instant is always input first, then the right channel data.

| LRP<br>(REG3, B1) |  |
|-------------------|--|
| L                 | LR High – left channel<br>LR Low – right channel |
| H                 | LR Low – left channel<br>LR High – right channel |

Table 12 Polarity of LR Input Clock

**INDIVIDUAL OR COMMON ATTENUATION CONTROL**

| ATC<br>(REG3, B2) |                          |
|-------------------|--------------------------|
| L                 | Individual control       |
| H                 | Common control from Reg0 |

Table 13 Individual or Common Attenuation Control

**DIGITAL FILTER ROLL-OFF SELECTION**

| SRO<br>(REG3, B3) |       |
|-------------------|-------|
| L                 | Sharp |
| H                 | Slow  |

Table 14 Digital Filter Roll-Off Selection

**ANALOGUE OUTPUT POLARITY REVERSAL**

| REV<br>(REG3, B4) |          |
|-------------------|----------|
| L                 | Normal   |
| H                 | Inverted |

Table 15 Analogue Output Polarity Reversal

**DE-EMPHASIS SAMPLE RATE**

| SF1<br>(REG3, B7) | SF0<br>(REG3, B6) | SAMPLE RATE    |
|-------------------|-------------------|----------------|
| 0                 | 0                 | No de-emphasis |
| 0                 | 1                 | 48kHz          |
| 1                 | 0                 | 44.1kHz        |
| 1                 | 1                 | 32kHz          |

Table 16 De-Emphasis Sample Rate

**INFINITE ZERO DETECT**

| IZD<br>(REG3, B8) |                      |
|-------------------|----------------------|
| L                 | Zero detect mute off |
| H                 | Zero detect mute on  |

Table 17 Infinite Zero Detect

**SOFTWARE DIFFERENTIAL MONO MODE**

To control the WM8740 in software differential mode register M4 must be written to. A 'key' register write must be made to register M2 to allow access to register M4 which is 'locked' as default. Bits B5 to B8 of register M2 must be set to '1' (0x01e0).

With register M4 'unlocked', bits B4 and B5 may be used to set the required differential output mode; normal stereo, reversed stereo, mono left or mono right, as shown in Table 18.

| DIFF[1:0]<br>B[5:4] | DIFFERENTIAL OUTPUT MODE   |
|---------------------|--|
| 00                  | Stereo   |
| 10                  | Stereo reverse.  |
| 01                  | Mono left – differential outputs.<br>VOUPL (17) is left channel.<br>VOUPLN (16) is left channel inverted.<br>VOUPLR (12) is left channel inverted.<br>VOUPLRN (13) is left channel.      |
| 11                  | Mono right – differential outputs.<br>VOUPL (17) is right channel inverted.<br>VOUPLN (16) is right channel.<br>VOUPLR (12) is right channel.<br>VOUPLRN (13) is right channel inverted. |

**Table 18 Differential Output Modes**

Using these controls a pair of WM8740 devices may be used to build a dual differential stereo implementation with higher performance and differential output.

Note: DIFFHW mode pin may be used to achieve the same result by hardware means.

**CLOCK LOSS DETECTOR DISABLE**

| CDD (REG4, B6) |                         |
|----------------|-------------------------|
| L              | Clock loss detector on  |
| R              | Clock loss detector off |

**Table 19 Clock Loss Detector Disable**

When the system clock is inactive for approximately 100µs, the clock loss detector circuit detects the loss of clock and the analogue circuitry is forced into a mute condition and the digital filters reset. Setting the CDD bit disables this behaviour.

MUTE MODES

The device has various mute modes.

|   | DIGITAL FILTER  | ANALOGUE |   |
|---|---|----------|---|
|   |   | ANRES    | ANMUTE  |
| Reg bit OPE = '1'                         | Unaffected  |          | Asserted  |
| MUTEB pin                                 | Gain ramped to zero<br>On release volume ramps to previous value                                    |          | Asserted when gain = 0                            |
| AUTOMUTE (detect 1024 zero input samples) | Automute has no effect on digital filters   |          | Asserted after 1024 zero input samples if IZD = 1 |
| Reg bit MUT                               | As MUTEB pin  |          | As MUTEB pin                                      |
| Gain = 00 (left and right)                | Gain = -∞dB   |          | Asserted  |
| RAM initialise                            | Gain initialised to 0dB   |          | Asserted  |
| Loss of system clock                      | Not running (no clock). On clock restart, filters initialised, RAM initialised. Registers unchanged | Asserted | Asserted  |
| No LRCLK or invalid SCLK/LRCLK ratio      | Filters initialised, RAM initialised. Registers unchanged   | Asserted | Asserted  |
| RB  | Reset – gain initialised to 0dB   | Asserted | Asserted  |
| Power-on reset                            | Reset   | Asserted | Asserted  |

Table 20 Mute Modes

- ANRES is the reset to the switched capacitor filter.
1. ANMUTE is an analogue muting signal gating the analogue signal at the output (after the SC filter)
  2. AUTOMUTE is asserted when both the IZD register bit is asserted and the input audio data has been zero on both left and right channels for 1024 input samples. The first non-zero sample de-asserts.
  3. Applying a logic low to MUTEB or setting MUT in Reg2 causes the gain registers to ramp to zero. When a logic high is applied, the gain ramps slowly back up to the value held in the appropriate attenuation register (AL or AR). The ramp rate = 128/fs s/0.5dB step.

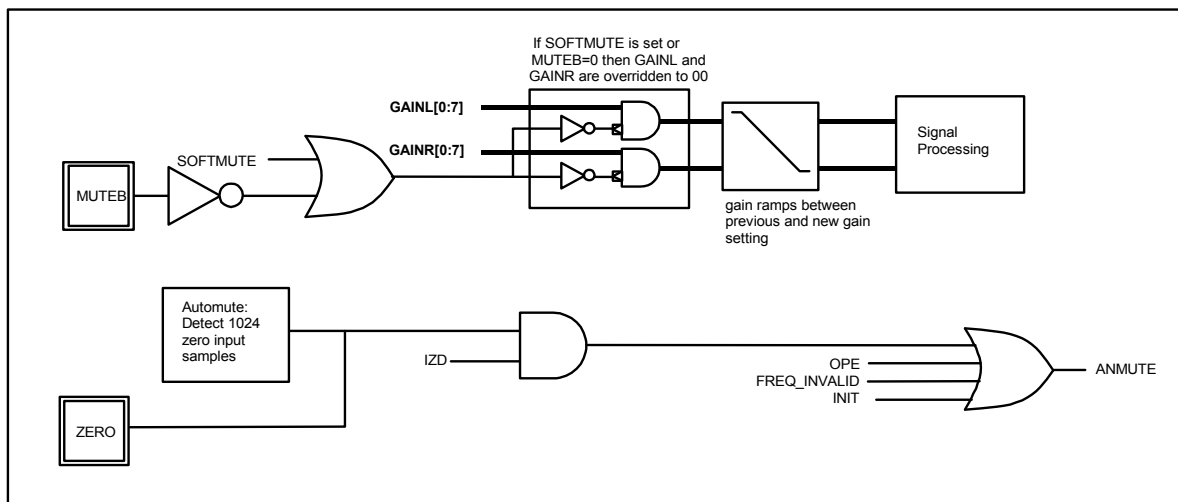
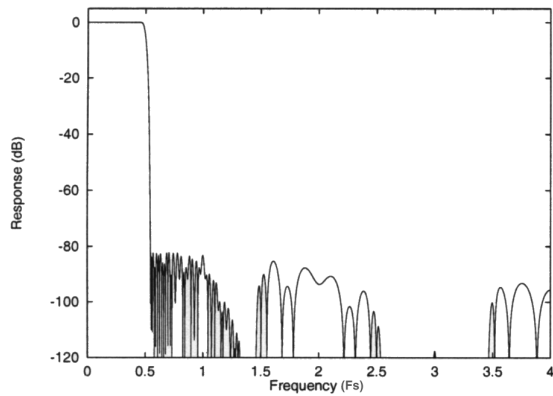
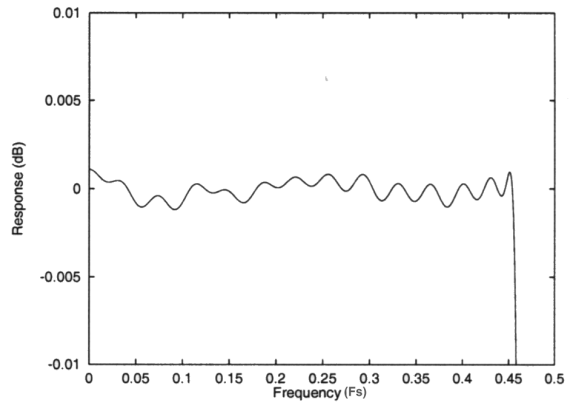


Figure 11 Mute Modes

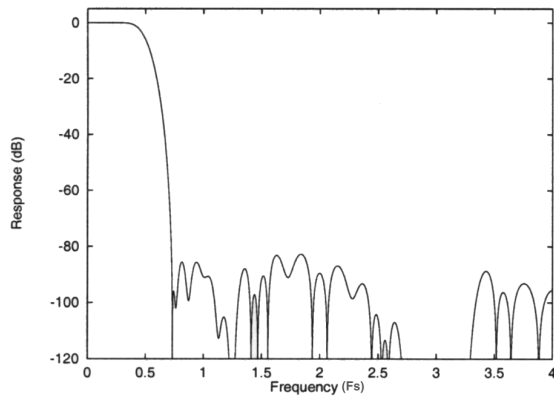
**FILTER RESPONSES**



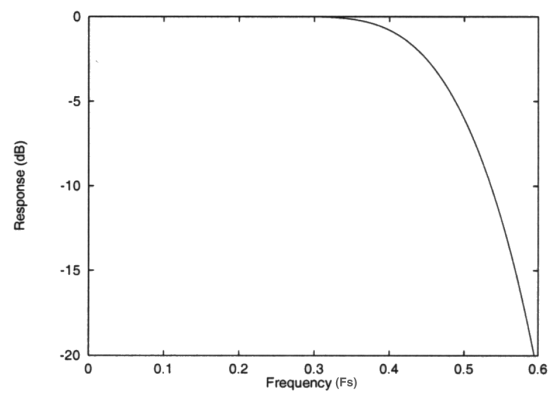
**Figure 12 Digital Filter Response (Sharp Roll-off Mode)**



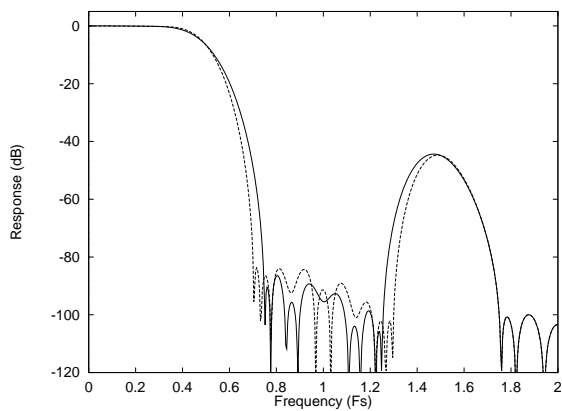
**Figure 13 Digital Filter Response (Sharp Roll-off Mode)**



**Figure 14 Digital Filter Response (Slow Roll-off Mode)**



**Figure 15 Digital Filter Response (Slow Roll-off Mode)**



**Figure 16 Digital Filter Response 128fs Mode (192kHz Sample Rate) Normal Mode – Solid, Slow Mode – Dashed**

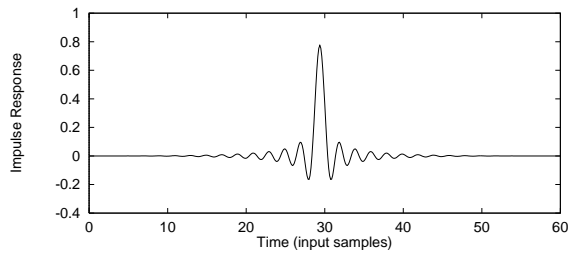


Figure 17 Impulse Response (Normal Roll-off, no De-emphasis)

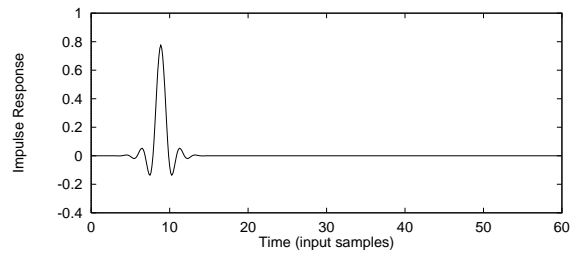


Figure 18 Impulse Response (Slow Roll-off, no De-emphasis)

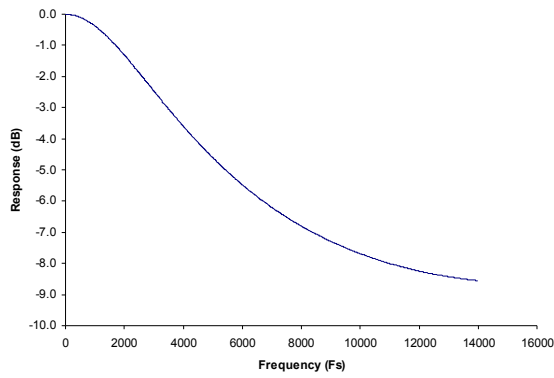


Figure 19 De-emphasis Frequency Response (fs=32kHz)

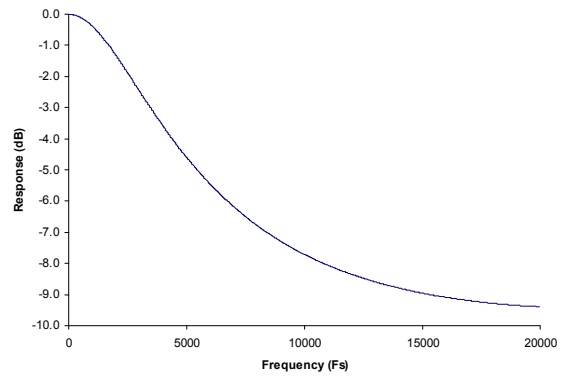


Figure 20 De-emphasis Frequency Response (fs=44.1kHz)

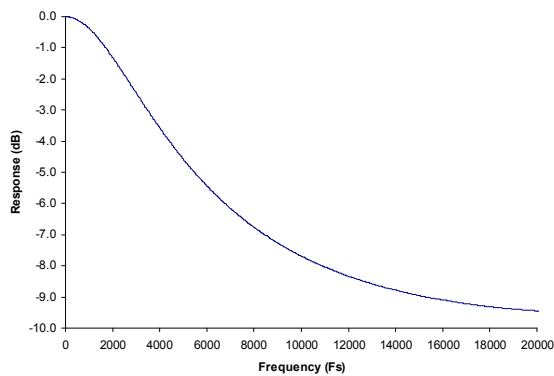


Figure 21 De-emphasis Frequency Response (fs=48kHz)

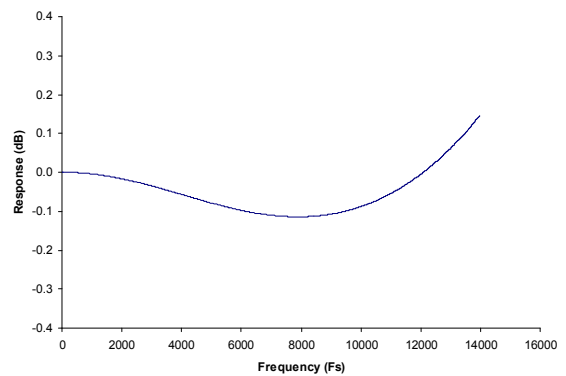


Figure 22 De-emphasis Frequency Response Error (fs=32kHz)

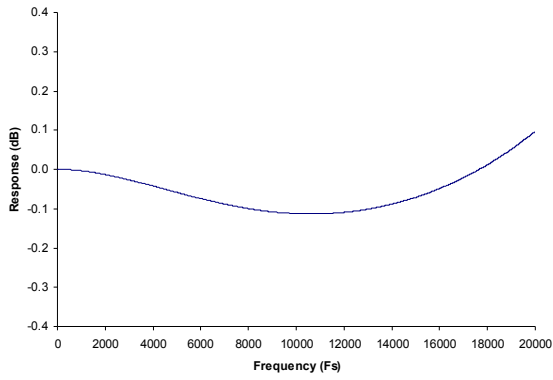


Figure 23 De-emphasis Frequency Response Error (fs=44.1kHz)

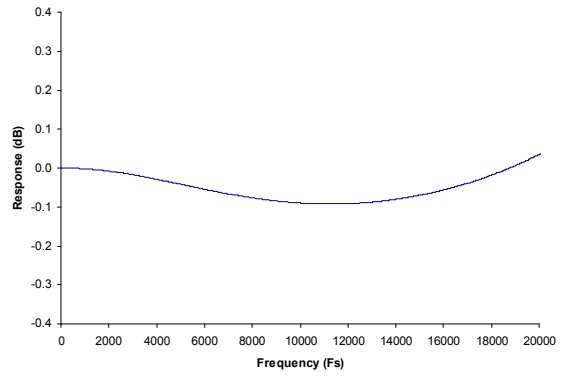


Figure 24 De-emphasis Frequency Response Error (fs=48kHz)

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

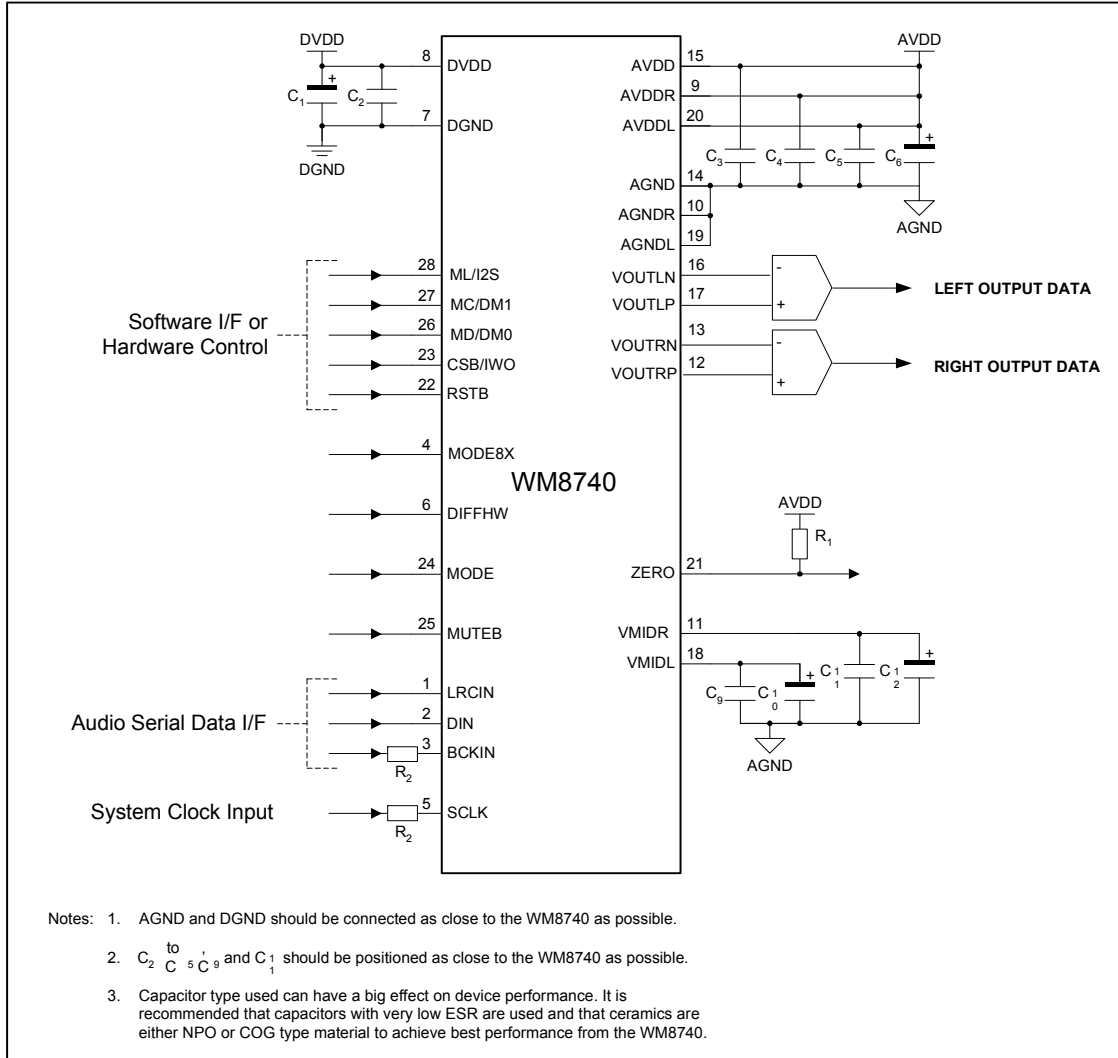


Figure 25 External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

| COMPONENT REFERENCE | SUGGESTED VALUE | DESCRIPTION   |
|---------------------|-----------------|---|
| C1 and C6           | 10 $\mu$ F      | De-coupling for DVDD and AVDD.                                |
| C2 to C5            | 0.1 $\mu$ F     | De-coupling for DVDD and AVDD.                                |
| C7 and C8           | 10 $\mu$ F      | Output AC coupling caps to remove VMID DC level from outputs. |
| C9 and C11          | 0.1 $\mu$ F     | Reference de-coupling capacitors for VMIDR and VMIDL.         |
| C10 and C12         | 10 $\mu$ F      |   |
| R1                  | 10k $\Omega$    | Resistor to AVDD for open drain output operation.             |
| R2                  | 51 $\Omega$     | Source termination resistors.                                 |

Table 21 External Components Description



SUGGESTED DIFFERENTIAL OUTPUT FILTER CIRCUIT

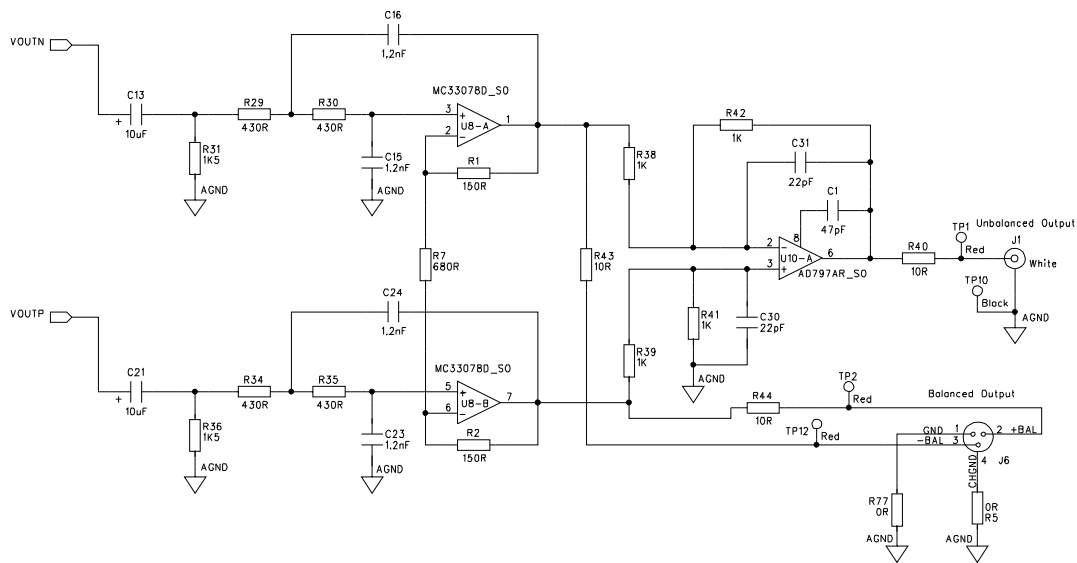


Figure 26 Suggested Differential Output Filter Circuit

RECOMMENDED DUAL DIFFERENTIAL HARDWARE SETUP

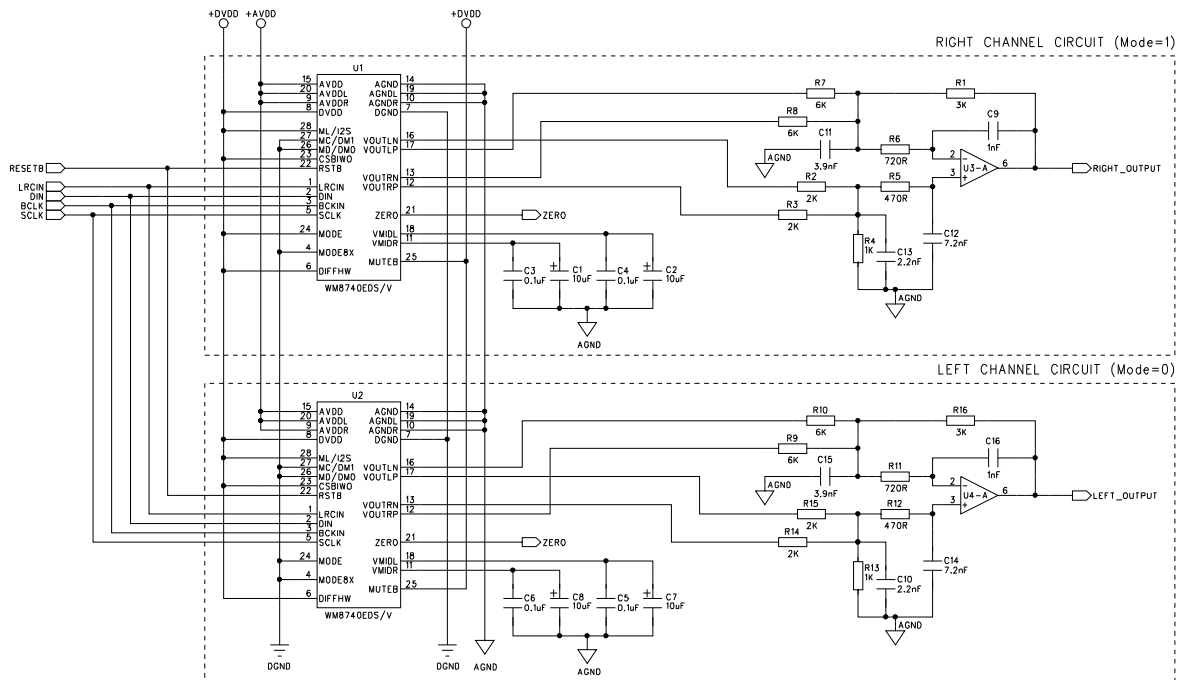
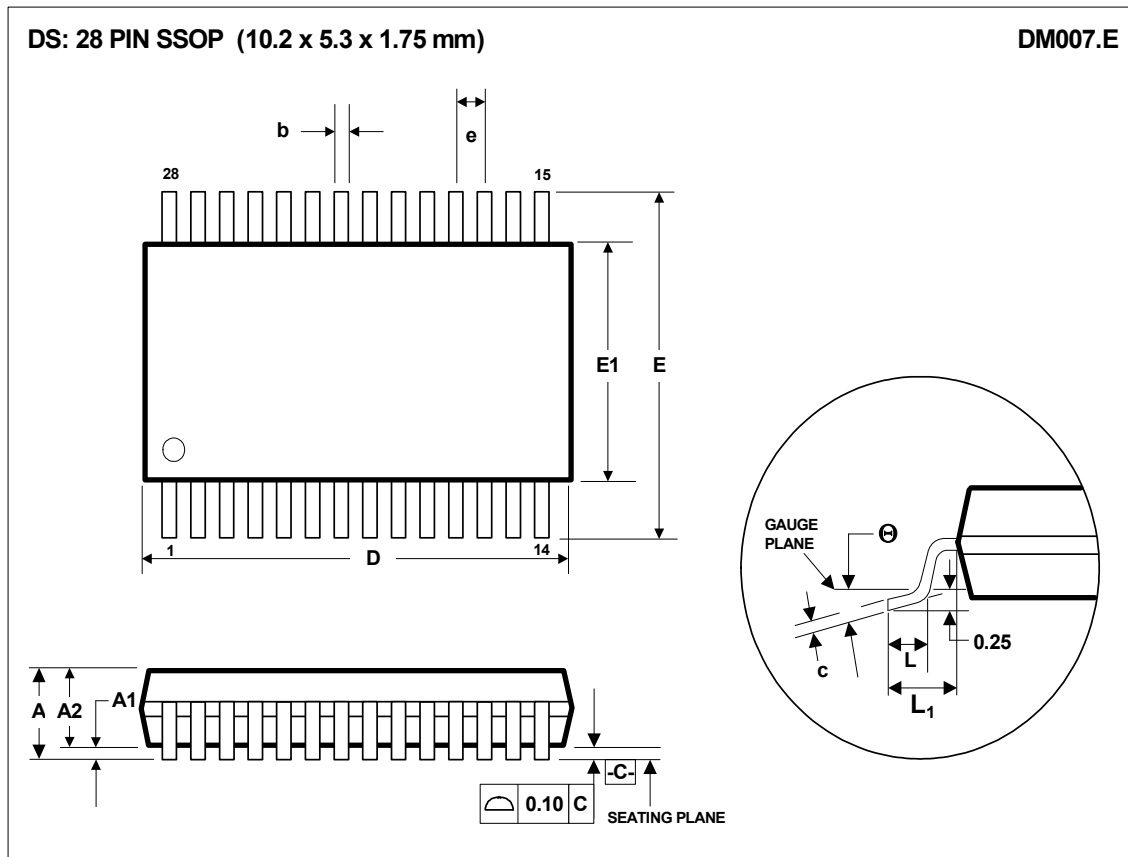


Figure 27 Recommended Dual Differential Hardware Setup

PACKAGE DIMENSIONS



| Symbols              | Dimensions (mm)  |       |       |
|----------------------|------------------|-------|-------|
|                      | MIN              | NOM   | MAX   |
| <b>A</b>             | -----            | ----- | 2.0   |
| <b>A<sub>1</sub></b> | 0.05             | ----- | 0.25  |
| <b>A<sub>2</sub></b> | 1.65             | 1.75  | 1.85  |
| <b>b</b>             | 0.22             | 0.30  | 0.38  |
| <b>c</b>             | 0.09             | ----- | 0.25  |
| <b>D</b>             | 9.90             | 10.20 | 10.50 |
| <b>e</b>             | 0.65 BSC         |       |       |
| <b>E</b>             | 7.40             | 7.80  | 8.20  |
| <b>E<sub>1</sub></b> | 5.00             | 5.30  | 5.60  |
| <b>L</b>             | 0.55             | 0.75  | 0.95  |
| <b>L<sub>1</sub></b> | 1.25 REF         |       |       |
| <b>θ</b>             | 0°               | 4°    | 8°    |
| <b>REF:</b>          | JEDEC.95, MO-150 |       |       |

- NOTES:  
 A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.  
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