

# Two Outputs PCI-Express Clock Generator

## Features

- 25 MHz crystal or clock input
- Two sets of differential PCI-Express clocks
- Pin selectable output frequencies
- Supports HCSL compatible output levels
- Spread Spectrum capability on all output clocks with pin selectable spread range
- 16-pin TSSOP package
- Operating voltage 3.3 V
- Commercial, Industrial operating temperature range

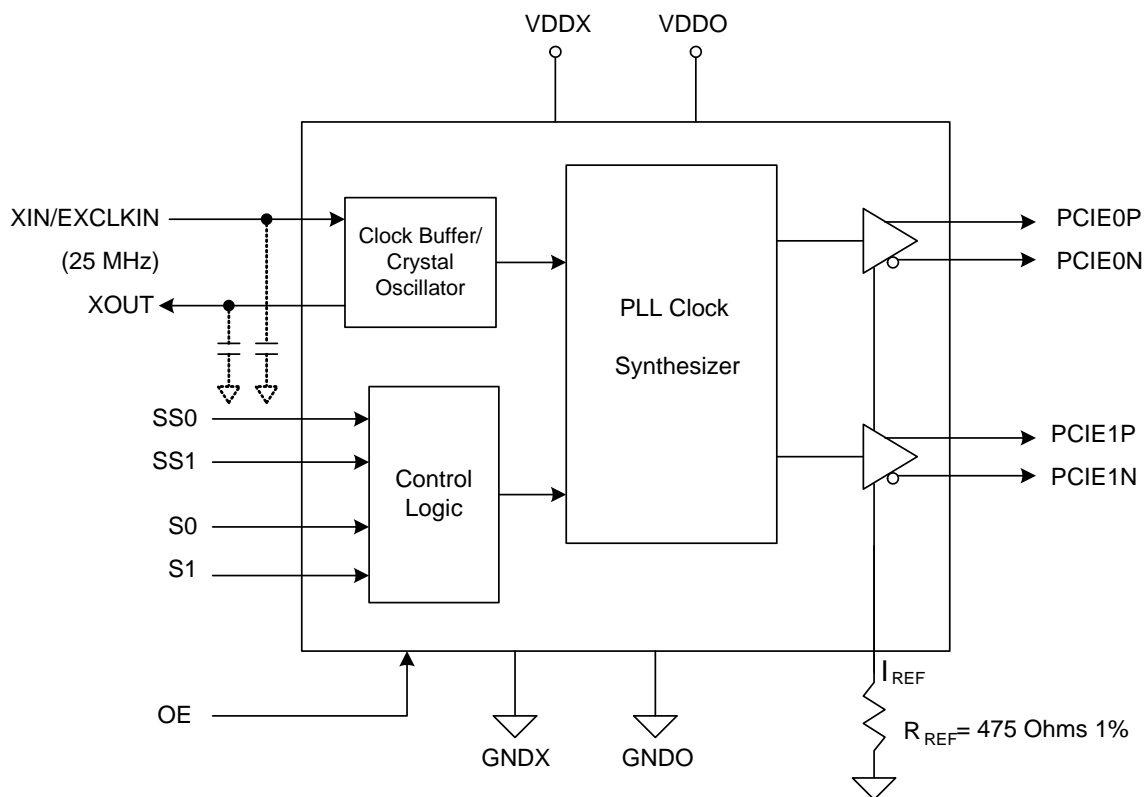
## Functional Description

CY24293 is a two output PCI-Express clock generator device intended for networking applications. The device takes 25 MHz crystal or clock input and provides two pairs of differential outputs at 25 MHz, 100 MHz, 125 MHz, or 200 MHz for HCSL signaling standard.

The device incorporates Lexmark Spread Spectrum profile for maximum electromagnetic interference (EMI) reduction. The spread type and amount can be selected using select pins.

For a complete list of related documentation, click [here](#).

## Logic Block Diagram

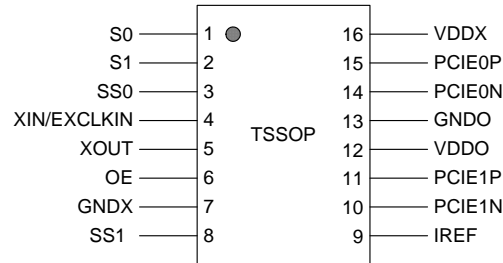


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## Pinouts

Figure 1. 16-pin TSSOP pinout



## Pin Definitions

### 16-pin TSSOP

Pin Number	Pin Name	Pin Type	Description
1	S0	Input	Frequency select pin. Has internal weak pull-up. Refer to <a href="#">Table 1</a> .
2	S1	Input	Frequency select pin. Has internal weak pull-up. Refer to <a href="#">Table 1</a> .
3	SS0 <sup>[1]</sup>	Input	Spread spectrum select pin 0. Has internal weak pull-up. Refer to <a href="#">Table 2</a> .
4	XIN/EXCLKIN	Input	Crystal or clock input. 25 MHz fundamental mode crystal or clock input.
5	XOUT	Output	Crystal output. 25 MHz fundamental mode crystal input. Float for clock input.
6	OE	Input	High true output enable pin. When set low, PCI-E outputs are tri-stated. Has internal weak pull-up.
7	GNDX	Power	Ground
8	SS1 <sup>[1]</sup>	Input	Spread spectrum select pin 1. has internal weak pull-up. Refer to <a href="#">Table 2</a> .
9	IREF	Output	Current set for all differential clock drivers. Connect 475 Ω resistor to ground.
10	PCIE1N	Output	Differential PCI-Express complementary clock output. Tristated when disabled.
11	PCIE1P	Output	Differential PCI-Express true clock output. Tristated when disabled.
12	VDDO <sup>[2]</sup>	Input	3.3 V Power supply for output driver and analog circuits.
13	GNDO	Power	Ground
14	PCIE0N	Output	Differential PCI-Express complementary clock output. Tristated when disabled.
15	PCIE0P	Output	Differential PCI-Express true clock output. Tristated when disabled.
16	VDDX <sup>[2]</sup>	Input	3.3 V Power supply for oscillator and digital circuits.

### Notes

- Once powered up, state of SS1/SS0 pins should be held constant at the desired state.
- VDDX must be supplied faster or equal to VDDO.

**Table 1. Output Frequency Selection Table**

S1	S0	PCIE0[N,P], PCIE1[N,P]
0	0	25 MHz
0	1	100 MHz
1	0	125 MHz
1	1	200 MHz

**Table 2. Spread Selection Table <sup>[3]</sup>**

SS1	SS0	Spread%
0	0	No Spread
0	1	-0.5%
1	0	-0.75%
1	1	No Spread

**Note**

3. Once powered up, state of SS1/SS0 pins should be held constant at the desired state.

## Application Information

### Crystal Recommendations

CY24293 requires a parallel resonance crystal. Substituting a series resonance crystal causes the CY24293 to operate at the wrong frequency and violate the ppm specification. For most applications, there is a 300 ppm frequency shift between series and parallel crystals due to incorrect loading.

Table 3. Crystal Recommendations

Frequency	Cut	Load Cap	Eff Series Rest (max)	Drive (max)	Tolerance (max)	Stability (max)	Aging (max)
25.00 MHz	Parallel	16 pF	30 Ω	1.0 mW	30 ppm	10 ppm	5 ppm/yr.

### Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, consider the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

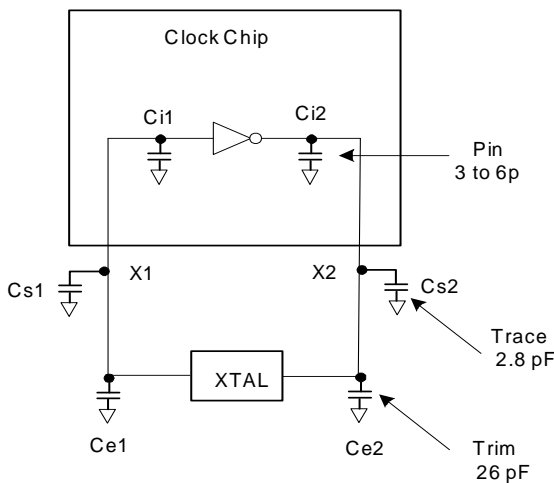
Figure 2 shows a typical crystal configuration using two trim capacitors. It is important to note that the trim capacitors in series with the crystal are not parallel. It is a common misconception that load capacitors are in parallel with the crystal and must be approximately equal to the load capacitance of the crystal. This is not true.

### Calculating Load Capacitors

In addition to the standard external trim capacitors, trace capacitance and pin capacitance must also be considered to correctly calculate crystal loading.

As mentioned in the previous section, the capacitance on each side of the crystal is in series with the crystal. This means the total capacitance on each side of the crystal must be twice the specified crystal load capacitance (CL). While the capacitance on each side of the crystal is in series with the crystal, trim capacitors (Ce1, Ce2) must be calculated to provide equal capacitive loading on both sides.

Figure 2. Crystal Loading Example



Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2:

#### Load capacitance (each side)

$$C_e = 2 * CL - (C_s + C_i)$$

#### Total capacitance (as seen by the crystal)

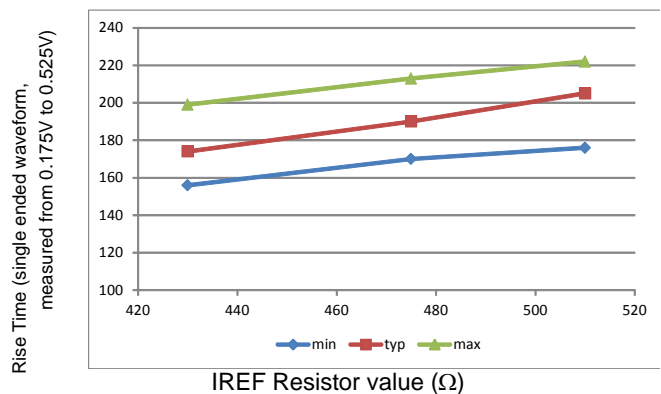
$$CL_e = \frac{1}{\left(\frac{1}{C_{e1} + C_{s1} + C_{i1}} + \frac{1}{C_{e2} + C_{s2} + C_{i2}}\right)}$$

- CL ..... Crystal load capacitance
- CLe ..... Actual loading seen by crystal using standard value trim capacitors
- Ce ..... External trim capacitors
- Cs ..... Stray capacitance (terraced)
- Ci ..... Internal capacitance

### Current Source (IREF) Reference Resistor

If the board target trace impedance (Z) is 50 Ω, then for RREF = 475 Ω (1%), provides IREF of 2.32 mA. The output current (IOH) is equal to 6\*IREF. For other values of RREF, the following graph can be referred. It demonstrates the relationship of variation of IREF w.r.t. rise time /fall time (TR/TF).

Figure 3. IREF vs. TR/TF relationship (Typical)



**Output Termination**

The PCI-Express differential clock outputs of the CY24293 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are explained in Figure 4.

**PCB Layout Recommendations**

For optimum device performance and the lowest phase noise, the following guidelines must be observed:

1. Each 0.01  $\mu$ F decoupling capacitor must be mounted on the component side of the board as close to the  $V_{DD}$  pin as possible.
2. No vias must be used between the decoupling capacitor and the  $V_{DD}$  pin.

3. The PCB trace to the  $V_{DD}$  pin and the ground via must be kept as short as possible. Distance of the ferrite bead and bulk decoupling from the device is less critical.
4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces must be routed away from the CY24293. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

**Decoupling Capacitors**

The decoupling capacitors of 0.01  $\mu$ F must be connected between  $V_{DD}$  and GND as close to the device as possible. Do not share ground vias between components. Route power from the power source through the capacitor pad and then into the CY24293 pin.

**PCI-Express (HCSL compatible) Layout Guidelines**

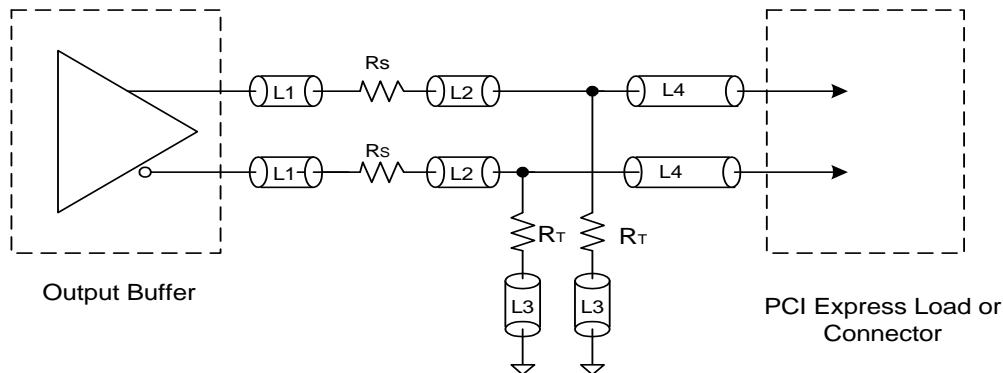
**Table 4. Common Recommendations for Differential Routing**

Differential Routing	Dimension or Value	Unit
L1 length, route as non-coupled 50 $\Omega$ trace	0.5 max	inch
L2 length, route as non-coupled 50 $\Omega$ trace	0.2 max	inch
L3 length, route as non-coupled 50 $\Omega$ trace	0.2 max	inch
$R_S$	33	$\Omega$
$R_T$	49.9	$\Omega$

**Table 5. Differential Routing for PCI-Express Load or Connector**

Differential Routing	Dimension or Value	Unit
L4 length, route as coupled microstrip 100 $\Omega$ differential trace	2 to 32	inch
L4 length, route as coupled stripline 100 $\Omega$ differential trace	1.8 to 30	inch

**Figure 4. PCI-Express Differential Routing**



## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Condition	Min	Max	Unit
V <sub>DD</sub>	Supply voltage		-0.5	4.6	V
V <sub>IN</sub>	Input voltage	Relative to V <sub>SS</sub>	-0.5	V <sub>DD</sub> + 0.5	V
T <sub>S</sub>	Temperature, Storage	Non Functional	-65	+150	°C
T <sub>J</sub>	Temperature, Junction	Non Functional	-65	+150	°C
ESD <sub>HBM</sub>	ESD Protection (Human Body Model)	JEDEC EIA/JESD22-A114-E	2000	-	V
UL-94	Flammability rating	-	V-0 at 1/8 in.		
MSL	Moisture sensitivity level	-	3		

## Recommended Operation Conditions

Parameter	Description	Min	Typ	Max	Unit
V <sub>DD</sub>	Supply voltage	3.0	-	3.6	V
T <sub>AC</sub>	Commercial ambient temperature	0	-	+70	°C
T <sub>AI/AA</sub>	Industrial ambient temperature	-40	-	+85	°C
t <sub>PU</sub>	Power up time for all V <sub>DD</sub> to reach minimum specified voltage (power ramps must be monotonic)	0.05	-	500	ms

## DC Electrical Characteristics

Unless otherwise stated, V<sub>DD</sub> = 3.3 V ± 0.3 V, ambient temperature = -40 °C to +85 °C Industrial, 0 °C to +70 °C Commercial

Parameter <sup>[4]</sup>	Description	Condition	Min	Typ	Max	Unit
V <sub>IL</sub>	Input low voltage	-	-0.3	-	0.8	V
V <sub>IH</sub>	Input high voltage	-	2.0	-	V <sub>DD</sub> + 0.3	V
V <sub>OL</sub>	Output low voltage of PCIE0[P/N], PCIE1[P/N]	HCSL termination (R <sub>S</sub> = 33 Ω, R <sub>T</sub> = 49.9 Ω). See note 18.	-0.2	0	0.05	V
V <sub>OH</sub>	Output high voltage of PCIE0[P/N], PCIE1[P/N]	HCSL termination (R <sub>S</sub> = 33 Ω, R <sub>T</sub> = 49.9 Ω). See note 18.	0.65	0.71	0.95	V
I <sub>DD</sub>	Operating supply current	No load, OE = 1	-	45	60	mA
I <sub>DDOD</sub>	Output disabled current	OE = 0	-	-	50	mA
C <sub>IN</sub>	Input capacitance	All input pins	-	5	-	pF
R <sub>PU</sub>	Pull-up resistance	S0, S1, SS0, SS1, OE	-	70k	-	Ω

### Note

4. Parameters are guaranteed by design and characterization. Not 100% tested in production.

## AC Electrical Characteristics

Unless otherwise stated:  $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$ , ambient temperature =  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$  Industrial,  $0\text{ }^{\circ}\text{C}$  to  $+70\text{ }^{\circ}\text{C}$  Commercial, Outputs HCSL terminated.

Parameter <sup>[5]</sup>	Description	Condition	Min	Typ	Max	Unit
$F_{IN}$	Input clock frequency (crystal or external clock)	–	–	25	–	MHz
$F_{OUT}$	Output frequency	HCSL termination	–	–	200	MHz
$F_{ERR}$	Frequency synthesis error	–	–	0	–	ppm
$T_{CCJ}$	Cycle-to-cycle jitter	See notes 6, 7	–	–	75	ps
$SP_{PROFILE}$	Spread modulation profile		–	–	Lexmark	type
$SP_{MOD}$	Spread modulation frequency		30	32	33	kHz
$T_{DC}$	Output clock duty cycle	See notes: 6, 8	45	50	55	%
$T_{OEHL}$	Output enable time	OE going high to differential outputs becoming valid	–	–	200	ns
$T_{OEL}$	Output disable time	OE going low to differential outputs becoming invalid	–	–	200	ns
$T_{LOCK}$	Clock stabilization from power up	Measured from 90% of the applied power supply level	–	1	2	ms
$T_R$	Output rise time	Measured from 0.175 V to 0.525 V. See notes: 6, 9	130	–	700	ps
$T_F$	Output fall time	Measured from 0.525 V to 0.175 V. See notes: 6, 9	130	–	700	ps
$DT_R$	Rise time variation	For a given frequency, Max ( $T_R$ ) – Min ( $T_R$ )	–	–	125	ps
$DT_F$	Fall time variation	For a given frequency, Max ( $T_F$ ) – Min ( $T_F$ )	–	–	125	ps
$T_{OSKEW}$	Output skew	Measured at $V_{CROSS}$ point. See note: 10	–	–	50	ps
$V_{CROSS}$	Absolute crossing point voltage	See notes: 8, 9, 11	0.25	0.35	0.55	V
$V_{Xdelta}$	Variation of $V_{CROSS}$ over all rising clock edges	See notes: 8, 9, 12	–	–	140	mV

### Notes

5. Parameters are guaranteed by design and characterization. Not 100% tested in production.
6. Measured with  $C_{load} = 4\text{ pF}$  max. (scope probe + trace load).
7. Measurement taken from differential waveform (PCIEP minus PCIEN). Either single ended probes with math or a differential probe can be used.
8. Measured at crossing point where the instantaneous voltage value of the rising edge of PCIEP equals the falling edge of PCIEN.
9. Measurement taken from single ended waveform.
10. Measured at the rising 0V point of the differential signal. Skew is the time difference of the rising 0V point between any two differential signal pairs. The measurement is taken over 1000 samples, and the average value is used.
11. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
12. Defined as the total variation of all crossing voltages of Rising PCIEP and Falling PCIEN. This is the maximum allowed variance in  $V_{CROSS}$  for any particular system.



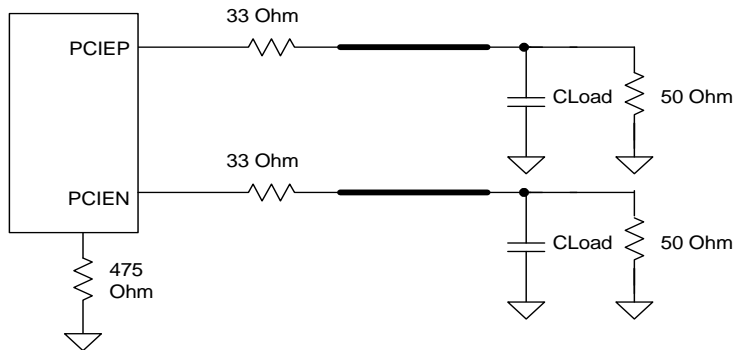
## AC Electrical Characteristics

Differential 100 MHz, HCSL Terminated Outputs (Parameters for the PCI Express Specification. Use above AC Characteristics parameter where it is not listed in this section)

Parameter	Description	Test Conditions	Min	Typ	Max	Units
F <sub>OUT</sub>	Output frequency		–	–	100	MHz
T <sub>PHJ</sub>	Peak-to-peak phase jitter	10 <sup>-6</sup> BER. Note: 13	–	30	86	ps
ER <sub>R</sub>	Rising edge rate	See notes: 14, 15	0.6	1.3	4.0	V/ns
ER <sub>F</sub>	Falling edge rate	See notes: 14, 15	0.6	1.3	4.0	V/ns
T <sub>PERIOD AVG</sub>	Average clock period accuracy	See notes: 14, 16	-300	–	2800	ppm
T <sub>PERIOD ABS</sub>	Absolute clock period	See notes: 14, 17	9.847	–	10.203	ns
RF <sub>MATCHING</sub>	Rising edge rate to falling edge rate matching	See note: 18, 19			20	%

## Test and Measurement Setup

Figure 5. Test Load Configuration for Differential Output Signals



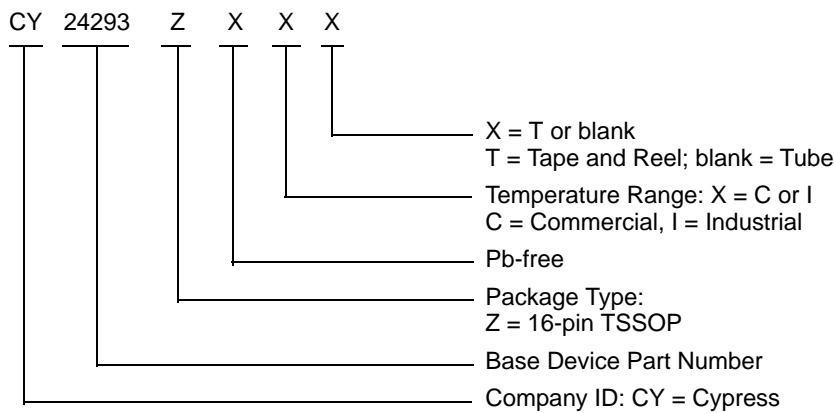
### Notes

13. Phase jitter is determined using data captured on an oscilloscope at a sample rate of 20 GS/sec, for a minimum 100,000 continuous clock periods. This data is then processed using the ClockJitter 1.3.0 software from PCISIG, using the PCI\_E\_1\_1 template.
14. Measurement taken from differential waveform (PCIEP minus PCIEEN). Either single ended probes with math or a differential probe can be used.
15. Measured from -150 mV to +150 mV on the differential waveform (derived from PCIEP minus PCIEEN). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
16. PPM refers to parts per million and is a DC absolute period accuracy specification. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum, there is an additional 2500 PPM nominal shift in maximum period resulting from the 0.5% down spread, resulting in a maximum average period specification of +2800 PPM.
17. Defined as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread spectrum modulation.
18. Measurement taken from single ended waveform.
19. Matching applies to rising edge rate for PCIEP and falling edge for PCIEEN. It is measured using a ± 75mV window centered on the median cross point where PCIEP rising meets PCIEEN falling.

**Ordering Information**

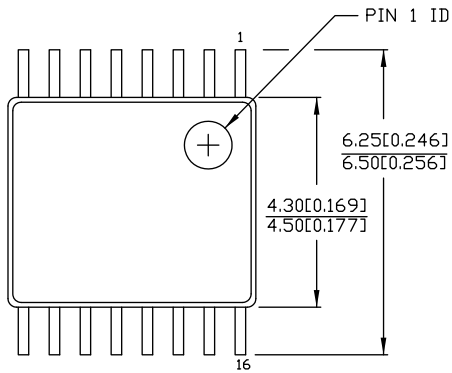
Part Number	Type	Production Flow
<b>Pb-free</b>		
CY24293ZXC	16-pin TSSOP	Commercial, 0 °C to 70 °C
CY24293ZXCT	16-pin TSSOP – Tape and Reel	Commercial, 0 °C to 70 °C
CY24293ZXI	16-pin TSSOP	Industrial, –40 °C to 85 °C
CY24293ZXIT	16-pin TSSOP – Tape and Reel	Industrial, –40 °C to 85 °C

**Ordering Code Definitions**



Package Diagram

Figure 6. 16-pin TSSOP 4.40 mm Body Z16.173/ZZ16.173 Package Outline, 51-85091

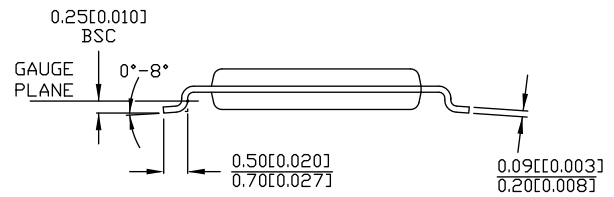
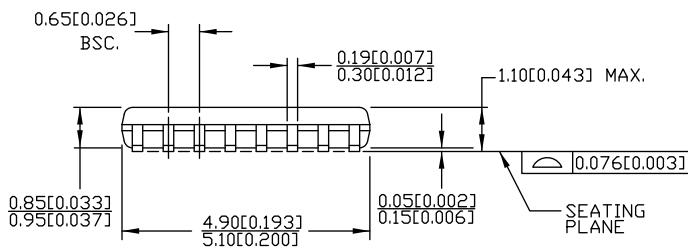


DIMENSIONS IN MM [INCHES] MIN. MAX.

REFERENCE JEDEC MO-153

PACKAGE WEIGHT 0.05gms

PART #	
Z16.173	STANDARD PKG.
ZZ16.173	LEAD FREE PKG.



51-85091 \*E

### Acronyms

Acronym	Description
EIA	electronic industries alliance
EMI	electromagnetic interference
ESD	electrostatic discharge
HCSL	high speed current steering logic
JEDEC	joint electron devices engineering council
PCB	printed circuit board
PCI	peripheral component interconnect
PLL	phase-locked loop
TSSOP	thin shrunk small outline package

### Document Conventions

#### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
MHz	megahertz
μF	microfarad
mA	milliampere
ms	millisecond
mV	millivolt
mW	milliwatt
ns	nanosecond
Ω	ohm
ppm	parts per million
%	percent
pF	picofarad
ps	picosecond
V	volt

Document History Page

Document Title: CY24293, Two Outputs PCI-Express Clock Generator				
Document Number: 001-46117				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	2490167	PYG / DPF / AESA	See ECN	New data sheet
*A	2507681	DPF / AESA	05/23/2008	Added Note 1: Parameters are guaranteed by design and characterization. Not 100% tested in production. Added Note 2 for Duty cycle spec in the AC Elect. Characteristics. Added HCSL termination in Condition for $V_{OL}$ , $V_{OH}$ DC Elect. Char. Added $V_{X\delta}$ value of 140 mV in the Differential 100 MHz HCSL output. Changed Cload from 2 pF to 4 pF in Note 2. Added internal weak Pull-ups for S0, S1, SS0, SS1 and OE pins. Updated $T_{OEH}$ and $T_{OEL}$ to 200 ns (max.). Updated data sheet template
*B	2621901	CXQ / AESA	12/19/2008	Updated $I_{DD}$ spec in DC Electrical Characteristics. Added max spec for $I_{DDOD}$ DC Electrical Characteristics. Added $R_{PU}$ in DC Electrical Characteristics. Replaced $T_{RFVAR}$ with $DT_R$ and $DT_F$ in AC Electrical Characteristics. Added definitions for rise and fall time variation, crossing point variation in AC Electrical Characteristics. Reduced cycle-to-cycle jitter spec to 75ps in AC Electrical Characteristics.
*C	2683343	CXQ / PYRA	04/03/2009	Removed "Preliminary" from data sheet title and headings Added "max" to crystal ESR spec. Changed "LVDS Down Device" to "LVDS Device" in Table 8 and Figure 4.
*D	3289802	BASH	06/27/2011	Added <a href="#">Ordering Code Definitions</a> . Updated <a href="#">Package Diagram</a> . Added <a href="#">Acronyms and Units of Measure</a> . Updated to new template.
*E	3395894	PURU	10/05/2011	Updated <a href="#">Features</a> (Removed LVDS related information). Updated <a href="#">Functional Description</a> (Removed LVDS related information). Updated <a href="#">Output Termination</a> under <a href="#">Application Information</a> (Removed LVDS related information). Removed the section LVDS Compatible Layout Guidelines under the main section <a href="#">PCI-Express (HCSL compatible) Layout Guidelines</a> . Updated <a href="#">AC Electrical Characteristics</a> (Removed LVDS related information). Updated <a href="#">Package Diagram</a> . Updated to new template.
*F	4467398	XHT	08/08/2014	Updated <a href="#">DC Electrical Characteristics</a> : Changed maximum value of $V_{OH}$ parameter from 0.85 V to 0.95 V.
*G	4581659	TAVA	11/28/2014	Updated <a href="#">Functional Description</a> : Added "For a complete list of related documentation, click <a href="#">here</a> ." at the end. Updated <a href="#">Package Diagram</a> .

**Document History Page** (continued)

Document Title: CY24293, Two Outputs PCI-Express Clock Generator Document Number: 001-46117				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*H	4817220	XHT	07/25/2015	<p>Updated <a href="#">Pin Definitions</a>:            Added Note 1 and referred the same note in SS0 and SS1 pins.            Added Note 2 and referred the same note in VDD0 and VDDX pins.</p> <p>Updated <a href="#">Table 2</a>:            Added Note 3 and referred the same note in <a href="#">Table 2</a>.</p> <p>Updated <a href="#">Application Information</a>:            Updated <a href="#">Current Source (Iref) Reference Resistor</a>:            Updated description.            Added <a href="#">Figure 3</a>.</p> <p>Updated <a href="#">AC Electrical Characteristics</a>:            Added SP<sub>PROFILE</sub> parameter and its details.            Added minimum value of SP<sub>MOD</sub> parameter (30 kHz).            Added maximum value of SP<sub>MOD</sub> parameter (33 kHz).            Updated Note 9 (Replaced differential with single ended).            Added <a href="#">AC Electrical Characteristics</a> (to specify PCIe parameter specifications).            Updated to new template.            Completing Sunset Review.</p>

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PSoC	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
Touch Sensing	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
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С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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