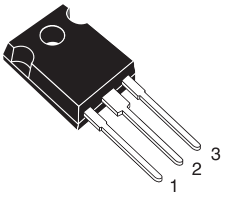
STW26NM50

N-channel 500 V, 0.10 Ω, 30 A TO-247 MDmesh™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STW26NM50	500 V	< 0.12 Ω	30 A

- High dv/dt and avalanche capabilities
- Improved ESD capability
- Low input capacitance and gate charge



TO-247

Application

- Switching applications

Description

MDmesh™ technology applies the benefits of the multiple drain process to STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product offers low on-resistance, high dv/dt capability and excellent avalanche characteristics.

Figure 1. Internal schematic diagram

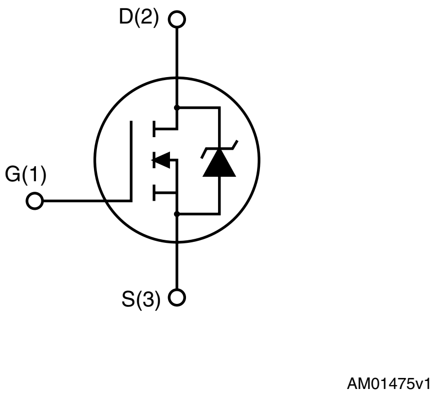


Table 1. Device summary

Order codes	Marking	Package	Packaging
STW26NM50	W26NM50	TO-247	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	500	V
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25 °C	30	A
I_D	Drain current (continuous) at T_C = 100 °C	18.9	A
I_{DM} (1)	Drain current (pulsed)	120	A
P_{TOT}	Total dissipation at T_C = 25 °C	313	W
	Derating factor	2.5	W/°C
$V_{ESD(G-S)}$	Gate source ESD (HBM-C=100 pF, R=1.5 kΩ)	6000	V
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 26$ A, di/dt ≤ 200 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.4	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_{j\ max}$)	13	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AR}, V_{DD}=50 V)	740	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			10 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 13 A		0.10	0.12	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}(1)	Forward transconductance	V_{DS}=15 V, I_D=13 A	-	20	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer Capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	3000 700 50	-	pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 400 V	-	300	-	pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400 V, I_D = 26 A, V_{GS} = 10 V, *(see Figure 15)*	-	76 20 36	-	nC nC nC

1. Pulsed: pulse duration=300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 250 V, I_D = 13 A, R_G = 4.7 Ω, V_{GS}=10 V, *(see Figure 15)*	-	28 15 13 19	-	ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		26 104	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 26 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 26 A, di/dt = 100 A/µs V_{DD} = 100 V *(see Figure 16)*	-	400 5.5 27.8		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 26 A, di/dt = 100 A/µs V_{DD} = 100 V, T_j = 150 °C *(see Figure 16)*	-	492 7 28.8		ns µC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1 mA (open drain)	30	-	-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device’s ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device’s integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

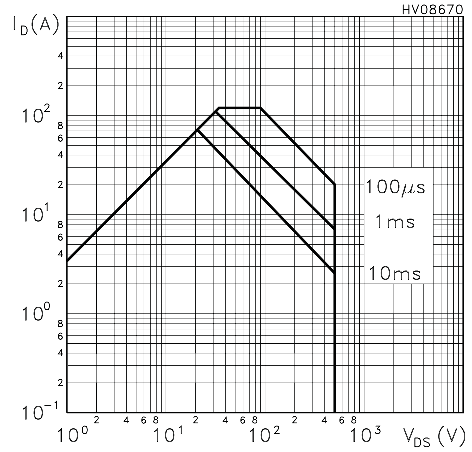


Figure 3. Thermal impedance

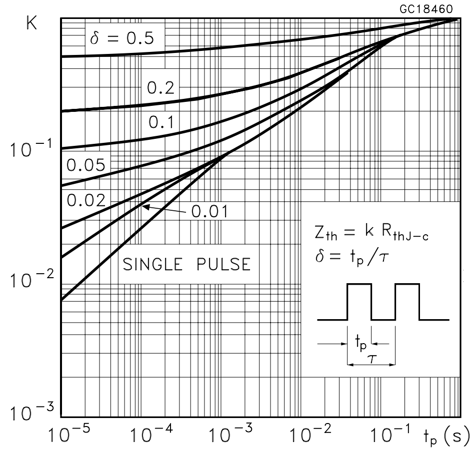


Figure 4. Output characteristics

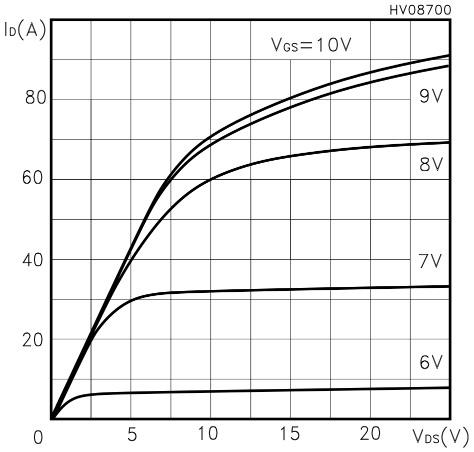


Figure 5. Transfer characteristics

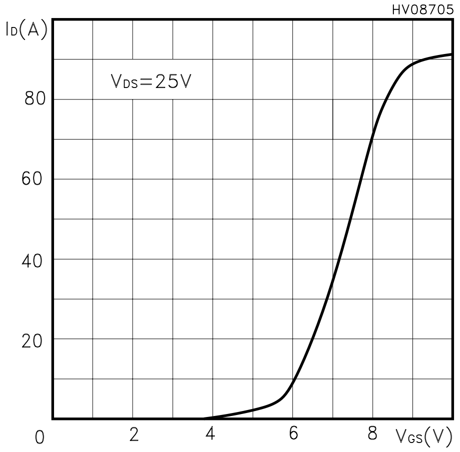


Figure 6. Transconductance

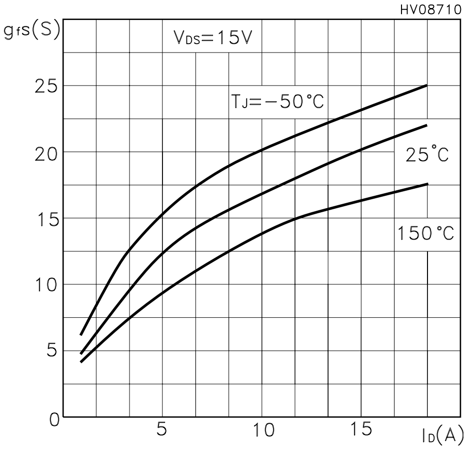


Figure 7. Static drain-source on resistance

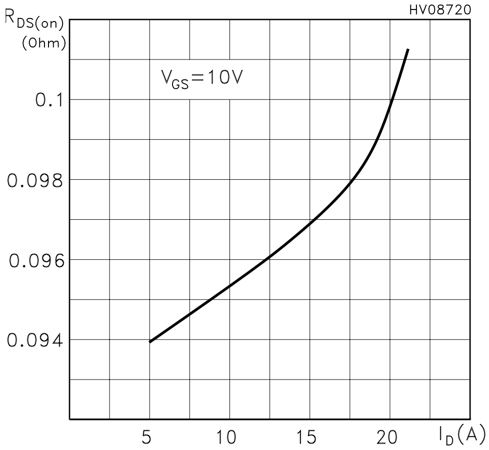


Figure 8. Gate charge vs gate-source voltage

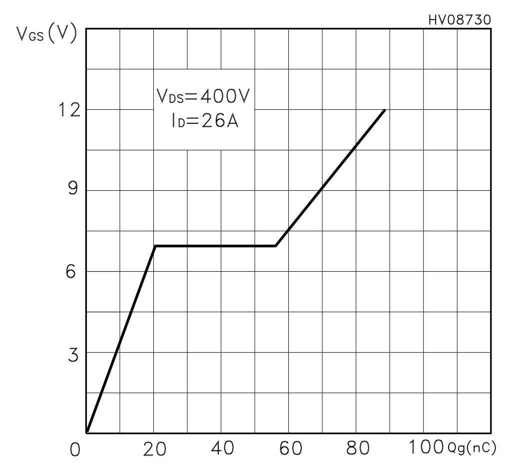


Figure 9. Capacitance variations

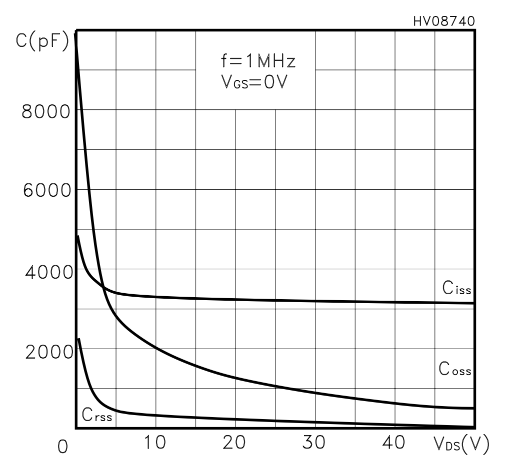


Figure 10. Normalized gate threshold voltage vs temperature

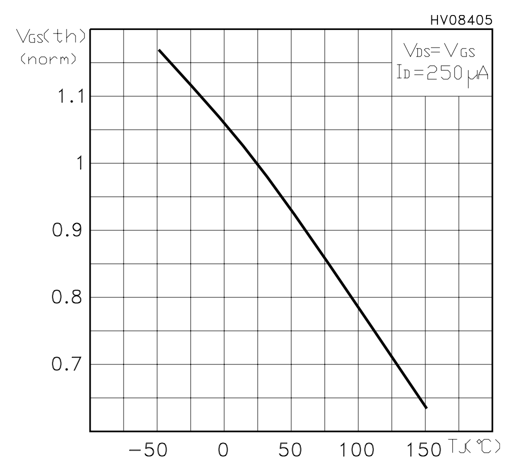


Figure 11. Normalized on resistance vs temperature

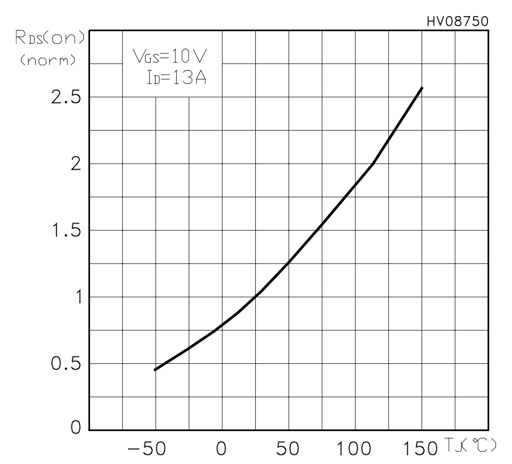


Figure 12. Source-drain diode forward characteristics

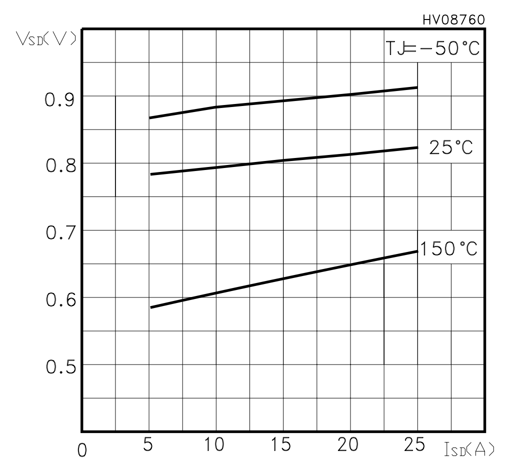
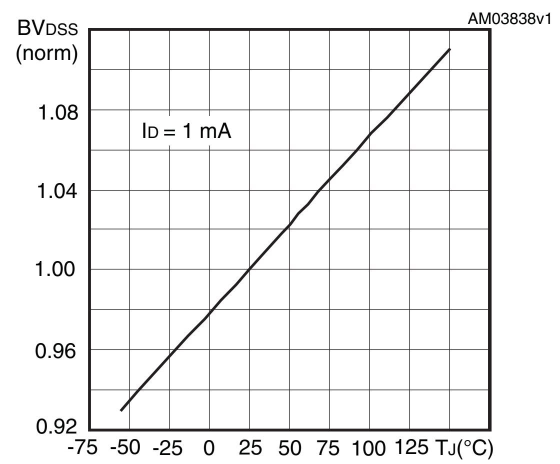


Figure 13. Normalized B_{VDSS} vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

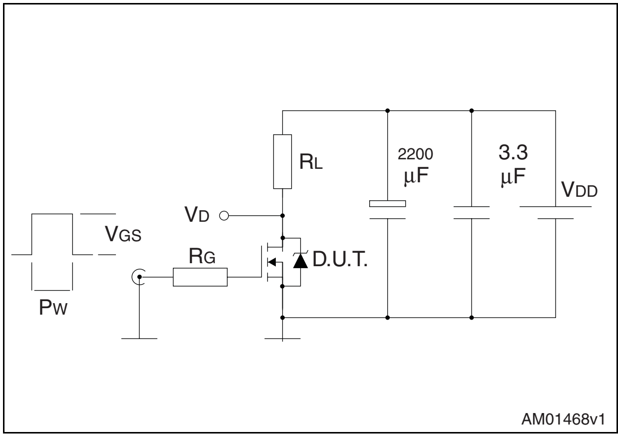


Figure 15. Gate charge test circuit

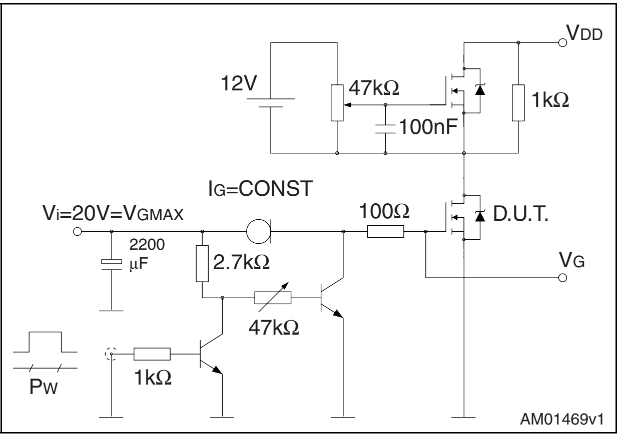


Figure 16. Test circuit for inductive load switching and diode recovery times

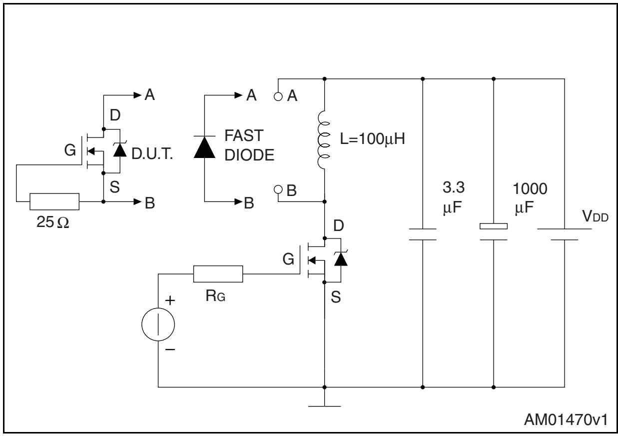


Figure 17. Unclamped inductive load test circuit

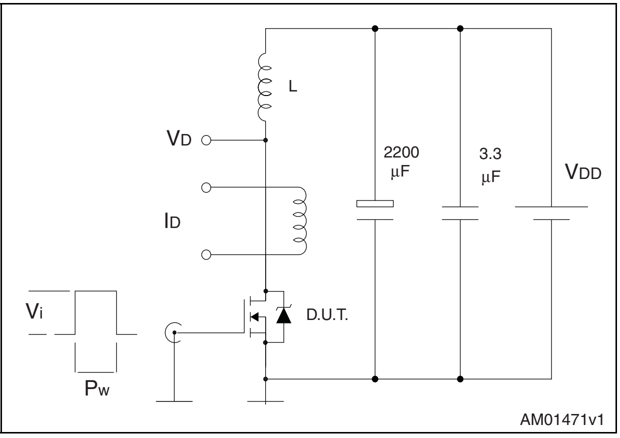


Figure 18. Unclamped inductive waveform

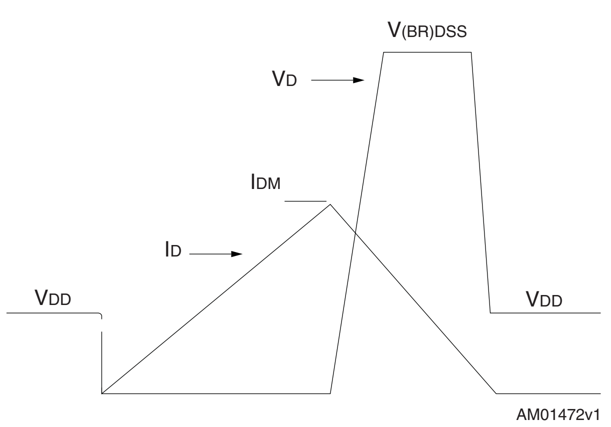
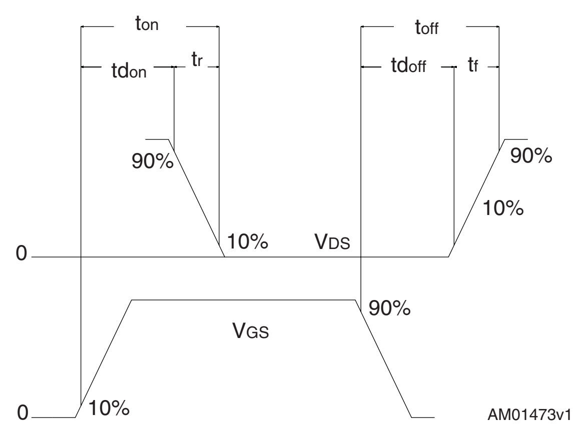


Figure 19. Switching time waveform



4 Package mechanical data

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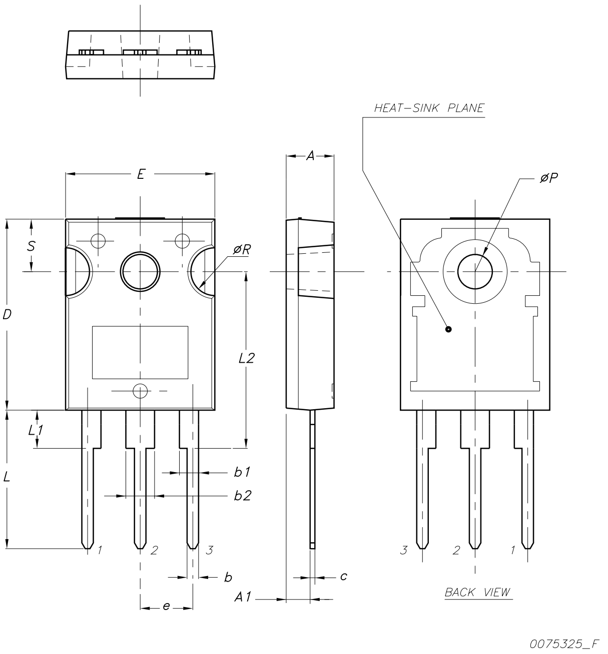
TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
24-Jun-2004	9	New stylesheet.
07-Feb-2005	10	I_D value changed
02-Oct-2009	11	Modified: test condition of $V_{(BR)DSS}$ in *Table 5*

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Email: org@lifeelectronics.ru

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