ECLTSSOP20EVB

Evaluation Board User's Manual for High Frequency TSSOP 20

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

INTRODUCTION

ON Semiconductor has developed an evaluation board for the devices in 20−lead TSSOP package. These evaluation boards are offered as a convenience for the customers interested in performing their own engineering assessment on the general performance of the 20−lead TSSOP device samples. The board provides a high bandwidth 50 Ω controlled impedance environment. Figures 1 and 2 show the top and bottom view of the evaluation board, which can be configured in several different ways, depending on device under test (see Table 1. Configuration List).

This evaluation board manual contains:

- Information on 20−lead TSSOP Evaluation Board
- Assembly Instructions
- Appropriate Lab Setup
- Bill of Materials

This manual should be used in conjunction with the device data sheet, which contains full technical details on the device specifications and operation.

Board Lay−Up

The 20−lead TSSOP evaluation board is implemented in four layers with split (dual) power supplies (see Figure 3. Evaluation Board Lay−Up). For standard ECL lab setup and test, a split (dual) power supply is essential to enable the 50 Ω internal impedance in the oscilloscope as a termination for ECL devices. The first layer or primary trace layer is 0.008″ thick Rogers RO4003 material, which is designed to have equal electrical length on all signal traces from the device under the test (DUT) to the sense output. The second layer is the 1.0 oz copper ground. The FR4 dielectric material is placed between second and third layer and between third and fourth layer. The third layer is the power plane (V_{CC} & V_{EE}) and a portion of this layer is a ground plane. The fourth layer is the secondary trace layer.

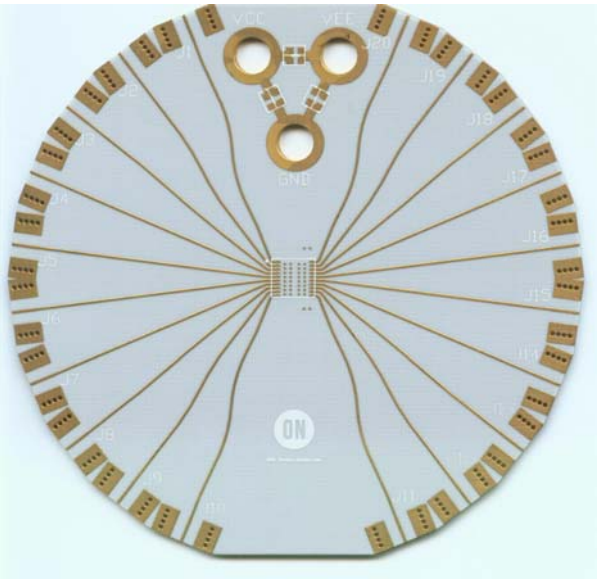

Figure 1. Top View of the 20−lead TSSOP Evaluation Board

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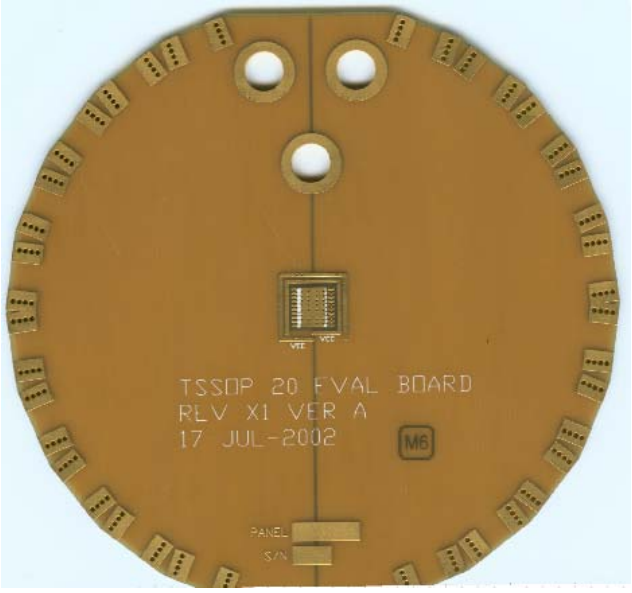
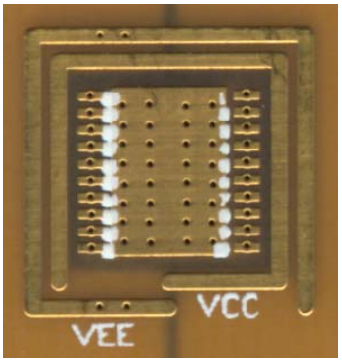


Bottom View



Expanded Bottom View

Figure 2. Bottom View of the 20−lead TSSOP Evaluation Board

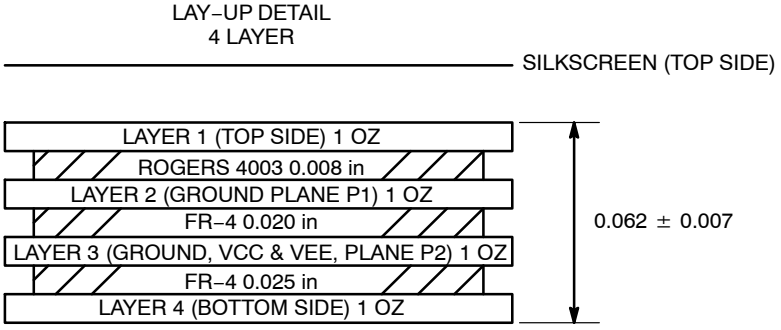
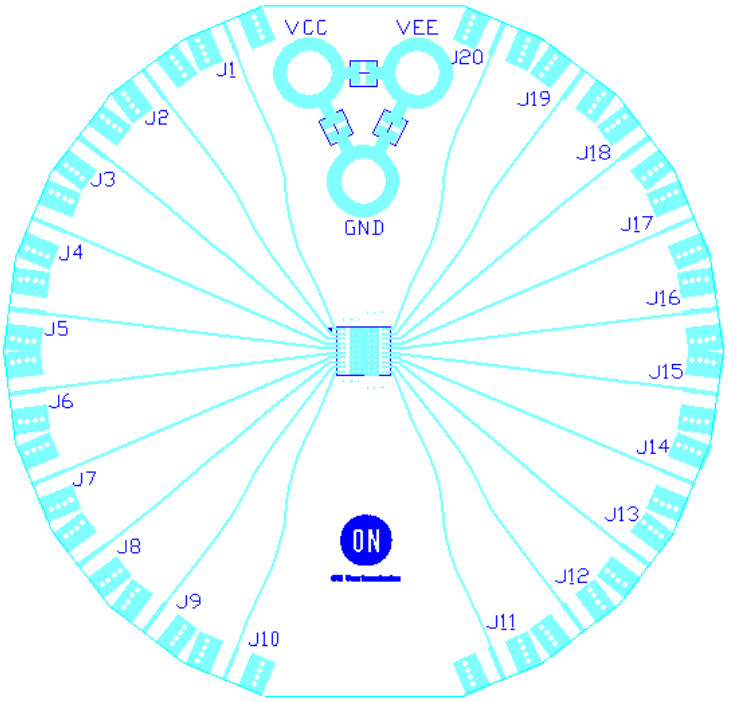


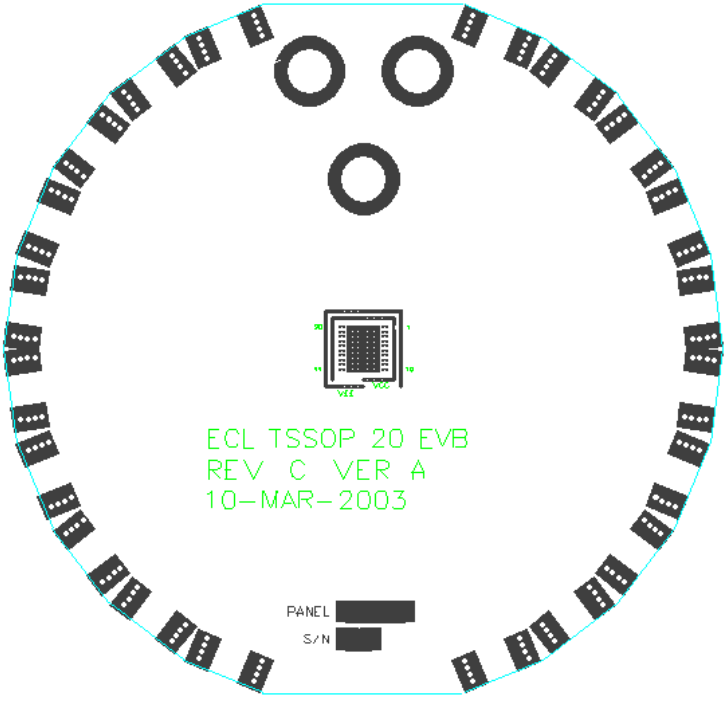
Figure 3. Evaluation Board Lay−up

Board Layout

The 20−lead TSSOP evaluation board was designed to be versatile and accommodate several different configurations. The input, output, and power pin layout of the evaluation board is shown in Figures 4 and 5. The evaluation board has at least eight possible configurable options. Table 1, list the devices and the relevant configuration that utilizes this PCB board. Lists of components and simple schematics are located in Figures 6 through 12. Place SMA connectors on J1 through J20, 50 Ω chip resistors between ground pad and Pin 1 pad through Pin 20 pad, and chip capacitors C1 through C5 according to configuration figures. (C4 and C5 are 0.01 μF and C1, C2, and C3 are 0.1 μF); (See Figure 5).



Top View



Bottom View

Figure 4. Evaluation Board Layout

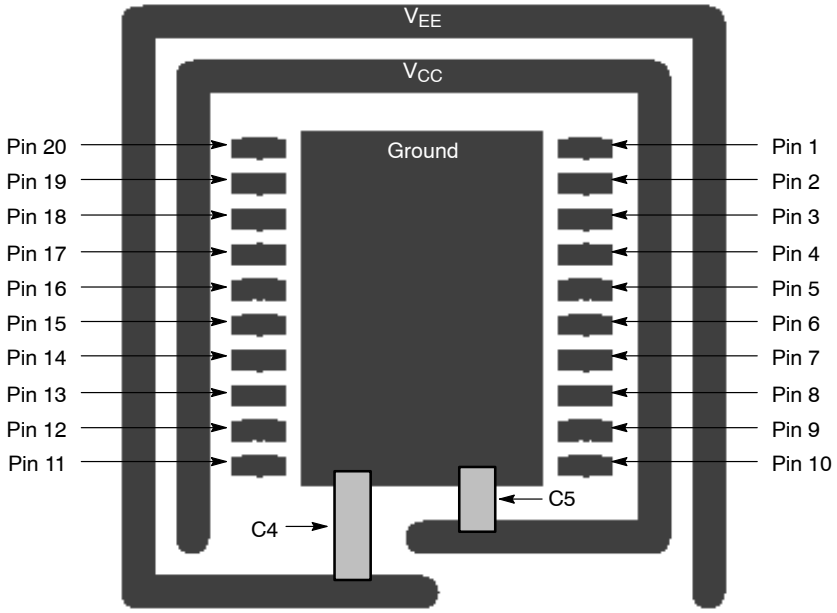


Figure 5. Enlarged Bottom View of the Evaluation Board

Table 1. Configuration List

Configuration	Comments	Device
1	See Figure 6	EP14, LVEP14
2	See Figure 7	EP17, LVEP17
3	See Figure 8	EP29
4	See Figure 9	EP40
5	See Figure 10	EP56, LVEP56
6	See Figure 11	EP57
7	See Figure 12	EP139

Evaluation Board Assembly Instructions

The 20−lead TSSOP evaluation board is designed for characterizing devices in a 50 Ω laboratory environment using high bandwidth equipment. Each signal trace on the board has a via, which has an option of placing a termination resistor depending on the input/output configuration (see Table 1, Configuration List). Table 11 contains the Bill of Materials for this evaluation board.

Solder the Device on the Evaluation Board

The soldering can be accomplished by hand soldering or soldering re−flow techniques. Make sure pin 1 of the device is located next to the white dotted mark and all the pins are aligned to the footprint pads. Solder the 20−lead TSSOP device to the evaluation board.

Connecting Power and Ground Planes

For standard ECL lab setup and test, a split (dual) power supply is required enabling the 50 Ω internal impedance in the oscilloscope to be used as a termination of the ECL signals ($V_{TT} = V_{CC} – 2.0$ V, in split power supply setup, V_{TT} is the system ground, V_{CC} is 2.0 V, and V_{EE} is –3.0 V or –1.3 V; see Table 2, Power Supply Levels).

Table 2. Power Supply Levels

Power Supply	V_{CC}	V_{EE}	GND
5.0 V	2.0 V	−3.0 V	0.0 V
3.3 V	2.0 V	−1.3 V	0.0 V
2.5 V	2.0 V	−0.5 V	0.0 V

Connect three banana jack sockets to V_{CC}, V_{EE}, and GND labeled holes. Wire bond the appropriate device pin pad on the bottom side of the board to V_{CC} and V_{EE} power stripes. (Device specific, please see configuration for each desired device. See Figure 5)

It is recommended to solder 0.01 μF capacitors to C4 and C5 to reduce the unwanted noise from the power supplies. C1, C2, and C3 pads are provided for 0.1 μF capacitor to further diminish the noise from the power supplies. Adding capacitors can improve edge rates, reduce overshoot and undershoot.

Termination

All ECL outputs need to be terminated to V_{TT} ($V_{TT} = V_{CC} –2.0$ V = GND) via a 50 Ω resistor. 0402 chip resistor pads are provided on the bottom side of the evaluation board to terminate the ECL driver (More information on termination is provided in AN8020). Solder the chip resistors to the bottom side of the board between the appropriate input of the device pin pads and the ground pads. For ease of assembly, it is advised to place and solder termination resistors on its vertical (side) position, instead of its original or flat position.

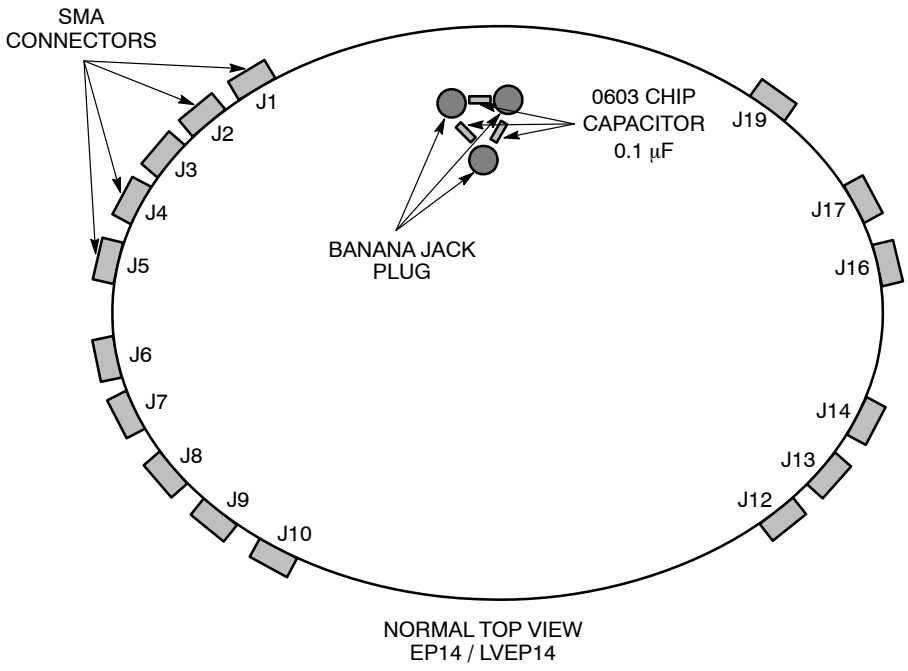
Installing the SMA Connectors

Each configuration indicates the number of SMA connectors needed to populate an evaluation board for a given configuration. Each input and output requires one SMA connector. Attach all the required SMA connectors onto the board and solder the connectors to the board on J1 through J20. Please note that alignment of the signal connector pin of the SMA can influence the lab results. The reflection and launch of the signals are largely influenced by imperfect alignment and soldering of the SMA connector.

Validating the Assembled Board

After assembling the evaluation board, it is recommended to perform continuity checks on all soldered areas before commencing with the evaluation process. Time Domain Reflectometry (TDR) is another highly recommended validation test.

CONFIGURATIONS



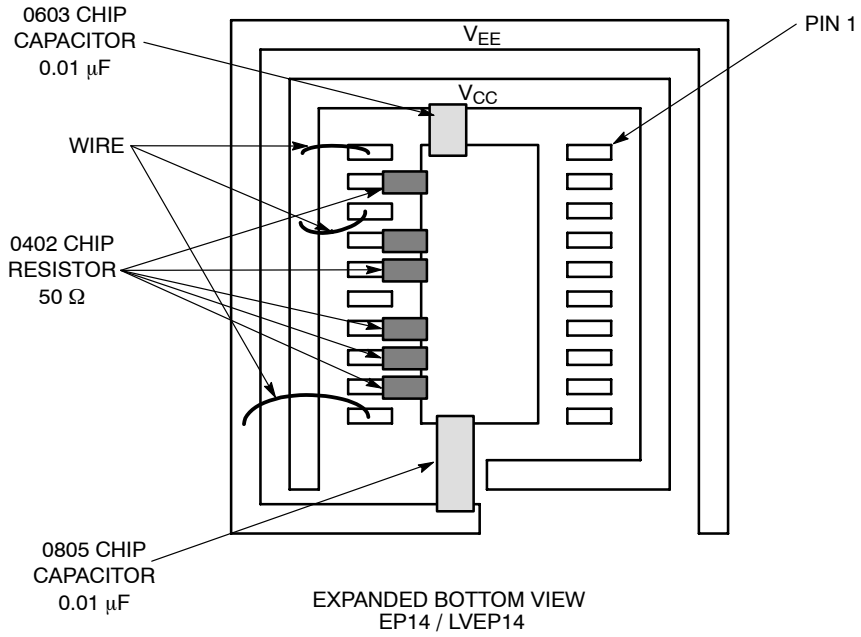
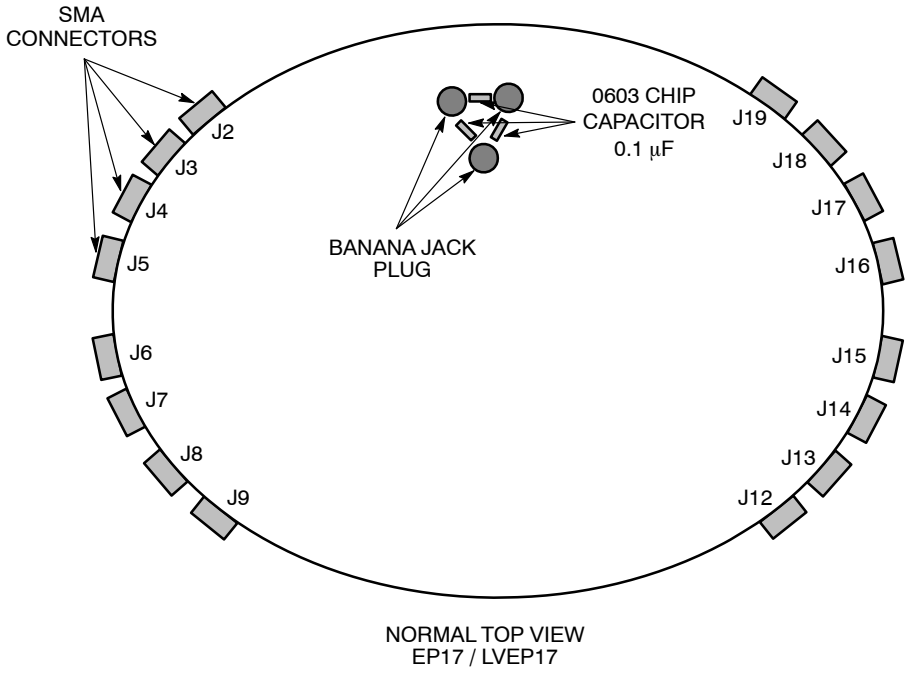


Figure 6. Configuration 1

Table 3. Configuration 1 (Device EP14 and LVEP14)

Device	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20
Pin #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
Connector	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	No
Resistor	No	No	No	No	No	No	No	No	No	No	No	Yes	Yes	Yes	No	Yes	Yes	No	Yes	No
Power	No	No	No	No	No	No	No	No	No	No	V_{EE}	No	No	No	No	No	No	V_{CC}	No	V_{CC}



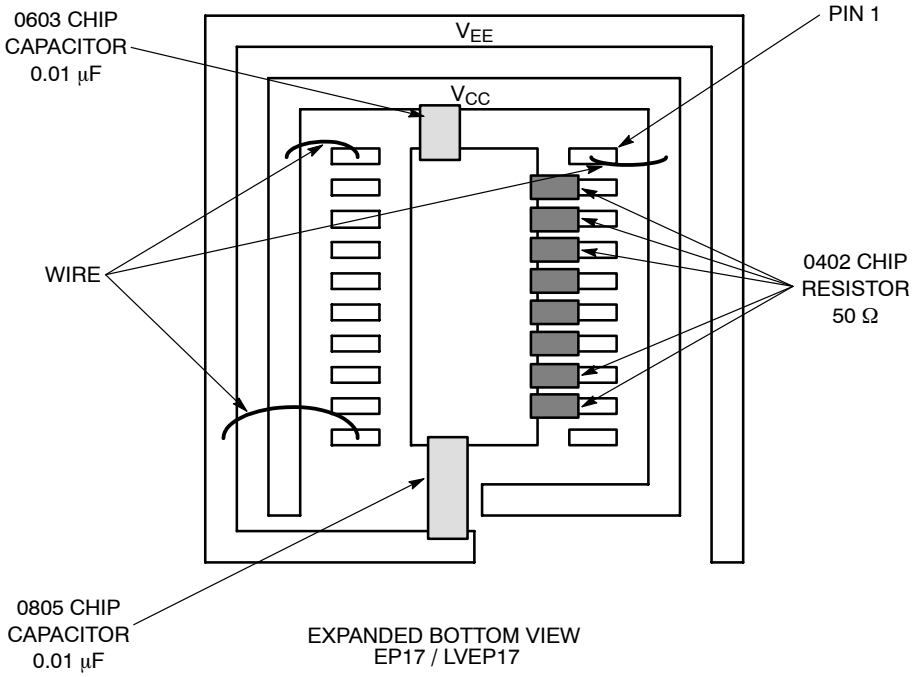
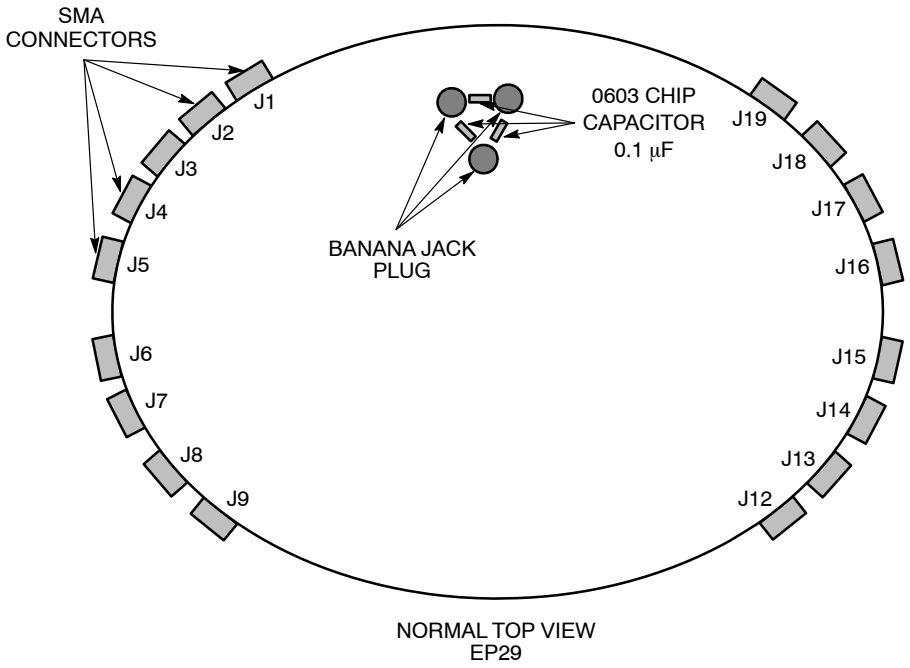


Figure 7. Configuration 2

Table 4. Configuration 2 (Device EP17 and LVEP17)

Device	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20
Pin #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
Connector	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Resistor	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No	No	No	No	No	No
Power	V_{CC}	No	No	No	No	No	No	No	No	No	V_{EE}	No	No	No	No	No	No	No	No	V_{CC}



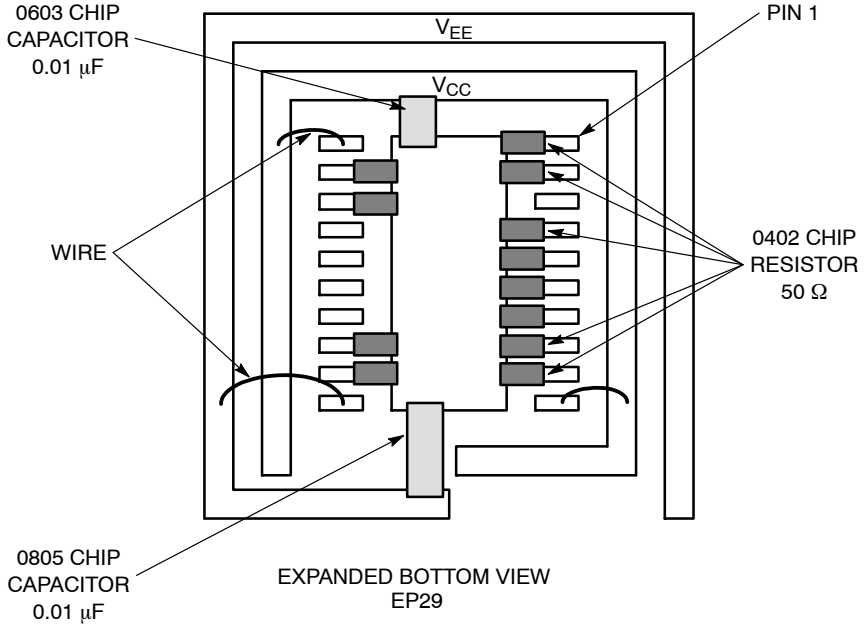


Figure 8. Configuration 3

Table 5. Configuration 3 (Device EP29)

Device	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20
Pin #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
Connector	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Resistor	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	Yes	Yes	No	No	No	No	Yes	Yes	No
Power	No	No	No	No	No	No	No	No	No	V_{CC}	V_{EE}	No	No	No	No	No	No	No	No	V_{CC}

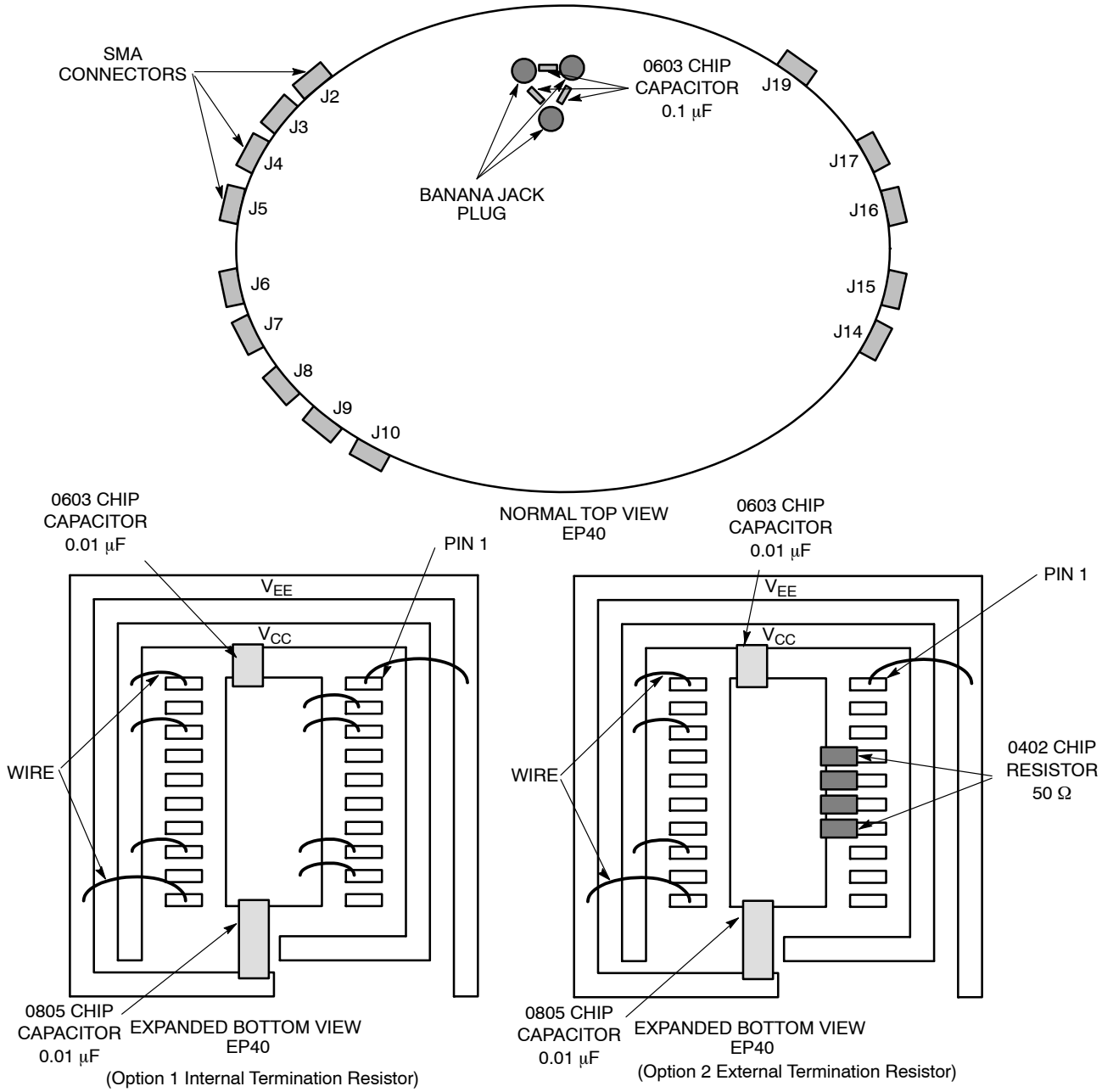


Figure 9. Configuration 4

Table 6. Configuration 4 (Device EP40) (Options 1 & 2)

Device	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20
Pin #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
Option 1 Internal Termination Resistor Configuration																				
Connector	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	Yes	Yes	Yes	Yes	No	Yes	No
Resistor	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No
Power	V_{EE}	Gnd	Gnd	No	No	No	No	Gnd	Gnd	No	V_{EE}	No	V_{CC}	No	No	No	No	V_{CC}	No	V_{CC}
Option 2 External Termination Resistor Configuration																				
Connector	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	Yes	Yes	Yes	Yes	No	Yes	No
Resistor	No	No	No	Yes	Yes	Yes	Yes	No	No	No	No	No	No	No	No	No	No	No	No	No
Power	V_{EE}	No	No	No	No	No	No	No	No	No	V_{EE}	No	V_{CC}	No	No	No	No	V_{CC}	No	V_{CC}

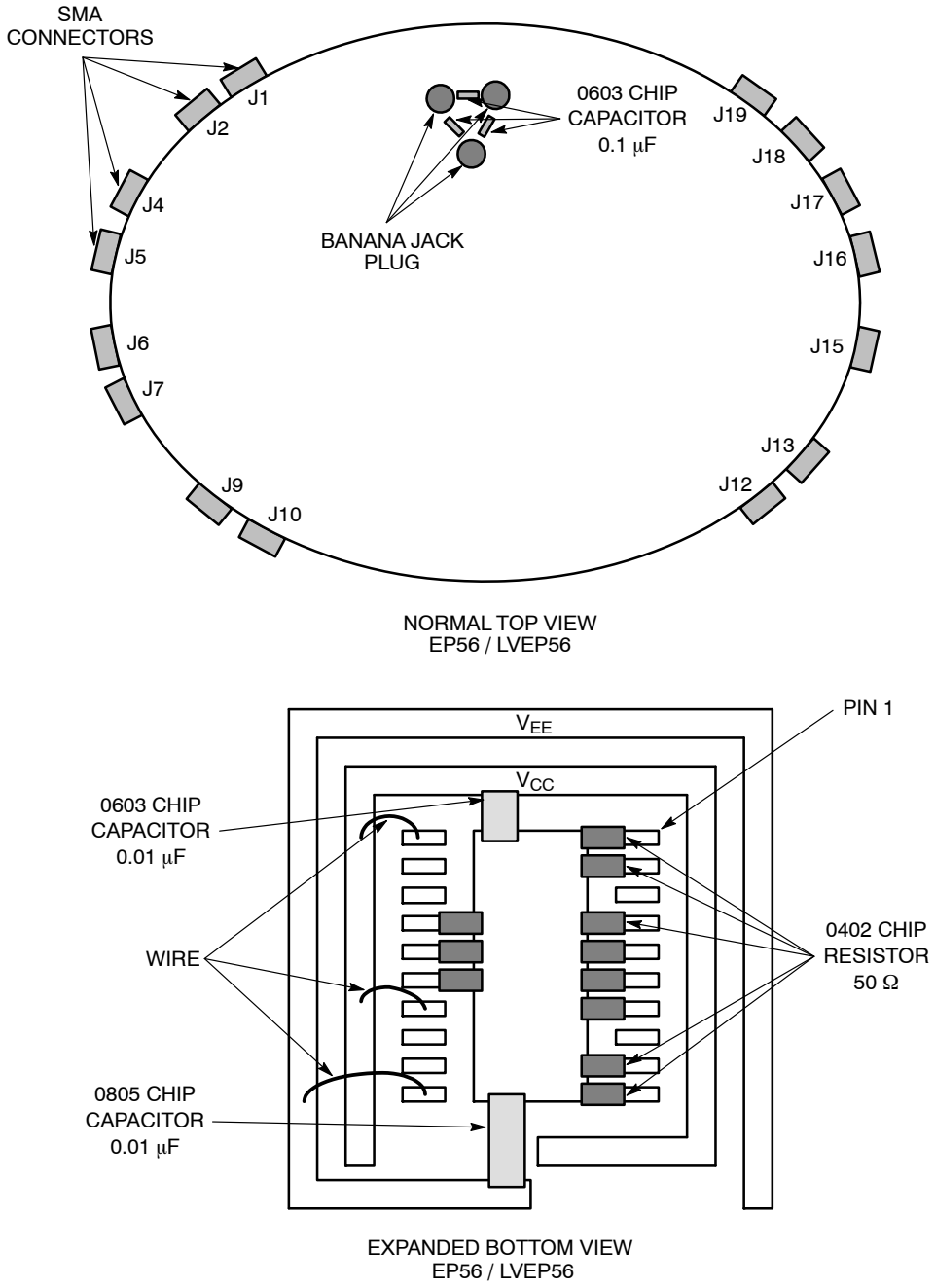


Figure 10. Configuration 5

Table 7. Configuration 5 (Device EP56 and LVEP56)

Device	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20
Pin #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
Connector	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	No
Resistor	Yes	Yes	No	Yes	Yes	Yes	Yes	No	Yes	Yes	No	No	No	No	Yes	Yes	Yes	No	No	No
Power	No	No	No	No	No	No	No	No	No	No	V_{EE}	No	No	V_{CC}	No	No	No	No	No	V_{CC}

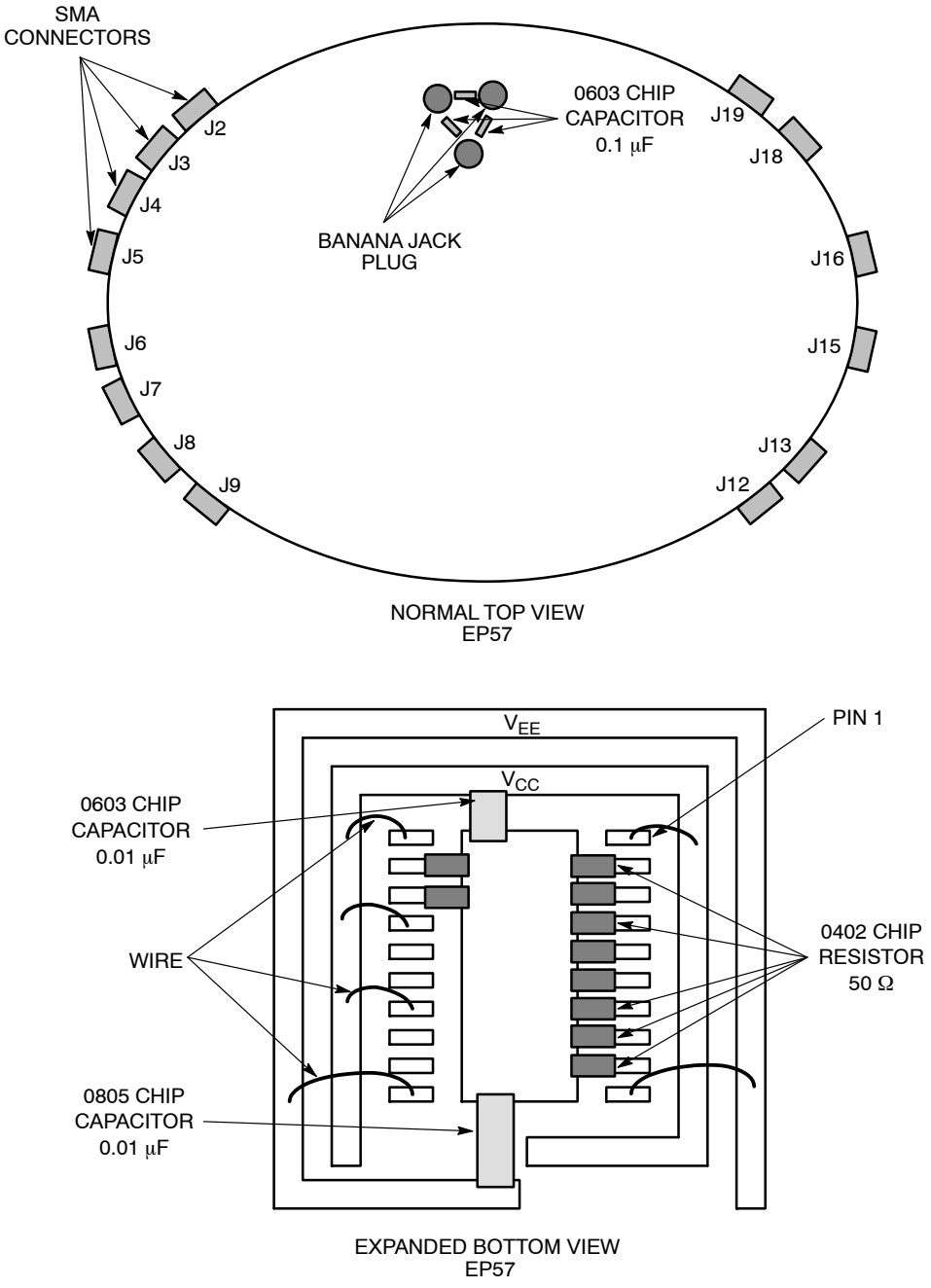
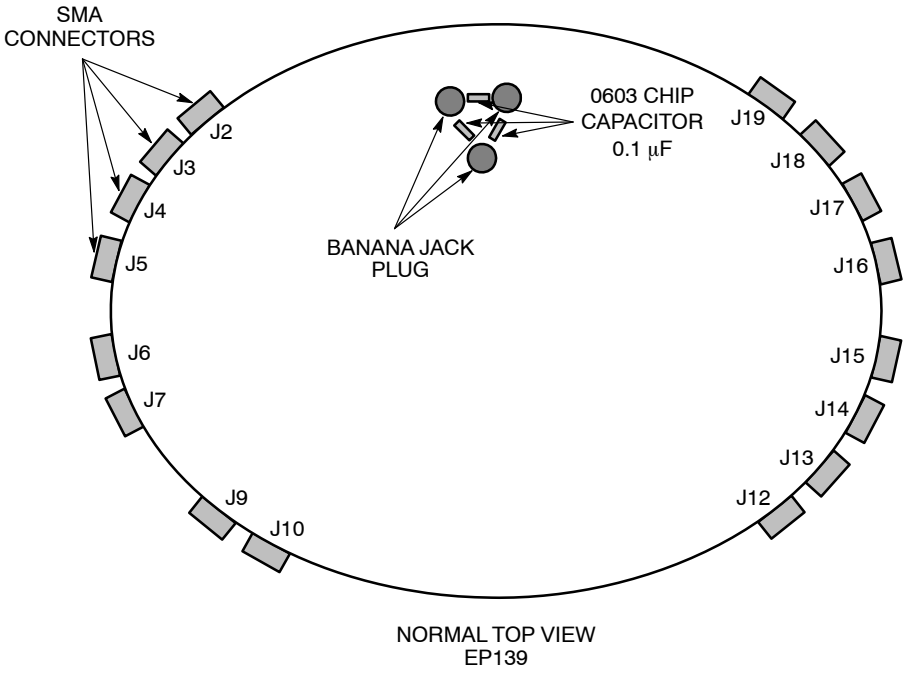


Figure 11. Configuration 6

Table 8. Configuration 6 (Device EP57)

Device	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20
Pin #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
Connector	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	Yes	Yes	No	Yes	Yes	No	Yes	Yes	No
Resistor	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	No	No	No	No	No	Yes	Yes	No
Power	V_{CC}	No	No	No	No	No	No	No	No	V_{EE}	V_{EE}	No	No	V_{CC}	No	No	V_{CC}	No	No	V_{CC}



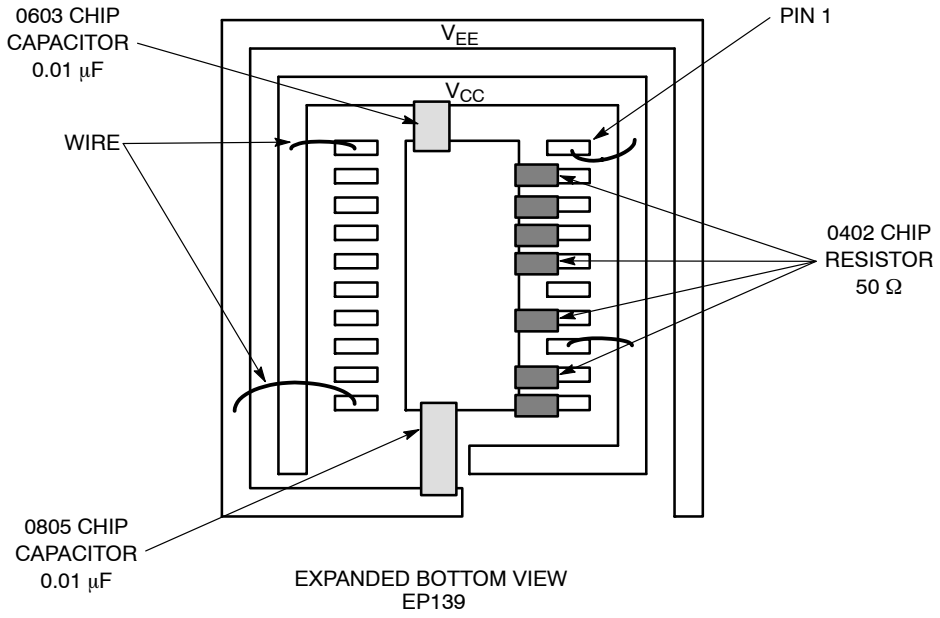


Figure 12. Configuration 7

Table 9. Configuration 7 (Device EP139)

Device	J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16	J17	J18	J19	J20
Pin #	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**
Connector	No	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No
Resistor	No	Yes	Yes	Yes	Yes	No	Yes	No	Yes	Yes	No	No	No	No	No	No	No	No	No	No
Power	V_{CC}	No	No	No	No	No	No	V_{CC}	No	No	V_{EE}	No	No	No	No	No	No	No	No	V_{CC}

LAB SETUP

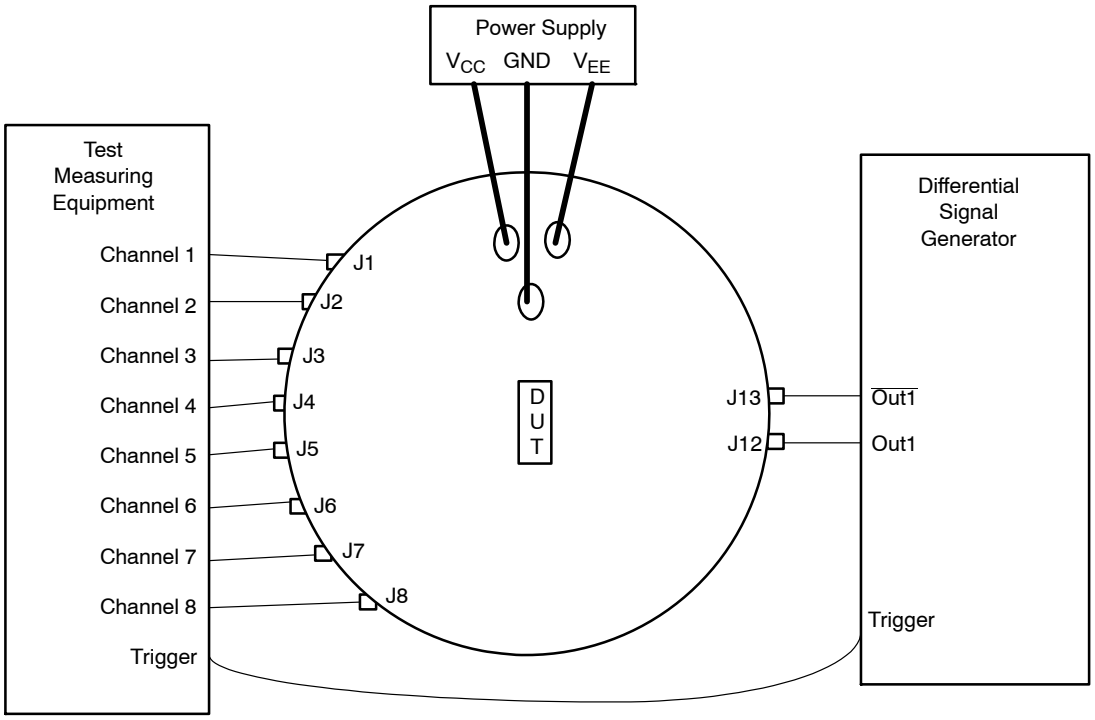


Figure 13. Example of Standard Lab Setup (Configuration 1)

1. Connect appropriate power supplies to V_{CC}, V_{EE}, and GND.
   For standard ECL lab setup and test, a split (dual) power supply is required enabling the 50 Ω internal impedance in the oscilloscope to be used as a termination of the ECL signals (V_{TT} = V_{CC} – 2.0 V, in split power supply setup, V_{TT} is the system ground, V_{CC} is 2.0 V, and V_{EE} is –3.0 V or –1.3 V; see Table 10).
2. Connect a signal generator to the input SMA connectors. Setup input signal according to the device data sheet.
3. Connect a test measurement device on the device output SMA connectors.

NOTE: The test measurement device must contain 50 Ω termination.

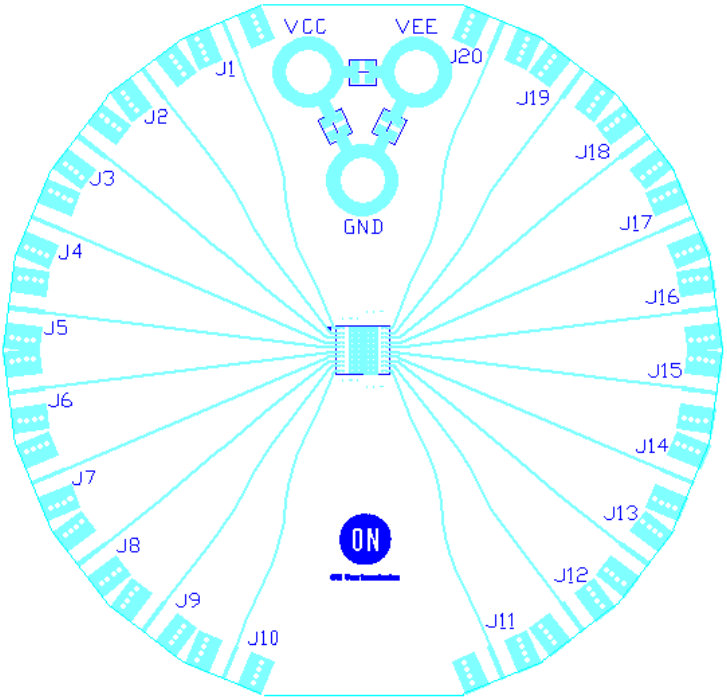
Table 10. Power Supply Levels

Power Supply	V_{CC}	V_{EE}	GND
5.0 V	2.0 V	–3.0 V	0.0 V
3.3 V	2.0 V	–1.3 V	0.0 V
2.5 V	2.0 V	–0.5 V	0.0 V

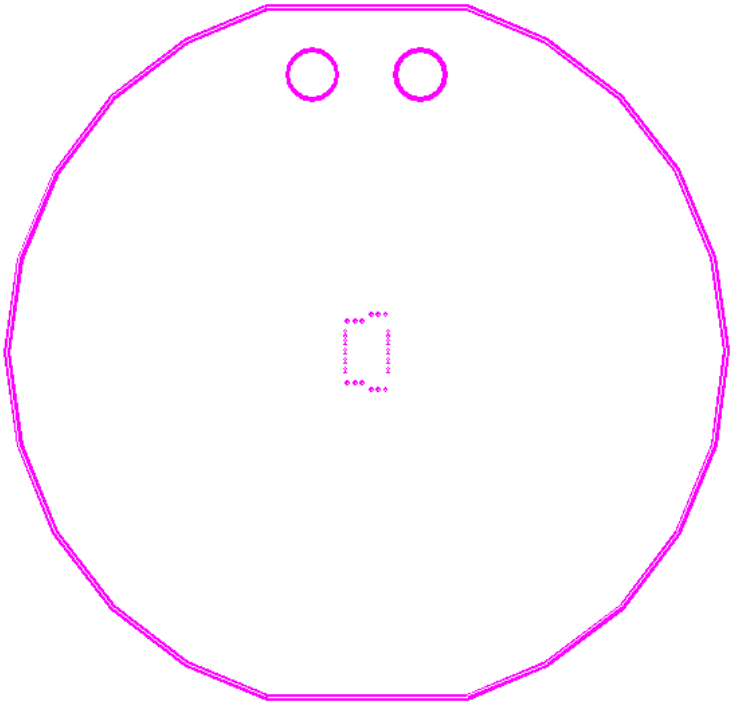
Table 11. Bill of Materials

Components	Manufacturer	Description	Part Number	Web Site
SMA Connector	Johnson Components*	SMA Connector, Side Launch, Gold Plated	142−0701−851	http://www.johnsoncomponents.com
Banana Jack	Keystone*	Standard Jack	6096	http://www.keyelco.com
		Miniature Jack	6090	
Chip Capacitor	Johanson Dielectric*	0603 0.01 μF	500R14Z100MV4E	http://www.johansondielectrics.com
		0805 0.01 μF	500R15Z100MV4E	
		0603 0.1 μF	250R14Z101MV4E	
Chip Resistor	Panasonic*	0402 50 Ω ± 1% Precision Think Film Chip Resistor	ERJ−2RKF49R9X	http://www.panasonic.com
Evaluation Board	ON Semiconductor	TSSOP 20 Evaluation Board	ECLTSSOP20EVB	http://www.onsemi.com
Device Samples	ON Semiconductor	TSSOP 20 Package Device	Various	http://www.onsemi.com

*Components are available through most distributors, i.e. www.newark.com, www.digikey.com.

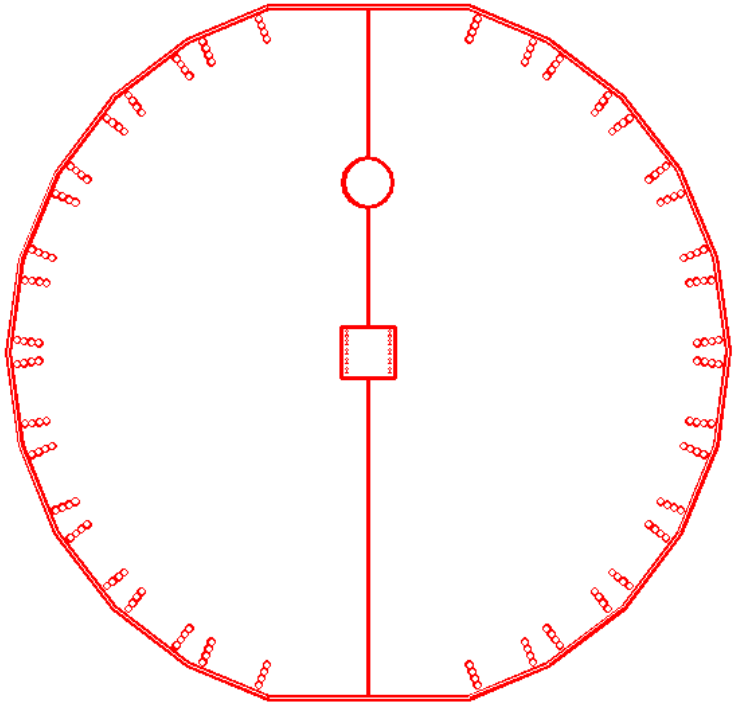


Top View

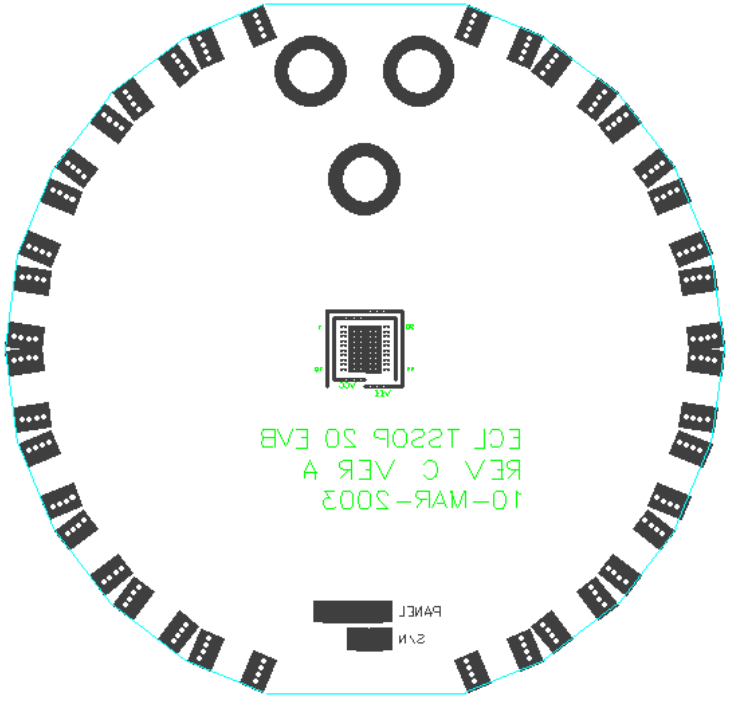


Second Layer (Ground Plane)

Figure 14. Gerber Files



Third Layer (Power and Ground Plane)
(Left side – V_{CC}, Right side – V_{EE}, Middle Box – Ground)



Bottom Layer

Figure 15. Gerber Files

ECLTSSOP20EVB

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