

DAC2813

## DUAL 12-BIT DIGITAL-TO-ANALOG CONVERTER (12-bit port interface)

### FEATURES

- COMPLETE WITH REFERENCE AND OUTPUT AMPLIFIERS
- 12-BIT PORT INTERFACE
- ANALOG OUTPUT RANGE:  $\pm 10V$
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- INTEGRAL LINEARITY ERROR:  $\pm 1/2LSB$  max
- $\pm 12V$  to  $\pm 15V$  SUPPLIES
- 28-PIN PLASTIC DIP PACKAGE

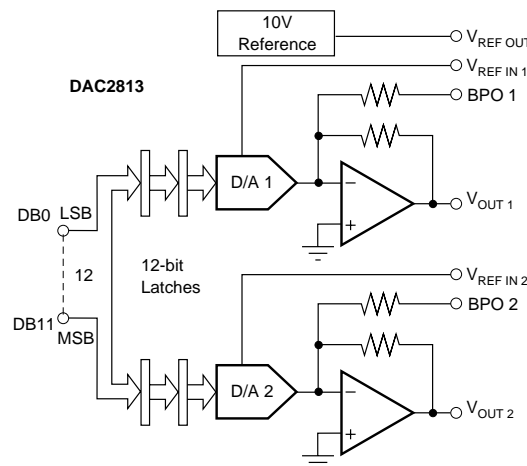
### DESCRIPTION

DAC2813 is a complete dual 12-bit digital-to-analog converter with bus interface logic. Each package includes a precision +10V voltage reference, double-buffered bus interface including a RESET function and 12-bit D/A converters with voltage-output operational amplifiers.

The double-buffered interface consists of a 12-bit input latch and a D/A latch for each D/A converter. A RESET control allows the D/A outputs to be asynchronously reset to bipolar zero, a feature useful for power-up reset, system initialization and recalibration.

DAC2813 output range resistors are internally connected for 20V full scale range. A 0 to 10V range can be connected using the bipolar offset resistor. Gain and bipolar offset of each D/A are adjustable with external trim potentiometers.

DAC2813 is available in one performance grade with an integral linearity error of  $1/2LSB$  and 12-bit monotonicity guaranteed over temperature. It is packaged in 28-pin 0.6in. wide plastic DIP package and specified over  $-40^{\circ}C$  to  $+85^{\circ}C$ .



# SPECIFICATIONS

## ELECTRICAL

At  $T_A = +25^\circ\text{C}$ ,  $+V_{CC} = +12\text{V}$  or  $+15\text{V}$ ,  $-V_{CC} = -12\text{V}$  or  $-15\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	DAC2813AP			UNITS
		MIN	TYP	MAX	
<b>INPUTS</b>					
<b>DIGITAL INPUTS</b>	Over Temperature Range		Bipolar Offset Binary		
Input Code <sup>(1)</sup>					
Logic Levels <sup>(2)</sup>					
$V_{IH}$		+2		+5.5 <sup>(3)</sup>	V
$V_{IL}$		0		+0.8	V
Logic Input Currents DB0-DB11, WR, LDAC, RESET, EN <sub>x</sub>	$V_I = +2.7\text{V}$ $V_I = +0.4\text{V}$			$\pm 20$ $\pm 20$	$\mu\text{A}$ $\mu\text{A}$
<b>TRANSFER CHARACTERISTICS</b>					
<b>ACCURACY</b>					
Linearity Error			$\pm 1/4$	$\pm 1/2$	LSB
Differential Linearity Error			$\pm 1/2$	$\pm 1$	LSB
Gain Error <sup>(5,6)</sup>			$\pm 0.05$	$\pm 0.2$	%
Bipolar Zero Error <sup>(5,7)</sup>			$\pm 0.05$	$\pm 0.2$	%FSR <sup>(4)</sup>
Power Supply Sensitivity Of Full Scale $+V_{CC}$ $-V_{CC}$			$\pm 5$ $\pm 1$	$\pm 20$ $\pm 10$	ppmFSR/% $+V_{CC}$ ppmFSR/% $-V_{CC}$
<b>DRIFT</b>					
Gain	Over Specification Temperature Range		$\pm 5$	$\pm 30$	ppm/ $^\circ\text{C}$
Bipolar Zero Drift			$\pm 5$	$\pm 15$	ppmFSR/ $^\circ\text{C}$
Linearity Error over Temperature			$\pm 1/2$	$\pm 3/4$	LSB
Monotonicity			Guaranteed		
<b>DYNAMIC CHARACTERISTICS</b>					
<b>SETTLING TIME <sup>(8)</sup></b>					
	To within $\pm 0.012\%$ FSR of Final Value 5k $\Omega$    500pF Load 20V Range				
Full Scale Range Change			4.5	6	$\mu\text{s}$
1LSB Output Step <sup>(9)</sup> At Major Carry			2		$\mu\text{s}$
Slew Rate			10		V/ $\mu\text{s}$
Crosstalk <sup>(10)</sup>	5k $\Omega$ Loads		0.1		LSB
<b>OUTPUT</b>					
Output Voltage Range	$\pm V_{CC} \geq \pm 11.4\text{V}$			$\pm 10$	V
Output Current		$\pm 5$			mA
Output Impedance			0.2		$\Omega$
Short Circuit to ACOM Duration			Indefinite		
<b>REFERENCE VOLTAGE</b>					
Voltage		+9.95	+10.00	+10.05	V
Source Current Available for External Loads		2			mA
Impedance			0.2		$\Omega$
Temperature Coefficient			$\pm 5$	$\pm 25$	ppm/ $^\circ\text{C}$
Short Circuit to Common Duration			Indefinite		
<b>POWER SUPPLY REQUIREMENTS</b>					
Voltage: $+V_{CC}$ $-V_{CC}$		+11.4 -11.4	+15 -15	+16.5 -16.5	V V
Current:	No Load $\pm V_{CC} = \pm 15\text{V}$				
$+V_{CC}$			24	30	mA
$-V_{CC}$			12	14	mA
Power Dissipation			540	660	mW
Potential at DCOM with Respect to ACOM <sup>(11)</sup>		-3		+3	V
<b>TEMPERATURE RANGES</b>					
Specification		-40		+85	$^\circ\text{C}$
Storage		-60		+100	$^\circ\text{C}$
Thermal Resistance, $\theta_{JA}$ , Plastic DIP			30		$^\circ\text{C}/\text{W}$

NOTES: (1) For Two's Complement Input Coding invert the MSB with an external logic inverter. (2) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (3) Open DATA input lines will be pulled above +5.5V. See discussion under LOGIC INPUT COMPATIBILITY section. (4) FSR means Full Scale Range. For example, for  $\pm 10\text{V}$  output, FSR = 20V. (5) Adjustable to zero with external trim potentiometer. (6) Specified with 500 $\Omega$  connected between  $V_{REF\ OUT}$  and  $V_{REF\ IN}$ . (7) Error at input code 800<sub>HEX</sub>. DAC2813 specified with 100 $\Omega$  connected between  $V_{REF\ OUT}$  and  $V_{REF\ IN}$ ; and with 500 $\Omega$  connected between  $V_{REF\ OUT}$  and BPO. (8) Maximum represents the 3 $\sigma$  limit. Not 100% tested for this parameter. (9) For the worst-case code change: 7FF<sub>HEX</sub> to 800<sub>HEX</sub> and 800<sub>HEX</sub> to 7FF<sub>HEX</sub>. (10) Crosstalk is defined as the change in any output as a result of any other output being driven from -10V to +10V at rated output current. (11) The maximum voltage at which ACOM and DCOM may be separated without affecting accuracy specifications.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

+V <sub>CC</sub> to ACOM	0 to +18V
-V <sub>CC</sub> to ACOM	0 to -18V
+V <sub>CC</sub> to -V <sub>CC</sub>	0 to +36V
ACOM to DCOM	±4V
Digital Inputs to DCOM	-1V to +V <sub>CC</sub>
External Voltage applied to BPO Resistor	±18V
V <sub>REF OUT</sub>	Indefinite short to ACOM
V <sub>OUT</sub>	Momentary to ±18V
Lead Temperature, soldering 10s	+300°C
Max Junction Temperature	165°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

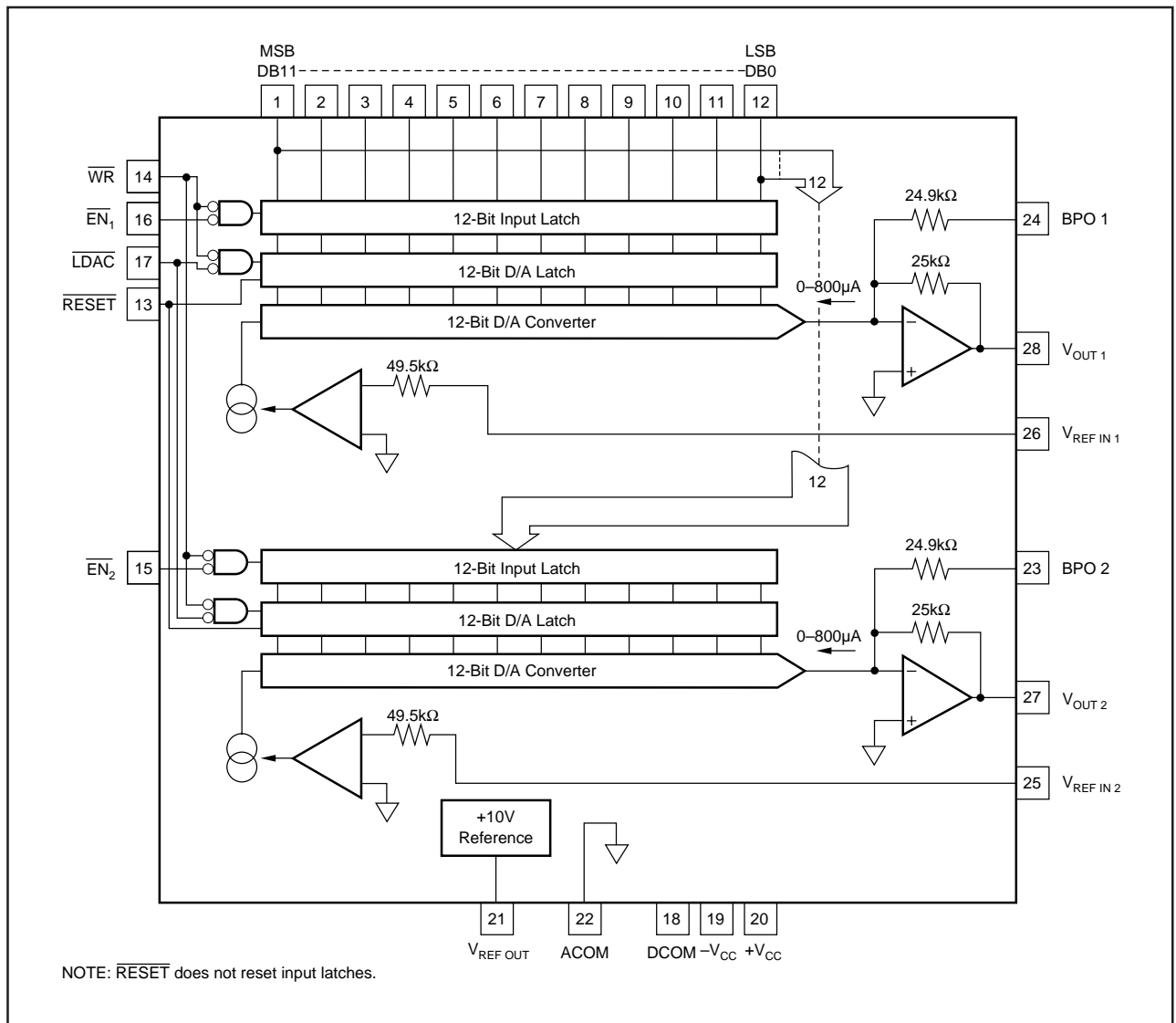
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

## PACKAGE/ORDERING INFORMATION

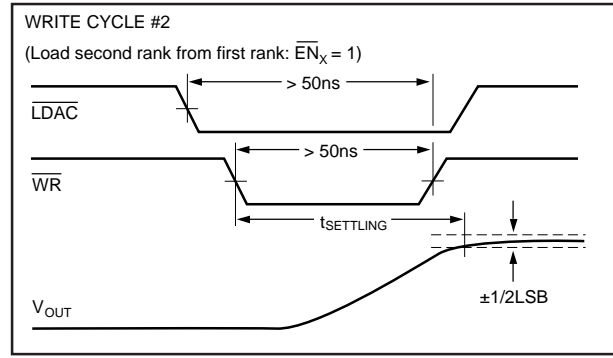
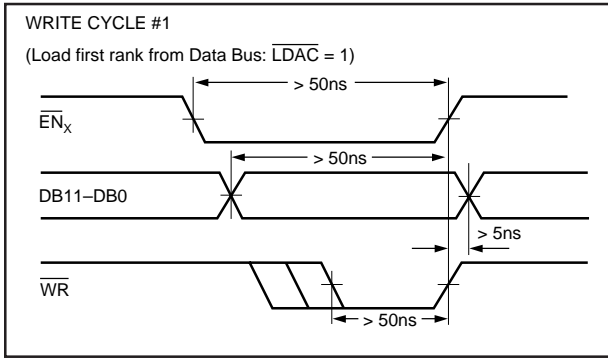
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>	TEMPERATURE RANGE
DAC2813AP	28-Pin DBL Wide DIP	215	-40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

## BLOCK DIAGRAM



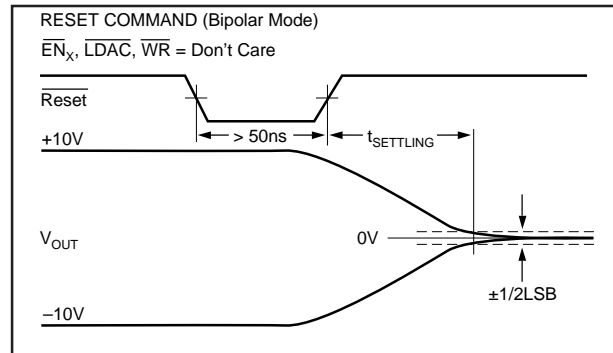
## TIMING DIAGRAMS



## TRUTH TABLE

WR	EN1	EN2	LDAC	RESET	OPERATION
X	X	X	X	0	Reset both D/A Latches. Does not reset input latches.
1	X	X	X	1	No Operation
X	1	1	1	1	No Operation
0	1	0	1	1	Load Data into First Rank for D/A 2
0	0	1	1	1	Load Data into First Rank for D/A 1
0	1	1	0	1	Load Second Rank from First Rank, both D/As
0	0	0	0	1	All Latches Transparent

"X" = Don't Care



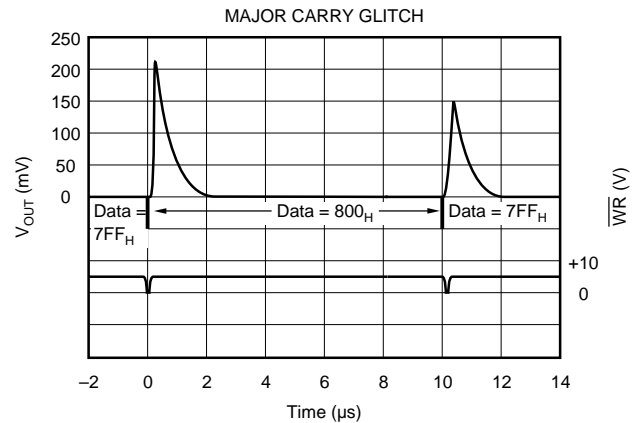
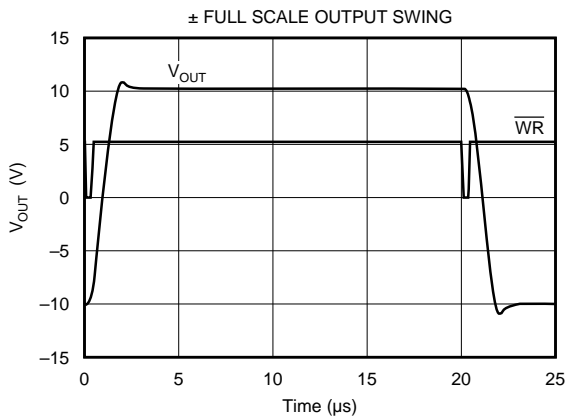
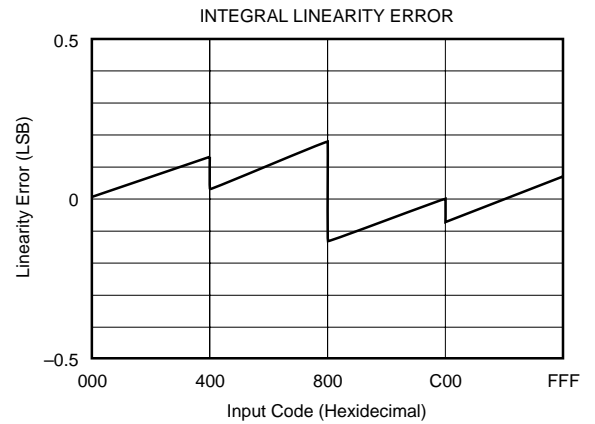
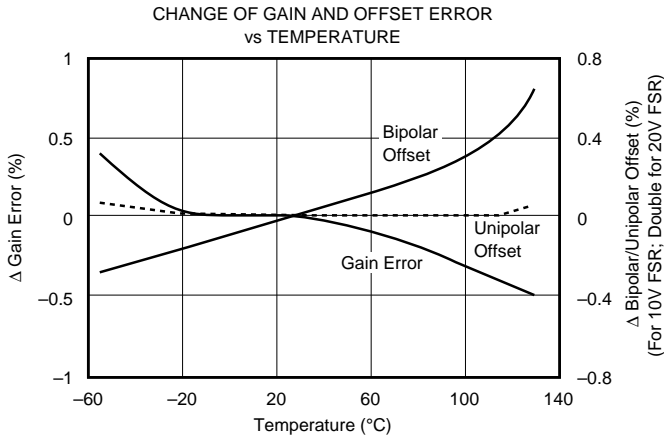
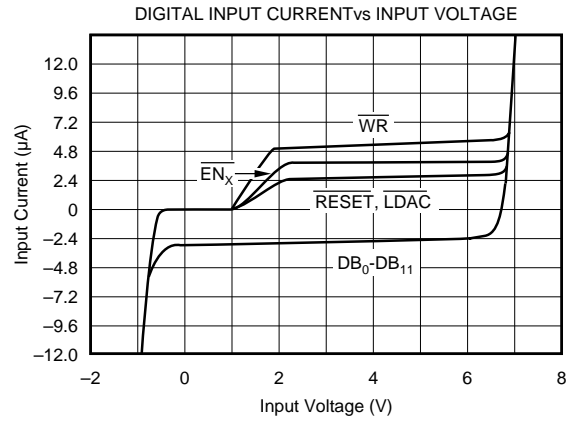
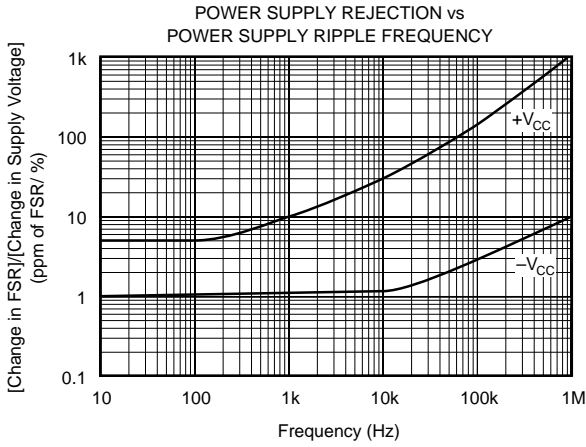
## PIN DESCRIPTIONS

PIN	NAME	FUNCTION
1	DB11	DATA, MSB, positive true.
2	DB10	DATA
3	DB9	DATA
4	DB8	DATA
5	DB7	DATA
6	DB6	DATA
7	DB5	DATA
8	DB4	DATA
9	DB3	DATA
10	DB2	DATA
11	DB1	DATA
12	DB0	DATA, LSB.
13	RESET	Resets output of all D/As to bipolar-zero. The D/A remains in this state until overwritten an $\overline{\text{LDAC}}\text{-}\overline{\text{WR}}$ command. RESET does not reset the input latch. After power-up and reset, input latches will be in an indeterminant state.
14	$\overline{\text{WR}}$	Write strobe. Must be low for data transfer to any latch (except RESET).
15	EN2	Enable for 12-bit input data latch of D/A 2. NOTE: This logic path is slower than the $\overline{\text{WR}}$ path.
16	EN1	Enable for 12-bit input data latch of D/A 1. NOTE: This logic path is slower than the $\overline{\text{WR}}$ path.
17	LDAC	Load DAC enable. Must be low with $\overline{\text{WR}}$ for data transfer to the D/A latch and simultaneous update of both D/A converters.
18	DCOM	Digital common, logic currents return.
19	$-V_{CC}$	Analog supply input, nominally $-12V$ or $-15V$ referred to ACOM.
20	$+V_{CC}$	Analog supply input, nominally $+12V$ or $+15V$ referred to ACOM.
21	$V_{REF\ OUT}$	$+10V$ reference output.
22	ACOM	Analog common, $+V_{CC}$ , $-V_{CC}$ supply return.
23	BPO2	Bipolar offset. Connect to pin 21 ( $V_{REF\ OUT}$ ) through a $100\Omega$ resistor or through a $200$ potentiometer for Bipolar Offset Adjust for D/A 2.
24	BPO1	Bipolar offset. Connect to pin 21 ( $V_{REF\ OUT}$ ) through a $100\Omega$ resistor or through a $200$ potentiometer for Bipolar Offset Adjust or D/A 1.
25	$V_{REF\ IN\ 2}$	Connect to $V_{REF\ OUT}$ through $500\Omega$ fixed resistor or through a $1k\Omega$ gain adjustment potentiometer for D/A 2.
26	$V_{REF\ IN\ 1}$	Connect to $V_{REF\ OUT}$ through $500\Omega$ fixed resistor or through a $1k\Omega$ gain adjustment potentiometer for D/A 1.
27	$V_{OUT\ 2}$	D/A 2 analog output.
28	$V_{OUT\ 1}$	D/A 1 analog output.

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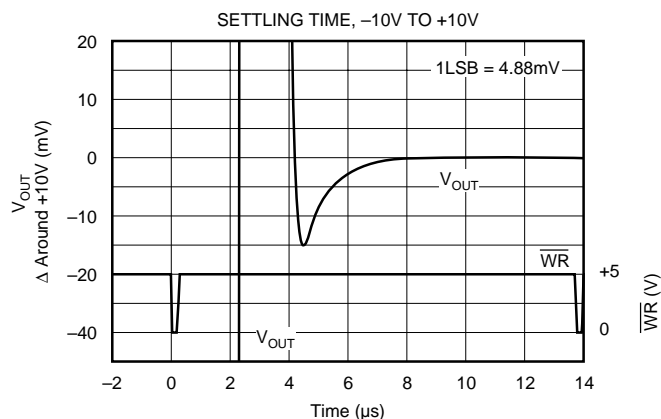
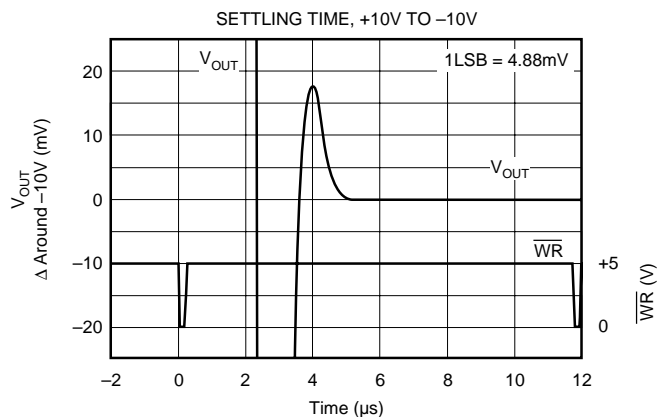
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{V}$ , unless otherwise noted.



## TYPICAL PERFORMANCE CURVES (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = \pm 15\text{V}$ , unless otherwise noted.



## DISCUSSION OF SPECIFICATIONS

### LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points (digital inputs all “1s” and all “0s”). DAC2813 linearity error is  $\pm 1/2\text{LSB}$  max at  $+25^\circ\text{C}$ .

### DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from a 1LSB output change from one adjacent state to the next. A DLE specification of  $1/2\text{LSB}$  means that the output step size can range from  $1/2\text{LSB}$  to  $3/2\text{LSB}$  when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than  $-1\text{LSB}$ , the D/A is said to be monotonic.

### MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. DAC2813 is monotonic over their specification temperature range  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

### DRIFT

*Gain Drift* is a measure of the change in the Full Scale Range (FSR) output over the specification temperature range. Gain Drift is expressed in parts per million per degree Celsius (ppm/ $^\circ\text{C}$ ).

*Bipolar Zero Drift* is measured with a data input of  $800_{\text{HEX}}$ . The D/A is configured for bipolar output. Bipolar Zero Drift is expressed in parts per million of Full Scale Range per degree Celsius (ppm of FSR/ $^\circ\text{C}$ ).

### SETTLING TIME

Settling Time is the total time (including slew time) for the output to settle to within an error band around its final value after a change in input. Settling times are specified to  $\pm 0.01\%$  of Full Scale Range (FSR) for two conditions: one for a FSR output change of 20V ( $25\text{k}\Omega$  feedback) and one for a 1LSB change. The 1LSB change is measured at the Major Carry ( $7\text{FF}_{\text{HEX}}$  to  $800_{\text{HEX}}$ , and  $800_{\text{HEX}}$  to  $7\text{FF}_{\text{HEX}}$ ), the input code transition at which worst-case settling time occurs.

## OPERATION

### INTERFACE LOGIC

The bus interface logic of the DAC2813 consists of two independently addressable latches in two ranks for each D/A converter. The first rank consists of one 12-bit input latch which can be loaded directly from a 12- or 16-bit microprocessor/microcontroller bus. The input latch holds data temporarily before it is loaded into the second latch, the D/A latch. This double buffered organization permits simultaneous update of all D/As.

All latches are level-triggered. Data present when the control signals are logic “0” will enter the latch. When the control signals return to logic “1”, the data is latched.

**CAUTION:** DAC2813 was designed to use  $\overline{WR}$  as the fast strobe.  $\overline{WR}$  has a much faster logic path than  $\overline{EN}_x$  (or LDAC). Therefore, if one permanently wires  $\overline{WR}$  to DCOM and uses only  $\overline{EN}_x$  to strobe data into the latches, the DATA

HOLD time will be long, approximately 20ns to 30ns and this time will vary considerably in this range from unit to unit. DATA HOLD time using  $\overline{WR}$  is 5ns max.

## RESET FUNCTION

The Reset function resets only the D/A latch. Therefore, after a RESET, good data must be written to **all** the input latches before an  $\overline{LDAC} - \overline{WR}$  command is issued. Otherwise, old data or unknown data is present in the input latches and will be transferred to the D/A latch producing an analog output value that may be unwanted.

## LOGIC INPUT COMPATIBILITY

DAC2813 digital inputs are TTL compatible (1.4V switching level) over the operating range of  $+V_{CC}$ . Each input has low leakage and high input impedance. Thus the inputs are suitable for being driven by any type of 5V logic. An equivalent circuit of a digital input is shown in Figure 1.

Open DATA input lines will float to 7V or more. Although this will not harm the DAC2813, current spikes will occur in the input lines when a logic 0 is asserted and, in addition, the speed of the interface will be slower. A digital output driving a DATA input line of the DAC2813 must not drive, **or let the DATA input float**, above +5.5V. Unused DATA inputs should be connected to DCOM.

Unused CONTROL inputs should be connected to a voltage greater than +2V but not greater than +5.5V. If this voltage is not available, the control inputs can be connected to  $+V_{CC}$  through a 100k $\Omega$  resistor to limit the input current.

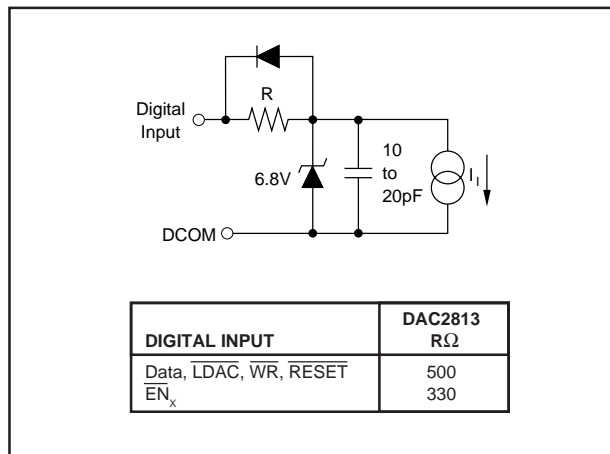


FIGURE 1. Equivalent Digital Input Circuit.

## INPUT CODING

DAC2813 accepts positive-true binary input codes. Input coding for bipolar analog outputs is Bipolar Offset Binary (BOB), where an input code of 000<sub>HEX</sub> gives a minus full-scale output, an input of FFF<sub>HEX</sub> gives an output 1LSB below positive full scale, and zero occurs for an input code of 800<sub>HEX</sub>.

DAC2813 can be used with two's complement coding if a logic inverter is used ahead of the MSB input (DB11).

DAC2813 can be connected for 0 to +10V unipolar operation by using the BPO resistors, plus a 100 $\Omega$  series resistor, in parallel with the internal feedback resistor. In this case, an input code of 000<sub>HEX</sub> gives zero volt output, an input of FFF<sub>HEX</sub> gives an output 1LSB below positive full scale.

## INTERNAL/EXTERNAL REFERENCE USE

DAC2813 contains a +10V  $\pm 50$ mV voltage reference,  $V_{REF}$ .  $V_{REF OUT}$  is available to drive external loads sourcing up to 2mA. The load current should be constant, otherwise the gain (and bipolar offset, if connected) of the D/A converters will vary.

For DAC2813  $V_{REF OUT}$  must be connected to  $V_{REF IN 1}$  and  $V_{REF IN 2}$  through gain adjust resistors with a nominal value of 500 $\Omega$ . Trim potentiometers with a nominal value of 1000 $\Omega$  can be used to provide adjustment to zero gain error.

It is possible to use references other than +10V. The recommended range of reference voltage is from +8V to +11V, which allows both 8.192V and 10.24V ranges to be used. However, DAC2813 is optimized for fixed-reference applications. If the reference voltage is expected to time-vary over a wide range, a CMOS multiplying D/A is a better choice.

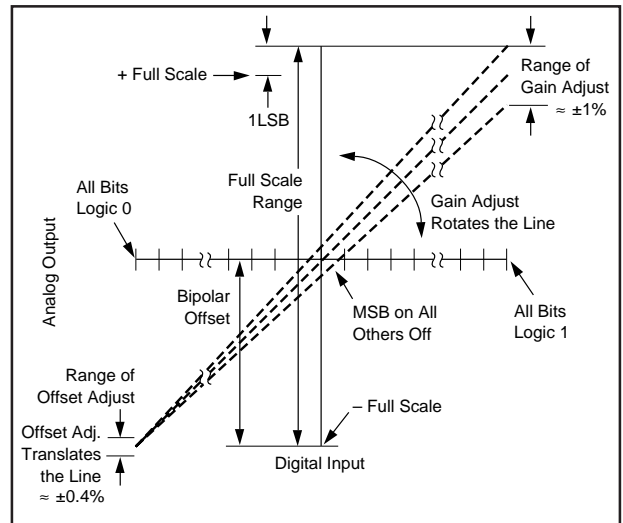


FIGURE 2. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

DIGITAL INPUT	ANALOG OUTPUT	
	UNIPOLAR 0 TO +10V	BIPOLAR $\pm 10$ V
FFF <sub>HEX</sub>	+9.9976V	+9.9951V
800 <sub>HEX</sub>	+5.0000V	0.0000V
7FF <sub>HEX</sub>	+4.9976V	-0.0049V
000 <sub>HEX</sub>	0.0000V	-10.0000V
1LSB	2.44mV	4.88mV

TABLE III. Analog Output Calibration Values.

## GAIN AND OFFSET ADJUSTMENTS

Figure 2 illustrates the relationship of offset and gain adjustments to a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments.

### Offset Adjustment

For bipolar analog output operation, apply digital input code  $000_{\text{HEX}}$  to produce the maximum negative output and adjust the offset potentiometer for  $-10.000\text{V}$ . See Table III for calibration values and codes.

### Gain Adjustment

For either unipolar or bipolar operation, apply digital input code  $FFF_{\text{HEX}}$  gives the maximum positive voltage output. Adjust the gain potentiometer for this positive full scale voltage. See Table III for calibration values.

## INSTALLATION

### POWER SUPPLY CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best settling time performance occurs using a 1 to  $10\mu\text{F}$  tantalum capacitor at  $-V_{\text{CC}}$ . Applications with less critical settling time may be able to use  $0.01\mu\text{F}$  at  $-V_{\text{CC}}$  as well as at  $+V_{\text{CC}}$ . The capacitors should be located close to the package.

DAC2813 features separate digital and analog power supply returns to permit optimum connections for low noise and high speed performance. It is recommended that both DIGITAL COMMON (DCOM) and ANALOG COMMON

(ACOM) be connected directly to a ground plane under the package. If a ground plane is not used, connect the ACOM and DCOM pins together close to the package. Since the reference point for  $V_{\text{OUT}}$  and  $V_{\text{REF OUT}}$  is the ACOM pin, it is also important to connect the load directly to the ACOM pin. The change in current in the ACOM pin due to an input data word change from  $000_{\text{HEX}}$  to  $FFF_{\text{HEX}}$  is only  $1\text{mA}$  for each D/A converter.

### OUTPUT VOLTAGE SWING AND RANGE CONNECTIONS

DAC2813 output amplifiers provide a  $\pm 10\text{V}$  output swing while operating on supplies as low as  $\pm 12\text{V} \pm 5\%$ .

DAC2813 is internally connected to provide  $\pm 10\text{V}$  output when the bipolar offset pins BPO1 and/or BPO2 are connected, through  $100\Omega$  resistors, to  $V_{\text{REF OUT}}$ . For a unipolar 0 to  $+10\text{V}$  output, the BPO resistor, in series with a  $100\Omega$  external resistor, may be paralleled with the internal feedback resistor to provide the correct scaling. The internal feedback resistors ( $25\text{k}\Omega$ ) and the bipolar offset resistor ( $24.9\text{k}\Omega$ ) are trimmed to an absolute tolerance of  $\pm 2\%$ .

### 12- AND 16-BIT BUS INTERFACES

DAC2813 data is latched into the input latches of each D/A by asserting low each  $\text{EN}_x$  individually and transferring the data from the bus to each input latch by asserting  $\text{WR}$  low. All D/A outputs in each package are then updated simultaneously by asserting  $\text{LDAC}$  and  $\text{WR}$  low. Be sure and read the CAUTION statement in the LOGIC INPUT COMPATIBILITY section.

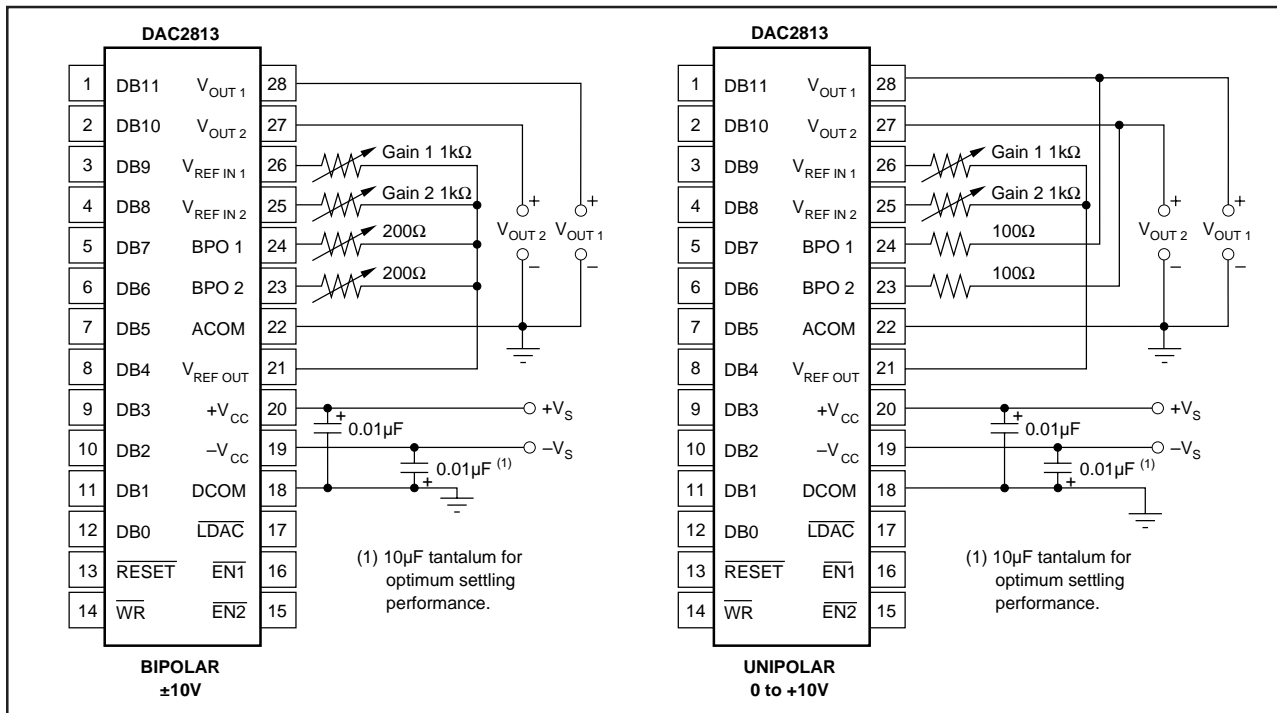


FIGURE 3. DAC2813 Power Supply, Output Range, Gain and Offset Adjust Connections. Unipolar output connected DAC2813s have Gain Adjust only.



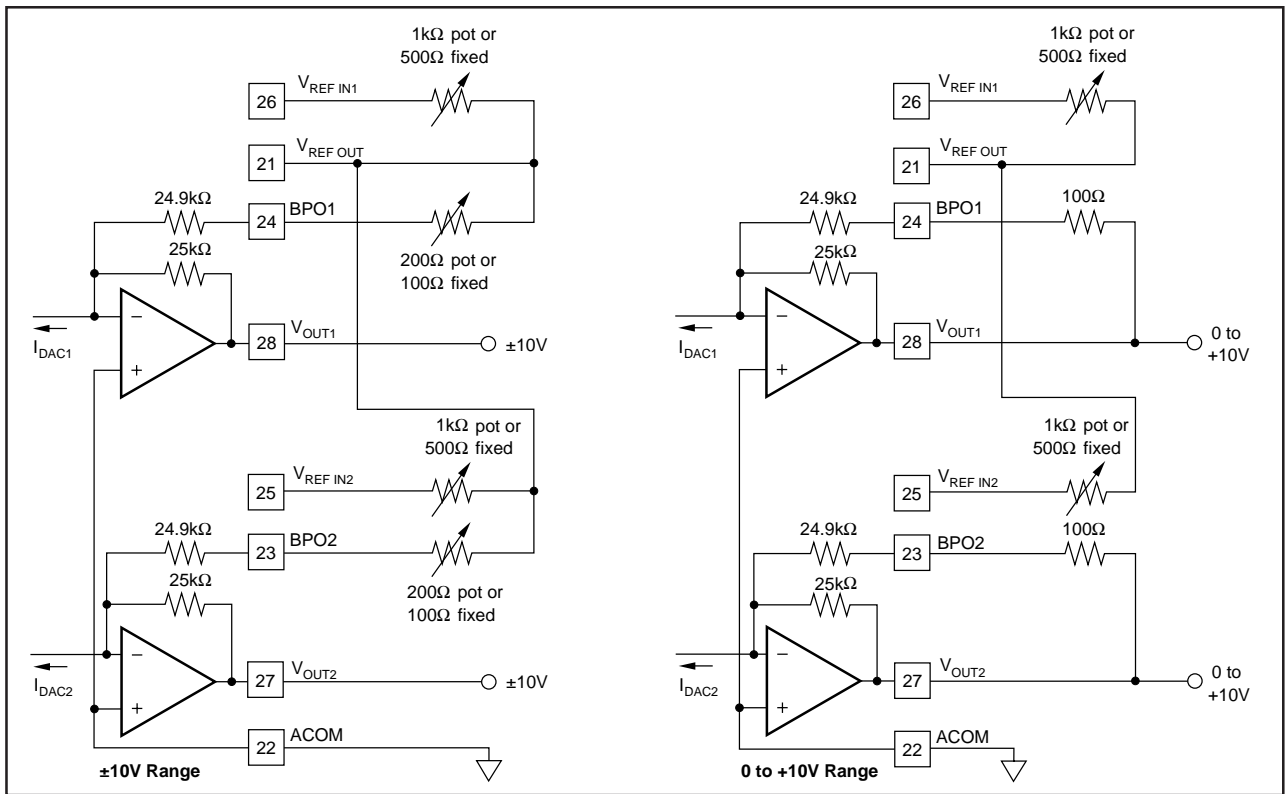


FIGURE 4. DAC2813 Output Amplifier Range Connections.

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- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
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- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



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