# KAF-09000

# 3056 (H) x 3056 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

### Description

Combining high resolution with outstanding sensitivity, the KAF−09000 image sensor has been specifically designed to meet the needs of next−generation low cost digital radiography and scientific imaging systems. The high sensitivity available from 12−micron square pixels combines with a low noise architecture to allow system designers to improve overall image quality, or to relax system tolerances to achieve lower cost. The excellent uniformity of the KAF−09000 image sensor improves overall image integrity by simplifying image corrections, while integrated anti−blooming protection prevents image bleed from over−exposure in bright areas of the image. To simplify device integration, the KAF−09000 image sensor uses the same pin−out and package as the KAF−16801 image sensor.

The sensor utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front−side illuminated polysilicon electrode.

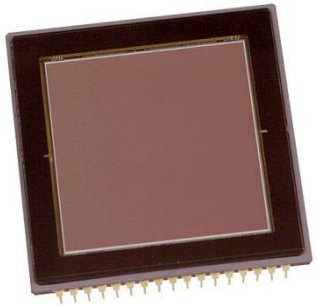


**Figure 1. KAF−09000 CCD Image Sensor**

**Table 1. GENERAL SPECIFICATIONS**

| Parameter | Typical Value |
|---|---|
| Architecture | Full Frame CCD [Square Pixels] |
| Total Number of Pixels | 3103 (H) x 3086 (V) = 9.6 Mp |
| Number of Effective Pixels | 3085 (H) x 3085 (V) = 9.5 Mp |
| Number of Active Pixels | 3056 (H) x 3056 (V) = 9.3 Mp |
| Pixel Size | 12 μm (H) x 12 μm (V) |
| Active Image Size | 36.7 mm (H) x 36.7 mm (V)<br>51.9 mm diagonal,<br>645 1.3x optical format |
| Aspect Ratio | Square |
| Horizontal Outputs | 1 |
| Saturation Signal | 110 ke$^-$ |
| Output Sensitivity | 24 μV/e$^-$ |
| Quantum Efficiency (550 nm) | 64% |
| Responsivity (550 nm) | 2595 ke/μJ/cm$^2$<br>62.3 V/μJ/cm$^2$ |
| Read Noise (f = 3 MHz) | 7 e$^-$ |
| Dark Signal (T = 25°C) | 5 e/pix/sec |
| Dark Current Doubling Temperature | 7°C |
| Linear Dynamic Range (f = 4 MHz) | 84 dB |
| Blooming Protection<br>(4 ms exposure time) | > 100 X saturation exposure |
| Maximum Data Rate | 10 MHz |
| Package | CERDIP, (sidebrazed pins, CuW) |
| Cover Glass | AR coated 2 sides Taped Clear |

NOTE: Parameters above are specified at T = 25°C unless otherwise noted.

### Features

- TRUESENSE Transparent Gate Electrode for High Sensitivity
- Large Pixel Size
- Large Image Area
- High Quantum Efficiency
- Low Noise Architecture
- Broad Dynamic Range

### Applications

- Medical
- Scientific

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

## ORDERING INFORMATION

**Table 2. ORDERING INFORMATION**

| Part Number | Description | Marking Code |
|---|---|---|
| KAF−09000−ABA−DP−BA | Monochrome, Microlens, CERDIP Package, (sidebrazed, CuW), Taped clear coverglass, Standard grade | KAF−09000−ABA [Serial Number] |
| KAF−09000−ABA−DP−AE | Monochrome, Microlens, CERDIP Package, (sidebrazed, CuW), Taped clear coverglass, Engineering sample | |
| KAF−09000−ABA−DD−BA | Monochrome, Microlens, CERDIP Package, (sidebrazed, CuW), AR coated 2 sides, Standard grade | |
| KAF−09000−ABA−DD−AE | Monochrome, Microlens, CERDIP Package, (sidebrazed, CuW), AR coated 2 sides, Engineering sample | |

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

## DEVICE DESCRIPTION

### Architecture

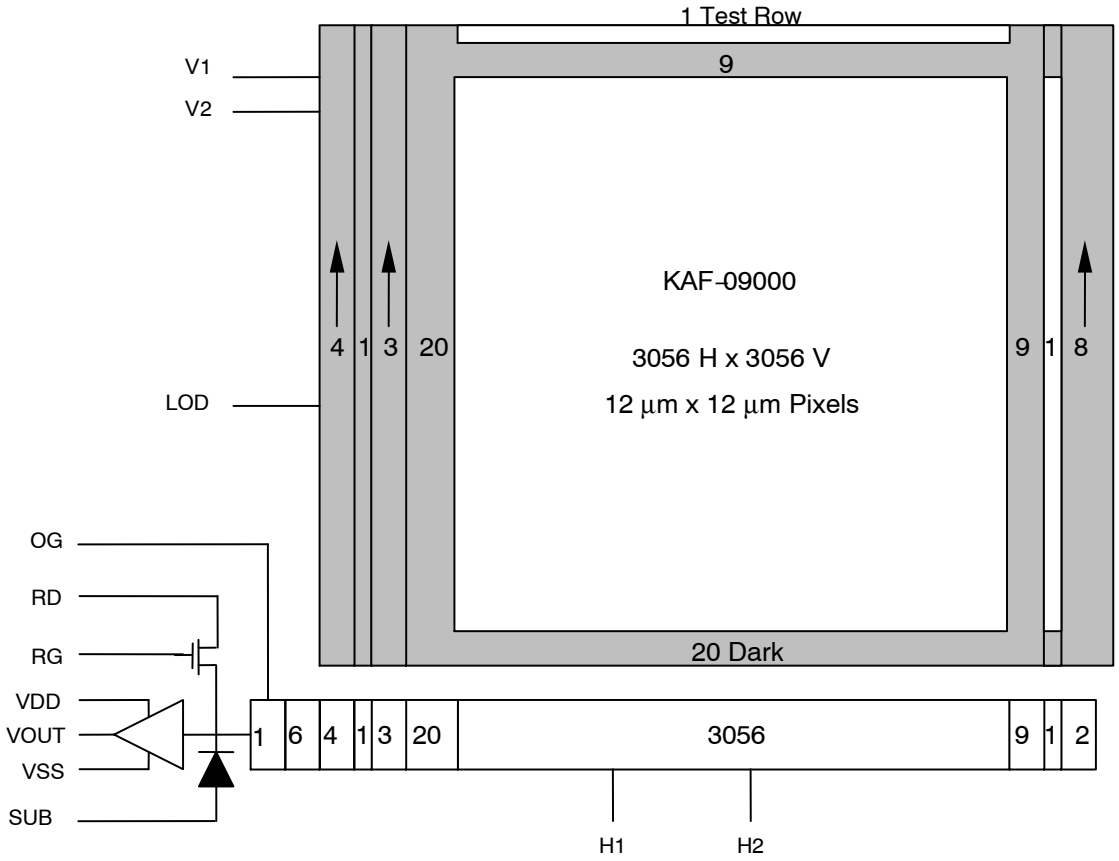



**Figure 2. Block Diagram**

### Dark Reference Pixels

The periphery of the device is surrounded with a border of light shielded pixels creating a dark region. Within this dark region, there are 20 leading dark pixels on every line as well as 20 full dark lines at the start and 9 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

### Dummy Pixels

Within each horizontal shift register there are 14 leading pixels and 3 trailing pixels. These are designated as dummy pixels and should not be used to determine a dark reference level.

### Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron−hole pairs within the device. These photon−induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non−linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

### Charge Transport

The integrated charge from each pixel is transported to the output using a two−step process. Each line (row) of charge is first transported from the vertical CCDs to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion.

## HORIZONTAL REGISTER

### Output Structure

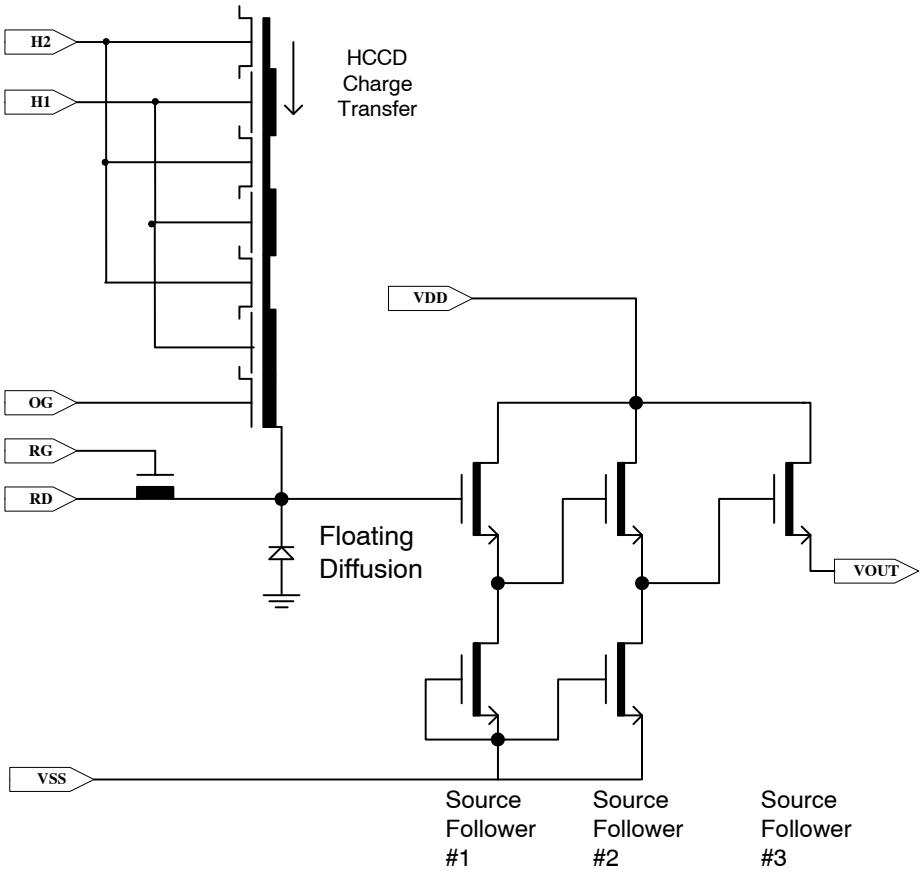
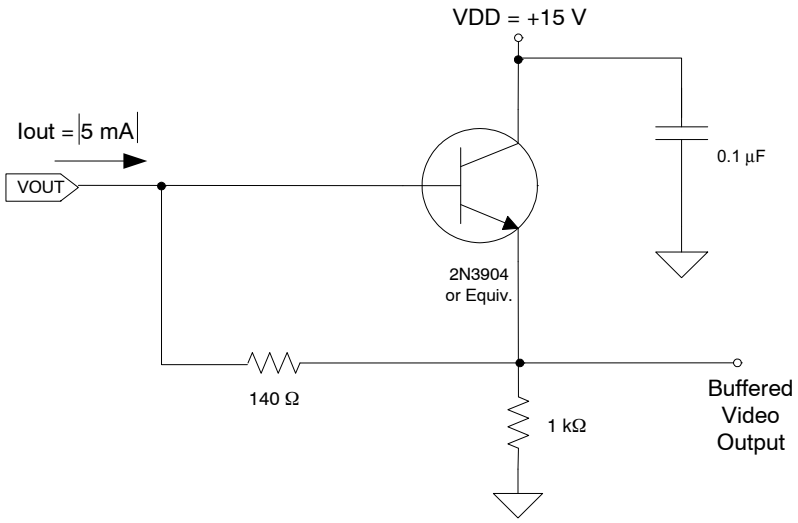



**Figure 3. Output Architecture (Left or Right)**

The output consists of a floating diffusion capacitance connected to a three−stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off−chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off−chip current source must be added to the VOUT pin of the device. See Figure 4.

**Output Load**

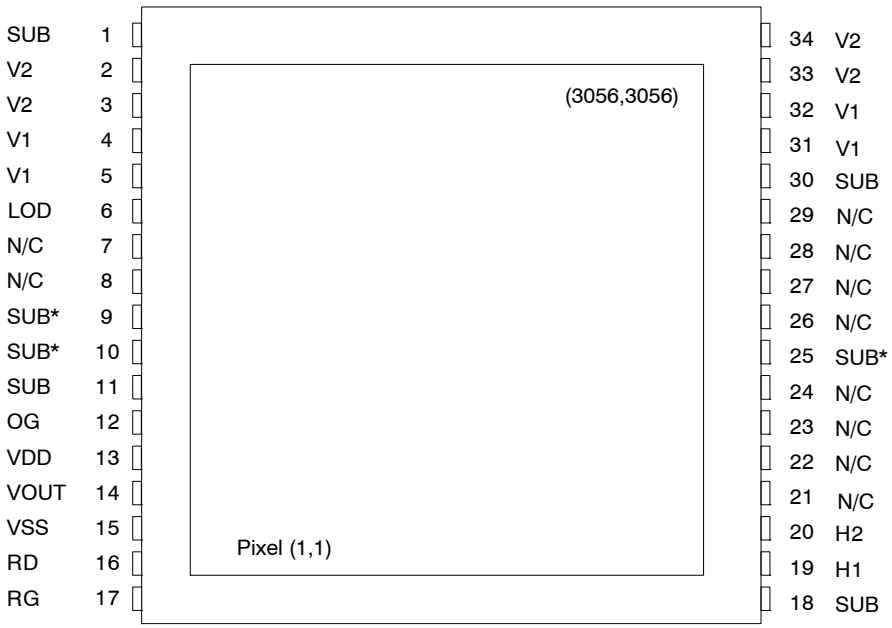



Note: Component values may be revised based on operating conditions and other design considerations.

**Figure 4. Recommended Output Structure Load Diagram**

## PHYSICAL DESCRIPTION

### Pin Description and Device Orientation




Notes: 1. Pins with the same name are to be tied together on the circuit board and have the same timing.
2. Unlike the KAF−16801, pins 9, 10, and, 25 are internally connected to SUB. They may be connected to SUB on the printed circuit board or may be left floating.

**Figure 5. Pinout Diagram**

**Table 3. PIN DESCRIPTION**

| Pin | Name | Description |
|---|---|---|
| 1 | SUB | Substrate |
| 2 | V2 | Vertical CCD Clock − Phase 2 |
| 3 | V2 | Vertical CCD Clock − Phase 2 |
| 4 | V1 | Vertical CCD Clock − Phase 1 |
| 5 | V1 | Vertical CCD Clock − Phase 1 |
| 6 | LOD | Anti Blooming Drain |
| 7 | N/C | No Connection |
| 8 | N/C | No Connection |
| 9 | SUB* | No Connection |
| 10 | SUB* | No Connection |
| 11 | SUB | Substrate |
| 12 | OG | Output Gate |
| 13 | VDD | Output Amplifier Supply |
| 14 | VOUT | Video Output |
| 15 | VSS | Output Amplifier Return |
| 16 | RD | Reset Drain |
| 17 | RG | Reset Gate |
| 18 | SUB | Substrate |
| 19 | H1 | Horizontal Phase 1 |
| 20 | H2 | Horizontal Phase 2 |
| 21 | N/C | No Connection |
| 22 | N/C | No Connection |
| 23 | N/C | No Connection |
| 24 | N/C | No Connection |
| 25 | SUB* | No Connection |
| 26 | N/C | No Connection |
| 27 | N/C | No Connection |
| 28 | N/C | No Connection |
| 29 | N/C | No Connection |
| 30 | SUB | Substrate |
| 31 | V1 | Vertical CCD Clock − Phase 1 |
| 32 | V1 | Vertical CCD Clock − Phase 1 |
| 33 | V2 | Vertical CCD Clock − Phase 2 |
| 34 | V2 | Vertical CCD Clock − Phase 2 |

*Unlike the KAF−16801, pins 9, 10, and, 25 are internally connected to SUB. They may be connected to SUB on the printed circuit board or must be left floating.

## IMAGING PERFORMANCE

### Table 4. TYPICAL OPERATIONAL CONDITIONS

| Description | Condition − Unless otherwise noted | Notes |
|---|---|---|
| Read out time treadout | 2533 ms | Includes over clock pixels |
| Integration time (tint) | variable | |
| Horizontal clock frequency | 4 MHz | |
| Temperature | 25°C | Room temperature |
| Mode | integrate − readout cycle | |
| Operation | Nominal operating voltages and timing with min. vertical pulse width tVw = 20 μs | |

### Table 5. SPECIFICATIONS

| Description | Symbol | Min. | Nom. | Max. | Units | Notes | Verification Plan |
|---|---|---|---|---|---|---|---|
| Saturation Signal | $Ne^-_{sat}$ | 95k | 110k | | $e^-$ | | die[11] |
| Quantum Efficiency (550 nm) | QE | | 64 | | % | 1 | design[12] |
| Photo Response Non−Linearity | PRNL | | 1 | | % | 2 | design[12] |
| Photo Response Non−Uniformity | PRNU | | 0.5 | 2.5 | % | 3 | die[11] |
| Integration Dark Signal | Vdark, int | | 5 | 20 | e/pix/sec | 4 | die[11] |
| | | | 0.6 | 2.8 | $pA/cm^2$ | | |
| Read out Dark Signal | Vdark, read | | 80 | 320 | electrons | 5 | die[11] |
| Dark Signal Non−Uniformity | DSNU | | | 20 | e/pix/sec | 6 | die[11] |
| Dark Signal Doubling Temperature | ΔT | | 7 | | °C | | design[12] |
| Read Noise | NR | | 7 | 14 | $e^-$ rms | 7 | design[12] |
| Linear Dynamic Range | DR | | 84 | | dB | 8 | design[12] |
| Blooming Protection | Xab | 100 | | | x Vsat | 9 | design[12] |
| Output Amplifier Sensitivity | $Vout/Ne^-$ | | 24 | | μV/e | | design[12] |
| DC Offset, output amplifier | Vodc | Vrd−4 | Vrd−2.0 | | V | 10 | die[11] |
| Output Amplifier Bandwidth | $f_{-3dB}$ | | 88 | | MHz | | design[12] |
| Output Impedance, Amplifier | ROUT | | 150 | 250 | Ω | | die[11] |

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst case deviation from straight line fit, between 1% and 90% of Vsat.
3. One Sigma deviation of a 128 x 128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25°C.
5. Read out dark current depends on the read out time, primarily when the vertical CCD clocks are at their high levels. This is approximately 0.125 sec/image for nominal timing conditions, tVw = 20 μs. The read out dark current will increase as tVw is increased. The readout dark current is also dependent on the operating temperature. The specification applies to 25°C.
6. Average integration dark signal of any of 32 x 32 blocks within the sensor. (each block is 128 x 128 pixels)
7. Output amplifier noise only. Operating at pixel frequency up to 4 MHz, bandwidth <20 MHz, tint = 0, and no dark current shot noise.
8. 20log (Vsat/VN)
9. Xab is the number of times above the Vsat illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. Xab is measured at 4 ms.
10. Video level offset with respect to ground.
11. A parameter that is measured on every sensor during production testing.
12. A parameter that is quantified during the design verification activity.

## TYPICAL PERFORMANCE CURVES (QE)

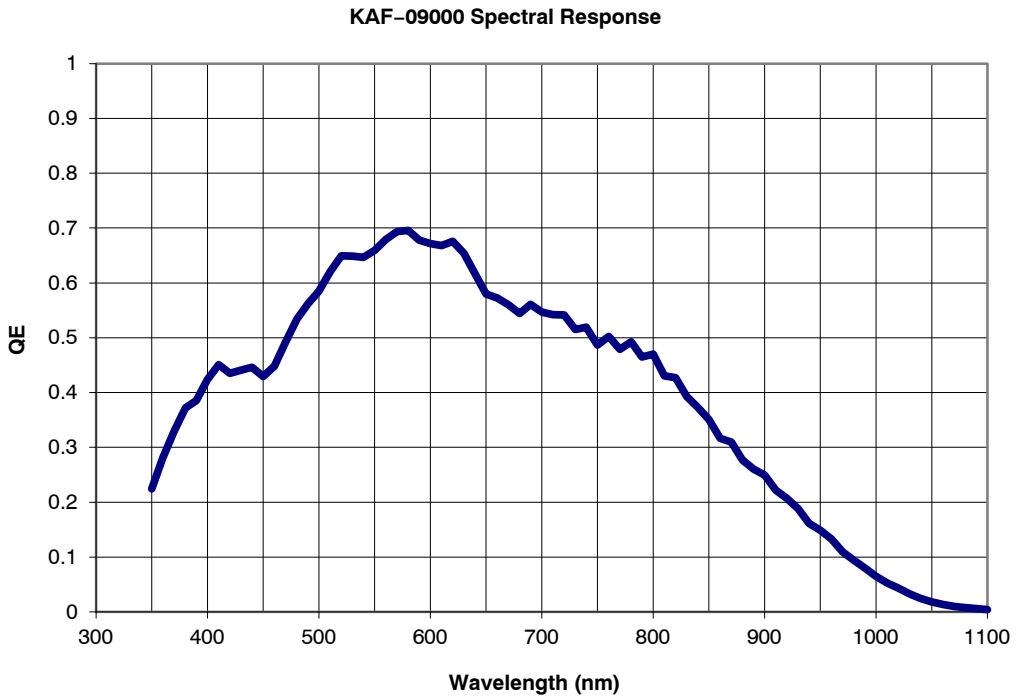



**Figure 6. Typical Spectral Response**

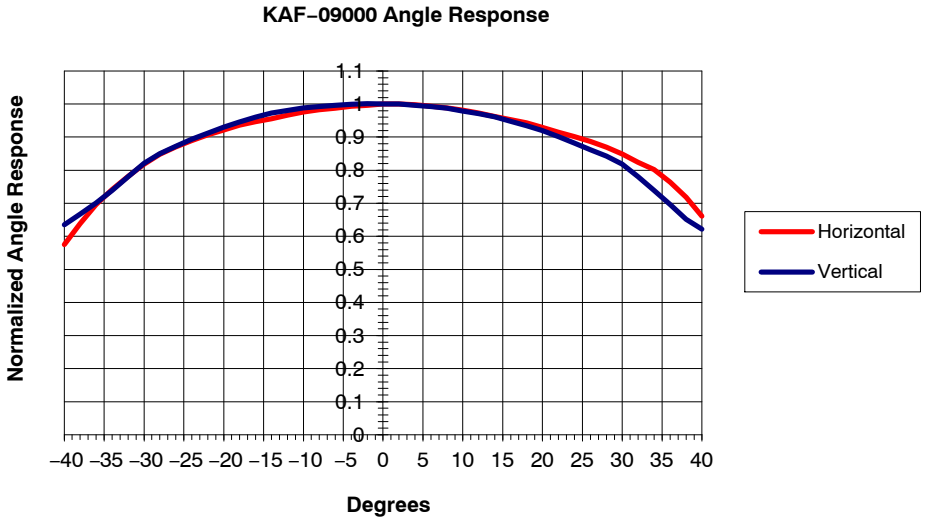



**Figure 7. Typical Angle Response**

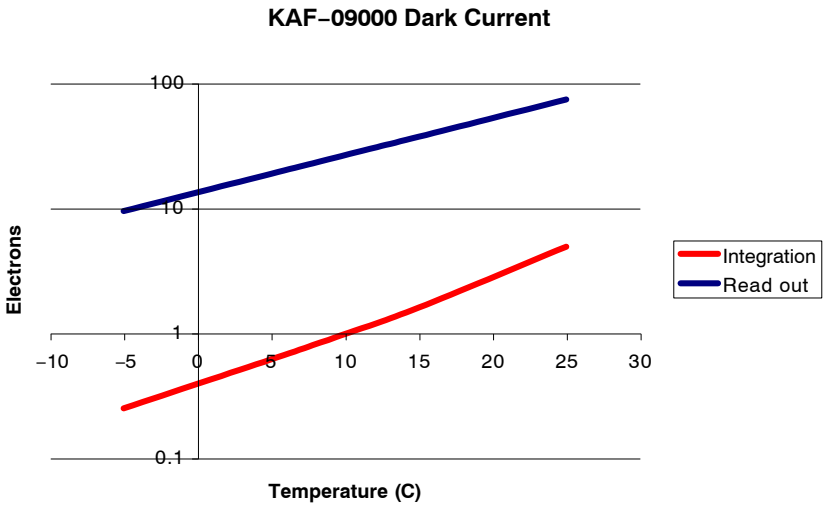



**Figure 8. Dark Current**

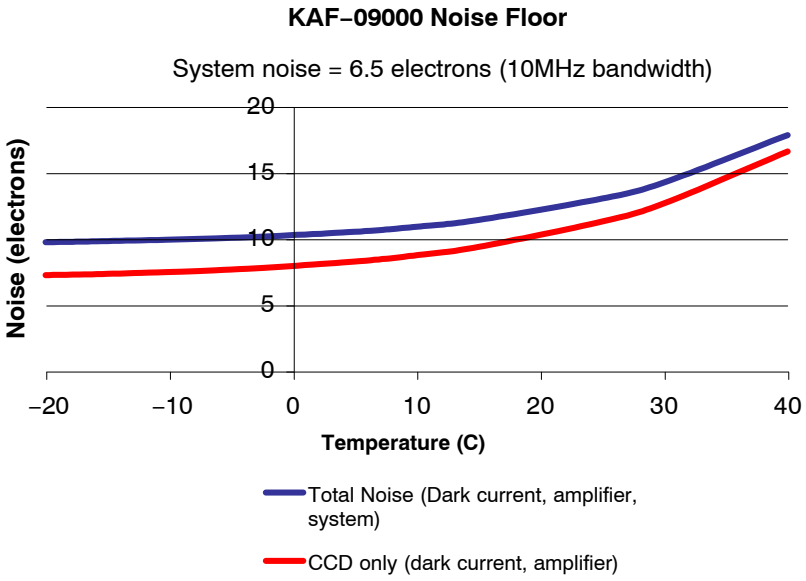



**Figure 9. Noise Floor**

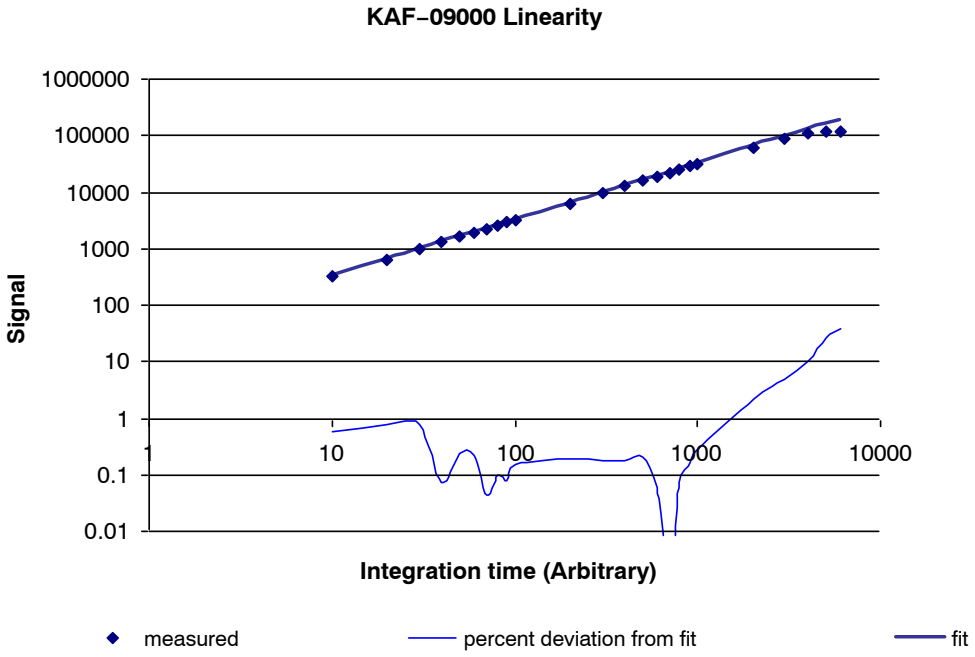



**Figure 10. Linearity**

## DEFECT DEFINITIONS

### Operating Conditions

All cosmetic tests performed at approximately 25°C.

**Table 6. SPECIFICATIONS**

| Classification | Points | Clusters | Columns | Includes Dead Columns |
|---|---|---|---|---|
| Standard Grade | < 200 | < 20 | < 10 | yes |

*Point Defects*

Dark: A pixel, which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation

−or−

Bright: A Pixel with dark current > 3,000 e/pixel/sec at 25°C

*Cluster Defect*

A grouping of not more than 10 adjacent point defects

Cluster defects are separated by no less than 4 good pixels in any direction

*Column Defect*

A grouping of more than 10 point defects along a single column

−or−

A column containing a pixel with dark current > 15,000 e/pixel/sec (bright column)

−or−

A column that does not meet the CTE specification for all exposures less than the specified Max sat. signal level and greater than 2 $ke^-$

A pixel, which loses more than 250 $e^-$ under 2 $ke^-$ illumination (trap defect)

Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

## OPERATION

### Table 7. ABSOLUTE MAXIMUM RATINGS

| Description | Symbol | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|---|
| Diode Pin Voltages | $V_{diode}$ | −0.5 | +20 | V | 1, 2 |
| Adjacent Gate Pin Voltages | $V_{gate1}$ | −18 | +18 | V | 1, 3 |
| Isolated Gate Pin Voltages | $V_{1-2}$ | −0.5 | +20 | V | 4 |
| Output Bias Current | $I_{out}$ | | −30 | mA | 5 |
| LOD Diode Voltage | $V_{LOD}$ | −0.5 | −13.0 | V | 6 |
| Operating Temperature | $T_{OP}$ | −60 | 60 | °C | 7 |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin SUB
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H2, VOG.
4. Includes pins: RG.
5. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity). Operation at these values will reduce MTTF.
6. V1, H1, V2, H2, H1L, VOG, and RD are tied to 0 V.
7. Noise performance will degrade at higher temperatures due to the temperature dependence of the dark current.
8. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time. If the level or condition is exceeded, the device will be degraded and may be damaged.

### Power−up Sequence

The sequence chosen to perform an initial power−up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (SUB).
2. Supply the appropriate biases and clocks to the remaining pins.

### Table 8. DC BIAS OPERATING CONDITIONS

| Description | Symbol | Minimum | Nominal | Maximum | Units | Maximum DC Current (mA) | Notes |
|---|---|---|---|---|---|---|---|
| Reset Drain | $V_{RD}$ | 12.8 | 13 | 13.2 | V | $I_{RD}$ = 0.01 | |
| Output Amplifier Supply | $V_{SS}$ | 1.8 | 2.0 | 2.2 | V | $I_{SS}$ = 3.0 | |
| Output Amplifier Return | $V_{DD}$ | 14.8 | 15.0 | 17.0 | V | $I_{OUT}$ + $I_{SS}$ | |
| Substrate | $V_{SUB}$ | | 0 | | V | 0.01 | |
| Output Gate | $V_{OG}$ | 0 | 1 | 2 | V | 0.01 | |
| Lateral Overflow Drain | $V_{LOD}$ | 7.8 | 8.0 | 9.0 | V | 0.01 | |
| Video Output Current | $I_{OUT}$ | −3 | −5 | −7 | mA | | 1 |

1. An output load sink must be applied to VOUT to activate output amplifier − see Figure 4.

### AC Operating Conditions

### Table 9. CLOCK LEVELS

| Description | Symbol | Level | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| V1 Low Level | V1L | Low | −9.5 | −9.0 | −8.5 | V | 1 |
| V1 High Level | V1H | High | 2.3 | 2.5 | 2.7 | V | 1 |
| V2 Low Level | V2L | Low | −9.5 | −9.0 | −8.5 | V | 1 |
| V2 High Level | V2H | High | 2.3 | 2.5 | 2.7 | V | 1 |
| H1 Low Level | H1L | Low | −2.5 | −2 | −1.7 | V | 1 |
| H1 High Level | H1H | High | 7.5 | 8 | 8.2 | V | 1 |

1. All pins draw less than 10 μA DC current. Capacitance values relative to SUB (substrate).

**Table 9. CLOCK LEVELS**

| Description | Symbol | Level | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| H2 Low Level | H2L | Low | −2.5 | −2 | −1.7 | V | 1 |
| H2 High Level | H2H | High | 7.5 | 8 | 8.2 | V | 1 |
| RG Low Level | RGL | Low | 5.3 | 5.5 | 5.7 | V | 1 |
| RG High Level | RGH | High | 11.2 | 11 | 10.8 | V | 1 |

1. All pins draw less than 10 μA DC current. Capacitance values relative to SUB (substrate).

### Capacitance Equivalent Circuit

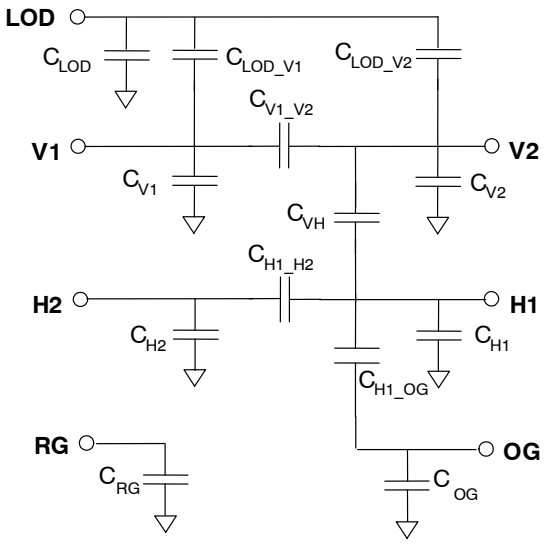



**Figure 11. Equivalent Circuit Model**

**Table 10.**

| Description | Label | Value | Unit |
|---|---|---|---|
| LOD−Sub Capacitance | $C_{LOD}$ | 6.5 | nF |
| LOD−V1 Capacitance | $C_{LOD\_V1}$ | 36 | nF |
| LOD−V2 Capacitance | $C_{LOD\_V2}$ | 36 | nF |
| V1−V2 Capacitance | $C_{V1\_V2}$ | 80 | nF |
| V1−Sub Capacitance | $C_{V1\_SUB}$ | 250 | nF |
| V2−Sub Capacitance | $C_{V2\_SUB}$ | 250 | nF |
| V2−H1 Capacitance | $C_{VH}$ | 36 | pF |
| H1−H2 Capacitance | $C_{H1\_H2}$ | 75 | pF |
| H1−Sub Capacitance | $C_{H1\_Sub}$ | 500 | pF |
| H2−Sub Capacitance | $C_{H2\_Sub}$ | 300 | pF |
| OG−Sub Capacitance | $C_{OG\_Sub}$ | 5 | pF |
| RG−Sub Capacitance | $C_{RG\_Sub}$ | 13 | pF |

## TIMING

**Table 11. REQUIREMENTS AND CHARACTERISTICS**

| Description | Symbol | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| H1, H2 Clock Frequency | $f_H$ | | 4 | 10 | MHz | 1 |
| H1, H2 Rise, Fall Times | $t_{H1r}$, $t_{H1f}$ | 5 | | | % | 3 |
| V1, V2 Rise, Fall Times | $t_{V1r}$, $t_{V1f}$ | 5 | | | % | 3 |
| V1 − V2 Cross−over | $V_{VCR}$ | −1 | 0 | 1 | V | |
| H1 − H2 Cross−over | $V_{HCR}$ | 2 | 3 | 5 | V | |
| H1, H2 Setup Time | $t_{HS}$ | 5 | 10 | | μs | |
| RG Clock Pulse Width | $t_{RGw}$ | 5 | 10 | | ns | 4 |
| V1, V2 Clock Pulse Width | $t_{Vw}$ | 20 | 20 | | μs | |
| Pixel Period (1 Count) | $t_e$ | | 250 | | ns | 2 |
| Readout Time | $t_{readout}$ | | 2,533 | | ms | 7 |
| Integration Time | $t_{int}$ | | | | | 5 |
| Line Time | $t_{line}$ | | 0.821 | | ms | 6 |

1. 50% duty cycle values.
2. CTE will degrade above the maximum frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration time is user specified.
6. $(3103 * t_e) + t_{HS} + (2 * t_{Vw}) = 0.821$ msec
7. $t_{readout} = t_{line} * 3086$ lines

### Edge Alignment

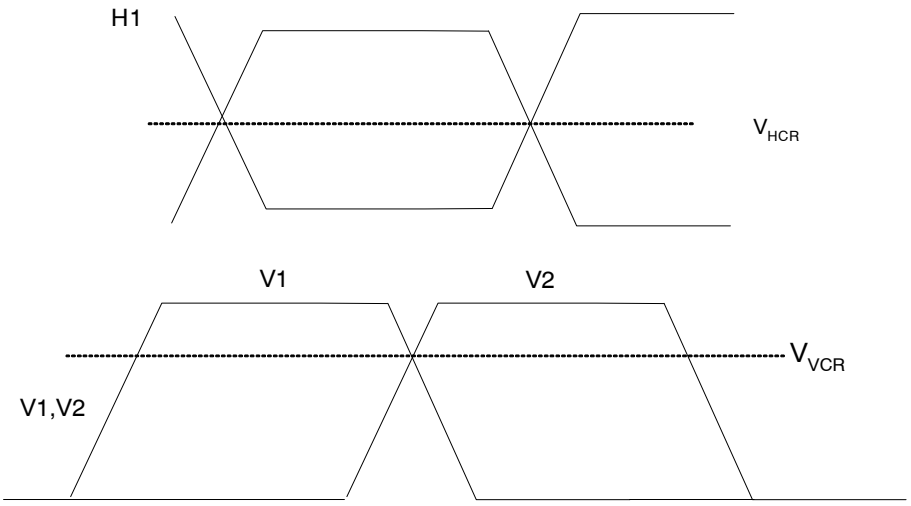



**Figure 12. Timing Edge Alignment**

### Frame Timing

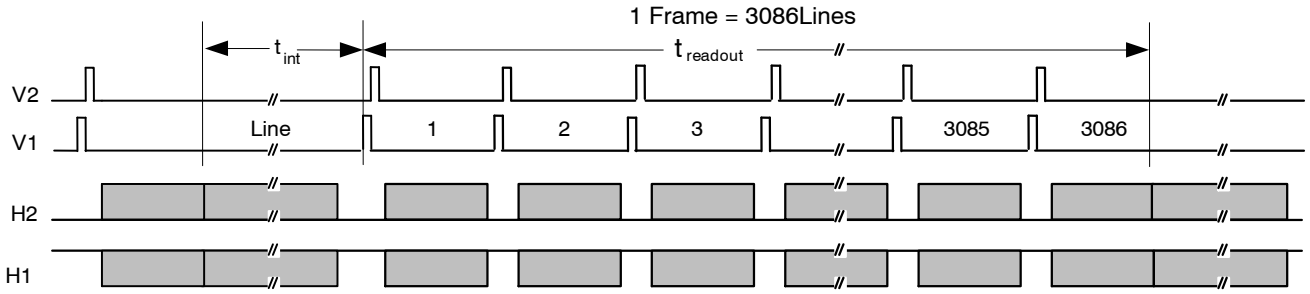



**Figure 13. Frame Timing**

### Frame Timing Detail

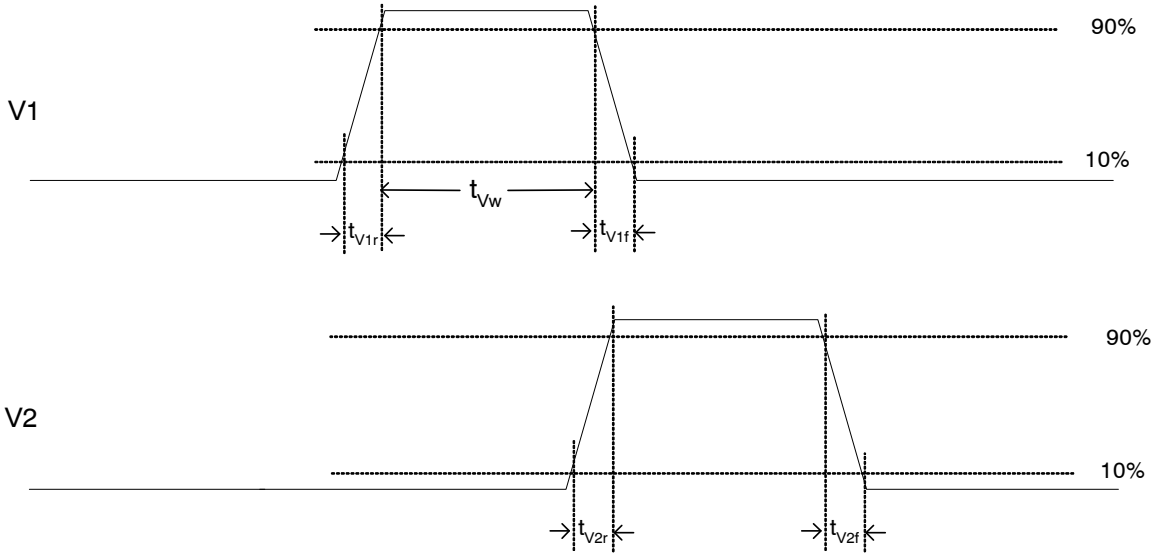



**Figure 14. Frame Timing Detail**

### Line Timing

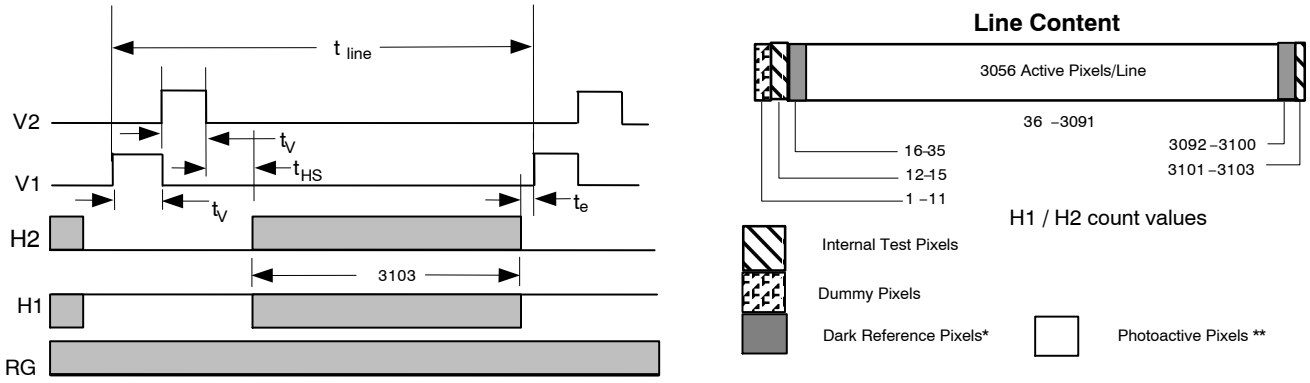



**Figure 15. Line Timing**

### Pixel Timing

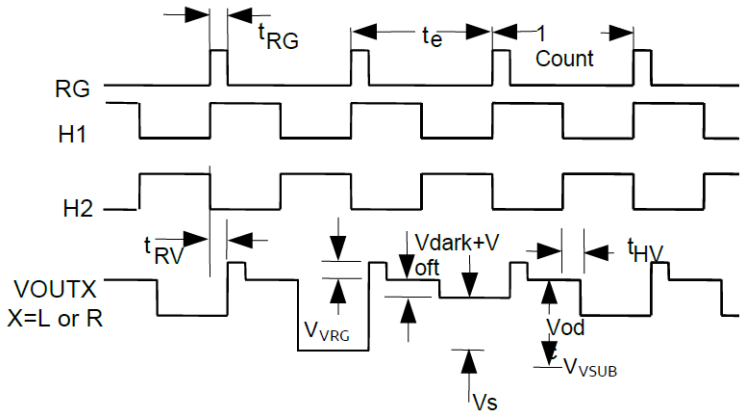



**Figure 16. Pixel Timing**

### Pixel Timing Detail

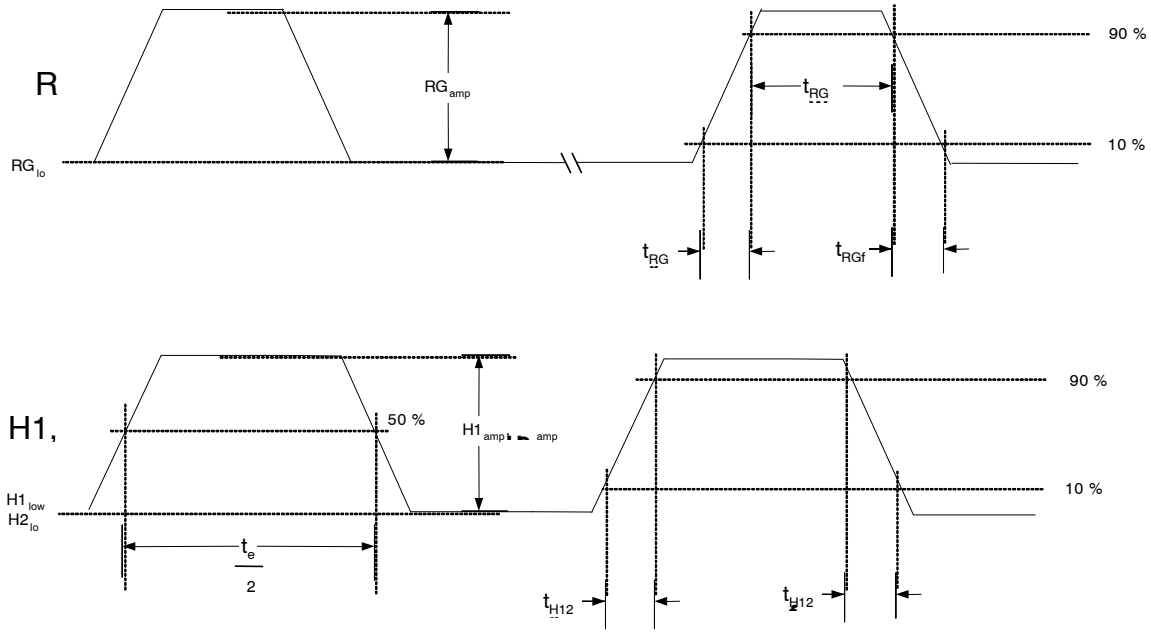



**Figure 17. Pixel Timing Detail**

### Example Waveforms

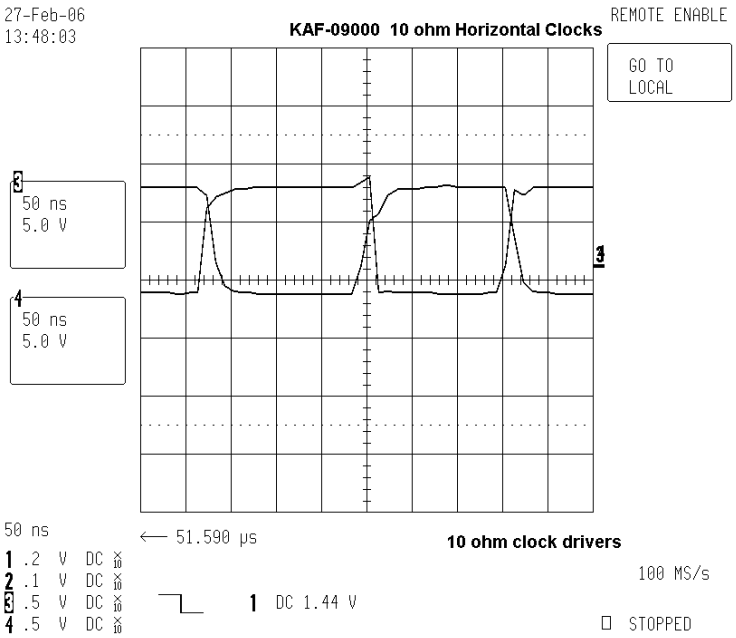



**Figure 18. Horizontal Clocks**

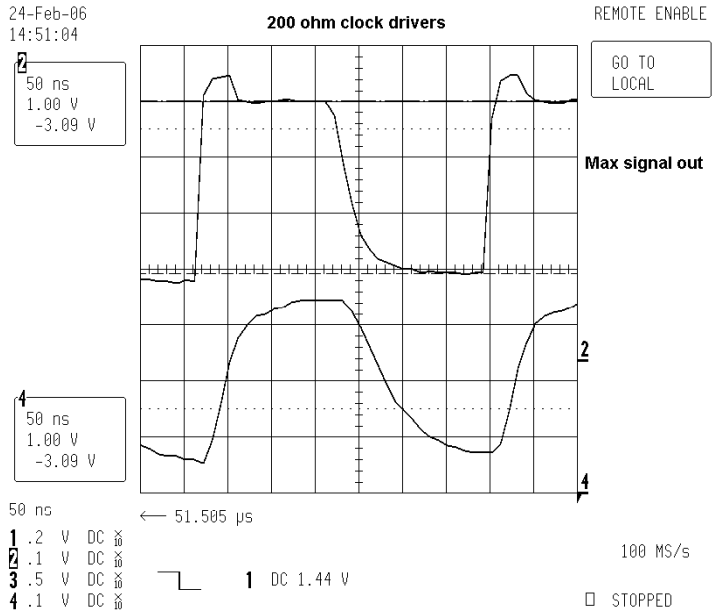



**Figure 19. Video Waveform**

NOTE: The upper waveform was taken at the CCD output and the lower waveform was taken at the analog to digital converter, and is bandwidth limited.

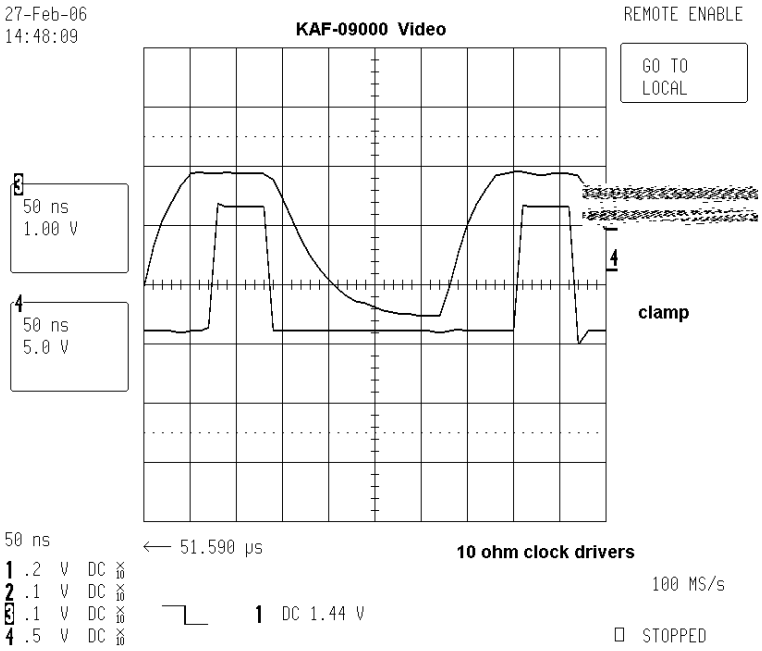



**Figure 20. Video Waveform and Clamp Clock**

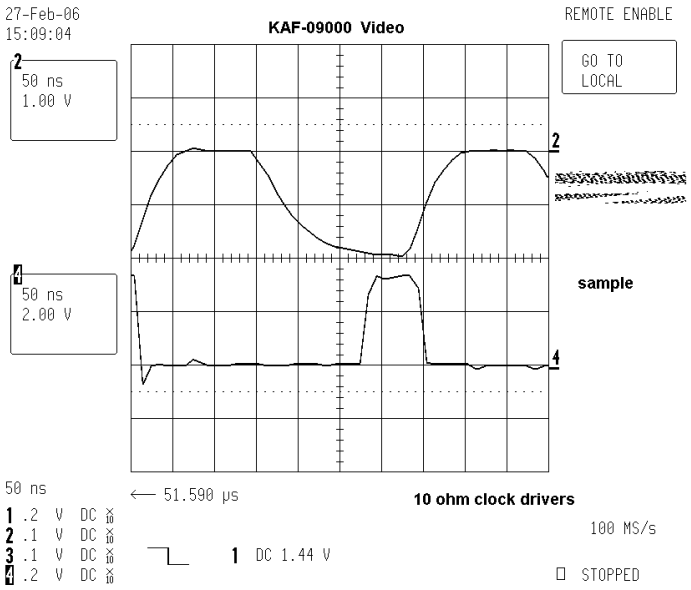



**Figure 21. Video Waveform and Sample Clock**

## STORAGE AND HANDLING

**Table 12. STORAGE CONDITIONS**

| Description | Symbol | Minimum | Maximum | Units | Notes |
|---|---|---|---|---|---|
| Storage Temperature | $T_{ST}$ | −20 | 70 | °C | 1 |

1. Long term storage toward the maximum temperature will accelerate color filter degradation.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

## MECHANICAL INFORMATION

### Completed Assembly

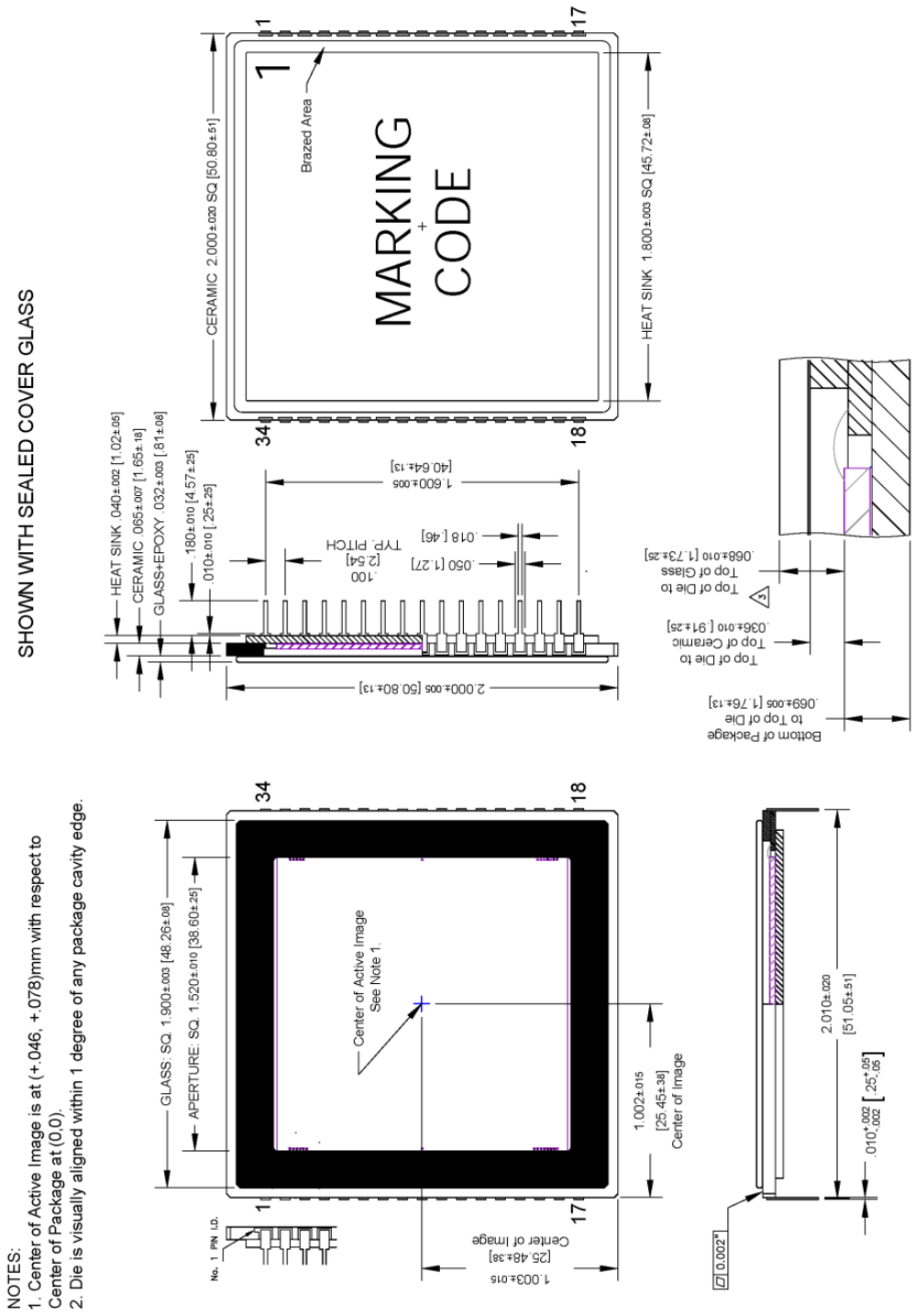



**Figure 22. Completed Assembly (1 of 1)**

### Cover Glass Specification

MAR Glass for Sealed Cover

1. Scratch and dig: 10 micron max
2. Substrate material Schott D263T eco or equivalent
3. Multilayer anti−reflective coating

**Table 13.**

| Wavelength | Total Reflectance |
|---|---|
| 420 – 450 | 2% |
| 450 – 630 | 1% |
| 630 – 680 | 2% |



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