

## 2.5V/3.3V, 500 MHz Twelve 2-to-1 Differential LVPECL Clock Multiplexer

### Features

- Pin-to-pin compatible to ICS85352I
- $F_{MAX} \leq 500$  MHz
- Propagation Delay  $< 4$  ns
- Output-to-output skew  $< 100$  ps
- 12 pairs of differential LVPECL outputs
- Selectable differential CLK and /CLK inputs
- CLK, /CLK pair accepts LVDS, LVPECL, LVHSTL, SSTL and HCSL input level
- Select input accept CMOS/LVTTL levels
- 2.5V/3.3V power supply
- Operating Temperature:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Packaging (Pb-free & Green):
  - 48-pin TQFP (FA)

### Description

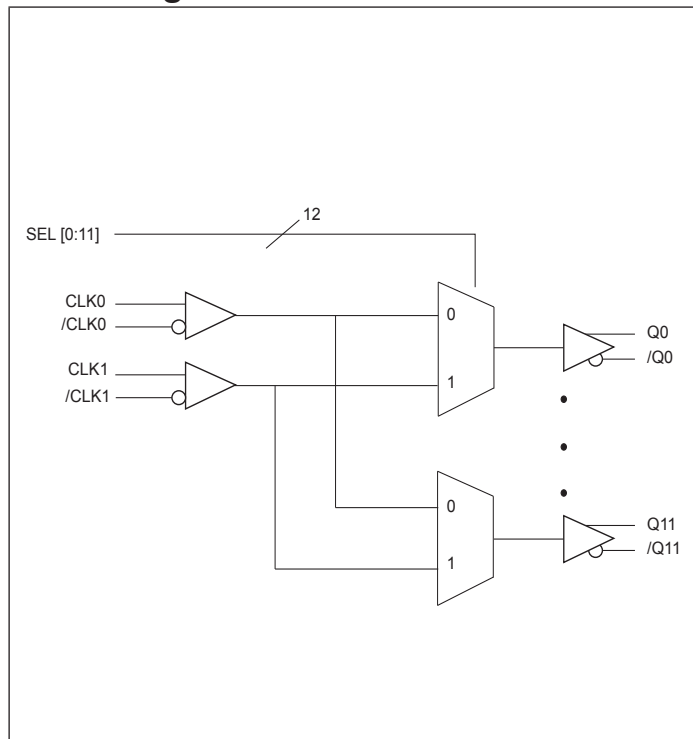
The PI6C485352 is a high-performance low-skew LVPECL fanout buffer. PI6C485352 features two selectable differential inputs and translates to twelve LVPECL output pairs. The inputs can also be configured to single-ended with external resistor bias circuit. The CLK input accepts LVPECL, LVDS, LVHSTL, SSTL or HCSL signals. The PI6C485352 is ideal for differential to LVPECL translations and/or LVPECL clock distribution.

Typical clock translation and distribution applications are data-communications and telecommunications.

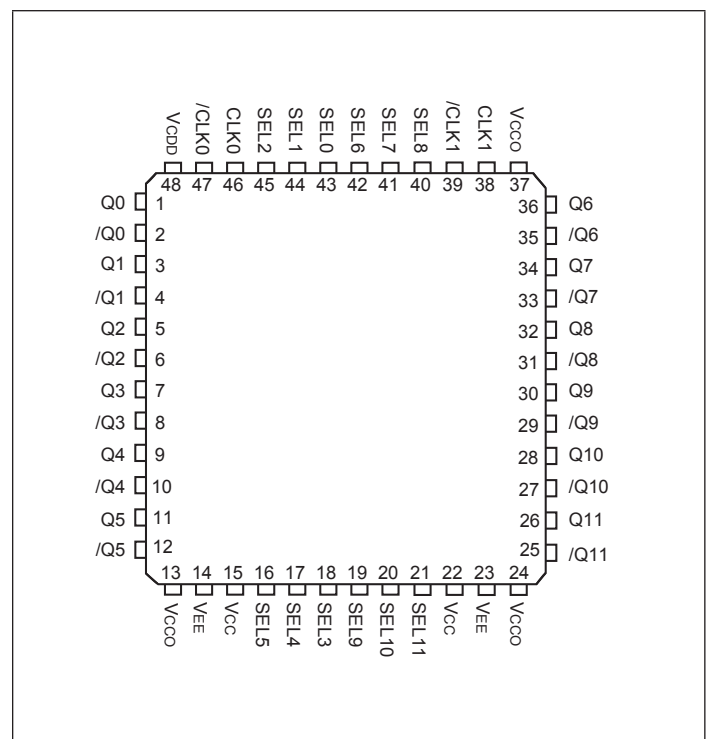
### Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

### Block Diagram



### Pin Configuration (48-Pin TQFP)



### Pinout Table

Pin #	Pin Name	Type	Description
1, 2	Q0, /Q0	Output	Differential LVPECL Output pairs. LVPECL interface levels
3, 4	Q1, /Q1		
5, 6	Q2, /Q2		
7, 8	Q3, /Q3		
9, 10	Q4, /Q4		
11, 12	Q5, /Q5		
25, 26	/Q11, Q11		
27, 28	/Q10, Q10		
29, 30	/Q9, Q9		
31, 32	/Q8, Q8		
33, 34	/Q7, Q7		
35, 36	/Q6, Q6		
13, 24	V <sub>CCO</sub>	Power	Output supply pins
37, 48			Ground pins
14, 23			V <sub>EE</sub>
15, 22	V <sub>CC</sub>		
16, 17	SEL5, SEL4,	Pulldown	Clock select inputs. LVCMOS/LVTTL interface levels
18, 19	SEL3, SEL9,		
20, 21	SEL10, SEL11,		
40, 41	SEL8, SEL7,		
42, 43	SEL6, SEL0,		
44, 45	SEL1, SEL2		
38	CLK1	Pulldown	Non-inverting differential clock input
39	/CLK1	Pullup/Pulldown	Inverting differential clock input
46	CLK0	Pulldown	Non-inverting differential clock input
47	/CLK0	Pullup/Pulldown	Inverting differential clock input

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$V_{CC}/V_{CC0}$	Supply Voltage	Referenced to GND			4.6	V
$V_{IN}$	Input voltage	Referenced to GND	-0.5		$V_{CC}+0.5V$	
Outputs, $I_O$	Surge current				100	mA
TSTG	Storage temperature		-65		150	°C
$\theta_{jA}$	Package thermal impedance				73	°C/W

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Pin Characteristics**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
$C_{IN}$	Input Capacitance				4	pF
$R_{pullup}$	Input Pullup Resistance			50		k $\Omega$
$R_{pulldown}$	Input Pulldown Resistance			50		k $\Omega$

**Control Input Function Table**

SELX	Selected Clock Inputs
0	CLK0, /CLK0
1	CLK1, /CLK1

### Operating Conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V <sub>CC</sub>	Power Supply Voltage		3.0	3.3	3.6	V
V <sub>CCO</sub>	Output Power Supply Voltage		2.375		3.6	V
T <sub>A</sub>	Ambient Temperature		-40		85	°C
I <sub>EE</sub>	Power Supply Current				200	mA

### LVCMOS/LVTTL DC Characteristics (T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 3.3V ±10%, V<sub>CCO</sub> = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V <sub>IH</sub>	Input High voltage	SEL0:SEL11	2		V <sub>CC</sub> +0.3	V
V <sub>IL</sub>	Input Low voltage	SEL0:SEL11	-0.3		0.8	
I <sub>IH</sub>	Input High current	SEL0:SEL11	V <sub>IN</sub> = V <sub>CC</sub> = 3.6V		150	μA
I <sub>IL</sub>	Input Low current	SEL0:SEL11	V <sub>IN</sub> = 0V, V <sub>CC</sub> = 3.6V		-5	μA

### Differential DC Characteristics (T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 3.3V ±10%, V<sub>CCO</sub> = 2.5V ±5% to 3.3V ±10%)

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
I <sub>IH</sub>	Input High Current	CLK0, CLK1	V <sub>IN</sub> = V <sub>CC</sub> = 3.6V		150	μA
		/CLK0, /CLK1	V <sub>IN</sub> = V <sub>CC</sub> = 3.6V		150	μA
I <sub>IL</sub>	Input Low Current	CLK0, CLK1	V <sub>CC</sub> = 3.6V, V <sub>IN</sub> = 0V	-5		μA
		/CLK0, /CLK1	V <sub>CC</sub> = 3.6V, V <sub>IN</sub> = 0V	-150		μA
V <sub>PP</sub>	Peak-to-peak Voltage		0.15		1.3	V
V <sub>CMR</sub>	Common Mode Input Voltage <sup>(1)</sup>		V <sub>EE</sub> +0.5		V <sub>CC</sub> -0.85V	V
V <sub>OH</sub>	Output High Voltage <sup>(2)</sup>	V <sub>CCO</sub> = 3.3V or 2.5V	V <sub>CCO</sub> -1.4		V <sub>CCO</sub> -0.9	V
V <sub>OL</sub>	Output Low Voltage <sup>(2)</sup>	V <sub>CCO</sub> = 3.3V or 2.5V	V <sub>CCO</sub> -2.0		V <sub>CCO</sub> -1.7	V

Note:

1. Outputs terminated with 50Ω to V<sub>CCO</sub> -2.0V

**AC Characteristics** (TA = -40°C to +85°C, VCC = 3.3V ±10%, VCCO = 2.5V ±5% to 3.3V ±10%)

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
fmax	Output Frequency				500	MHz
tpd	Propagation Delay <sup>(1)</sup>				4	ns
Tsk	Output-to-output Skew <sup>(2)</sup>				100	ps
Tskpp	Part-to-part Skew <sup>(3)</sup>				500	ps
tr/tf	Output Rise/Fall time	20% - 80%	150		700	ps
odc	Output duty cycle		45		55	%
Tj	Buffer additive jitter RMS			0.05		ps

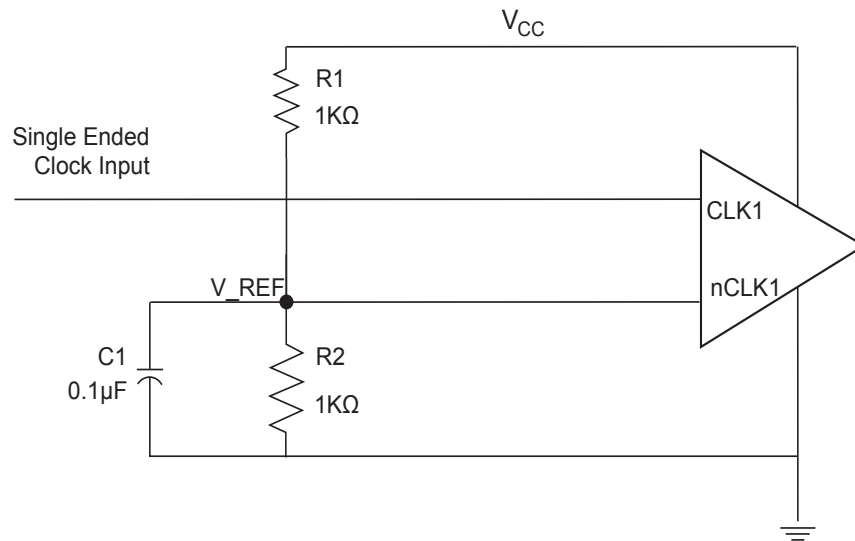
Note:

1. Measured from the differential input to the differential output crossing point
2. Defined as skew between outputs at the same supply voltage and with equal loads. Measured at the output differential crossing point.
3. Defined as skew between outputs on different parts operating at the same supply voltage and with equal loads. Measured at the outputs differential crossing point.

**Applications Information**

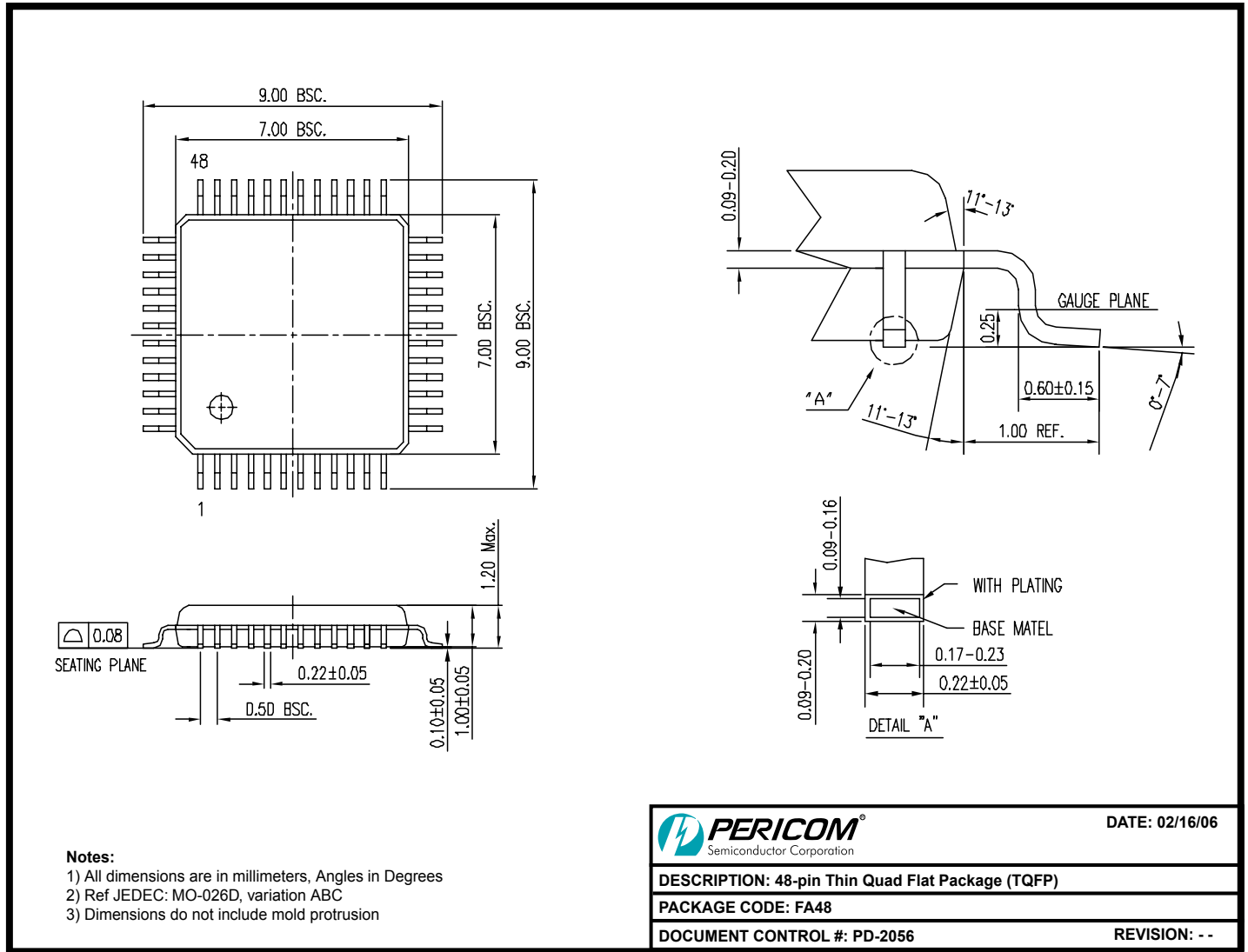
*Wiring the differential input to accept single ended levels*

Figure 1 shows how the differential input can be wired to accept single-ended levels. The reference voltage  $V_{REF} = V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be placed as close as possible to the input pin. The ratio of R1 and R2 should be adjusted to position the  $V_{REF}$  at the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R1/R2 = 0.609$ .



**Figure 1: Single-ended Signal Driving Differential Input**

**Packaging Mechanical: 48-Pin TQFP (FA)**



06-0182

**Ordering Information**

Ordering Number	Package Code	Package Description
PI6C485352FAE	FA	Pb-free & Green, 48-pin, 276-mil wide TQFP

- Thermal characteristics can be found on the company web site at [www.pericom.com/packaging/](http://www.pericom.com/packaging/)
- E = Pb-free and Green
- X suffix = Tape/Reel

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