

# CAT93C46

## 1 kb Microwire Serial EEPROM

### Description

The CAT93C46 is a 1 kb Serial EEPROM memory device which is configured as either 64 registers of 16 bits (ORG pin at  $V_{CC}$ ) or 128 registers of 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C46 features a self-timed internal write with auto-clear. On-chip Power-On Reset circuit protects the internal logic against powering up in the wrong state.

### Features

- High Speed Operation: 4 MHz (5 V), 2 MHz (1.8 V)
- 1.8 V (1.65 V\*) to 5.5 V Supply Voltage Range
- Selectable x8 or x16 Memory Organization
- Self-Timed Write Cycle with Auto-Clear
- Sequential Read (New Product)
- Software Write Protection
- Power-up Inadvertant Write Protection
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Ranges
- 8-pin PDIP, SOIC, TSSOP and 8-pad UDFN and TDFN Packages
- This Device is Pb-Free, Halogen Free/BFR Free and RoHS Compliant†

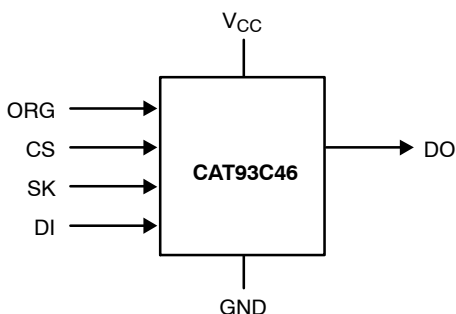


Figure 1. Functional Symbol

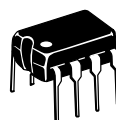
\*CAT93C46xx-xxL ( $T_A = -20^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

†For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

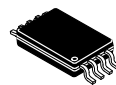


ON Semiconductor®

<http://onsemi.com>



PDIP-8  
L SUFFIX  
CASE 646AA



TSSOP-8  
Y SUFFIX  
CASE 948AL



SOIC-8  
V, W\*\* SUFFIX  
CASE 751BD



SOIC-8  
X SUFFIX  
CASE 751BE

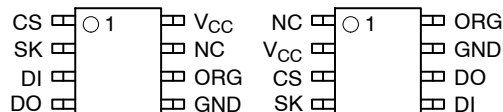


UDFN-8  
HU4 SUFFIX  
CASE 517AZ



TDFN-8\*\*  
VP2 SUFFIX  
CASE 511AK

### PIN CONFIGURATIONS



PDIP (L), SOIC (V, X),  
TSSOP (Y), UDFN (HU4),  
TDFN (VP2)\*\*  
(Top View)

SOIC (W)\*\*  
(Top View)

\*\* Not recommended for new designs.

### PIN FUNCTION

| Pin Name | Function            |
|----------|---------------------|
| CS       | Chip Select         |
| SK       | Clock Input         |
| DI       | Serial Data Input   |
| DO       | Serial Data Output  |
| $V_{CC}$ | Power Supply        |
| GND      | Ground              |
| ORG      | Memory Organization |
| NC       | No Connection       |

Note: When the ORG pin is connected to  $V_{CC}$ , the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

# CAT93C46

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameter                                          | Value        | Units |
|----------------------------------------------------|--------------|-------|
| Storage Temperature                                | -65 to +150  | °C    |
| Voltage on Any Pin with Respect to Ground (Note 1) | -0.5 to +6.5 | V     |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than -0.5 V or higher than  $V_{CC} + 0.5$  V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than  $V_{CC} + 1.5$  V, for periods of less than 20 ns.

**Table 2. RELIABILITY CHARACTERISTICS** (Note 2)

| Symbol             | Parameter      | Min       | Units                  |
|--------------------|----------------|-----------|------------------------|
| $N_{END}$ (Note 3) | Endurance      | 1,000,000 | Program / Erase Cycles |
| $T_{DR}$           | Data Retention | 100       | Years                  |

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Block Mode,  $V_{CC} = 5$  V, 25°C

**Table 3. D.C. OPERATING CHARACTERISTICS – MATURE PRODUCT (Not Recommended for New Designs)**

( $V_{CC} = +1.8$  V to +5.5 V,  $T_A = -40^{\circ}\text{C}$  to +85°C, unless otherwise specified.)

| Symbol    | Parameter                                 | Test Conditions                                                                            | Min                 | Max                 | Units |
|-----------|-------------------------------------------|--------------------------------------------------------------------------------------------|---------------------|---------------------|-------|
| $I_{CC1}$ | Power Supply Current (Write)              | $f_{SK} = 1$ MHz<br>$V_{CC} = 5.0$ V                                                       |                     | 1                   | mA    |
| $I_{CC2}$ | Power Supply Current (Read)               | $f_{SK} = 1$ MHz<br>$V_{CC} = 5.0$ V                                                       |                     | 500                 | μA    |
| $I_{SB1}$ | Power Supply Current (Standby) (x8 Mode)  | $V_{IN} = \text{GND or } V_{CC}$ ,<br>$CS = \text{GND}$<br>$ORG = \text{GND}$              |                     | 2                   | μA    |
| $I_{SB2}$ | Power Supply Current (Standby) (x16 Mode) | $V_{IN} = \text{GND or } V_{CC}$ ,<br>$CS = \text{GND}$<br>$ORG = \text{Float or } V_{CC}$ |                     | 1                   | μA    |
| $I_{LI}$  | Input Leakage Current                     | $V_{IN} = \text{GND to } V_{CC}$                                                           |                     | 1                   | μA    |
| $I_{LO}$  | Output Leakage Current                    | $V_{OUT} = \text{GND to } V_{CC}$ ,<br>$CS = \text{GND}$                                   |                     | 1                   | μA    |
| $V_{IL1}$ | Input Low Voltage                         | $4.5 \text{ V} \leq V_{CC} < 5.5 \text{ V}$                                                | -0.1                | 0.8                 | V     |
| $V_{IH1}$ | Input High Voltage                        | $4.5 \text{ V} \leq V_{CC} < 5.5 \text{ V}$                                                | 2                   | $V_{CC} + 1$        | V     |
| $V_{IL2}$ | Input Low Voltage                         | $1.8 \text{ V} \leq V_{CC} < 4.5 \text{ V}$                                                | 0                   | $V_{CC} \times 0.2$ | V     |
| $V_{IH2}$ | Input High Voltage                        | $1.8 \text{ V} \leq V_{CC} < 4.5 \text{ V}$                                                | $V_{CC} \times 0.7$ | $V_{CC} + 1$        | V     |
| $V_{OL1}$ | Output Low Voltage                        | $4.5 \text{ V} \leq V_{CC} < 5.5 \text{ V}$<br>$I_{OL} = 2.1 \text{ mA}$                   |                     | 0.4                 | V     |
| $V_{OH1}$ | Output High Voltage                       | $4.5 \text{ V} \leq V_{CC} < 5.5 \text{ V}$<br>$I_{OH} = -400 \text{ μA}$                  | 2.4                 |                     | V     |
| $V_{OL2}$ | Output Low Voltage                        | $1.8 \text{ V} \leq V_{CC} < 4.5 \text{ V}$<br>$I_{OL} = 1 \text{ mA}$                     |                     | 0.2                 | V     |
| $V_{OH2}$ | Output High Voltage                       | $1.8 \text{ V} \leq V_{CC} < 4.5 \text{ V}$<br>$I_{OH} = -100 \text{ μA}$                  | $V_{CC} - 0.2$      |                     | V     |

# CAT93C46

**Table 4. D.C. OPERATING CHARACTERISTICS – NEW PRODUCT (REV P)**

( $V_{CC} = +1.8\text{ V}$  to  $+5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +1.65\text{ V}$  to  $+5.5\text{ V}$ ,  $T_A = -20^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise specified.)

| Symbol    | Parameter                  | Test Conditions                                                                      | Min                                              | Max                 | Units         |
|-----------|----------------------------|--------------------------------------------------------------------------------------|--------------------------------------------------|---------------------|---------------|
| $I_{CC1}$ | Supply Current (Write)     | Write, $V_{CC} = 5.0\text{ V}$                                                       |                                                  | 1                   | mA            |
| $I_{CC2}$ | Supply Current (Read)      | Read, DO open, $f_{SK} = 2\text{ MHz}$ , $V_{CC} = 5.0\text{ V}$                     |                                                  | 500                 | $\mu\text{A}$ |
| $I_{SB1}$ | Standby Current (x8 Mode)  | $V_{IN} = \text{GND or } V_{CC}$<br>$CS = \text{GND, ORG} = \text{GND}$              | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$  | 2                   | $\mu\text{A}$ |
|           |                            |                                                                                      | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | 5                   |               |
| $I_{SB2}$ | Standby Current (x16 Mode) | $V_{IN} = \text{GND or } V_{CC}$<br>$CS = \text{GND, ORG} = \text{Float or } V_{CC}$ | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$  | 1                   | $\mu\text{A}$ |
|           |                            |                                                                                      | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | 3                   |               |
| $I_{LI}$  | Input Leakage Current      | $V_{IN} = \text{GND to } V_{CC}$                                                     | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$  | 1                   | $\mu\text{A}$ |
|           |                            |                                                                                      | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | 2                   |               |
| $I_{LO}$  | Output Leakage Current     | $V_{OUT} = \text{GND to } V_{CC}$<br>$CS = \text{GND}$                               | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$  | 1                   | $\mu\text{A}$ |
|           |                            |                                                                                      | $T_A = -40^\circ\text{C to } +125^\circ\text{C}$ | 2                   |               |
| $V_{IL1}$ | Input Low Voltage          | $4.5\text{ V} \leq V_{CC} < 5.5\text{ V}$                                            | -0.1                                             | 0.8                 | V             |
| $V_{IH1}$ | Input High Voltage         | $4.5\text{ V} \leq V_{CC} < 5.5\text{ V}$                                            | 2                                                | $V_{CC} + 1$        | V             |
| $V_{IL2}$ | Input Low Voltage          | $1.8\text{ V} \leq V_{CC} < 4.5\text{ V}$                                            | 0                                                | $V_{CC} \times 0.2$ | V             |
| $V_{IH2}$ | Input High Voltage         | $1.8\text{ V} \leq V_{CC} < 4.5\text{ V}$                                            | $V_{CC} \times 0.7$                              | $V_{CC} + 1$        | V             |
| $V_{OL1}$ | Output Low Voltage         | $4.5\text{ V} \leq V_{CC} < 5.5\text{ V}$ , $I_{OL} = 3\text{ mA}$                   |                                                  | 0.4                 | V             |
| $V_{OH1}$ | Output High Voltage        | $4.5\text{ V} \leq V_{CC} < 5.5\text{ V}$ , $I_{OH} = -400\text{ }\mu\text{A}$       | 2.4                                              |                     | V             |
| $V_{OL2}$ | Output Low Voltage         | $1.8\text{ V} \leq V_{CC} < 4.5\text{ V}$ , $I_{OL} = 1\text{ mA}$                   |                                                  | 0.2                 | V             |
| $V_{OH2}$ | Output High Voltage        | $1.8\text{ V} \leq V_{CC} < 4.5\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$       | $V_{CC} - 0.2$                                   |                     | V             |

**Table 5. PIN CAPACITANCE** ( $T_A = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ ,  $V_{CC} = 5\text{ V}$ )

| Symbol             | Test                                | Conditions             | Min | Typ | Max | Units |
|--------------------|-------------------------------------|------------------------|-----|-----|-----|-------|
| $C_{OUT}$ (Note 4) | Output Capacitance (DO)             | $V_{OUT} = 0\text{ V}$ |     |     | 5   | pF    |
| $C_{IN}$ (Note 4)  | Input Capacitance (CS, SK, DI, ORG) | $V_{IN} = 0\text{ V}$  |     |     | 5   | pF    |

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

**Table 6. A.C. CHARACTERISTICS – MATURE PRODUCT (Not Recommended for New Designs)**

( $V_{CC} = +1.8\text{ V}$  to  $+5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ , unless otherwise specified.) (Note 5)

| Symbol            | Parameter                    | Min Limit | Max Limit | Units         |
|-------------------|------------------------------|-----------|-----------|---------------|
| $t_{CSS}$         | CS Setup Time                | 50        |           | ns            |
| $t_{CSH}$         | CS Hold Time                 | 0         |           | ns            |
| $t_{DIS}$         | DI Setup Time                | 100       |           | ns            |
| $t_{DIH}$         | DI Hold Time                 | 100       |           | ns            |
| $t_{PD1}$         | Output Delay to 1            |           | 0.25      | $\mu\text{s}$ |
| $t_{PD0}$         | Output Delay to 0            |           | 0.25      | $\mu\text{s}$ |
| $t_{HZ}$ (Note 6) | Output Delay to High-Z       |           | 100       | ns            |
| $t_{EW}$          | Program/Erase Pulse Width    |           | 5         | ms            |
| $t_{CSMIN}$       | Minimum CS Low Time          | 0.25      |           | $\mu\text{s}$ |
| $t_{SKHI}$        | Minimum SK High Time         | 0.25      |           | $\mu\text{s}$ |
| $t_{SKLOW}$       | Minimum SK Low Time          | 0.25      |           | $\mu\text{s}$ |
| $t_{SV}$          | Output Delay to Status Valid |           | 0.25      | $\mu\text{s}$ |
| $SK_{MAX}$        | Maximum Clock Frequency      | DC        | 2000      | kHz           |

5. Test conditions according to "AC Test Conditions" table.

6. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

# CAT93C46

**Table 7. A.C. CHARACTERISTICS – NEW PRODUCT (Rev P)**

( $V_{CC} = +1.8\text{ V}$  to  $+5.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ,  $V_{CC} = +1.65\text{ V}$  to  $+5.5\text{ V}$ ,  $T_A = -20^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise specified.)

| Symbol            | Parameter                    | $V_{CC} = 1.8\text{ V} - 5.5\text{ V}$ |      | $V_{CC} = 4.5\text{ V} - 5.5\text{ V}$ |      | Units         |
|-------------------|------------------------------|----------------------------------------|------|----------------------------------------|------|---------------|
|                   |                              | Min                                    | Max  | Min                                    | Max  |               |
| $t_{CSS}$         | CS Setup Time                | 50                                     |      | 50                                     |      | ns            |
| $t_{CSH}$         | CS Hold Time                 | 0                                      |      | 0                                      |      | ns            |
| $t_{DIS}$         | DI Setup Time                | 100                                    |      | 50                                     |      | ns            |
| $t_{DIH}$         | DI Hold Time                 | 100                                    |      | 50                                     |      | ns            |
| $t_{PD1}$         | Output Delay to 1            |                                        | 0.25 |                                        | 0.1  | $\mu\text{s}$ |
| $t_{PD0}$         | Output Delay to 0            |                                        | 0.25 |                                        | 0.1  | $\mu\text{s}$ |
| $t_{HZ}$ (Note 7) | Output Delay to High-Z       |                                        | 100  |                                        | 100  | ns            |
| $t_{EW}$          | Program/Erase Pulse Width    |                                        | 5    |                                        | 5    | ms            |
| $t_{CSMIN}$       | Minimum CS Low Time          | 0.25                                   |      | 0.1                                    |      | $\mu\text{s}$ |
| $t_{SKHI}$        | Minimum SK High Time         | 0.25                                   |      | 0.1                                    |      | $\mu\text{s}$ |
| $t_{SKLOW}$       | Minimum SK Low Time          | 0.25                                   |      | 0.1                                    |      | $\mu\text{s}$ |
| $t_{SV}$          | Output Delay to Status Valid |                                        | 0.25 |                                        | 0.1  | $\mu\text{s}$ |
| $SK_{MAX}$        | Maximum Clock Frequency      | DC                                     | 2000 | DC                                     | 4000 | kHz           |

7. This parameter is tested initially and after a design or process change that affects the parameter.

**Table 8. POWER-UP TIMING** (Notes 8 and 9)

| Symbol    | Parameter                   | Max | Units |
|-----------|-----------------------------|-----|-------|
| $t_{PUR}$ | Power-up to Read Operation  | 1   | ms    |
| $t_{PUW}$ | Power-up to Write Operation | 1   | ms    |

8. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

9.  $t_{PUR}$  and  $t_{PUW}$  are the delays required from the time  $V_{CC}$  is stable until the specified operation can be initiated.

**Table 9. A.C. TEST CONDITIONS**

|                           |                                                              |                                              |
|---------------------------|--------------------------------------------------------------|----------------------------------------------|
| Input Rise and Fall Times | $\leq 50\text{ ns}$                                          |                                              |
| Input Pulse Voltages      | 0.4 V to 2.4 V                                               | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ |
| Timing Reference Voltages | 0.8 V, 2.0 V                                                 | $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$ |
| Input Pulse Voltages      | 0.2 $V_{CC}$ to 0.7 $V_{CC}$                                 | $1.8\text{ V} \leq V_{CC} \leq 4.5\text{ V}$ |
| Timing Reference Voltages | 0.5 $V_{CC}$                                                 | $1.8\text{ V} \leq V_{CC} \leq 4.5\text{ V}$ |
| Output Load               | Current Source $I_{OLmax}/I_{OHmax}$ ; $C_L = 100\text{ pF}$ |                                              |

## Device Operation

The CAT93C46 is a 1024-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C46 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 9-bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 10-bit instructions control the reading, writing and erase operations of the device. The CAT93C46 operates on a single power supply and will generate on chip the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status during a write operation. The serial communication protocol follows the timing shown in Figure 2.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy "1" into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The Ready/Busy flag can be disabled only in Ready state; no change is allowed in Busy state.

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 6-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organization).

## Read

Upon receiving a READ command (Figure 3) and an address (clocked into the DI pin), the DO pin of the CAT93C46 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay ( $t_{PD0}$  or  $t_{PD1}$ ).

After the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit. *Note: The sequential READ mode is available for CAT93C46 New Product only.*

## Erase/Write Enable and Disable

The CAT93C46 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46 write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status. The EWEN and EWDS instructions timing is shown in Figure 4.

**Table 10. INSTRUCTION SET**

| Instruction | Start Bit | Opcode | Address |        | Data  |        | Comments            |
|-------------|-----------|--------|---------|--------|-------|--------|---------------------|
|             |           |        | x8      | x16    | x8    | x16    |                     |
| READ        | 1         | 10     | A6-A0   | A5-A0  |       |        | Read Address AN-A0  |
| ERASE       | 1         | 11     | A6-A0   | A5-A0  |       |        | Clear Address AN-A0 |
| WRITE       | 1         | 01     | A6-A0   | A5-A0  | D7-D0 | D15-D0 | Write Address AN-A0 |
| EWEN        | 1         | 00     | 11XXXXX | 11XXXX |       |        | Write Enable        |
| EWDS        | 1         | 00     | 00XXXXX | 00XXXX |       |        | Write Disable       |
| ERAL*       | 1         | 00     | 10XXXXX | 10XXXX |       |        | Clear All Addresses |
| WRAL*       | 1         | 00     | 01XXXXX | 01XXXX | D7-D0 | D15-D0 | Write All Addresses |

\* Not available at  $V_{CC} < 1.8 V$

# CAT93C46

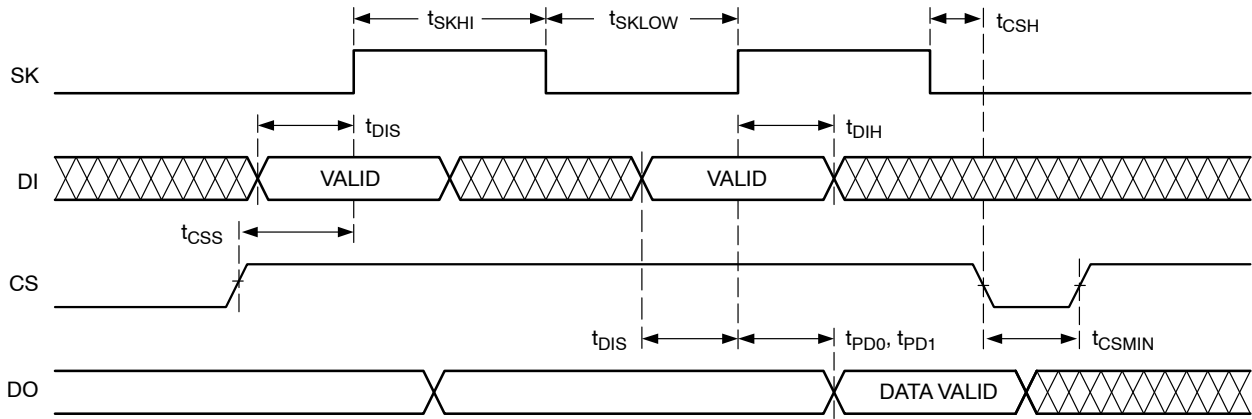


Figure 2. Synchronous Data Timing

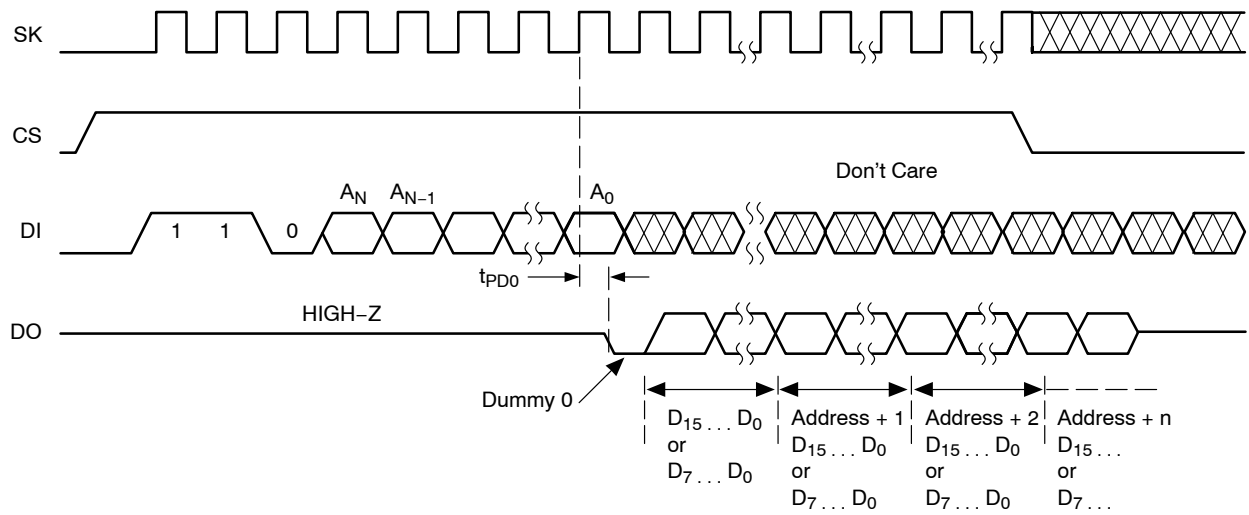


Figure 3. Read Instruction Timing

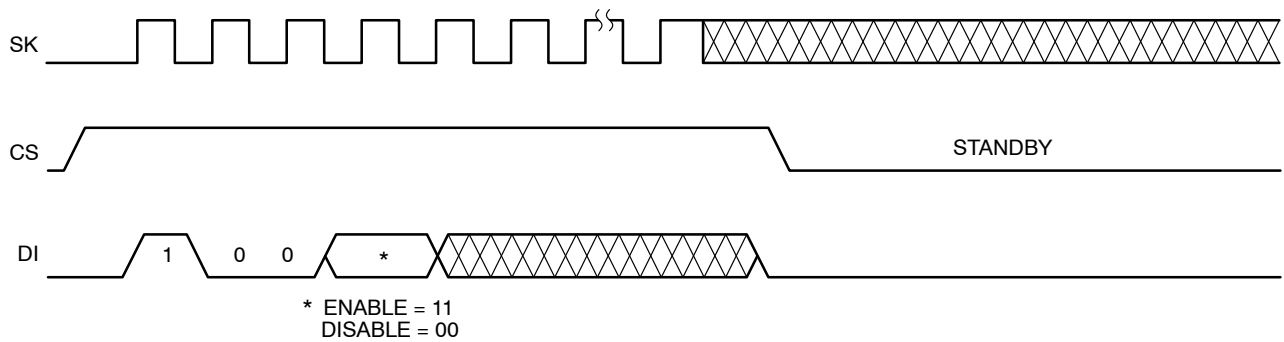


Figure 4. EWEN/EWDS Instruction Timing

### Write

After receiving a WRITE command (Figure 5), address and the data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking for auto-clear and data store cycles on the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

### Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be de-asserted for a minimum of  $t_{CSMIN}$  (Figure 6). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

### Erase All

Upon receiving an ERAL command (Figure 7), the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$ . The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical "1" state.

### Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of  $t_{CSMIN}$  (Figure 8). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

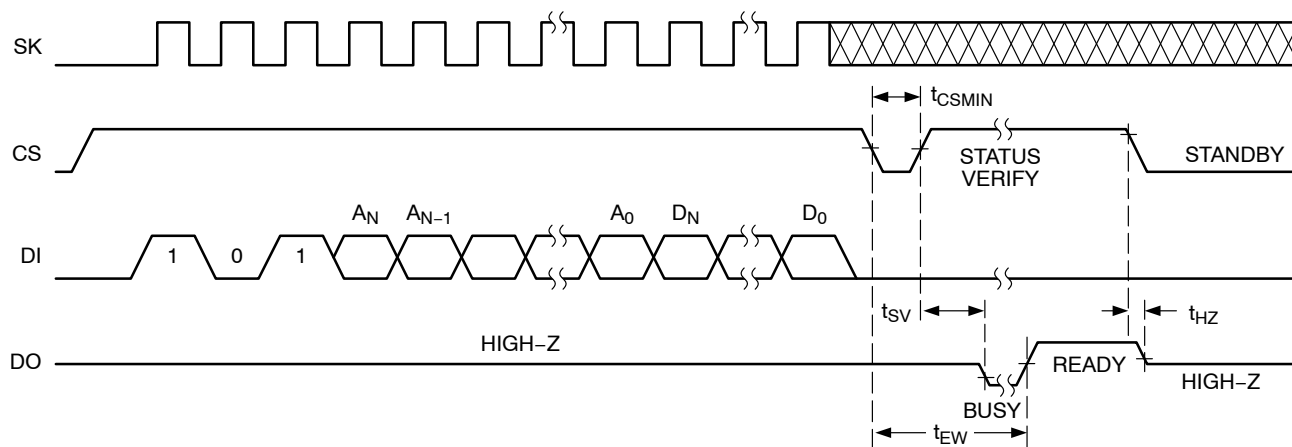


Figure 5. Write Instruction Timing

# CAT93C46

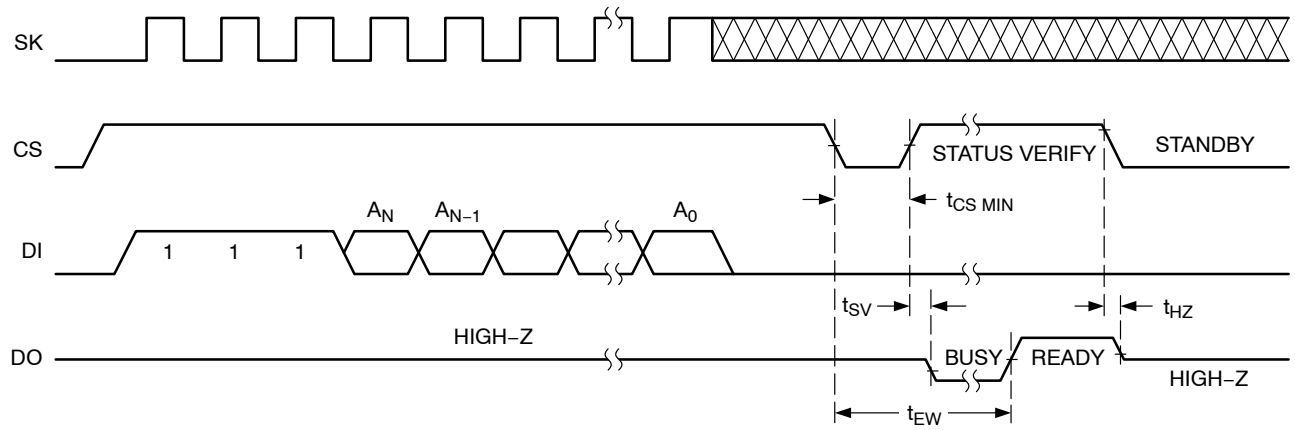


Figure 6. Erase Instruction Timing

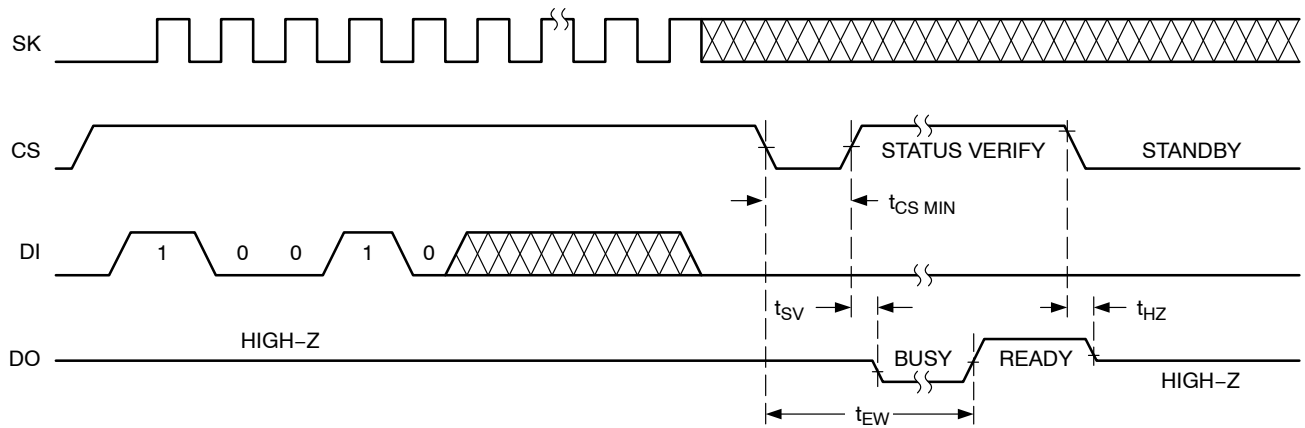


Figure 7. ERAL Instruction Timing

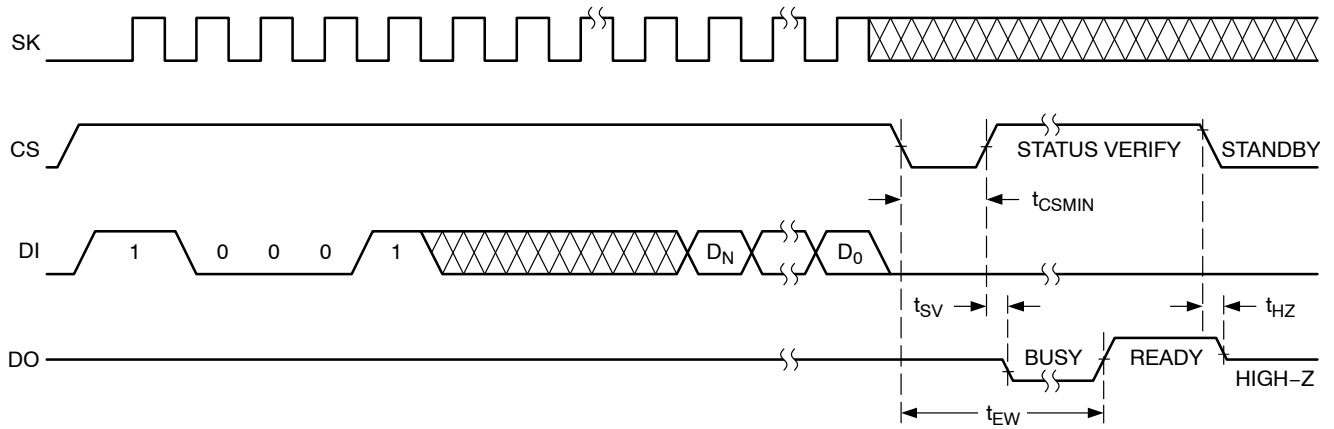
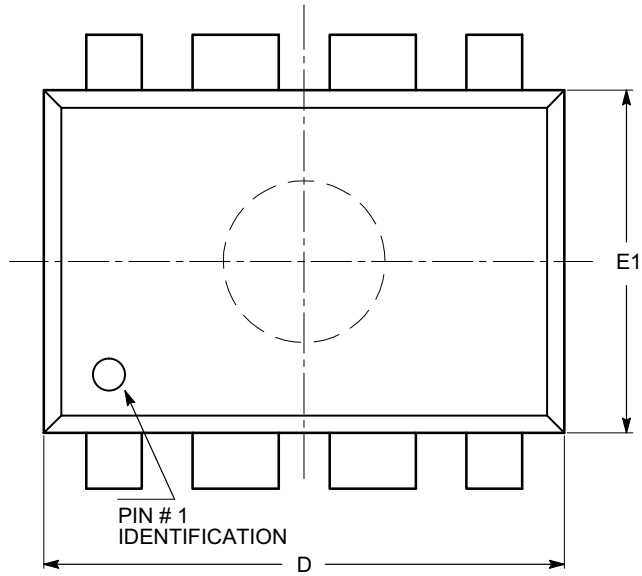


Figure 8. WRAL Instruction Timing

# CAT93C46

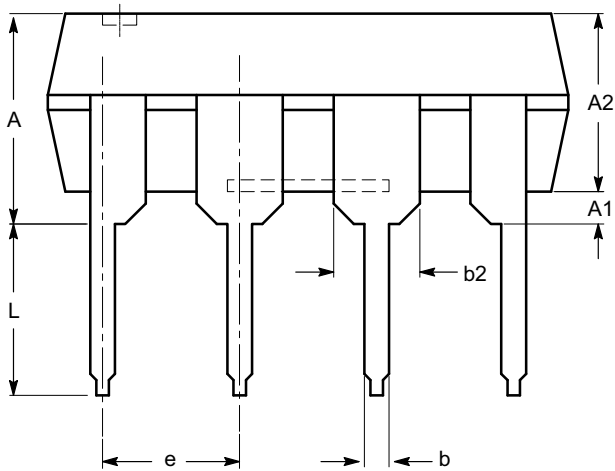
## PACKAGE DIMENSIONS

PDIP-8, 300 mils  
CASE 646AA-01  
ISSUE A

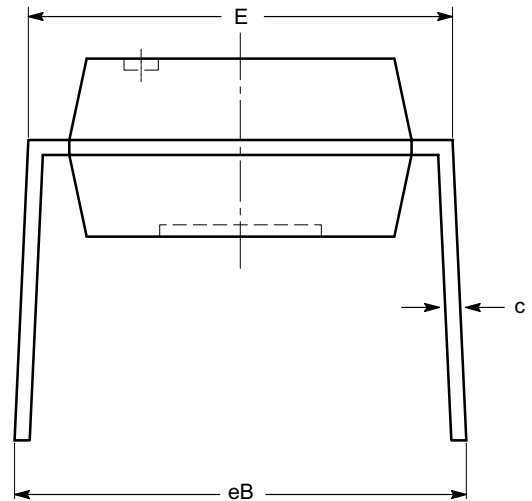


| SYMBOL | MIN      | NOM  | MAX   |
|--------|----------|------|-------|
| A      |          |      | 5.33  |
| A1     | 0.38     |      |       |
| A2     | 2.92     | 3.30 | 4.95  |
| b      | 0.36     | 0.46 | 0.56  |
| b2     | 1.14     | 1.52 | 1.78  |
| c      | 0.20     | 0.25 | 0.36  |
| D      | 9.02     | 9.27 | 10.16 |
| E      | 7.62     | 7.87 | 8.25  |
| E1     | 6.10     | 6.35 | 7.11  |
| e      | 2.54 BSC |      |       |
| eB     | 7.87     |      | 10.92 |
| L      | 2.92     | 3.30 | 3.80  |

TOP VIEW



SIDE VIEW



END VIEW

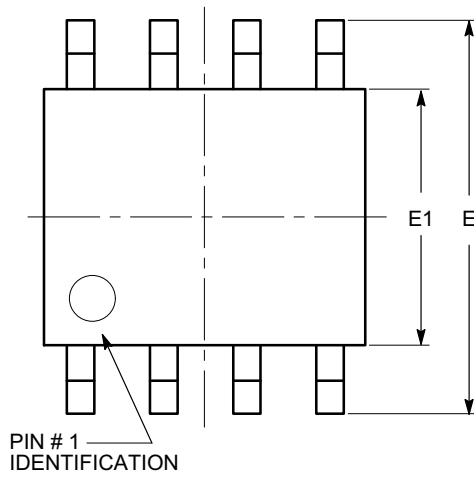
### Notes:

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-001.

# CAT93C46

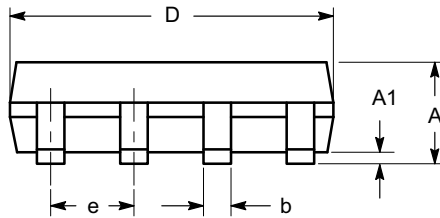
## PACKAGE DIMENSIONS

SOIC 8, 150 mils  
CASE 751BD-01  
ISSUE O

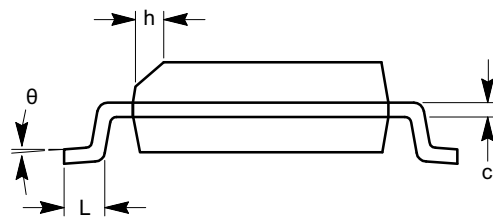


TOP VIEW

| SYMBOL   | MIN      | NOM | MAX  |
|----------|----------|-----|------|
| A        | 1.35     |     | 1.75 |
| A1       | 0.10     |     | 0.25 |
| b        | 0.33     |     | 0.51 |
| c        | 0.19     |     | 0.25 |
| D        | 4.80     |     | 5.00 |
| E        | 5.80     |     | 6.20 |
| E1       | 3.80     |     | 4.00 |
| e        | 1.27 BSC |     |      |
| h        | 0.25     |     | 0.50 |
| L        | 0.40     |     | 1.27 |
| $\theta$ | 0°       |     | 8°   |



SIDE VIEW



END VIEW

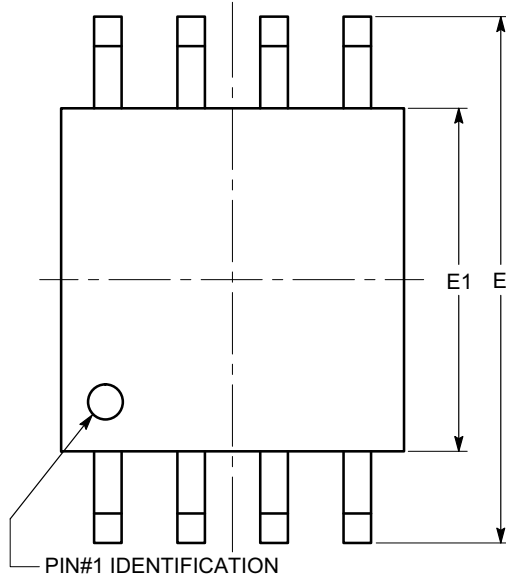
### Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

# CAT93C46

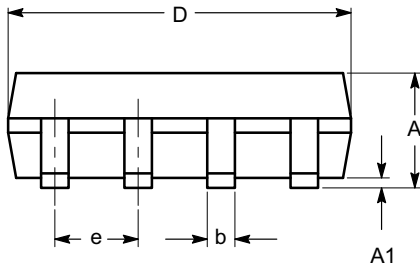
## PACKAGE DIMENSIONS

SOIC-8, 208 mils  
CASE 751BE-01  
ISSUE O

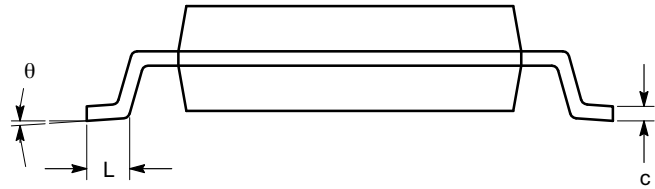


TOP VIEW

| SYMBOL   | MIN      | NOM | MAX  |
|----------|----------|-----|------|
| A        |          |     | 2.03 |
| A1       | 0.05     |     | 0.25 |
| b        | 0.36     |     | 0.48 |
| c        | 0.19     |     | 0.25 |
| D        | 5.13     |     | 5.33 |
| E        | 7.75     |     | 8.26 |
| E1       | 5.13     |     | 5.38 |
| e        | 1.27 BSC |     |      |
| L        | 0.51     |     | 0.76 |
| $\theta$ | 0°       |     | 8°   |



SIDE VIEW



END VIEW

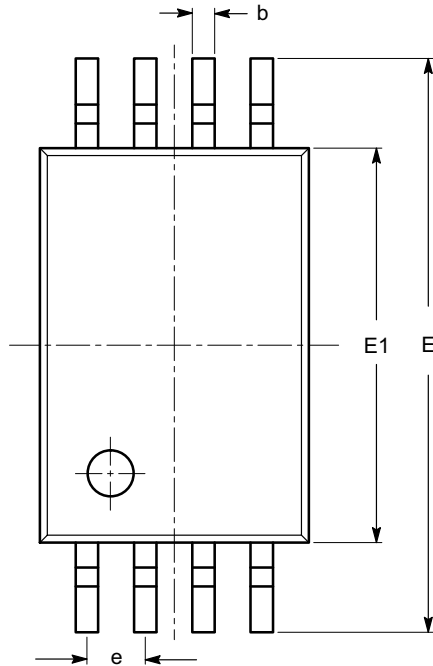
### Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with EIAJ EDR-7320.

# CAT93C46

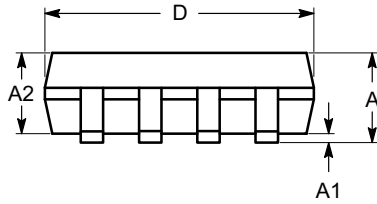
## PACKAGE DIMENSIONS

TSSOP8, 4.4x3  
CASE 948AL-01  
ISSUE O

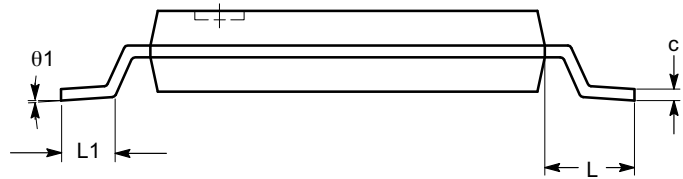


| SYMBOL   | MIN      | NOM  | MAX  |
|----------|----------|------|------|
| A        |          |      | 1.20 |
| A1       | 0.05     |      | 0.15 |
| A2       | 0.80     | 0.90 | 1.05 |
| b        | 0.19     |      | 0.30 |
| c        | 0.09     |      | 0.20 |
| D        | 2.90     | 3.00 | 3.10 |
| E        | 6.30     | 6.40 | 6.50 |
| E1       | 4.30     | 4.40 | 4.50 |
| e        | 0.65 BSC |      |      |
| L        | 1.00 REF |      |      |
| L1       | 0.50     | 0.60 | 0.75 |
| $\theta$ | 0°       |      | 8°   |

TOP VIEW



SIDE VIEW



END VIEW

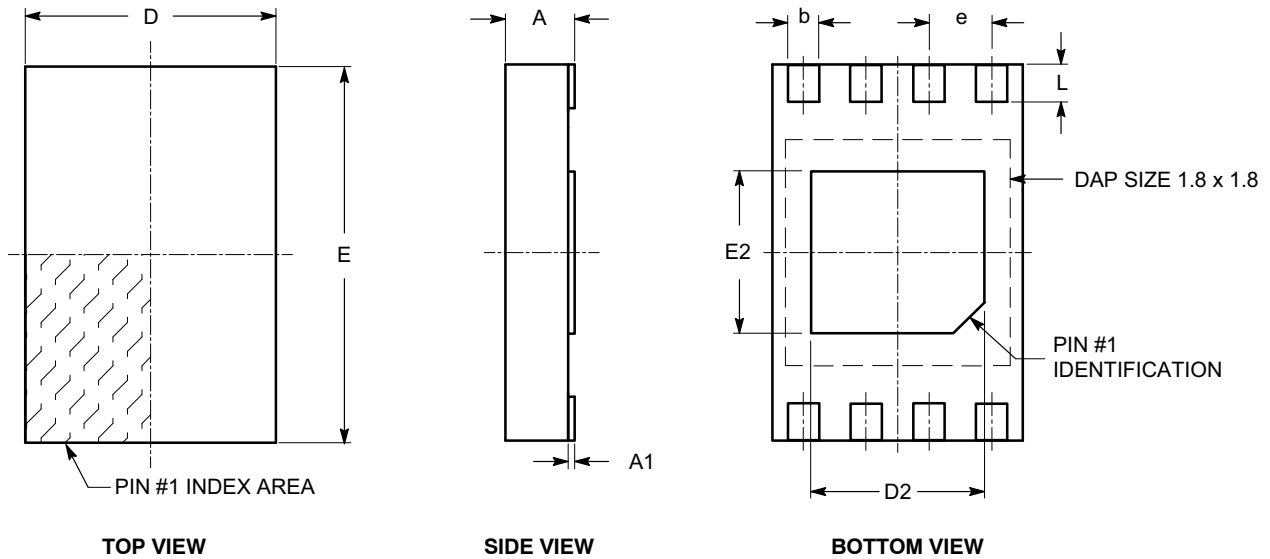
### Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

# CAT93C46

## PACKAGE DIMENSIONS

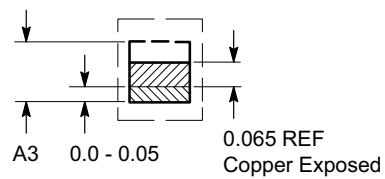
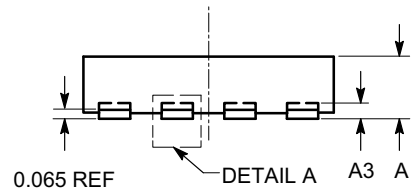
UDFN8, 2x3 EXTENDED PAD  
CASE 517AZ-01  
ISSUE O



| SYMBOL | MIN       | NOM  | MAX  |
|--------|-----------|------|------|
| A      | 0.45      | 0.50 | 0.55 |
| A1     | 0.00      | 0.02 | 0.05 |
| A3     | 0.127 REF |      |      |
| b      | 0.20      | 0.25 | 0.30 |
| D      | 1.95      | 2.00 | 2.05 |
| D2     | 1.35      | 1.40 | 1.45 |
| E      | 2.95      | 3.00 | 3.05 |
| E2     | 1.25      | 1.30 | 1.35 |
| e      | 0.50 REF  |      |      |
| L      | 0.25      | 0.30 | 0.35 |

### Notes:

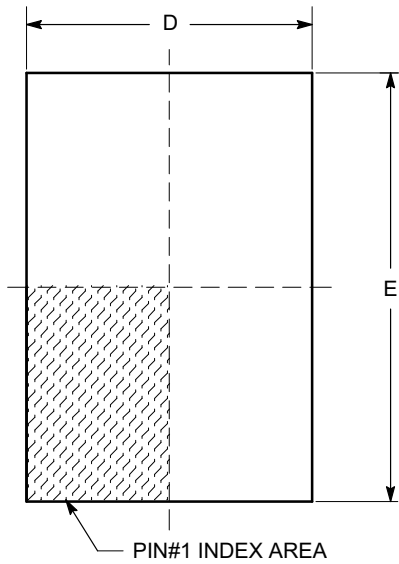
- (1) All dimensions are in millimeters.
- (2) Refer JEDEC MO-236/MO-252.



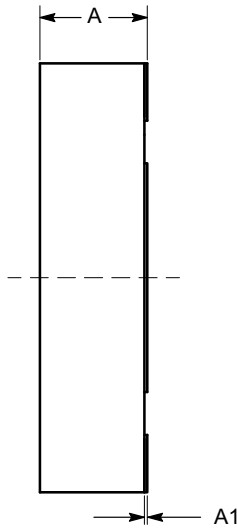
# CAT93C46

## PACKAGE DIMENSIONS

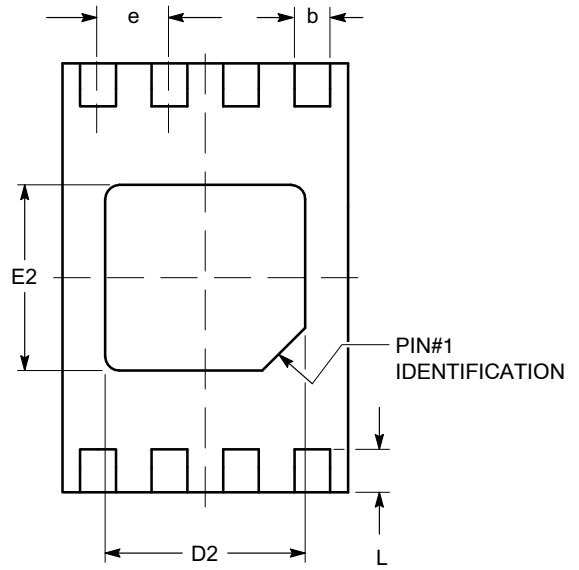
TDFN8, 2x3  
CASE 511AK-01  
ISSUE A



TOP VIEW

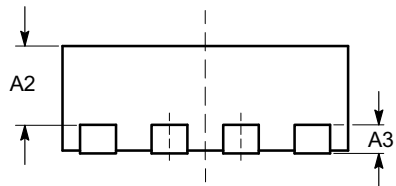


SIDE VIEW



BOTTOM VIEW

| SYMBOL | MIN      | NOM  | MAX  |
|--------|----------|------|------|
| A      | 0.70     | 0.75 | 0.80 |
| A1     | 0.00     | 0.02 | 0.05 |
| A2     | 0.45     | 0.55 | 0.65 |
| A3     | 0.20 REF |      |      |
| b      | 0.20     | 0.25 | 0.30 |
| D      | 1.90     | 2.00 | 2.10 |
| D2     | 1.30     | 1.40 | 1.50 |
| E      | 2.90     | 3.00 | 3.10 |
| E2     | 1.20     | 1.30 | 1.40 |
| e      | 0.50 TYP |      |      |
| L      | 0.20     | 0.30 | 0.40 |



FRONT VIEW

### Notes:

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MO-229.

## CAT93C46

### Example of Ordering Information

| Device Order Number           | Specific Device Marking* | Package Type  | Temperature Range                    | Lead Finish | Shipping                           |
|-------------------------------|--------------------------|---------------|--------------------------------------|-------------|------------------------------------|
| CAT93C46LI-G                  | 93C46P                   | PDIP-8        | I = Industrial<br>(-40°C to +85°C)   | NiPdAu      | Tube, 50 Units / Tube              |
| CAT93C46LE-G                  | 93C46P                   | PDIP-8        | E = Extended<br>(-40°C to +125°C)    | NiPdAu      | Tube, 50 Units / Tube              |
| CAT93C46VE-GT3                | 93C46P                   | SOIC-8, JEDEC | E = Extended<br>(-40°C to +125°C)    | NiPdAu      | Tape & Reel,<br>3,000 Units / Reel |
| CAT93C46VI-G                  | 93C46P                   | SOIC-8, JEDEC | I = Industrial<br>(-40°C to +85°C)   | NiPdAu      | Tube, 100 Units / Tube             |
| CAT93C46VI-GT3                | 93C46P                   | SOIC-8, JEDEC | I = Industrial<br>(-40°C to +85°C)   | NiPdAu      | Tape & Reel,<br>3,000 Units / Reel |
| CAT93C46VI-GT3L               | 93C46P                   | SOIC-8, JEDEC | I = Industrial**<br>(-20°C to +85°C) | NiPdAu      | Tape & Reel,<br>3,000 Units / Reel |
| CAT93C46VP2I-GT3<br>(Note 10) | M0T                      | TDFN-8        | I = Industrial<br>(-40°C to +85°C)   | NiPdAu      | Tape & Reel,<br>3,000 Units / Reel |
| CAT93C46WI-G<br>(Note 10)     | 93C46P                   | SOIC-8, JEDEC | I = Industrial<br>(-40°C to +85°C)   | NiPdAu      | Tube, 100 Units / Tube             |
| CAT93C46WI-GT3<br>(Note 10)   | 93C46P                   | SOIC-8, JEDEC | I = Industrial<br>(-40°C to +85°C)   | NiPdAu      | Tape & Reel,<br>3,000 Units / Reel |
| CAT93C46XI-T2                 | 93C46P                   | SOIC-8, EIAJ  | I = Industrial<br>(-40°C to +85°C)   | Matte-Tin   | Tape & Reel,<br>2,000 Units / Reel |
| CAT93C46XE-T2                 | 93C46P                   | SOIC-8, EIAJ  | E = Extended<br>(-40°C to +125°C)    | Matte-Tin   | Tape & Reel,<br>2,000 Units / Reel |
| CAT93C46YI-G                  | M46P                     | TSSOP-8       | I = Industrial<br>(-40°C to +85°C)   | NiPdAu      | Tube, 100 Units / Tube             |
| CAT93C46YI-GT3                | M46P                     | TSSOP-8       | I = Industrial<br>(-40°C to +85°C)   | NiPdAu      | Tape & Reel,<br>3,000 Units / Reel |
| CAT93C46YI-GT3L               | M46P                     | TSSOP-8       | I = Industrial**<br>(-20°C to +85°C) | NiPdAu      | Tape & Reel,<br>3,000 Units / Reel |
| CAT93C46YE-GT3                | M46P                     | TSSOP-8       | E = Extended<br>(-40°C to +125°C)    | NiPdAu      | Tape & Reel,<br>3,000 Units / Reel |
| CAT93C46HU4I-GT3              | M0U                      | UDFN-8        | I = Industrial<br>(-40°C to +85°C)   | NiPdAu      | Tape & Reel,<br>3,000 Units / Reel |
| CAT93C46HU4E-GT3              | M0U                      | UDFN-8        | E = Extended<br>(-40°C to +125°C)    | NiPdAu      | Tape & Reel,<br>3,000 Units / Reel |

10. Not recommended for new designs.

11. All packages are RoHS-compliant (Lead-free, Halogen-free).

12. **The standard lead finish is NiPdAu.**

13. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

14. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

15. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at [www.onsemi.com](http://www.onsemi.com)

\*Marking for New Product (Rev P)

\*\* Works only for the -20°C to +85°C interval of the Industrial range

**ON Semiconductor** and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910

**Japan Customer Focus Center**  
Phone: 81-3-5817-1050

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local  
Sales Representative

Компания «Life Electronics» занимается поставками электронных компонентов импортного и отечественного производства от производителей и со складов крупных дистрибьюторов Европы, Америки и Азии.

С конца 2013 года компания активно расширяет линейку поставок компонентов по направлению коаксиальный кабель, кварцевые генераторы и конденсаторы (керамические, пленочные, электролитические), за счёт заключения дистрибьюторских договоров

Мы предлагаем:

- Конкурентоспособные цены и скидки постоянным клиентам.
- Специальные условия для постоянных клиентов.
- Подбор аналогов.
- Поставку компонентов в любых объемах, удовлетворяющих вашим потребностям.
- Приемлемые сроки поставки, возможна ускоренная поставка.
- Доставку товара в любую точку России и стран СНГ.
- Комплексную поставку.
- Работу по проектам и поставку образцов.
- Формирование склада под заказчика.
- Сертификаты соответствия на поставляемую продукцию (по желанию клиента).
- Тестирование поставляемой продукции.
- Поставку компонентов, требующих военную и космическую приемку.
- Входной контроль качества.
- Наличие сертификата ISO.

В составе нашей компании организован Конструкторский отдел, призванный помогать разработчикам, и инженерам.

Конструкторский отдел помогает осуществить:

- Регистрацию проекта у производителя компонентов.
- Техническую поддержку проекта.
- Защиту от снятия компонента с производства.
- Оценку стоимости проекта по компонентам.
- Изготовление тестовой платы монтаж и пусконаладочные работы.



Тел: +7 (812) 336 43 04 (многоканальный)

Email: [org@lifeelectronics.ru](mailto:org@lifeelectronics.ru)

[www.lifeelectronics.ru](http://www.lifeelectronics.ru)