

## MAX30112

## Optimized Pulse-Oximeter and Heart Rate AFE for Wearable Health

### General Description

The MAX30112 is a complete optical pulse oximetry and heart rate detection integrated analog front-end. The MAX30112 has a high-resolution, optical readout signal-processing channel with built-in ambient light cancellation, as well as high-current LED driver DACs, to form a complete optical readout signal chain. With external LED(s) and photo diode(s), the MAX30112 offers the lowest power, highest performance heart rate detection solution for wrist applications.

The MAX30112 operates on a 1.8V main supply voltage, with a separate 3.1V to 5.25V LED driver power supply. The device supports a standard I<sup>2</sup>C compatible interface, as well as shutdown modes through the software with near-zero standby current, allowing the power rails to remain powered at all times.

### Applications

- Wrist-Worn Wearable Devices
- In-Ear Wearable Devices
- SpO<sub>2</sub> Monitoring Devices
- Fitness Wearable Devices

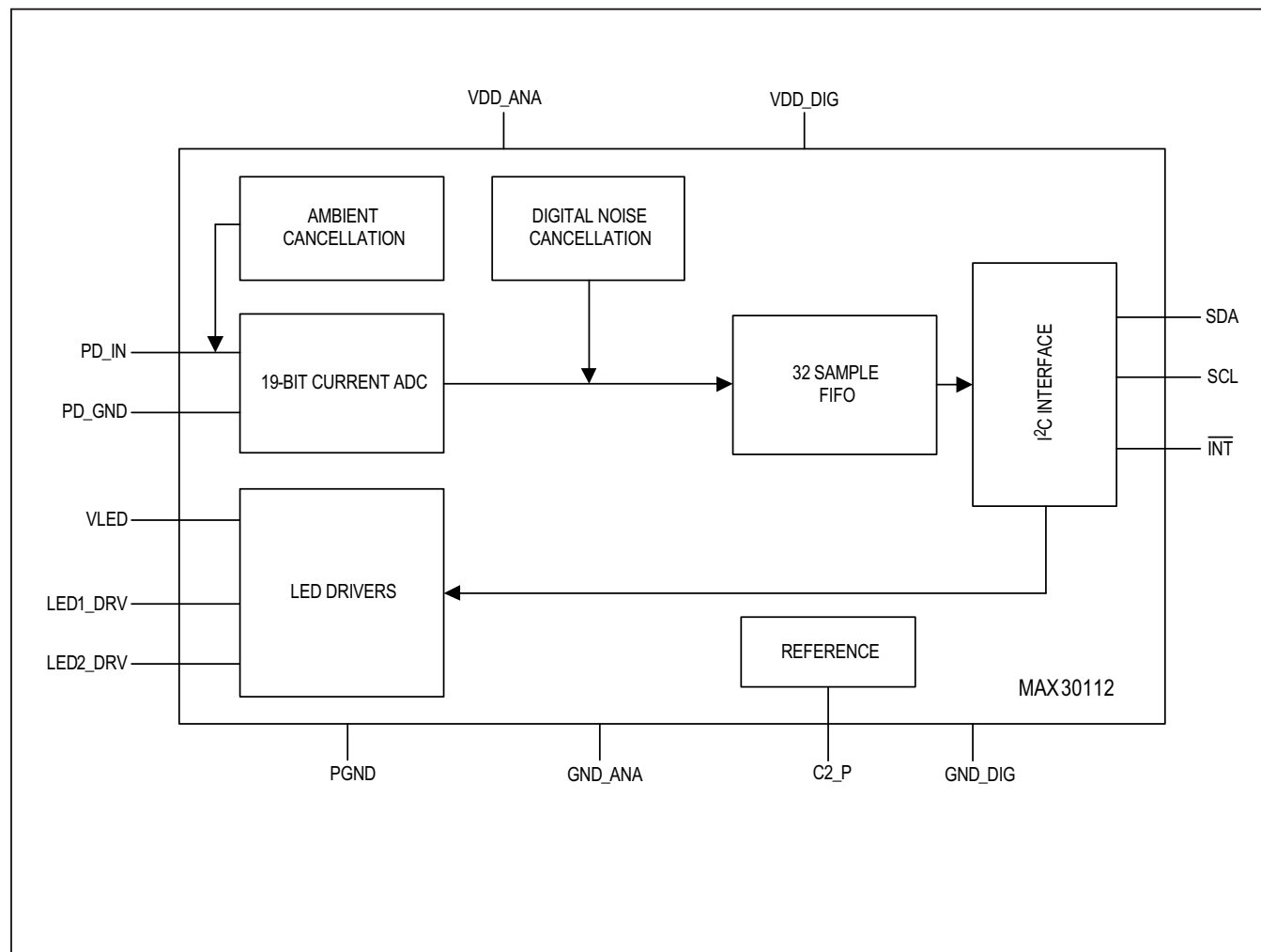
### Benefits and Features

- Reflective or Transmissive Heart Rate, Heart Rate Variability, or SpO<sub>2</sub> Monitoring
- Transmit Section
  - Two 8-bit LED Current DACs
  - Four Current Ranges 50mA, 100mA, 150mA, 200mA
  - Low Noise Current Sources for High Peak Transmit to Receive Dynamic Range
  - Low 160mV Dropout to Support Direct Drive From Rechargeable Li Battery
  - High Output Impedance and High Supply Rejection to Support Unregulated Supply or Direct Drive From Boost Switcher Supply

- Receive Section
  - 19-bit Optical ADC Path to Support the Lowest Perfusions Situations
  - Low 25pA-RMS Input Referred Noise to Minimize LED Power Under Most Conditions
  - High Ambient Light Input Range of 200μA and to Support Extraction of HRM Signal in the Most Adverse Lighting Conditions
  - Built-in Front And Back End Ambient Light Cancellation, Improving Rejection and Eliminating System Complexity of Dealing with Ambient Light
  - Short Exposure Pulse Widths of 52μs, 104μs, 206μs, 417μs for Efficient Uses of LED Light
  - Multiple Sample Rate Options from 20sps to 3.2ksps
- Ultra-Low-Power Operation for Mobile and Body-Wearable Device
  - Dynamic Power Down Modes to 100sps for Low-Power Consumption
  - Full AFE Power Consumption of Less Than 25μA (typ) at 25sps
  - Large 32 Sample FIFO to Support Batch Processing in the Microcontroller
  - Variety of System Monitors Mappable to Interrupts to Off-Load System Monitoring Functions From the Microcontroller
  - Low Shutdown Current = 1.4μA (typ)
- I<sup>2</sup>C interface
- Supports a Single 1.8V Supply with Separate 3.1V to 5.25V LED Supply
- Miniature 2.8mm x 2.0mm, 6x4, 0.4mm Ball Pitch WLP Package
- -40°C to +85°C Operating Temperature Range

Ordering Information appears at end of data sheet.

## Simplified Block Diagram



## Absolute Maximum Ratings

VDD\_ANA to GND\_ANA ..... -0.3V to +2.2V  
 VDD\_DIG to GND\_ANA ..... -0.3V to +2.2V  
 VDD\_ANA to VDD\_DIG ..... -0.3V to +0.3V  
 PGND to GND\_ANA ..... -0.3V to +0.3V  
 GND\_DIG to GND\_ANA ..... -0.3V to +0.3V  
 VLED to PGND ..... -0.3V to +6.0V  
 LED1\_DRV to PGND ..... -0.3V to  $V_{LED} + 0.3V$   
 LED2\_DRV to PGND ..... -0.3V to  $V_{LED} + 0.3V$   
 PD\_GND to GND\_ANA ..... Internally Shorted  
 SDA, SCL,  $\overline{INT}$  to GND\_ANA ..... -0.3V to +6.0V

All other pins to GND\_ANA ..... -0.3V to +2.2V  
 Output Short-Circuit Duration ..... Continuous  
 Continuous Input Current Into Any Pin  
     (except LEDx\_DRV Pins) .....  $\pm 20mA$   
 Continuous Power Dissipation, WLP  
     ( $T_A = +70^\circ C$ , derate 5.5mW/ $^\circ C$  above  $+70^\circ C$ ) ..... 440mW  
 Operating Temperature Range .....  $-40^\circ C$  to  $+85^\circ C$   
 Storage Temperature Range .....  $-40^\circ C$  to  $+105^\circ C$   
 Soldering Temperature (reflow) .....  $+260^\circ C$

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

### 24-Bump WLP

| PACKAGE CODE                                 | W241C2+1                                       |
|----------------------------------------------|------------------------------------------------|
| Outline Number                               | <a href="#">21-100088</a>                      |
| Land Pattern Number                          | Refer to <a href="#">Application Note 1891</a> |
| <b>THERMAL RESISTANCE, FOUR-LAYER BOARD:</b> |                                                |
| Junction to Ambient ( $\theta_{JA}$ )        | 49 $^\circ C/W$                                |

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

## Electrical Characteristics

( $V_{DD} = V_{DD\_ANA} = V_{DD\_DIG} = 1.8V$ ,  $V_{LED} = 3.3V$ ,  $C_{LOAD} = 10pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1))

| PARAMETER                      | SYMBOL           | CONDITIONS                                                                                      |                                                   | MIN | TYP | MAX  | UNITS |
|--------------------------------|------------------|-------------------------------------------------------------------------------------------------|---------------------------------------------------|-----|-----|------|-------|
| POWER SUPPLY                   |                  |                                                                                                 |                                                   |     |     |      |       |
| Power Supply Voltage           | V <sub>DD</sub>  | Guaranteed by V <sub>DD</sub> DC PSR                                                            |                                                   | 1.7 | 1.8 | 2.0  | V     |
| LED Supply Voltage             | V <sub>LED</sub> | Guaranteed by V <sub>LED</sub> DC PSR                                                           |                                                   | 3.1 | 3.3 | 5.25 | V     |
| V <sub>DD</sub> Supply Current | I <sub>DD</sub>  | Low Power = Off, LED1 or LED2 (FD1 = 0x01 or FD1 = 0x02, PPG_TINT = 0x0, LP_MODE = 0x0), Note 2 | Sample Rate = 100sps, single pulse (PPG_SR = 0x4) | 241 |     | 308  | μA    |
|                                |                  | Low Power = On, LED1 or LED2 (FD1 = 0x01 or FD1 = 0x02, PPG_TINT = 0x0, LP_MODE = 0x1), Note 2  | Sample Rate = 100sps, single pulse (PPG_SR = 0x4) | 72  |     |      |       |
|                                |                  |                                                                                                 | Sample Rate = 50sps, single pulse (PPG_SR = 0x2)  | 40  |     |      |       |
|                                |                  |                                                                                                 | Sample Rate = 25sps, single pulse (PPG_SR = 0x1)  | 24  | 43  |      |       |
|                                |                  |                                                                                                 | Sample Rate = 50sps, dual pulse (PPG_SR = 0xD)    | 94  |     |      |       |
|                                | I <sub>DD</sub>  | Sample Rate = 25sps, dual pulse (PPG_SR = 0xC)                                                  | 51                                                |     | μA  |      |       |

**Electrical Characteristics (continued)**

(V<sub>DD</sub> = VDD\_ANA = VDD\_DIG = 1.8V, V<sub>LED</sub> = 3.3V, C<sub>LOAD</sub> = 10pF, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1))

| PARAMETER                                              | SYMBOL                | CONDITIONS                                                                                                                             |                                                   | MIN | TYP  | MAX | UNITS |
|--------------------------------------------------------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------|-----|------|-----|-------|
| V <sub>LED</sub> Supply Current                        | I <sub>LED</sub>      | Low Power = On, LED1 or LED2, LED driver 0mA (FD1 = 0x01 or FD1 = 0x02, PPG_TINT = 0x0, LP_MODE = 0x1, LEDx_DRV = 0x00)                | Sample Rate = 100sps, single pulse (PPG_SR = 0x4) |     | 0.1  | ±1  | μA    |
|                                                        |                       | Low Power = On, LED1 or LED2, LED driver full scale (FD1 = 0x01 or FD1 = 0x02, PPG_TINT = 0x0, LP_MODE = 0x1, LEDx_DRV = 0xFF)         | Sample Rate = 100sps, single pulse (PPG_SR = 0x4) |     | 308  |     |       |
|                                                        |                       |                                                                                                                                        | Sample Rete = 50sps, single pulse (PPG_SR = 0x2)  |     | 155  |     |       |
|                                                        |                       |                                                                                                                                        | Sample Rate = 25sps, single pulse (PPG_SR = 0x1)  |     | 74   | 110 | μA    |
|                                                        |                       | Low Power = On, LED1 and LED2, LED driver full scale (FD1 = 0x1, FD2 = 0x2, FD3 = 0x0, PPG_TINT = 0x0, LP_MODE = 0x1, LEDx_DRV = 0xFF) | Sample Rate = 100sps, single pulse (PPG_SR = 0x4) |     | 616  |     |       |
|                                                        |                       |                                                                                                                                        | Sample Rate = 50sps, single pulse (PPG_SR = 0x2)  |     | 304  |     |       |
|                                                        |                       |                                                                                                                                        | Sample Rate = 25sps, single pulse (PPG_SR = 0x1)  |     | 149  |     |       |
| V <sub>DD</sub> Current in Shutdown                    |                       | T <sub>A</sub> = +25°C, Note 2                                                                                                         |                                                   |     | 1.6  | 5   | μA    |
| V <sub>LED</sub> Current in Shutdown                   |                       | T <sub>A</sub> = +25°C                                                                                                                 |                                                   |     |      | 1   | μA    |
| V <sub>DD</sub> Undervoltage Interrupt Threshold       |                       | T <sub>A</sub> = +25°C                                                                                                                 |                                                   |     | 1.64 |     | V     |
| V <sub>DD</sub> Overvoltage Interrupt Threshold        |                       | T <sub>A</sub> = +25°C                                                                                                                 |                                                   |     | 2.0  |     | V     |
| OPTICAL RECEIVE CHANNEL                                |                       |                                                                                                                                        |                                                   |     |      |     |       |
| ADC Resolution                                         |                       |                                                                                                                                        |                                                   |     | 19   |     | bits  |
| ADC Full-Scale Input Current                           |                       | PPG_ADC_RGE = 0x0                                                                                                                      |                                                   |     | 6.0  |     | μA    |
| ADC Full-Scale Input Current (Including DC Offset DAC) |                       | PPG_ADC_RGE = 0x1                                                                                                                      |                                                   |     | 12.0 |     | μA    |
|                                                        |                       | PPG_ADC_RGE = 0x2                                                                                                                      |                                                   |     | 24.0 |     |       |
|                                                        |                       | PPG_ADC_RGE = 0x3                                                                                                                      |                                                   |     | 48.0 |     |       |
| ADC Integration Time                                   | t <sub>PPG_TINT</sub> | LED_SETLNG = 0x3                                                                                                                       | PPG_TINT = 0x0                                    |     | 52   |     | μs    |
|                                                        |                       |                                                                                                                                        | PPG_TINT = 0x1                                    |     | 104  |     |       |
|                                                        |                       |                                                                                                                                        | PPG_TINT = 0x2                                    |     | 208  |     |       |
|                                                        |                       |                                                                                                                                        | PPG_TINT = 0x3                                    |     | 417  |     |       |

**Electrical Characteristics (continued)**

(V<sub>DD</sub> = VDD\_ANA = VDD\_DIG = 1.8V, V<sub>LED</sub> = 3.3V, C<sub>LOAD</sub> = 10pF, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Note 1))

| PARAMETER                                           | SYMBOL           | CONDITIONS                                                                                                                              |                   | MIN | TYP  | MAX  | UNITS |
|-----------------------------------------------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------|-------------------|-----|------|------|-------|
| Minimum PPG Sample Rate                             |                  | PPG_SR = 0x0                                                                                                                            |                   |     | 20   |      | sps   |
| Maximum PPG Sample Rate                             |                  | PPG_SR = 0xA                                                                                                                            |                   |     | 3200 |      | sps   |
| Sample Rate Error                                   |                  | From nominal as indicated in the PPG_SR table                                                                                           |                   | -2  |      | +2   | %     |
| DC Ambient Light Input Range                        | ALR              | T <sub>A</sub> = +25°C                                                                                                                  |                   |     | 200  |      | μA    |
| Total Integrated Input Referred Noise Current       |                  | PPG_ADC_RGE = 0x0,<br>T <sub>A</sub> = +25°C                                                                                            | PPG_TINT = 0x0    |     | 71   |      | pArms |
|                                                     |                  |                                                                                                                                         | PPG_TINT = 0x1    |     | 50   |      |       |
|                                                     |                  |                                                                                                                                         | PPG_TINT = 0x2    |     | 35   |      | pArms |
|                                                     |                  |                                                                                                                                         | PPG_TINT = 0x3    |     | 25   |      |       |
| Maximum Photodiode Input Capacitance                |                  |                                                                                                                                         |                   |     | 1000 |      | pF    |
| Transmit and Receive Channel V <sub>DD</sub> DC PSR |                  | Loopback test,<br>exposure current = 1.6μA<br>nominal,<br>PPG_TINT = 0x3,<br>V <sub>LED</sub> = 3.3V,<br>V <sub>DD</sub> = 1.7V to 2.0V | PPG_ADC_RGE = 0x0 |     | 2420 |      | LSB/V |
|                                                     |                  |                                                                                                                                         | PPG_ADC_RGE = 0x1 |     | 2010 |      |       |
|                                                     |                  |                                                                                                                                         | PPG_ADC_RGE = 0x2 |     | 1790 |      |       |
|                                                     |                  |                                                                                                                                         | PPG_ADC_RGE = 0x3 |     | 1664 |      |       |
| LED TRANSMIT DRIVER                                 |                  |                                                                                                                                         |                   |     |      |      |       |
| LED Current Resolution                              |                  |                                                                                                                                         |                   |     | 8    |      | Bits  |
| Driver DNL                                          |                  |                                                                                                                                         |                   |     | 1    |      | LSB   |
| Driver INL                                          |                  |                                                                                                                                         |                   |     | 1    |      | LSB   |
| Full-Scale LED Current                              | I <sub>LED</sub> | LEDx_PA = 0xFF                                                                                                                          | LEDx_RGE = 0x0    | 45  | 50   | 55   | mA    |
|                                                     |                  |                                                                                                                                         | LEDx_RGE = 0x1    |     | 100  |      |       |
|                                                     |                  |                                                                                                                                         | LEDx_RGE = 0x2    |     | 150  |      |       |
|                                                     |                  | LEDx_PA = 0xF2, LEDx_RGE = 0x3                                                                                                          |                   |     | 190  |      |       |
|                                                     | I <sub>LED</sub> | LEDx_PA = 0xFF, LEDx_RGE = 0x3 (Note 3)                                                                                                 |                   |     | 200  |      | mA    |
| Minimum Output Voltage                              |                  | LEDx_PA = 0xFF,<br>V <sub>DD</sub> = 1.8V, V <sub>LED</sub> = 3.3V,<br>95% of the desired LED<br>current                                | LEDx_RGE = 0x0    |     | 0.16 | 0.25 | V     |
|                                                     |                  |                                                                                                                                         | LEDx_RGE = 0x1    |     | 0.32 |      |       |
|                                                     |                  |                                                                                                                                         | LEDx_RGE = 0x2    |     | 0.49 |      |       |
|                                                     |                  | LEDx_RGE = 0x3 LEDx_PA = 0xF2, V <sub>DD</sub> = 1.8V,<br>V <sub>LED</sub> = 3.3V, 95% of the desired LED current                       |                   |     | 0.64 |      |       |

**Electrical Characteristics (continued)**

( $V_{DD} = V_{DD\_ANA} = V_{DD\_DIG} = 1.8V$ ,  $V_{LED} = 3.3V$ ,  $C_{LOAD} = 10pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Note 1))

| PARAMETER                                                 | SYMBOL              | CONDITIONS                                                                                                |                | MIN      | TYP   | MAX  | UNITS |
|-----------------------------------------------------------|---------------------|-----------------------------------------------------------------------------------------------------------|----------------|----------|-------|------|-------|
| Transmit Driver V <sub>LED</sub><br>DC PSR                |                     | LEDx_PA = 0xFF,<br>V <sub>DD</sub> = 1.8V, V <sub>LEDx_DRV</sub> = 0.9V, V <sub>LED</sub> = 3.1V to 5.25V | LEDx_RGE = 0x0 | -0.9     | -0.04 | +0.9 | mA/V  |
|                                                           |                     |                                                                                                           | LEDx_RGE = 0x1 | -0.06    |       |      |       |
|                                                           |                     |                                                                                                           | LEDx_RGE = 0x2 | -0.02    |       |      |       |
|                                                           |                     | LEDx_PA = 0xF2, V <sub>DD</sub> = 1.8V, V <sub>LEDx_DRV</sub> = 0.9V, V <sub>LED</sub> = 3.1V to 5.25V    | LEDx_RGE = 0x3 | -0.025   |       |      |       |
| Transmit Driver V <sub>DD</sub><br>DC PSR                 |                     | LEDx_PA = 0xFF, V <sub>LED</sub> = 3.3V, V <sub>LEDx_DRV</sub> = 0.9V, V <sub>DD</sub> = 1.7V to 2.0V     | LEDx_RGE = 0x0 | -4       | ±0.08 | +4   | mA/V  |
|                                                           |                     |                                                                                                           | LEDx_RGE = 0x1 | 0.014    |       |      |       |
|                                                           |                     |                                                                                                           | LEDx_RGE = 0x2 | 0.16     |       |      | µA/V  |
|                                                           |                     | LEDx_PA = 0xF2, V <sub>LED</sub> = 3.3V, V <sub>LEDx_DRV</sub> = 0.9V, V <sub>DD</sub> = 1.7V to 2.0V     | LEDx_RGE = 0x3 | 0.02     |       |      | mA/V  |
| LED Driver Compliance Interrupt                           | LED <sub>COMP</sub> | LEDx_RGE = 0x0, LED1_DRV only                                                                             |                | 170      |       |      | mV    |
| DIGITAL / I/O CHARACTERISTICS                             |                     |                                                                                                           |                |          |       |      |       |
| Output Low Voltage                                        | V <sub>OL</sub>     | SDA, $\overline{INT}$ , I <sub>SINK</sub> = 6mA                                                           |                | 0.4      |       |      | V     |
| I <sup>2</sup> C Input Voltage Low                        | V <sub>IL_I2C</sub> | SDA, SCL                                                                                                  |                | 0.4      |       |      | V     |
| I <sup>2</sup> C Input Voltage High                       | V <sub>IH_I2C</sub> | SDA, SCL                                                                                                  |                | 1.4      |       |      | V     |
| Input Hysteresis                                          | V <sub>HYS</sub>    | SDA, SCL                                                                                                  |                | 200      |       |      | mV    |
| Pin Capacitance                                           | C <sub>PIN</sub>    | SDA, SCL, $\overline{INT}$ (when inactive)                                                                |                | 10       |       |      | pF    |
| Pin Leakage Current                                       | I <sub>PIN</sub>    | SDA, SCL, $\overline{INT}$ (when inactive), T <sub>A</sub> = +25°C                                        |                | ±0.01 ±1 |       |      | µA    |
| DIGITAL / I <sup>2</sup> C TIMING CHARACTERISTICS, NOTE 3 |                     |                                                                                                           |                |          |       |      |       |
| I <sup>2</sup> C Write Address                            |                     |                                                                                                           |                | C0       |       |      | Hex   |
| I <sup>2</sup> C Read Address                             |                     |                                                                                                           |                | C1       |       |      | Hex   |
| Serial Clock Frequency                                    | f <sub>SCL</sub>    |                                                                                                           |                | 0        | 400   |      | kHz   |
| Bus Free Time Between STOP and START Conditions           | t <sub>BUF</sub>    |                                                                                                           |                | 1.3      | µs    |      |       |
| Hold Time START and Repeat START Condition                | t <sub>HD,STA</sub> |                                                                                                           |                | 0.6      | µs    |      |       |
| SCL Pulse-Width Low                                       | t <sub>LOW</sub>    |                                                                                                           |                | 1.3      | µs    |      |       |
| SCL Pulse-Width High                                      | t <sub>HIGH</sub>   |                                                                                                           |                | 0.6      | µs    |      |       |
| Setup Time for a Repeated START Condition                 | t <sub>SU,STA</sub> |                                                                                                           |                | 0.6      | µs    |      |       |

**Electrical Characteristics (continued)**

( $V_{DD} = V_{DD\_ANA} = V_{DD\_DIG} = 1.8V$ ,  $V_{LED} = 3.3V$ ,  $C_{LOAD} = 10pF$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1))

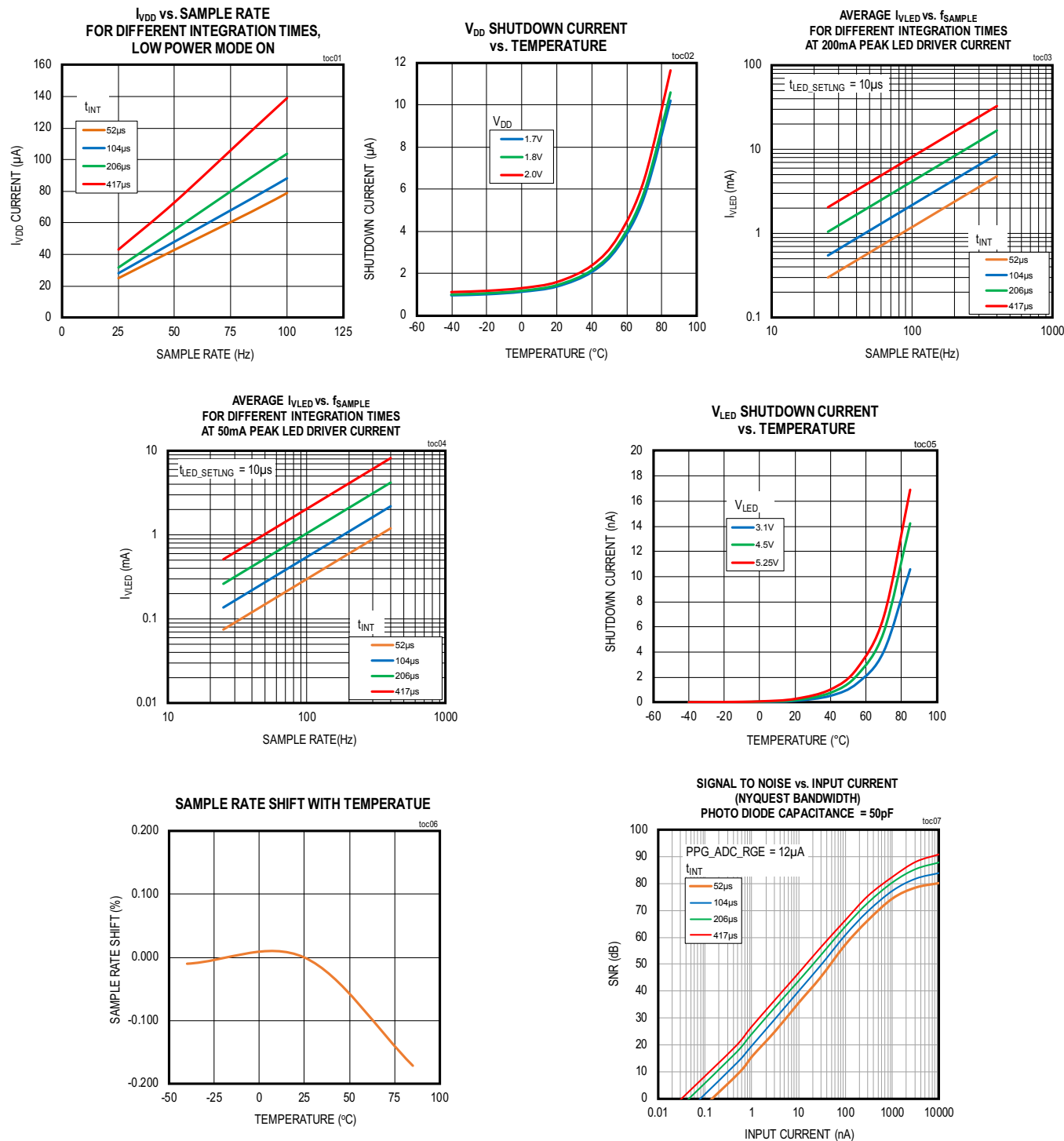
| PARAMETER                       | SYMBOL       | CONDITIONS | MIN           | TYP | MAX | UNITS   |
|---------------------------------|--------------|------------|---------------|-----|-----|---------|
| Data Hold Time                  | $t_{HD,DAT}$ |            | 0             |     | 900 | ns      |
| Data Setup Time                 | $t_{SU,DAT}$ |            | 100           |     |     | ns      |
| Setup Time for STOP Condition   | $t_{SU,STO}$ |            | 0.6           |     |     | $\mu s$ |
| Pulse Width of Suppressed Spike | $t_{SP}$     |            | 0             |     | 50  | ns      |
| Bus Capacitance                 | CB           |            |               |     | 400 | pF      |
| SDA and SCL Receiving Rise Time | $t_R$        |            | 20 +<br>0.1CB |     | 300 | ns      |
| SDA and SCL Receiving Fall Time | $t_F$        |            | 20 +<br>0.1CB |     | 300 | ns      |
| SDA Transmitting Fall Time      | $t_{TF}$     |            | 20 +<br>0.1CB |     | 300 | ns      |

**Note 1:** Limits are 100% tested at  $T_A = +25^{\circ}C$ . Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

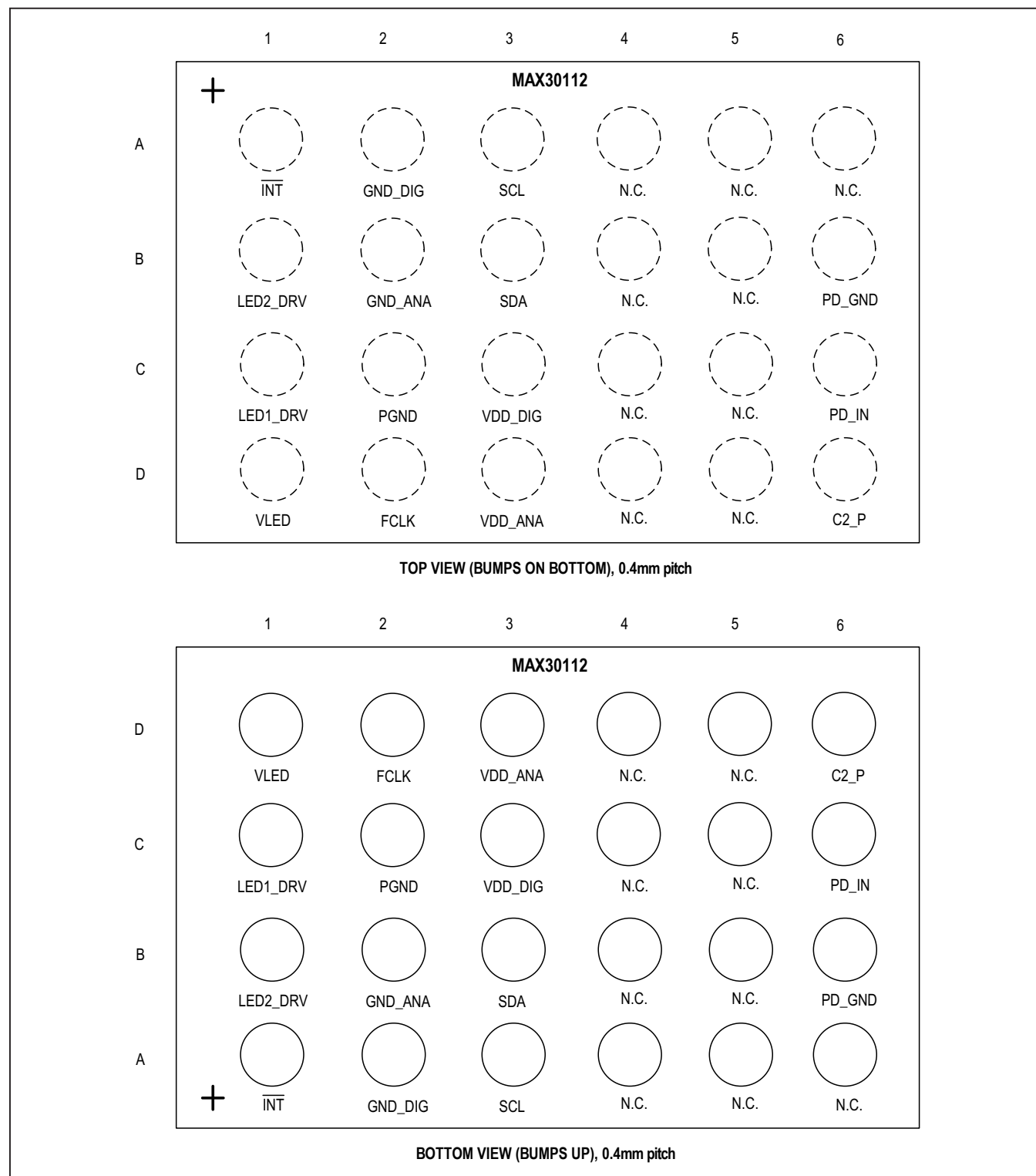
**Note 2:** Limit assumes that all user-programmable memory is programmed. If user programmable memory is left unprogrammed, currents can exceed the limit shown.

## Typical Operating Characteristics

VDD\_ANA = VDD\_DIG = 1.8V, VLED = 3.3V, GND\_ANA = GND\_DIG = PGND = 0V, T<sub>A</sub> = +25°C, min/max are from T<sub>A</sub> = -40°C to +85°C, unless otherwise noted. (Note 2)



## Pin Configurations



## Pin Description

| PIN                                      | NAME     | FUNCTION                                                                                                                                 |
|------------------------------------------|----------|------------------------------------------------------------------------------------------------------------------------------------------|
| <b>POWER</b>                             |          |                                                                                                                                          |
| C3                                       | VDD_DIG  | Digital Logic Supply. Connect to externally-regulated supply. Suggest to connect to VDD_ANA.                                             |
| A2                                       | GND_DIG  | Digital Logic and Digital Pad Return. Suggest to connect to common PCB ground.                                                           |
| D3                                       | VDD_ANA  | Analog Supply. Connect to externally-regulated supply. Bypass with a 0.1μF as close as possible to bump and a 10μF capacitor to GND_ANA. |
| B2                                       | GND_ANA  | Analog Power Return. Suggest to connect to common PCB ground.                                                                            |
| D1                                       | V_LED    | LED Power Supply Input. Connect to external voltage supply. Bypass with a 10μF capacitor to PGND.                                        |
| C2                                       | PGND     | LED Power Return.                                                                                                                        |
| <b>CLOCK</b>                             |          |                                                                                                                                          |
| D2                                       | FCLK     | Optional External Clock input. Leave FCLK unconnected/floating, if external clock is not used.                                           |
| <b>I<sup>2</sup>C CONTROL INTERFACE</b>  |          |                                                                                                                                          |
| A3                                       | SCL      | SCL Input. I <sup>2</sup> C clock input                                                                                                  |
| B3                                       | SDA      | SDA Input/Output. I <sup>2</sup> C data I/O                                                                                              |
| A1                                       | INT      | Interrupt. Programmable Open-Drain Interrupt output signal pin (Active Low)                                                              |
| <b>OPTICAL</b>                           |          |                                                                                                                                          |
| C6                                       | PD_IN    | Photodiode Cathode Input. Keep traces as short as possible, shield with PD_GND.                                                          |
| B6                                       | PD_GND   | Photodiode Anode. Connect to PCB GND plane only at PD_GND pin. Use as shield trace for PD_IN.                                            |
| C1                                       | LED_DRV1 | LED Driver Output 1. Connect the LED cathode to LED_DRV1 output and its anode to the V_LED supply.                                       |
| B1                                       | LED_DRV2 | LED Driver Output 2. Connect the LED cathode to LED_DRV2 output and its anode to the V_LED supply.                                       |
| <b>REFERENCE</b>                         |          |                                                                                                                                          |
| D6                                       | C2_P     | Internal Reference Decoupling Point. Bypass with a 10μF capacitor to GND_ANA                                                             |
| <b>N.C.</b>                              |          |                                                                                                                                          |
| A4, A5, A6,<br>B4, B5, C4,<br>C5, D4, D5 | N.C.     | No Connection. Internally connected, leave N.C. unconnected.                                                                             |

## Detailed Description

The MAX30112 is a complete optical pulse oximetry and heart rate detection integrated analog front-end readout circuit designed for the demanding requirements of mobile and wearable devices. Minimal external hardware components are necessary for integration into a mobile device. The MAX30112 is fully adjustable through software registers, with the digital output data being stored in a 32-samples FIFO within the IC.

### Optical Subsystem

The optical subsystem in MAX30112 is composed of ambient light cancellation (ALC), a continuous-time, sigma-delta ADC, and proprietary discrete time filter. ALC incorporates a proprietary scheme to cancel ambient-light-generated photo diode current up to 200 $\mu$ A, allowing the sensor to work in high ambient light conditions. The ADC has programmable full-scale ranges of between 6 $\mu$ A and 48 $\mu$ A. The internal ADC is a continuous-time oversampling sigma-delta converter with 19-bit resolution. The ADC output data rate can be programmed from 20sps (samples per second) to 3200sps. The MAX30112 includes a proprietary discrete time filter to reject 50Hz/60Hz interference and changing residual ambient light from the sensor measurements.

MAX30112 supports Dynamic Power Down mode (Low Power mode) in which the power consumption is decreased between samples. This mode is only supported for sample rates 100sps and below. For more details on the power consumption at each sample rates, refer to the [Electrical Characteristics](#) table.

### LED Driver

The MAX30112 integrates two precision LED-driver-current DACs that modulate LED pulses for both SpO<sub>2</sub> and HR measurements. The LED current DACs have 8-bits of dynamic range with four programmable full-scale ranges of 50mA, 100mA, 150mA, and 200mA. The LED drivers are low-dropout current sources, allowing for

low-noise, power-supply independent LED currents to be sourced at the lowest supply voltage possible; thus minimizing LED power consumption. The LED pulse width and the LED settling time can be programmed to allow the algorithms to optimize SpO<sub>2</sub> and HR accuracy at the lowest dynamic power consumption dictated by the application.

### I<sup>2</sup>C/SMBus Compatible Serial Interface

The MAX30112 features an I<sup>2</sup>C/SMBus™ compatible, 2-wire serial interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX30112 and the master at clock rates up to 400kHz.

Figure 1 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX30112 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX30112 is 8-bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX30112 transmits the proper slave address followed by a series of nine SCL pulses. The MAX30112 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START (S) or REPEATED START (Sr) condition, a not acknowledge, and a STOP (P) condition. SDA operates as both an input and an open-drain output. A pullup resistor is required on SDA. SCL operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX30112 from high voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

### Detailed I<sup>2</sup>C Timing Diagram

The detailed timing diagram of various electrical characteristics is shown in [Figure 1](#).

#### Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the [START and STOP Conditions](#) section).

#### START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high ([Figure 2](#)). A START condition from the master signals the beginning of a transmission to the MAX30112. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

#### Early STOP Conditions

The MAX30112 recognizes a STOP condition at any point during data transmission unless the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

#### Slave Address

The slave address is defined as the seven most significant bits (MSBs), followed by the read/write bit. For the MAX30112, the seven most significant bits are 0b1100000. For read mode, set the read/write bit to 1 (slave address = 0xC1). For write mode, set the read/write bit to 0 (slave address = 0xC0). The address is the first byte of information sent to the IC after the START condition.

#### Acknowledge Bit

The acknowledge bit (ACK) is a clocked 9th bit that the MAX30112 uses to handshake receipt each byte of data when in write mode ([Figure 3](#)). The MAX30112 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master will retry communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX30112 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not-acknowledge is sent when the master reads the final byte of data from the MAX30112, followed by a STOP condition.

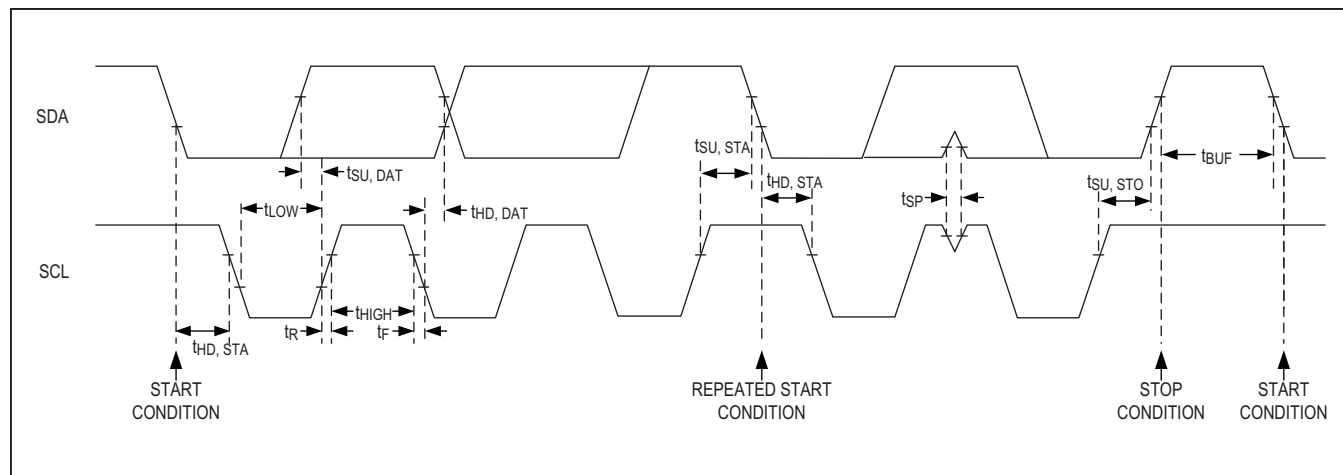


Figure 1. Detailed I<sup>2</sup>C Timing Diagram

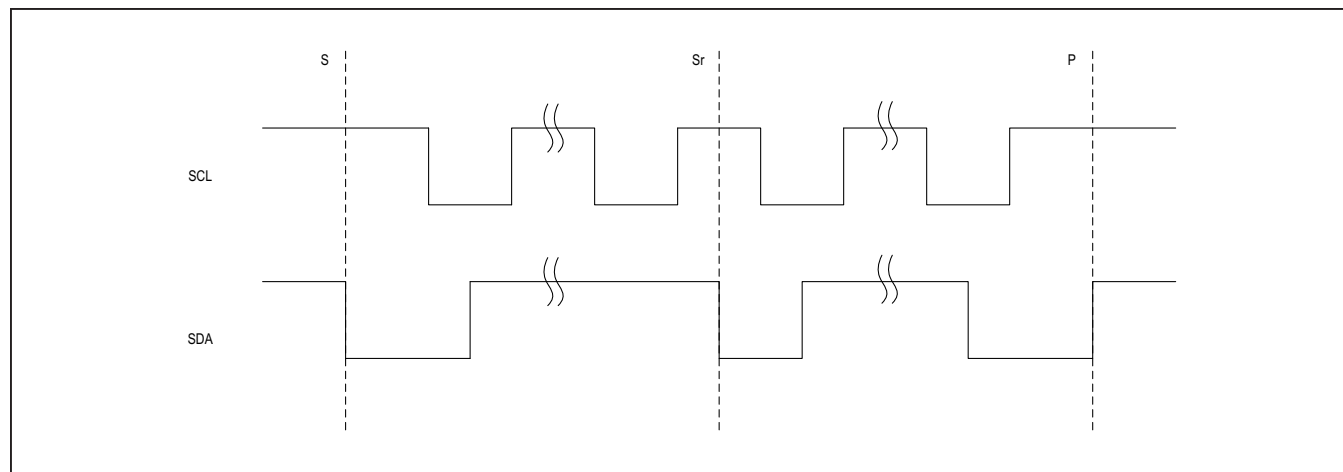


Figure 2: I<sup>2</sup>C START, STOP, and REPEATED START Condition

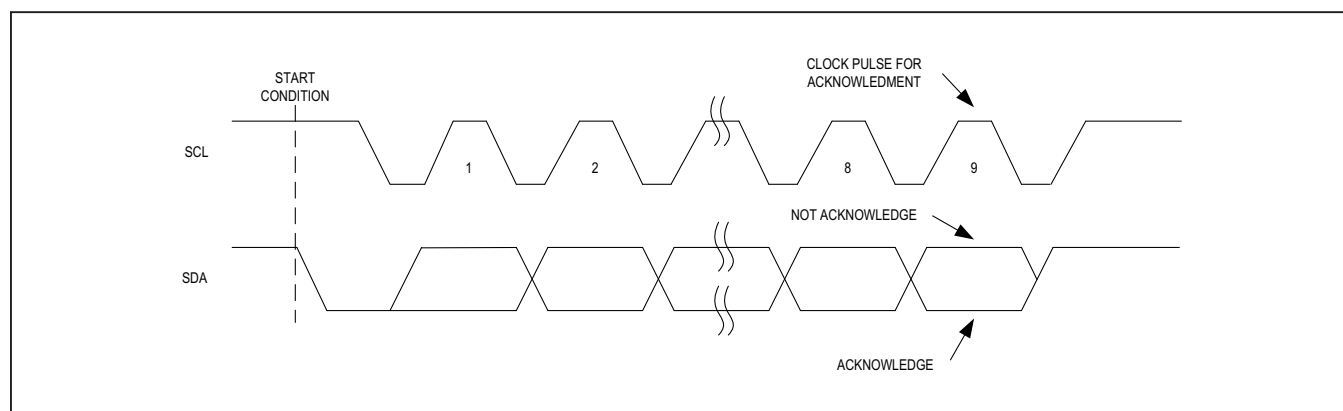


Figure 3. I<sup>2</sup>C Acknowledge Bit

## I<sup>2</sup>C Write Data Format

A write to the MAX30112 includes transmission of a START condition, the slave address with the  $R/\overline{W}$  bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition.

[Figure 4](#) illustrates the proper frame format for writing one byte of data to the MAX30112. [Figure 5](#) illustrates the frame format for writing n-bytes of data to the MAX30112.

The slave address with the  $\overline{R}/\overline{W}$  bit set to 0 indicates that the master intends to write data to the MAX30112. The MAX30112 acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX30112's internal register address pointer. The pointer tells the MAX30112 where to write the next byte of data. An acknowledge pulse is sent by the MAX30112 upon receipt of the address pointer data.

The third byte sent to the MAX30112 contains the data that will be written to the chosen register. An acknowledge pulse from the MAX30112 signals receipt of the data byte. The address pointer auto increments to the next register address after each received data byte. This auto-increment feature allows a master to write to sequential registers within one continuous frame. The master signals the end of transmission by issuing a STOP condition. The auto\_increment feature is disabled when there is an attempt to write to the FIFO DATA register.

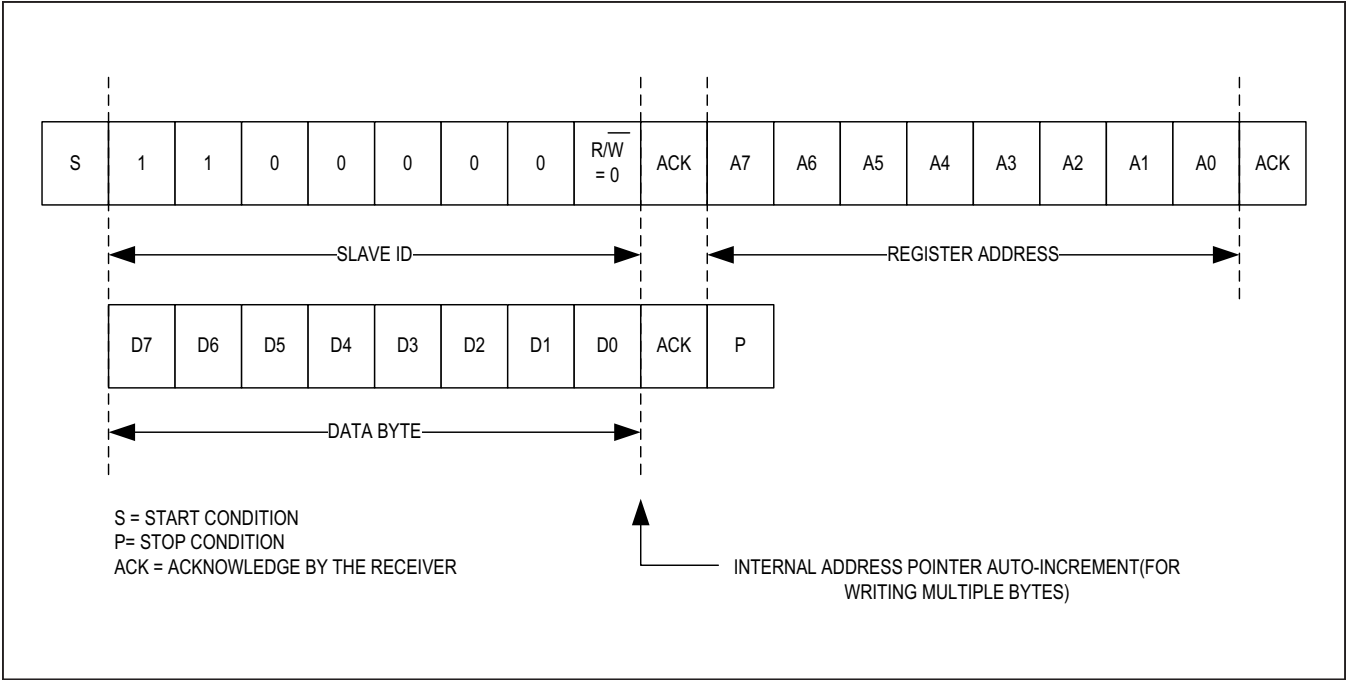


Figure 4. I2C Single-Byte Write Transaction

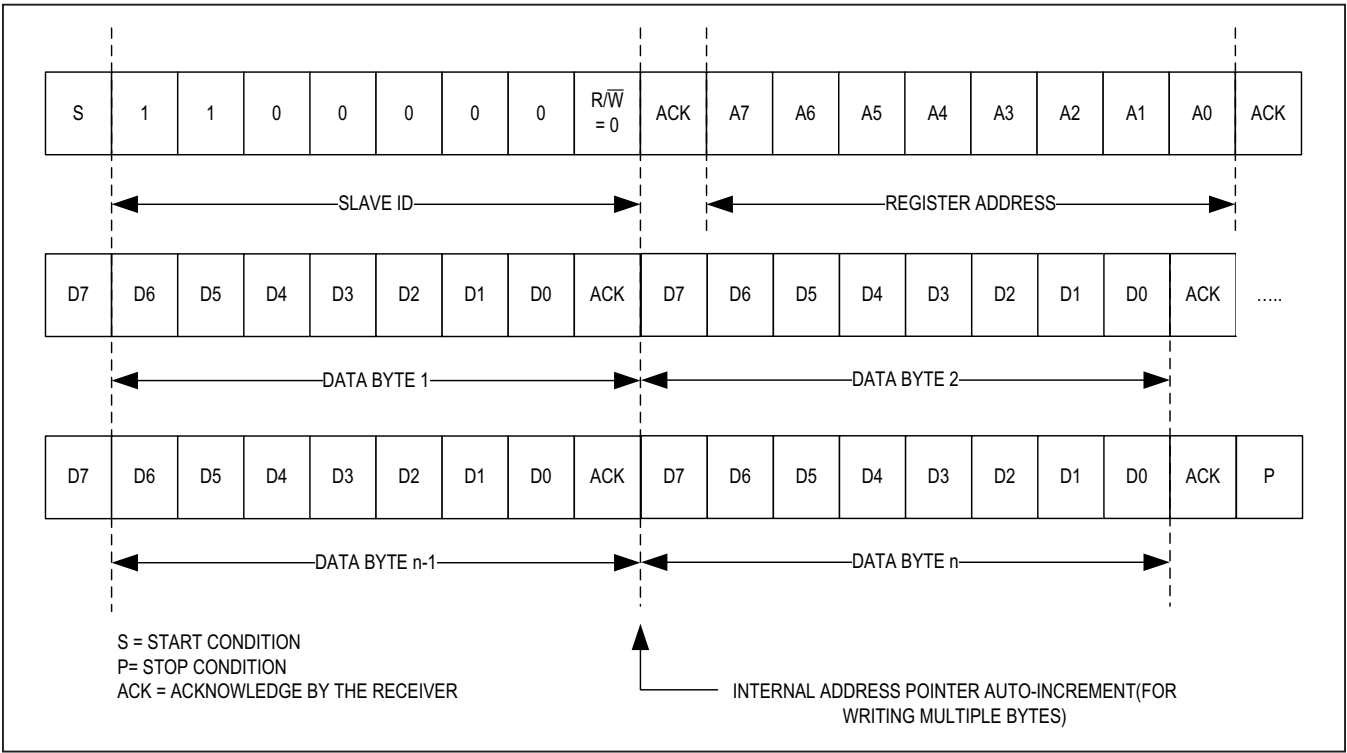


Figure 5. I2C Multi-Byte Write Transaction

I2C Read Data Format

Send the slave address with the  $\overline{R/\overline{W}}$  bit set to 1 to initiate a read operation. The MAX30112 acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX30112 will be the contents of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer auto-increments after each read data byte. This auto-increment feature allows all registers to be read sequentially within one continuous frame. The auto\_increment feature is disabled when there is an attempt to read from the FIFO\_DATA register. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read will be from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX30112 slave address with the  $\overline{R/\overline{W}}$  bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the  $\overline{R/\overline{W}}$  bit set to 1. The MAX30112 then transmits the contents of the specified register. The address pointer auto-increments after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. [Figure 6](#) illustrates the frame format for reading one byte from the MAX30112. [Figure 7](#) illustrates the frame format for reading multiple bytes from the MAX30112.

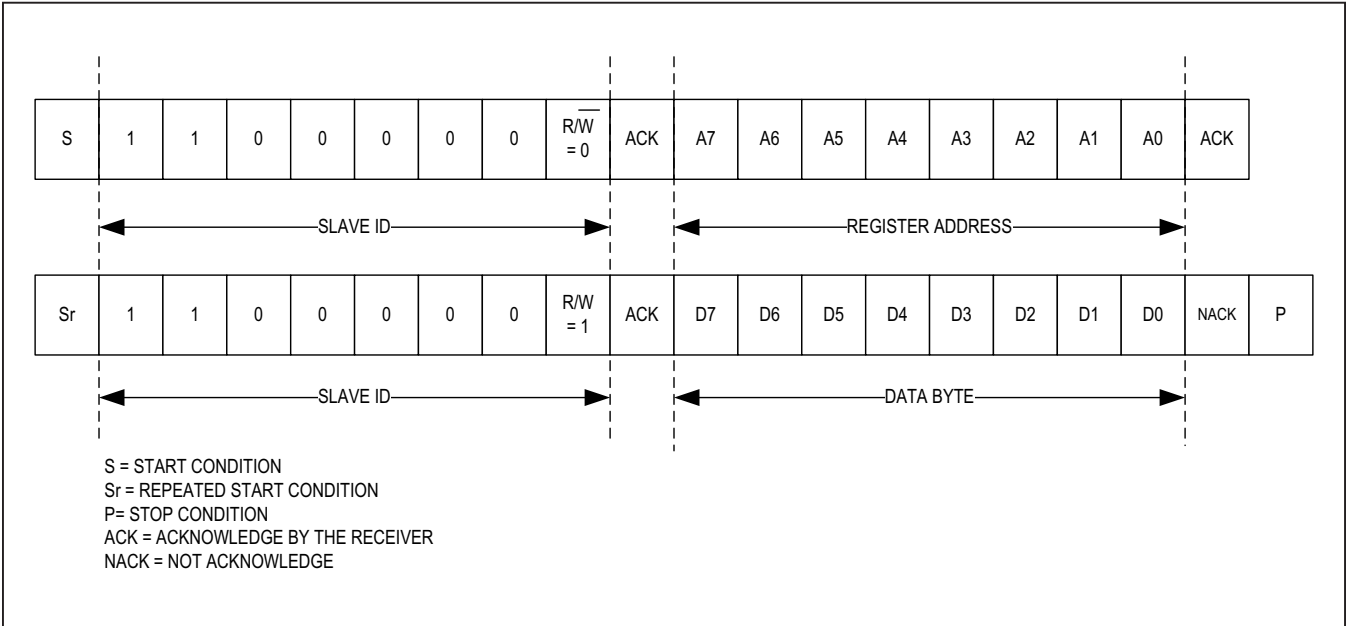


Figure 6. I2C Single-Byte Read Transaction

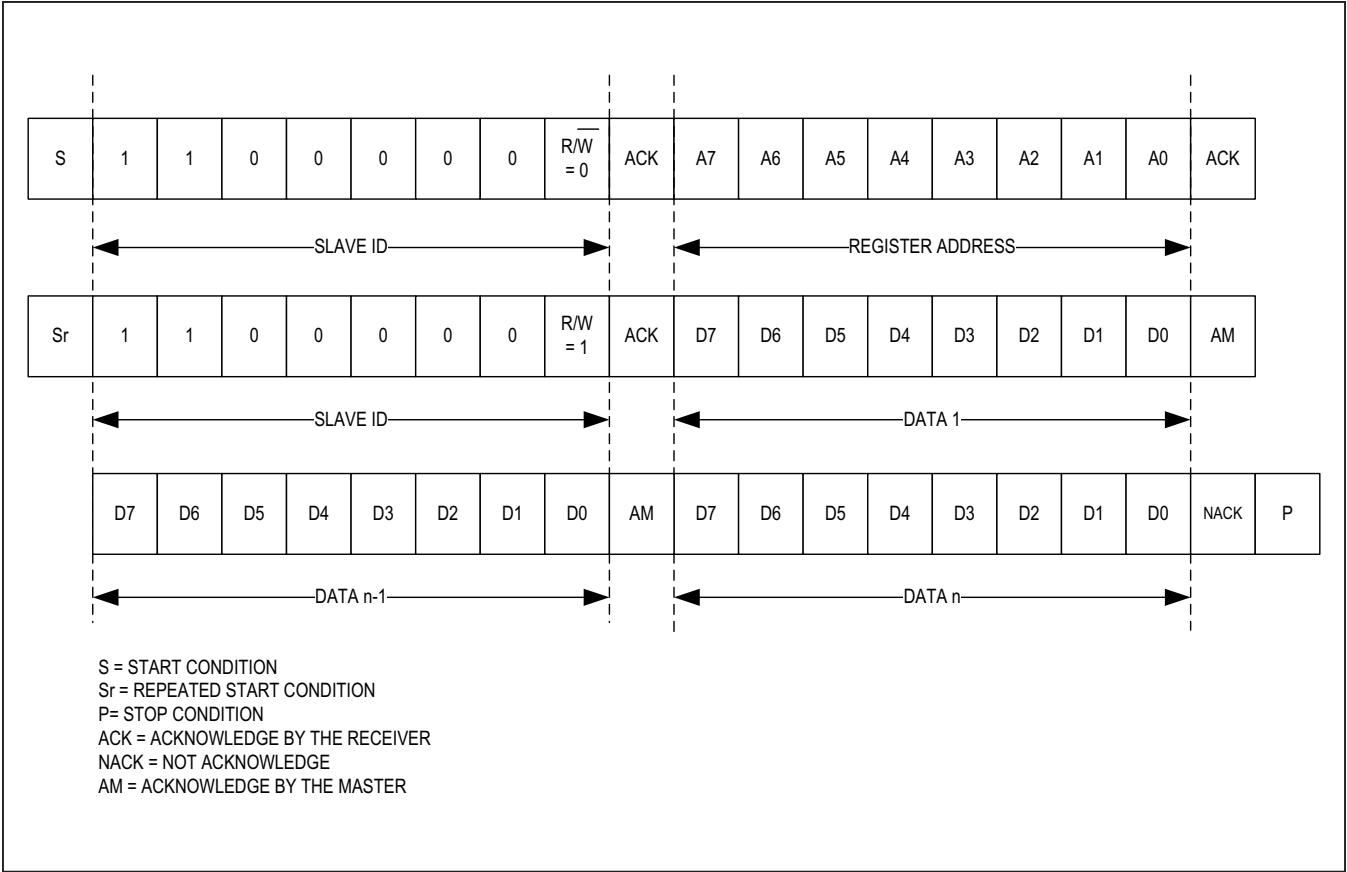


Figure 7. I2C Multi-Byte Read Transaction

**FIFO Configuration**

The FIFO can hold up to 32 samples of data, with each sample comprised of up to 4 data items (time slots). Each data item is 3 bytes. The content of each data item is programmed through register FD1 to FD4 (FIFO data control). These data items are ADC counts from the analog front-end of this device. The FIFO supports the following features:

- Maximum 32 samples (depth)
- Supports up to four data items in each sample
- FIFO roll-on full
- Different interrupt modes based on watermark

There are seven registers that control how the FIFO is configured and read out. These registers are illustrated below.

**FIFO Data Control (Address 0x09 and 0x0A)**

The data format in the FIFO, as well as the sequencing of exposures, are controlled by the FIFO Data Control registers through FD1 through FD4. There are four FIFO data items available, each holding up to 32 samples. The exposure sequence cycles through the FIFO data bit fields, starting from FD1 to FD4. The first FIFO data field set to NONE (0000) ends the sequence.

**Table 1. FIFO Information, Control and Configuration Registers**

| ADDRESS | REGISTER NAME       | DEFAULT VALUE | B7             | B6            | B5          | B4               | B3               | B2       | B1 | B0 |
|---------|---------------------|---------------|----------------|---------------|-------------|------------------|------------------|----------|----|----|
| 0X04    | FIFO Write Pointer  | 00            | -              | -             | -           | FIFO_WR_PTR[4:0] |                  |          |    |    |
| 0X05    | Overflow Counter    | 00            | -              | -             | -           | OVF_COUNTER[4:0] |                  |          |    |    |
| 0X06    | FIFO Read Pointer   | 00            | -              | -             | -           | FIFO_RD_PTR[4:0] |                  |          |    |    |
| 0X07    | FIFO Data Register  | 00            | FIFO_DATA[7:0] |               |             |                  |                  |          |    |    |
| 0X08    | FIFO Configuration  | 0F            | -              | FIFO_STAT_CLR | A_FULL_TYPE | FIFO_RO          | FIFO_A_FULL[3:0] |          |    |    |
| 0x09    | FIFO Data Control 1 | 00            | FD2[3:0]       |               |             |                  |                  | FD1[3:0] |    |    |
| 0x0A    | FIFO Data Control 2 | 00            | FD4[3:0]       |               |             |                  |                  | FD3[3:0] |    |    |

**Table 2: Data Items Type for FIFO Control Registers**

| FDX[3:0]* | DATA TYPE      | FIFO DATA CONTENT | NOTE                     |
|-----------|----------------|-------------------|--------------------------|
| 0000      | NONE           | -                 | -                        |
| 0001      | LED1           | PPG_DATA[18:0]    | MS bits should be masked |
| 0010      | LED2           | PPG_DATA[18:0]    | MS bits should be masked |
| 0011      | Reserved       | -                 | -                        |
| 0100      | Reserved       | -                 | -                        |
| 0101      | PILOT LED1     | PPG_DATA[18:0]    | MS bits should be masked |
| 0110      | Reserved       | -                 | -                        |
| 0111      | Reserved       | -                 | -                        |
| 1000      | Reserved       | -                 | -                        |
| 1001      | Reserved       | -                 | -                        |
| 1010      | Reserved       | -                 | -                        |
| 1011      | Reserved       | -                 | -                        |
| 1100      | DIRECT_AMBIENT | PPG_DATA[18:0]    | MS bits should be masked |
| 1101      | LED1 and LED2  | PPG_DATA[18:0]    | MS bits should be masked |
| 1110      | Reserved       | -                 | -                        |
| 1111      | Reserved       | --                | -                        |

\* Note: In FDX, x is 1, 2, 3, or 4 for the corresponding FIFO bank.

**Write Pointer (Register 0X04)**

FIFO\_WR\_PTR[4:0] points to the FIFO location where the next sample will be written. This pointer advances for each sample pushed on to the FIFO by the internal conversion process. The write pointer is a 5-bit counter and will wrap around to count 0x00 on the next sample after count 0x1F.

**Overflow Counter (Register 0X05)**

OVF\_COUNTER[4:0] logs the number of samples lost if the FIFO is not read in a timely fashion. This counter holds at count value 0x1F. When a complete sample is popped from the FIFO (when the read pointer advances), and OVF\_COUNTER is reset to zero. This counter is essentially a debug tool. It should be read immediately before reading the FIFO in order to check if an overflow condition has occurred.

**Read Pointer (Register 0X06)**

FIFO\_RD\_PTR[4:0] points to the location from where the next sample from the FIFO will be read through the interface. This advances each time a sample is read from the FIFO. The read pointer can be both read and written to. This allows a sample to be reread from the FIFO if it has not already been overwritten. The read pointer is updated from a 5-bit counter and will wrap around to count 0x00 from count 0x1F.

**FIFO Data (Register 0X07)**

FIFO\_DATA[7:0] is a read-only register used to retrieve data from the FIFO. The format and data type of the data stored in the FIFO is determined by the FIFO data control register. Readout from the FIFO follows a progression defined by the FIFO data control register as well. This configuration is best illustrated by a few examples.

Assume it is desired to perform an SpO<sub>2</sub> measurement simultaneously with monitoring the ambient level on the photodiode to adjust the IR and red LED intensity. To perform this measurement, config the following registers,

**FIFO Data Control field**

```
FD1[3:0] = 0x1 (LED1)
FD2[3:0] = 0x2 (LED2)
FD3[3:0] = 0xC (DIRECT_AMBIENT)
FD4[3:0] = 0x0 (NONE)
```

**PPG Configuration**

```
PPG_ADC_RGE[1:0] (Gain Range Control)
PPG_SR[3:0]      (Sample Rate Control)
PPG_TINT[1:0]    (Integration Time)
```

**LED Pulse Amplitude**

```
LED1_PA[7:0] (LED1 Current Pulse Amplitude)
LED2_PA[7:0] (LED2 Current Pulse Amplitude)
```

When done, the sample sequence and the data format in the FIFO will follow the following time/location sequence.

```
LED1 sample 1
LED2 sample 1
DIRECT_AMBIENT sample 1
LED1 sample 2
LED2 sample 2
DIRECT_AMBIENT sample 2
.
.
.
LED1 sample n
LED2 sample n
DIRECT_AMBIENT sample n
```

where:

LED1 sample x = ambient light corrected photodiode ADC count exposure data from LED1 for the sample x

LED2 sample x = ambient light corrected photodiode ADC count exposure data from LED2 for the sample x

DIRECT\_AMBIENT sample x = direct ambient sample x

n is the number of samples in the FIFO, which can be up to 32 samples.

For a second example, assume it is desired to pulse LED1 and LED2 simultaneously while also monitoring the ambient level. In this case, set the following registers,

**FIFO Data Control field**

```
FD1[3:0] = 0xD (LED1 and LED2)
FD2[3:0] = 0xC (DIRECT_AMBIENT)
FD3[3:0] = 0x0 (NONE)
FD4[3:0] = 0x0 (NONE)
```

The sequencing in the FIFO will then be,

```
LED1 and LED2 sample1
DIRECT_AMBIENT sample 1
LED1 and LED2 sample2
DIRECT_AMBIENT 2
.
.
.
LED1 and LED2 sample n
DIRECT_AMBIENT n
```

where:

LED1 and LED2 sample x = ambient light corrected photodiode ADC count exposure data when both LED1 and LED2 are active simultaneously

DIRECT\_AMBIENT sample x = direct ambient corrected sample x

The number of bytes of active data samples is given by:  
3 x K x N,

where:

K = the number of active sampled channels as defined in the FIFO\_Data\_Control register 0x09 and 0x0A

N = the number of active data samples in the FIFO

The number of active data samples in the FIFO is directly readable by subtracting the FIFO\_RD\_PTR[4:0] from the FIFO\_WR\_PTR[4:0], and taking wrap around of the pointers into consideration. It is typically controlled in the system by generating an interrupt on the INT line when the FIFO reaches a watermark level computed from the FIFO\_A\_FULL[3:0] field in the FIFO Configuration register (0x08). In this case, when the active data samples in the FIFO reach a level given by 32 - FIFO\_A\_FULL[3:0], an A\_FULL interrupt is generated.

To calculate the number of active samples when the  $\overline{\text{INT}}$  signal is asserted, execute the following pseudo-code:

```
read the OVF_COUNTER register
read the FIFO_WR_PTR register
read the FIFO_RD_PTR register
if (OVF_COUNTER == 0), then // no overflow
occurred
    if (FIFO_WR_PTR > FIFO_RD_PTR) then
        NUM_AVAILABLE_SAMPLES = FIFO_WR_PTR
        - FIFO_RD_PTR
    else
        NUM_AVAILABLE_SAMPLES = FIFO_WR_PTR
        + 32 - FIFO_RD_PTR
    endif
else
    NUM_AVAILABLE_SAMPLES = 32 // overflow
    occurred and data has been lost
endif
```

FIFO data format depends on the data type being stored. Optical data, whether ambient-corrected LED exposure, ambient-corrected proximity, or direct ambient-sampled data is as shown in the [Table 3](#). The ADC data is left-justified at FIFO\_DATA[18] and the MSBs (FIFO\_DATA[23:18]) are don't care and should be masked as shown in [Table 3](#). In other words, the MSB bit of the ADC data is always in the bit 18 position.

The ADC resolution is set by the PPG\_LED\_PW[1:0] in the PPG Configuration 1 Register. This field generates an ADC resolution of 19, 18, 17, or 16 bits and is tied to the selected integration time of 417μs, 206μs, 104μs, or 52μs, respectively. In lower ADC resolutions, the unused LSBs should be masked.

**Table 3. Integration Pulse Width, Resulting ADC Resolution, and FIFO Data Format**

|                            |            | FIFO DATA FORMAT (FIFO_DATA[23:0]) |     |     |     |     |     |     |     |     |     |     |     |     |     |    |    |    |    |    |    |    |    |    |    |  |  |  |  |
|----------------------------|------------|------------------------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|----|----|----|----|----|----|----|----|----|--|--|--|--|
| Integration<br>Pulse Width | ADC<br>Res | ADC Value                          |     |     |     |     |     |     |     |     |     |     |     |     |     |    |    |    |    |    |    |    |    |    |    |  |  |  |  |
|                            |            | F23                                | F22 | F21 | F20 | F19 | F18 | F17 | F16 | F15 | F14 | F13 | F12 | F11 | F10 | F9 | F8 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 |  |  |  |  |
| 417μs                      | 19-bits    | X                                  | X   | X   | X   | X   | 018 | 017 | 016 | 015 | 014 | 013 | 012 | 011 | 010 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |  |  |  |  |
| 206μs                      | 18-bits    | X                                  | X   | X   | X   | X   | 018 | 017 | 016 | 015 | 014 | 013 | 012 | 011 | 010 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | X  |  |  |  |  |
| 104μs                      | 17-bits    | X                                  | X   | X   | X   | X   | 018 | 017 | 016 | 015 | 014 | 013 | 012 | 011 | 010 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | X  | X  |  |  |  |  |
| 52μs                       | 16-bits    | X                                  | X   | X   | X   | X   | 018 | 017 | 016 | 015 | 014 | 013 | 012 | 011 | 010 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | X  | X  | X  |  |  |  |  |

**FIFO Almost Full (Watermark)**

The FIFO\_A\_FULL[3:0] register in the FIFO\_Configuration register (0x08) determines when the A\_FULL bit in the Interrupt\_Status 1 register (0x00) gets asserted. The FIFO is almost full when it has 32 minus FIFO\_A\_FULL[3:0] samples. Then, if A\_FULL\_EN mask bit in the Interrupt\_Enable 1 register (0x02) is set, the A\_FULL bit in the Interrupt\_Status 1 will be set and routed to the INT pin on the MAX30112 interface. This condition prompts the Application Processor to read samples from the FIFO before it gets filled. The A\_FULL bit is cleared and INT is deasserted when the status register is read, or when the FIFO\_DATA register (0x07) is read and FIFO\_STAT\_CLR (0x08) bit is set.

When the application processor receives an interrupt, there are at least 32 minus FIFO\_A\_FULL[3:0] samples available in the FIFO. It is not necessary to read the FIFO\_WR\_PTR and FIFO\_RD\_PTR registers. The Application Processor may read all the available samples in the FIFO, or only a portion of it. At high sample rates, it is recommended that only a portion of the available samples are read on an A\_FULL interrupt, to ensure that FIFO reading does not happen when the next sample conversion is in progress. The remaining samples will be read on the next interrupt.

If the A\_FULL interrupt is not enabled, the Application Processor has to read the FIFO in polling mode. In this mode the Application Processor has to read the FIFO\_WR\_PTR and FIFO\_RD\_PTR registers to calculate the number of samples available in the FIFO, and then decide how many samples to read. However, polling mode is not recommended, because in this mode an interface transaction will inevitably overlap an optical sample, potentially adding noise to the optical data. Because of this concern, the interface transaction should occur during the dead time between optical samples to avoid adding additional noise.

**FIFO\_RO (FIFO Rollover)**

The FIFO\_RO bit in the FIFO\_Configuration register (0x08) determines whether samples get pushed on to the FIFO when it is full. If push is enabled when FIFO is full, old samples are lost. If FIFO\_RO is not set, the new sample is dropped and the FIFO is not updated.

**A\_FULL\_TYPE**

The A\_FULL\_TYPE bit defines the behavior of the A\_FULL interrupt. If the A\_FULL\_TYPE bit is set low, the A\_FULL interrupt gets asserted when the A\_FULL condition is detected and cleared by status register read, but reasserts for every sample if the A\_FULL condition persists.

If A\_FULL\_TYPE bit is set high, the A\_FULL interrupt gets asserted only when the A\_FULL condition is detected. The interrupt gets cleared on status register read, and does not re-assert for every sample until a new A\_FULL condition is detected.

**FIFO\_STAT\_CLR**

The FIFO\_STAT\_CLR bit defines whether the A-FULL interrupt should get cleared by FIFO\_DATA register read. If FIFO\_STAT\_CLR is set low, A\_FULL and DATA\_RDY interrupts do not get cleared by FIFO\_DATA register read but get cleared by status register read. If FIFO\_STAT\_CLR is set high, A\_FULL and DATA\_RDY interrupts get cleared by a FIFO\_DATA register read or a status register read.

**Optical Timing**

The AFE can be configured to make a variety of measurements which involves the following options:

- LED1
- LED2
- LED1 + LED2
- Direct Ambient Measurement

For more details on the available modes, refer to [FIFO Configuration](#) section.

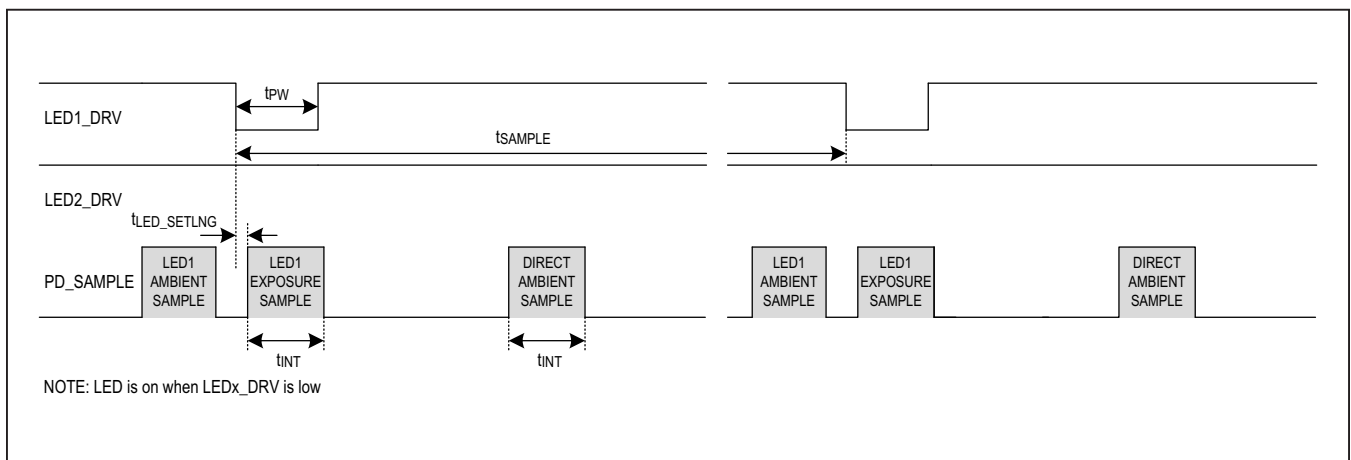
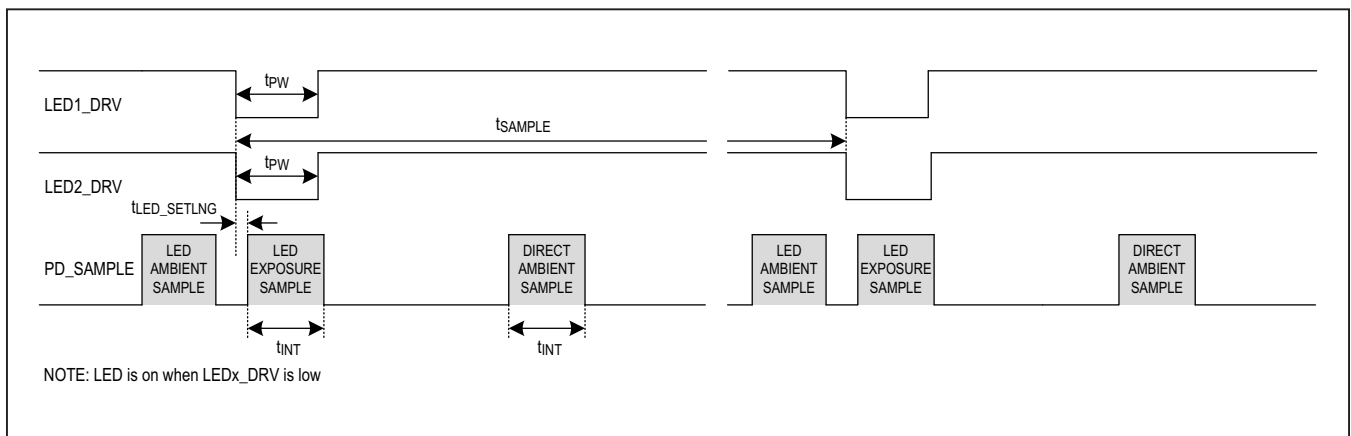
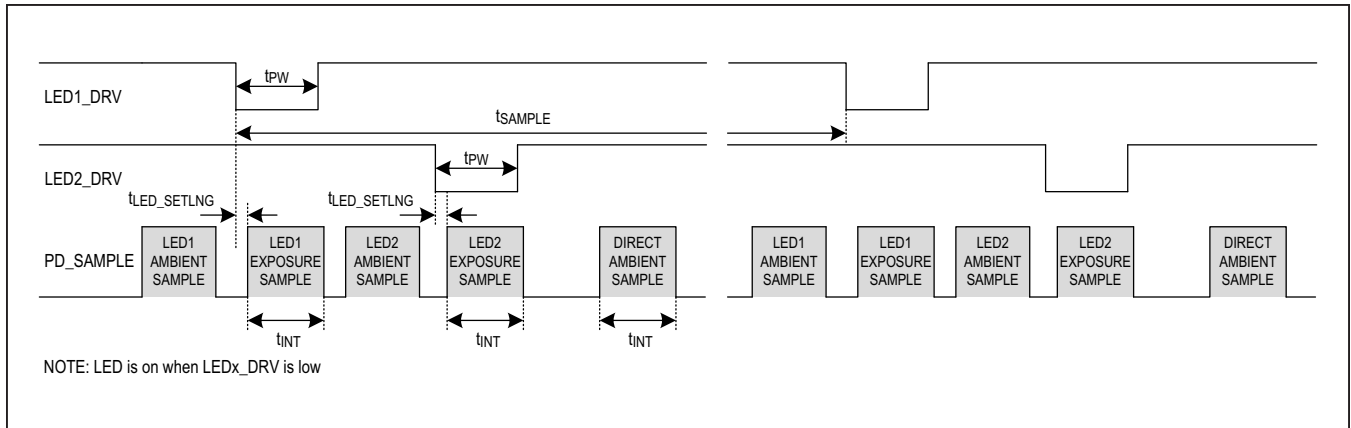
The “LED Ambient Sample” is integrated without turning on the LED, while “LED Exposure Sample” is integrated with LED illumination driven by the on-chip LED driver. Each “LED Exposure Sample” output is then compensated by the “LED Ambient Sample” at the front-end before the ADC conversion. The final FIFO exposure value for each LED mode represents an ambient corrected LED exposure signal.

The controller is also configurable to measure direct ambient level for every exposure sample. The direct ambient measurement can be used to adjust the LED drive level to compensate for increased noise levels when high interfering ambient signals are present.

The following optical timing diagrams illustrate the possible measurement configurations.

**Sequential LED1 and LED2 Pulsing with Direct Ambient Sampling**

The optical timing diagram in [Figure 8](#) illustrates the optical timing when both LED1 and LED2 are enabled to pulse sequentially followed by a direct ambient measurement. This timing mode is an example of when measuring SpO<sub>2</sub> with IR and red LEDs. The converted values of the optical measurements made by each LED followed by the converted direct ambient value will appear successively in the FIFO.



Dual-LED Pulsing with Direct Ambient Sampling

The optical timing diagram in [Figure 9](#) represents both LED1 and LED2 pulsing simultaneously with direct ambient sampling enabled. This timing mode would be used when heart rate is being measured with two green LEDs. In this mode, a single optical sampled value followed by the ambient sampled value will appear in successive the FIFO locations.

LED1 Pulsing with Direct Ambient Sampling

The optical timing diagram in [Figure 10](#) represents only LED1 pulsing during the data sampling time with direct ambient sampling enabled. This timing mode would be used when heart rate is being measured with a single green LED. In this mode, a single optical-sampled value, followed by the ambient sampled value, will appear successively in the FIFO.

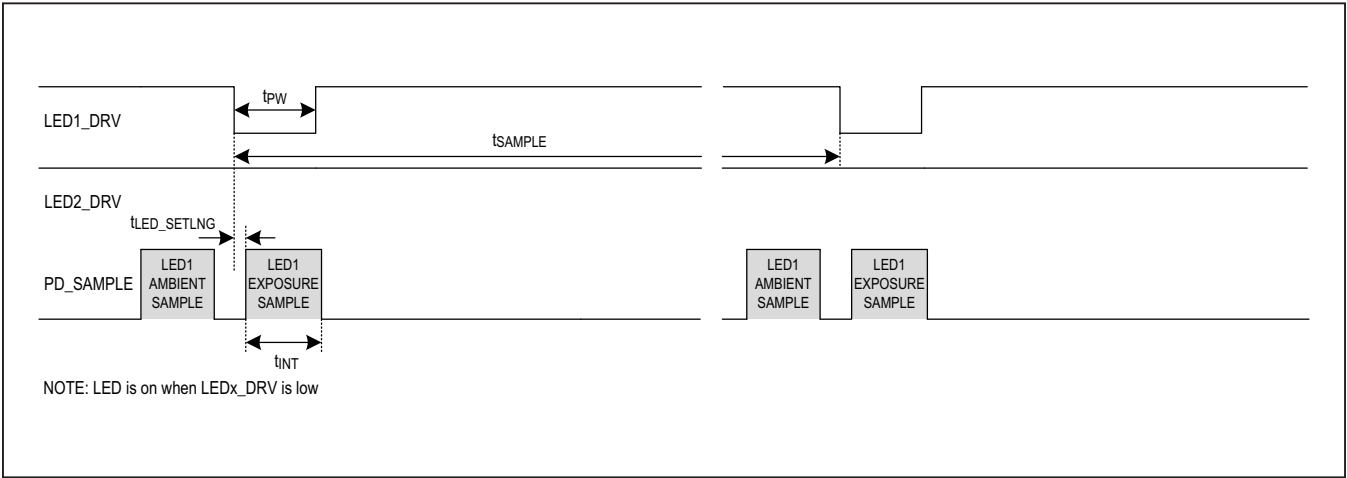


Figure 11: Timing for LED1 Pulsing with No Ambient Sampling

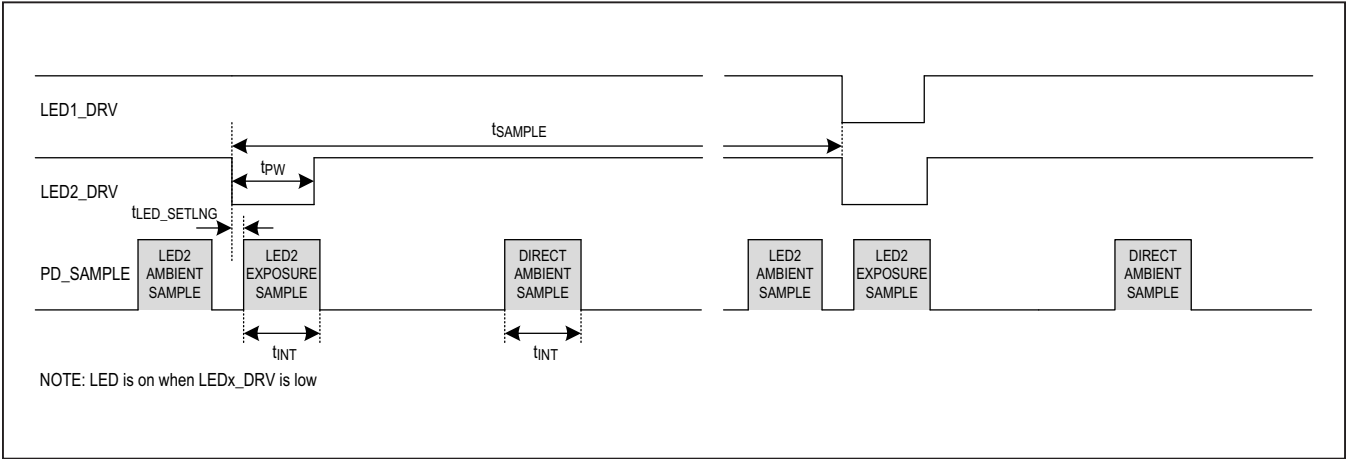


Figure 12: Timing for LED2 Pulsing with Direct Ambient Sampling

**LED1 Pulsing with No Ambient Sampling**

The optical timing diagram in [Figure 11](#) represents only LED1 pulsing during the data sampling time with no direct ambient sampling enabled. This timing mode would be used when heart rate is being measured with a single green LED. In this mode, a single optical sampled value will appear successively in the FIFO.

**LED2 Pulsing with Direct Ambient Sampling**

The optical timing diagram in [Figure 12](#) represents only LED2 firing during the data sampling time with direct

ambient sampling enabled. This timing mode would be used when heart rate is being measured with a single green LED. In this mode, a single optical sampled value, followed by the ambient sampled value, will appear successively in the FIFO.

**LED2 Pulsing with No Ambient Sampling**

The optical timing diagram in [Figure 13](#) represents only LED2 firing during the data sampling time with no direct ambient sampling enabled. This timing mode would be used when heart rate is being measured with a single

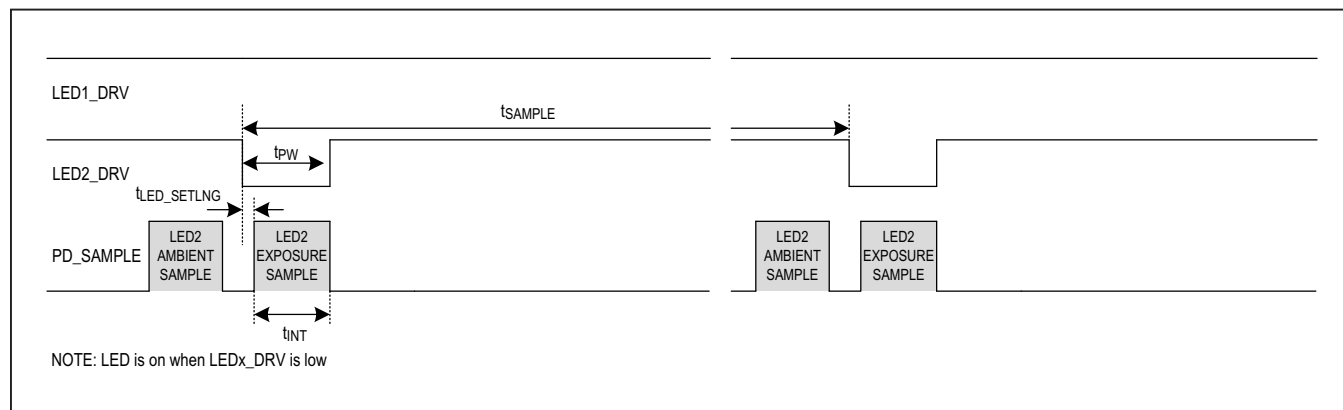


Figure 13: Timing for LED2 Pulsing with No Ambient Sampling

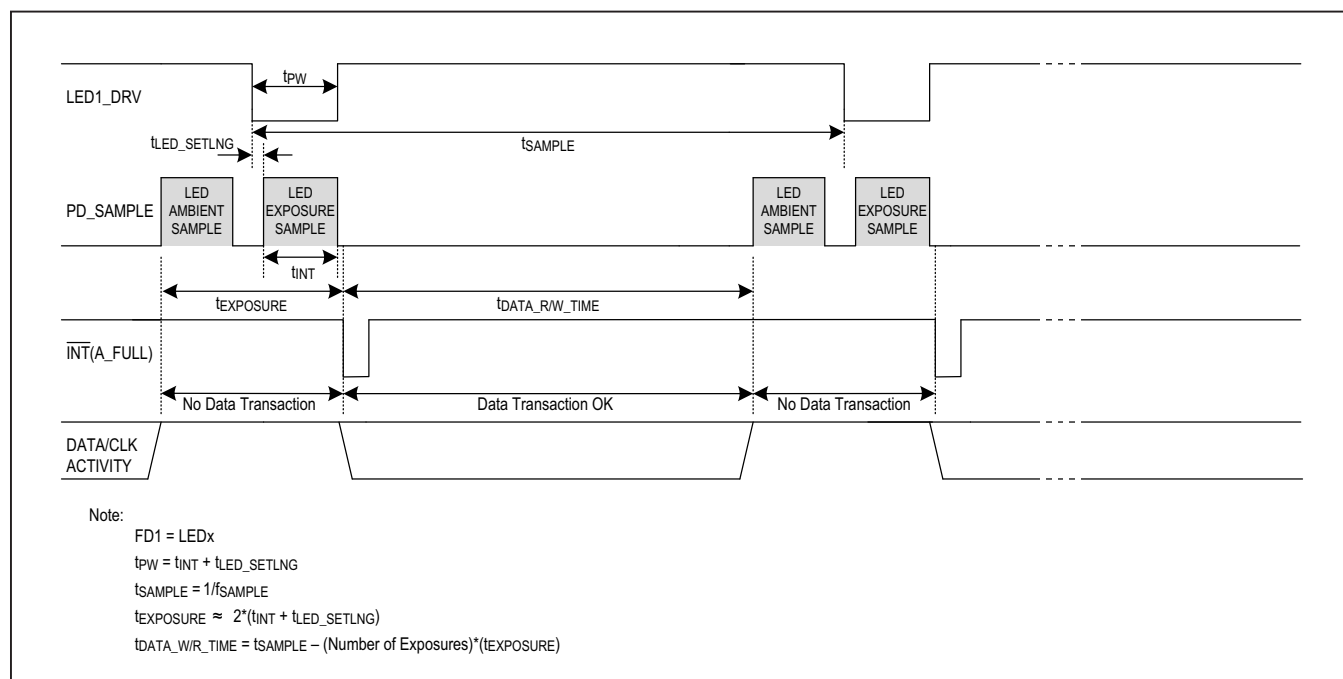


Figure 14. Readout Window for FIFO Read

green LED. In this mode, a single optical sampled value will appear successively in the FIFO.

#### FIFO Data Read Synchronization

Activity on the interface pins can bounce the on-chip GND potential, disturbing an optical sample, resulting in higher noise. Therefore, during a FIFO read event, it is recommended to time the FIFO read to occur between optical samples. This can be accomplished by reading the FIFO when the FIFO\_A\_FULL interrupt occurs and then limit the number of samples in the FIFO to those that can be read out during the time between samples. [Figure 14](#) illustrates how to place this read relative to the FIFO\_A\_FULL interrupt and the chosen sample rate, integration pulse width and LED settling time.

#### Proximity Function

The MAX30112 features proximity mode, which could significantly reduce energy consumption and extend battery life. In proximity mode, LED1 is pulsing at a lower current. When an object is present, the ADC count will exceed the preset threshold (PROX\_INT\_THRESH) and trigger the interrupt (PROX\_INT). This functionality is only available when the FD1 timing slot is assigned to LED1. To use this function, it is necessary to set four register/bit fields correctly. These variables are the normal state LED current on LED1, LED1\_PA (0x11), the proximity LED current, LED\_PILOT\_PA (0x15), the threshold code, PROX\_INT\_THRESH (0x10) and the proximity mode enable bit (Interrupt Enable1 (0x02, bit 4). Note that the threshold value is the code in register PROX\_INT\_THRESH (0x10) times 2048.

If the proximity feature is enabled, it will be switched to proximity mode when the LED1 ADC count drops below the threshold code, PROX\_INT\_THRESH(0x10). At this point, the LED1 drive current will be set from LED1\_PA(0x11) to LED\_PILOT\_PA(0x15). Note that the threshold value is the code in register PROX\_INT\_THRESH (0x10) times 2048. This drop in LED current should generate sufficient hysteresis to guarantee that the MAX30112 does not toggle back and forth between proximity and normal mode operation.

Once in proximity mode, the MAX30112 will return to normal operating mode when the ADC count generated by the current programmed into the LED\_PILOT\_PA (0x15) register passes above the threshold in the PROX\_INT\_THRESH (0x10) register. When this occurs, the LED1 current will increase to the value assigned in LED1\_PA (0x11) register, again providing sufficient hysteresis to guarantee a clean transition. Note that the threshold value is the code in register PROX\_INT\_THRESH (0x10) times 2048.

It is necessary to experiment with the specific optical geometry when configuring the proximity function. As a means of a starting point of this experimental work, it is recommended that the LED\_PILOT\_PA (0x15) register be set to about 1/10th the value of the LED1\_PA (0x11) register. It is also recommended that the PROX\_INT\_THRESH (0x10) be set to roughly mid-way between the output code produced by the values of LED1\_PA (0x11) and LED\_PILOT\_PA (0x15) when the optical device is correctly mounted to a subject.

## Register Map

## User Register Map

| ADDRESS | NAME                    | MSB            |               |             |                  |                  |   |   | LSB     |
|---------|-------------------------|----------------|---------------|-------------|------------------|------------------|---|---|---------|
| STATUS  |                         |                |               |             |                  |                  |   |   |         |
| 0x00    | Interrupt Status 1[7:0] | A_FULL         | PPG_RDY       | ALC_OVF     | PROX_INT         | LED_COMPB        | – | – | PWR_RDY |
| 0x01    | Interrupt Status 2[7:0] | VDD_OOR        | –             | –           | –                | –                | – | – | –       |
| 0x02    | Interrupt Enable 1[7:0] | A_FULL_EN      | PPG_RDY_EN    | ALC_OVF_EN  | PROX_INT_EN      | LED_COMPB_EN     | – | – | –       |
| 0x03    | Interrupt Enable 2[7:0] | VDD_OOR_EN     | –             | –           | –                | –                | – | – | –       |
| FIFO    |                         |                |               |             |                  |                  |   |   |         |
| 0x04    | FIFO Write Pointer[7:0] | –              | –             | –           | FIFO_WR_PTR[4:0] |                  |   |   |         |
| 0x05    | Overflow Counter[7:0]   | –              | –             | –           | OVF_COUNTER[4:0] |                  |   |   |         |
| 0x06    | FIFO Read Pointer[7:0]  | –              | –             | –           | FIFO_RD_PTR[4:0] |                  |   |   |         |
| 0x07    | FIFO Data Register[7:0] | FIFO_DATA[7:0] |               |             |                  |                  |   |   |         |
| 0x08    | FIFO Configuration[7:0] | –              | FIFO_STAT_CLR | A_FULL_TYPE | FIFO_RO          | FIFO_A_FULL[3:0] |   |   |         |

## User Register Map continued

| FIFO DATA CONTROL   |                                   |                      |   |             |                 |               |               |               |       |
|---------------------|-----------------------------------|----------------------|---|-------------|-----------------|---------------|---------------|---------------|-------|
| 0x09                | FIFO Data Control Register 1[7:0] | FD2[3:0]             |   |             |                 | FD1[3:0]      |               |               |       |
| 0x0A                | FIFO Data Control Register 2[7:0] | FD4[3:0]             |   |             |                 | FD3[3:0]      |               |               |       |
| SYSTEM CONTROL      |                                   |                      |   |             |                 |               |               |               |       |
| 0x0D                | System Control[7:0]               | –                    | – | –           | FCLK_CTRL       | LP_MODE       | FIFO_EN       | SHDN          | RESET |
| PPG CONFIGURATION   |                                   |                      |   |             |                 |               |               |               |       |
| 0x0E                | PPG Configuration 1[7:0]          | PPG_ADC_RGE[1:0]     |   | PPG_SR[3:0] |                 |               | PPG_TINT[1:0] |               |       |
| 0x0F                | PPG Configuration 2[7:0]          | –                    | – | –           | LED_SETLNG[1:0] |               | SMP_AVE[2:0]  |               |       |
| 0x10                | Prox Interrupt Threshold[7:0]     | PROX_INT_THRESH[7:0] |   |             |                 |               |               |               |       |
| LED PULSE AMPLITUDE |                                   |                      |   |             |                 |               |               |               |       |
| 0x11                | LED1 PA[7:0]                      | LED1_PA[7:0]         |   |             |                 |               |               |               |       |
| 0x12                | LED2 PA[7:0]                      | LED2_PA[7:0]         |   |             |                 |               |               |               |       |
| 0x14                | LED Range[7:0]                    | –                    | – | –           | –               | LED2_RGE[1:0] |               | LED1_RGE[1:0] |       |
| 0x15                | LED PILOT PA[7:0]                 | PILOT_PA[7:0]        |   |             |                 |               |               |               |       |
| PART ID             |                                   |                      |   |             |                 |               |               |               |       |
| 0xFF                | Part ID[7:0]                      | PART_ID[7:0]         |   |             |                 |               |               |               |       |

## Interrupt Status 1 (0x00)

| BIT         | 7         | 6         | 5         | 4         | 3         | 2 | 1 | 0         |
|-------------|-----------|-----------|-----------|-----------|-----------|---|---|-----------|
| Field       | A_FULL    | PPG_RDY   | ALC_OVF   | PROX_INT  | LED_COMPB | – | – | PWR_RDY   |
| Reset       | 0x0       | 0x0       | 0x0       | 0x0       | 0x0       | – | – | 0x0       |
| Access Type | Read Only | Read Only | Read Only | Read Only | Read Only | – | – | Read Only |

## A\_FULL

| VALUE | ENUMERATION | DECODE                                                                                                                                                                                                                                         |
|-------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | OFF         | Normal Operation                                                                                                                                                                                                                               |
| 1     | ON          | Indicates that the FIFO buffer will overflow the threshold set by FIFO_A_FULL[3:0] on the next sample. This bit is cleared when the Interrupt Status 1 Register is read. It is also cleared when FIFO_DATA register is read, if A_FULL_CLR = 1 |

## PPG\_RDY

| VALUE | ENUMERATION | DECODE                                                                                                                                                                                                                                                                                 |
|-------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | OFF         | Normal Operation                                                                                                                                                                                                                                                                       |
| 1     | ON          | In LED1 and/or LED2 modes, this interrupt triggers if PPG_RDY_EN is set to 1, when there is a new sample in the data FIFO. The interrupt is cleared by reading the Interrupt Status 1 register (0x00). It is also cleared by reading the FIFO_DATA register if A_FULL_CLR is set to 1. |

**ALC\_OVF**

| VALUE | ENUMERATION | DECODE                                                                                                                                                                                                                                                                                 |
|-------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | OFF         | Normal Operation                                                                                                                                                                                                                                                                       |
| 1     | ON          | This interrupt triggers when the ambient light cancellation function of the PPG photodiode has reached its maximum limit due to overflow, and therefore, ambient light is affecting the output of the ADC. The interrupt is cleared by reading the Interrupt Status 1 register (0x00). |

**PROX\_INT**

| VALUE | ENUMERATION | DECODE                                                                                                                                                                                                                                               |
|-------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | OFF         | Normal Operation                                                                                                                                                                                                                                     |
| 1     | ON          | Indicates that the proximity threshold has been crossed when in proximity mode. If PROX_INT is masked then the prox mode is disabled and the selected PPG mode begins immediately. This bit is cleared when the Interrupt Status 1 Register is read. |

**LED\_COMPB**

LED1 is not voltage compliant meaning that  $V_{LED1} < 160\text{mV}$  while LED1 pulses.: At the end of each sample, if the LED1 Driver is not voltage compliant, LED\_COMPB interrupt is asserted if LED\_COMPB\_EN is set to 1. The interrupt is cleared when the status register is read.

| VALUE | ENUMERATION   | DECODE                                   |
|-------|---------------|------------------------------------------|
| 0     | COMPLIANT     | LED1 driver voltage is in compliance     |
| 1     | NOT_COMPLIANT | LED1 driver voltage is not in compliance |

**PWR\_RDY**

| VALUE | ENUMERATION | DECODE                                                                                                                                                                             |
|-------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | OFF         | Normal Operation                                                                                                                                                                   |
| 1     | ON          | Indicates that VDD_DIG went below the 1.55V under voltage lockout threshold. This bit is also set upon a soft reset. This bit is cleared when Interrupt Status 1 Register is read. |

**Interrupt Status 2 (0x01)**

| BIT         | 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-----------|---|---|---|---|---|---|---|
| Field       | VDD_OOR   | – | – | – | – | – | – | – |
| Reset       | 0x0       | – | – | – | – | – | – | – |
| Access Type | Read Only | – | – | – | – | – | – | – |

**VDD\_OOR**

This is an indicator to check if the VDD\_ANA supply voltage is within supported range.

| VALUE | ENUMERATION | DECODE                                                                                                                                                                                                                                                               |
|-------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | OFF         | VDD_ANA within supported range.                                                                                                                                                                                                                                      |
| 1     | ON          | Indicates that VDD_ANA is greater than 2.05V or less than 1.65V. This bit is automatically cleared when the Interrupt Status 2 register is read. The detection circuitry has a 10ms delay time, and will continue to trigger as long as the VDD_ANA is out of range. |

**Interrupt Enable 1 (0x02)**

| BIT         | 7           | 6           | 5           | 4           | 3            | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|--------------|---|---|---|
| Field       | A_FULL_EN   | PPG_RDY_EN  | ALC_OVF_EN  | PROX_INT_EN | LED_COMPB_EN | – | – | – |
| Reset       | 0x0         | 0x0         | 0x0         | 0x0         | 0x0          | – | – | – |
| Access Type | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read  | – | – | – |

**A\_FULL\_EN**

| VALUE | ENUMERATION | DECODE                       |
|-------|-------------|------------------------------|
| 0     | OFF         | A_FULL interrupt is disabled |
| 1     | ON          | A_FULL interrupt is enabled  |

**PPG\_RDY\_EN**

| VALUE | ENUMERATION | DECODE                        |
|-------|-------------|-------------------------------|
| 0     | OFF         | PPG_RDY interrupt is disabled |
| 1     | ON          | PPG_RDY interrupt is enabled. |

**ALC\_OVF\_EN**

| VALUE | ENUMERATION | DECODE                        |
|-------|-------------|-------------------------------|
| 0     | OFF         | ALC_OVF interrupt is disabled |
| 1     | ON          | ALC_OVF interrupt is enabled  |

**PROX\_INT\_EN**

When this is enabled, program LED1 into FD1 in FIFO Data Control register 1. LED1 must be used for proximity detection. If the ADC reading for this exposure is below 2048 times the threshold programmed in PROX\_INT\_THRESH register, the device is in proximity mode, otherwise it is in normal mode.

When the device is in proximity mode, the device starts data acquisition using only one exposure of LED1 and the LED current programmed in PILOT\_PA register.

When the device is in normal mode, the device starts data acquisition using all the exposures programmed in the FIFO Data Control registers and appropriate LED currents.

When PROX\_INT\_EN is programmed to 1, PROX\_INT interrupt is asserted when the device enters normal mode (exit Proximity mode).

| VALUE | ENUMERATION | DECODE                         |
|-------|-------------|--------------------------------|
| 0     | OFF         | PROX_INT interrupt is disabled |
| 1     | ON          | PROX_INT interrupt is enabled  |

**LED\_COMPB\_EN**

| VALUE | ENUMERATION | DECODE                                               |
|-------|-------------|------------------------------------------------------|
| 0     | DISABLE     | LED1 driver voltage compliance interrupt is disabled |
| 1     | ENABLE      | LED1 driver voltage compliance interrupt is enabled  |

**Interrupt Enable 2 (0x03)**

| BIT         | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|---|---|---|---|---|---|---|
| Field       | VDD_OOR_EN  | – | – | – | – | – | – | – |
| Reset       | 0x0         | – | – | – | – | – | – | – |
| Access Type | Write, Read | – | – | – | – | – | – | – |

**VDD\_OOR\_EN**

| VALUE | ENUMERATION | DECODE                         |
|-------|-------------|--------------------------------|
| 0     | OFF         | Disables the VDD_OVR interrupt |
| 1     | ON          | Enables the VDD_OVR interrupt  |

**FIFO Write Pointer (0x04)**

| BIT         | 7 | 6 | 5 | 4                | 3 | 2 | 1 | 0 |
|-------------|---|---|---|------------------|---|---|---|---|
| Field       | – | – | – | FIFO_WR_PTR[4:0] |   |   |   |   |
| Reset       | – | – | – | 0x00             |   |   |   |   |
| Access Type | – | – | – | Write, Read      |   |   |   |   |

**FIFO\_WR\_PTR**

This points to the location where the next sample will be written. This pointer advances for each sample pushed on to the FIFO. Refer to FIFO Configuration for details.

**Overflow Counter (0x05)**

| BIT         | 7 | 6 | 5 | 4                | 3 | 2 | 1 | 0 |
|-------------|---|---|---|------------------|---|---|---|---|
| Field       | – | – | – | OVF_COUNTER[4:0] |   |   |   |   |
| Reset       | – | – | – | 0x00             |   |   |   |   |
| Access Type | – | – | – | Read Only        |   |   |   |   |

**OVF\_COUNTER**

When FIFO is full any new samples will result in new or old samples getting lost depending on FIFO\_RO. OVF\_COUNTER counts the number of samples lost. It saturates at 0x1F. Refer to FIFO Configuration for details.

**FIFO Read Pointer (0x06)**

| BIT         | 7 | 6 | 5 | 4                | 3 | 2 | 1 | 0 |
|-------------|---|---|---|------------------|---|---|---|---|
| Field       | – | – | – | FIFO_RD_PTR[4:0] |   |   |   |   |
| Reset       | – | – | – | 0x00             |   |   |   |   |
| Access Type | – | – | – | Write, Read      |   |   |   |   |

**FIFO\_RD\_PTR**

The FIFO Read Pointer points to the location from where the processor gets the next sample from the FIFO. This advances each time a sample is popped from the FIFO. The processor can also write to this pointer after reading the samples. This allows rereading (or retrying) samples from the FIFO. Refer to FIFO Configuration for details.

**FIFO Data Register (0x07)**

| BIT         | 7              | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------|---|---|---|---|---|---|---|
| Field       | FIFO_DATA[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x00           |   |   |   |   |   |   |   |
| Access Type | Write, Read    |   |   |   |   |   |   |   |

**FIFO\_DATA**

This is a read-only register and is used to get data from the FIFO. Refer to [FIFO Configuration](#) for details.

**FIFO Configuration (0x08)**

| BIT         | 7 | 6             | 5           | 4           | 3                | 2 | 1 | 0 |
|-------------|---|---------------|-------------|-------------|------------------|---|---|---|
| Field       | – | FIFO_STAT_CLR | A_FULL_TYPE | FIFO_RO     | FIFO_A_FULL[3:0] |   |   |   |
| Reset       | – | 0x0           | 0x0         | 0x0         | 0xF              |   |   |   |
| Access Type | – | Write, Read   | Write, Read | Write, Read | Write, Read      |   |   |   |

**FIFO\_STAT\_CLR**

This defines whether the A\_FULL interrupt should get cleared by FIFO\_DATA register read.

| VALUE | ENUMERATION   | DECODE                                                                                                     |
|-------|---------------|------------------------------------------------------------------------------------------------------------|
| 0     | RD_DATA_NOCLR | A_FULL interrupt does not get cleared by FIFO_DATA register read. It gets cleared by status register read. |
| 1     | RD_DATA_CLR   | A_FULL interrupt gets cleared by FIFO_DATA register read or status register read.                          |

**A\_FULL\_TYPE**

This defines the behavior of the A\_FULL interrupt.

| VALUE | ENUMERATION | DECODE                                                                                                                                                                                                           |
|-------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | AFULL_RPT   | A_FULL interrupt gets asserted when the a_full condition is detected. It is cleared by status register read, but re-asserts for every sample if the a_full condition persists.                                   |
| 1     | AFULL_ONCE  | A_FULL interrupt gets asserted only when the a_full condition is detected. The interrupt gets cleared on status register read, and does not re-assert for every sample until a new a-full condition is detected. |

**FIFO\_RO**

Push enable when FIFO is full:

This bit controls the behavior of the FIFO when the FIFO becomes completely filled with data.

Push to FIFO is enabled when FIFO is full if FIFO\_RO = 1. In this mode old samples are overwritten. FIFO\_WR\_PTR increments for each sample. FIFO\_RD\_PTR also increments for each sample pushed to the FIFO.

Push to FIFO is disabled when FIFO is full if FIFO\_RO = 0. In this mode old samples are not overwritten and new samples are discarded. FIFO\_WR\_PTR does not increment for each sample after the FIFO is full.

When the device is in proximity mode, push to FIFO is enabled independent of FIFO\_RO setting.

| VALUE | ENUMERATION | DECODE                                     |
|-------|-------------|--------------------------------------------|
| 0     | OFF         | The FIFO stops on full.                    |
| 1     | ON          | The FIFO automatically rolls over on full. |

**FIFO\_A\_FULL**

These bits indicate how many unread samples are in the FIFO when the interrupt is asserted. For example, if set to 0xF, the interrupt triggers when there are 17 data samples in the FIFO (15 empty spaces left).

| FIFO_A_FULL[3:0] | FREE SPACES AT INTERRUPT | # OF SAMPLES IN FIFO |
|------------------|--------------------------|----------------------|
| 0000             | 0                        | 32                   |
| 0001             | 1                        | 31                   |
| 0010             | 2                        | 30                   |
| 0011             | 3                        | 29                   |
| ----             | ----                     | ----                 |
| 1110             | 14                       | 18                   |
| 1111             | 15                       | 17                   |

**FIFO Data Control Register 1 (0x09)**

| BIT         | 7           | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
|-------------|-------------|---|---|---|-------------|---|---|---|
| Field       | FD2[3:0]    |   |   |   | FD1[3:0]    |   |   |   |
| Reset       | 0x0         |   |   |   | 0x0         |   |   |   |
| Access Type | Write, Read |   |   |   | Write, Read |   |   |   |

**FD2**

These bits set the data type for Data Item 2 of the FIFO.

See [FIFO Configuration](#) for mode information.

**FD1**

These bits set the data type for Data Item 1 of the FIFO.

See [FIFO Configuration](#) for mode information.

**FIFO Data Control Register 2 (0x0A)**

| BIT         | 7           | 6 | 5 | 4 | 3           | 2 | 1 | 0 |
|-------------|-------------|---|---|---|-------------|---|---|---|
| Field       | FD4[3:0]    |   |   |   | FD3[3:0]    |   |   |   |
| Reset       | 0x0         |   |   |   | 0x0         |   |   |   |
| Access Type | Write, Read |   |   |   | Write, Read |   |   |   |

**FD4**

These bits set the data type for Data Item 4 of the FIFO.

See [FIFO Configuration](#) for mode information.

**FD3**

These bits set the data type for Data Item 3 of the FIFO.

See [FIFO Configuration](#) for mode information.

**System Control (0x0D)**

| BIT         | 7 | 6 | 5 | 4           | 3           | 2           | 1           | 0           |
|-------------|---|---|---|-------------|-------------|-------------|-------------|-------------|
| Field       | – | – | – | FCLK_CTRL   | LP_MODE     | FIFO_EN     | SHDN        | RESET       |
| Reset       | – | – | – | 0x0         | 0x0         | 0x0         | 0x0         | 0x0         |
| Access Type | – | – | – | Write, Read | Write, Read | Write, Read | Write, Read | Write, Read |

**FCLK\_CTRL**

FCLK pin can be used for external 32kHz clock input when the PPG sample rate is 100sps and below. Used to synchronous multiple devices into one Clock domain.

| VALUE | ENUMERATION | DECODE                                                                                  |
|-------|-------------|-----------------------------------------------------------------------------------------|
| 0x0   |             | FCLK pin is not used.<br>Use internal 32KHz clock for PPG sample rates 100Hz and below. |
| 0x1   |             | Use external 32KHz clock at FCLK input for PPG sample rates 100Hz and below.            |

**LP\_MODE**

In low power mode, the sensor can be dynamically powered down between samples to conserve power. This dynamic power-down mode option only supports samples rates of 100Hz and below.

| VALUE | ENUMERATION | DECODE                                                                                                                                                                                  |
|-------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | OFF         | Dynamic power down is disabled                                                                                                                                                          |
| 1     | ON          | Dynamic power down is enabled. The device automatically enters low power mode between samples for samples rates 100Hz and below.<br>This mode is not available for higher sample rates. |

**FIFO\_EN**

| VALUE | ENUMERATION | DECODE                                                                                                                                                                                                                       |
|-------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | OFF         | Push to FIFO is disabled, but the read and write pointers and the data in the FIFO are all held at their values before FIFO_EN is set to 0. The conversion and LED drivers are active until FD1 is set to NONE               |
| 1     | ON          | The FIFO is enabled. When this bit is set the FIFO is flushed of all old data and the new samples start loading from pointer zero. Setting this bit starts conversions and LED drivers enable according to the FDx settings. |

**SHDN**

The part can be put into a power-save mode by setting this bit to one. While in power-save mode, all registers retain their values, and write/read operations function as normal. All interrupts are cleared to zero in this mode.

| VALUE | ENUMERATION | DECODE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|-------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | OFF         | The part is in normal operation. No action taken.                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 1     | ON          | The part can be put into a power-save mode by writing a '1' to this bit. While in this mode all registers remain accessible and retain their data. ADC conversion data contained in the registers are previous values. Writeable registers also remain accessible in shutdown. All interrupts are cleared. In this mode the oscillator is shutdown and the part draws minimum current. If this bit is asserted during an active conversion then the conversion completes before the part shuts down. |

**RESET**

| VALUE | ENUMERATION | DECODE                                                                                                                                                                                                                  |
|-------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0     | OFF         | The part is in normal operation. No action taken.                                                                                                                                                                       |
| 1     | ON          | The part under-goes a forced power-on-reset sequence. All configuration, threshold and data registers are reset to their power-on-state. This bit then automatically becomes '0' after the reset sequence is completed. |

**PPG Configuration 1 (0x0E)**

| BIT         | 7                | 6 | 5           | 4 | 3 | 2 | 1             | 0 |
|-------------|------------------|---|-------------|---|---|---|---------------|---|
| Field       | PPG_ADC_RGE[1:0] |   | PPG_SR[3:0] |   |   |   | PPG_TINT[1:0] |   |
| Reset       | 0x0              |   | 0x0         |   |   |   | 0x0           |   |
| Access Type | Write, Read      |   | Write, Read |   |   |   | Write, Read   |   |

**PPG\_ADC\_RGE**

These bits set the ADC range of the photodiode sensor as shown in the table below.

| PPG_ADC_RGE[1:0] | LSB (PA) | FULL SCALE (UA) |
|------------------|----------|-----------------|
| 00               | 11.4     | 6               |
| 01               | 22.9     | 12              |
| 10               | 45.8     | 24              |
| 11               | 91.6     | 48              |

**PPG\_SR**

These bits set the effective sampling rate of the PPG sensor as shown in the table below.

In Dual Pulse mode there are two pulses per sample, and the pulses are spaced to produce an additional 20dB of ambient rejection for indoor lighting cases (100Hz or 120Hz rejection).

If the sample rate, integration time, and number of Data Item are set to an invalid combination, the highest available sample rate will be automatically set for the integration and number of exposure setting. The user can read this register to confirm the sample rate.

| PPG_SR[3:0] | FSAMPLE (SPS) | DUAL PULSE MODE |
|-------------|---------------|-----------------|
| 0000        | 20            | No              |
| 0001        | 25            | No              |
| 0010        | 50            | No              |
| 0011        | 84            | No              |
| 0100        | 100           | No              |
| 0101        | 200           | No              |
| 0110        | 400           | No              |
| 0111        | 800           | No              |
| 1000        | 1000          | No              |
| 1001        | 1600          | No              |
| 1010        | 3200          | No              |
| 1011        | 20            | Yes             |
| 1100        | 25            | Yes             |
| 1101        | 50            | Yes             |
| 1110        | 84            | Yes             |
| 1111        | 100           | Yes             |

See the following table for the maximum sample rates supported for all the integration time and number of Data Items.

| NUMBER OF DATA ITEM PER SAMPLE  | PPG_TINT = 0 (50US)                        | PPG_TINT= 1 (100US)                        | PPG_TINT= 2 (200US)                       | PPG_TINT= 3 (400US)                       |
|---------------------------------|--------------------------------------------|--------------------------------------------|-------------------------------------------|-------------------------------------------|
| 1 DATA ITEM, SINGLE PULSE MODE  | 3200                                       | 1600                                       | 1600                                      | 1000                                      |
| 2 DATA ITEMS, SINGLE PULSE MODE | 1600                                       | 800                                        | 800                                       | 400                                       |
| 3 DATA ITEMS, SINGLE PULSE MODE | 1000                                       | 800                                        | 400                                       | 200                                       |
| 4 DATA ITEMS, SINGLE PULSE MODE | 1000                                       | 400                                        | 400                                       | 200                                       |
| 1 DATA ITEM, DUAL PULSE MODE    | 100                                        | 100                                        | 100                                       | 100                                       |
| 2 DATA ITEMS, DUAL PULSE MODE   | 100 for LP_MODE = 0,<br>50 for LP_MODE = 1 | 100 for LP_MODE = 0;<br>50 for LP_MODE = 1 | 84 for LP_MODE = 0;<br>50 for LP_MODE = 1 | 84 for LP_MODE = 0;<br>50 for LP_MODE = 1 |
| 3 DATA ITEMS, DUAL PULSE MODE   | 50                                         | 50                                         | 50                                        | 50                                        |
| 4 DATA ITEMS, DUAL PULSE MODE   | 50 for LP_MODE = 0;<br>25 for LP_MODE= 1   | 50 for LP_MODE = 0;<br>25 for LP_MODE = 1  | 25                                        | 25                                        |

### PPG\_TINT

These bits set the integration time of PPG ADC as well as the pulse width of the LEDS as shown in the table below.

$t_{LED\_SETLNG}$  is the delay programmed in the LED\_SETLNG[1:0] register.

| PPG_TINT[1:0] | TPW, LED PULSE WIDTH (MS) | TINT, INTEGRATION TIME (MS) | RESOLUTION BITS |
|---------------|---------------------------|-----------------------------|-----------------|
| 00            | $52 + t_{LED\_SETLNG}$    | 52                          | 16              |
| 01            | $104 + t_{LED\_SETLNG}$   | 104                         | 17              |
| 10            | $206 + t_{LED\_SETLNG}$   | 206                         | 18              |
| 11            | $417 + t_{LED\_SETLNG}$   | 417                         | 19              |

### PPG Configuration 2 (0x0F)

| BIT         | 7 | 6 | 5 | 4               | 3 | 2            | 1 | 0 |
|-------------|---|---|---|-----------------|---|--------------|---|---|
| Field       | — | — | — | LED_SETLNG[1:0] |   | SMP_AVE[2:0] |   |   |
| Reset       | — | — | — | 0x3             |   | 0x0          |   |   |
| Access Type | — | — | — | Write, Read     |   | Write, Read  |   |   |

### LED\_SETLNG

Delay from rising edge of LED to start of ADC integration. This allows for the LED current to settle before the start of ADC integration.

| LED_SETLNG[1:0] | DELAY $t_{LED\_SETLNG}$ (MS) |
|-----------------|------------------------------|
| 00              | 2.5                          |
| 01              | 5.0                          |
| 10              | 10.0                         |
| 11              | 20.0                         |

**SMP\_AVE**

Adjacent samples (in each individual channel) can be internally averaged to reduce the amount of data throughput.

These bits set the number of samples that are averaged on chip before being written to the FIFO. The effective output sample rate is the PPG\_SR rate divided by the SMP\_AVE value.

| SMP_AVE[2:0] | SAMPLE AVERAGE   |
|--------------|------------------|
| 000          | 1 (no averaging) |
| 001          | 2                |
| 010          | 4                |
| 011          | 8                |
| 100          | 16               |
| 101          | 32               |
| 110          | 32               |
| 111          | 32               |

**Prox Interrupt Threshold (0x10)**

| BIT         | 7                    | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|----------------------|---|---|---|---|---|---|---|
| Field       | PROX_INT_THRESH[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x00                 |   |   |   |   |   |   |   |
| Access Type | Write, Read          |   |   |   |   |   |   |   |

**PROX\_INT\_THRESH**

This register sets the LED1 ADC count value that will trigger the transition between proximity mode to normal mode. The threshold is defined as the 8 MSB bits of the ADC count. For example, if PROX\_INT\_THRESH[7:0] = 0x01, then an ADC value of 2048 (decimal) or higher triggers the PROX interrupt. If PROX\_INT\_THRESH[7:0] = 0xFF, then only a saturated ADC triggers the interrupt.

See the [Proximity Function](#) section in the detailed description for more details on the operation of proximity mode.

**LED1 PA (0x11)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | LED1_PA[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x00         |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

**LED1\_PA**

These bits set the nominal peak current pulse amplitude of LEDx\_DRV pin as shown in the table below.

Note: x denotes the respective LED channel.

| LEDX_RGE[1:0] | 00                         | 01                         | 10                         | 11                         |
|---------------|----------------------------|----------------------------|----------------------------|----------------------------|
| LEDx_PA[7:0]  | I <sub>LEDx_DRV</sub> (mA) | I <sub>LEDx_DRV</sub> (mA) | I <sub>LEDx_DRV</sub> (mA) | I <sub>LEDx_DRV</sub> (mA) |
| 0x00          | 0                          | 0                          | 0                          | 0                          |
| 0x01          | 0.2                        | 0.4                        | 0.6                        | 0.8                        |
| 0x02          | 0.4                        | 0.8                        | 1.2                        | 1.6                        |
| 0x03          | 0.6                        | 1.2                        | 1.8                        | 2.4                        |
| .....         |                            |                            |                            |                            |
| 0xFC          | 49.4                       | 98.8                       | 148.2                      | 197.6                      |
| 0xFD          | 49.6                       | 99.2                       | 148.8                      | 198.4                      |
| 0xFE          | 49.8                       | 99.6                       | 149.4                      | 198.2                      |
| 0xFF          | 50                         | 100                        | 150                        | 200                        |
| LSB           | 0.196                      | 0.392                      | 0.588                      | 0.784                      |

**LED2 PA (0x12)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | LED2_PA[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x00         |   |   |   |   |   |   |   |
| Access Type | Write, Read  |   |   |   |   |   |   |   |

**LED2\_PA**

Refer to LED1\_PA[1:0] for more details.

**LED Range (0x14)**

| BIT         | 7 | 6 | 5 | 4 | 3             | 2 | 1             | 0 |
|-------------|---|---|---|---|---------------|---|---------------|---|
| Field       | – | – | – | – | LED2_RGE[1:0] |   | LED1_RGE[1:0] |   |
| Reset       | – | – | – | – | 0x00          |   | 0x00          |   |
| Access Type | – | – | – | – | Write, Read   |   | Write, Read   |   |

**LED2\_RGE**

Range selection of the LED 2 current.

Refer to LED1\_PA[1:0] for more details.

| LED2_RGE[1:0] | MAX LED CURRENT RANGE(MA) |
|---------------|---------------------------|
| 00            | 50                        |
| 01            | 100                       |
| 10            | 150                       |
| 11            | 200                       |

**LED1\_RGE**

Range selection of the LED 1 current.

Refer to LED1\_PA[1:0] for more details.

| LED1_RGE[1:0] | MAX LED CURRENT RANGE(MA) |
|---------------|---------------------------|
| 00            | 50                        |
| 01            | 100                       |
| 10            | 150                       |
| 11            | 200                       |

**LED PILOT PA (0x15)**

| BIT         | 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------|---|---|---|---|---|---|---|
| Field       | PILOT_PA[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x00          |   |   |   |   |   |   |   |
| Access Type | Write, Read   |   |   |   |   |   |   |   |

**PILOT\_PA**

In proximity mode, PILOT\_PA[7:0] sets LED1 proximity mode current. These bits set the current pulse amplitude for proximity mode as shown in the table below. In proximity mode, LED1\_RGE[1:0] and PILOT\_PA[1:0] sets the LED1\_DRV current.

See [Proximity Function](#) for more details on the operation of proximity mode.

| LED1_RGE[1:0] | 00                         | 01                         | 10                         | 11                         |
|---------------|----------------------------|----------------------------|----------------------------|----------------------------|
| PILOT_PA[7:0] | I <sub>LED1_DRV</sub> (mA) | I <sub>LED1_DRV</sub> (mA) | I <sub>LED1_DRV</sub> (mA) | I <sub>LED1_DRV</sub> (mA) |
| 0x00          | 0                          | 0                          | 0                          | 0                          |
| 0x01          | 0.2                        | 0.4                        | 0.6                        | 0.8                        |
| 0x02          | 0.4                        | 0.8                        | 1.2                        | 1.6                        |
| 0x03          | 0.6                        | 1.2                        | 1.8                        | 2.4                        |
| .....         |                            |                            |                            |                            |
| 0xFC          | 49.4                       | 98.8                       | 148.2                      | 197.6                      |
| 0xFD          | 49.6                       | 99.2                       | 148.8                      | 198.4                      |
| 0xFE          | 49.8                       | 99.6                       | 149.4                      | 199.2                      |
| 0xFF          | 50                         | 100                        | 150                        | 200                        |
| LSB           | 0.2                        | 0.4                        | 0.6                        | 0.8                        |

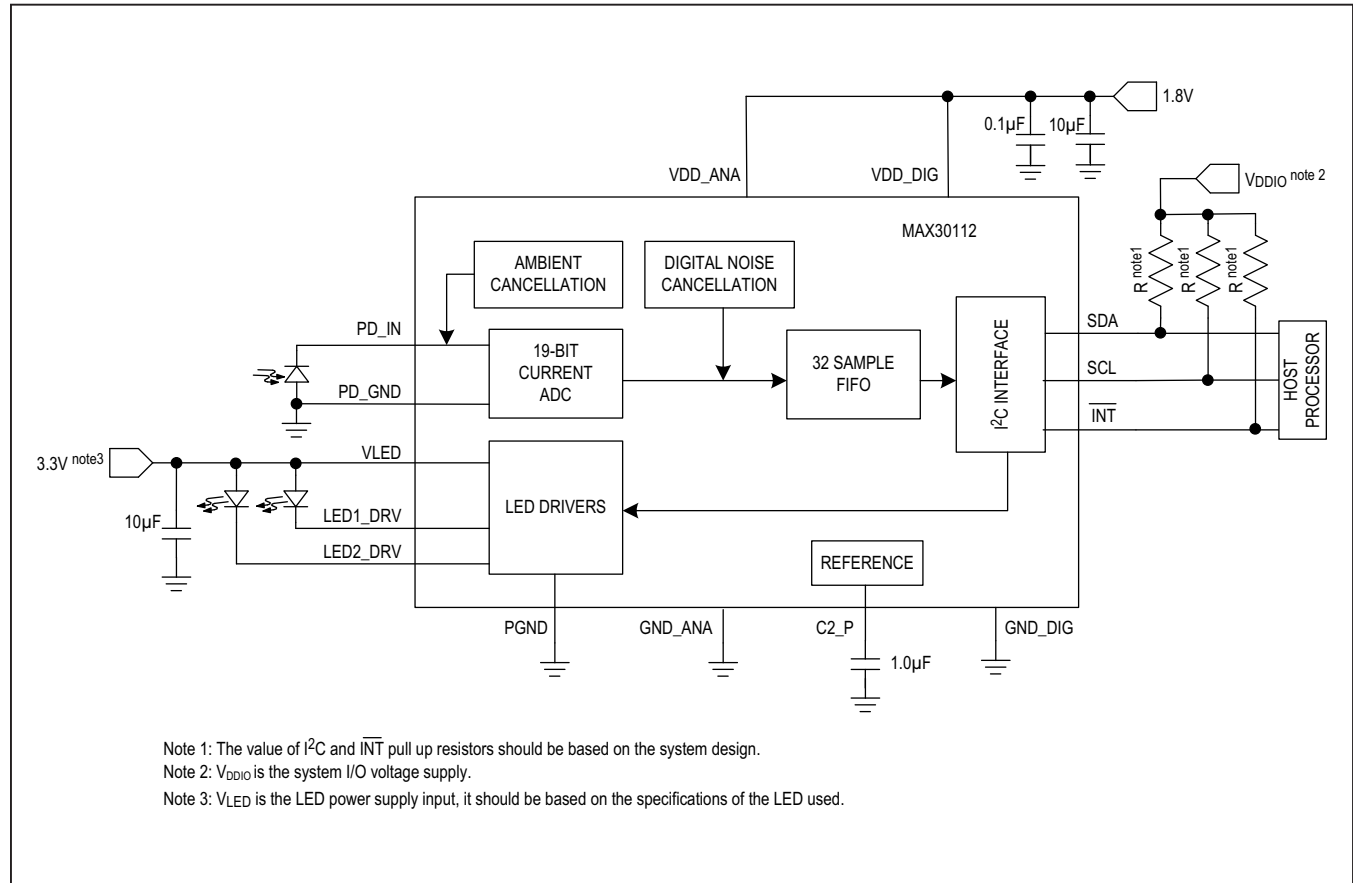
**Part ID (0xFF)**

| BIT         | 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|--------------|---|---|---|---|---|---|---|
| Field       | PART_ID[7:0] |   |   |   |   |   |   |   |
| Reset       | 0x20         |   |   |   |   |   |   |   |
| Access Type | Read Only    |   |   |   |   |   |   |   |

**PART\_ID**

This register stores the part identifier for the chip.

## Typical Application Circuit



## Ordering Information

| PART         | TEMP. RANGE    | BUMP-PACKAGE                           |
|--------------|----------------|----------------------------------------|
| MAX30112EWG+ | -40°C to +85°C | 24-BUMP WLP 2.8mm x 2.0mm, 0.4mm Pitch |

+Denotes a lead(Pb)-free/RoHS-compliant package

**Revision History**

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION     | PAGES<br>CHANGED |
|--------------------|------------------|-----------------|------------------|
| 0                  | 5/17             | Initial release | —                |

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