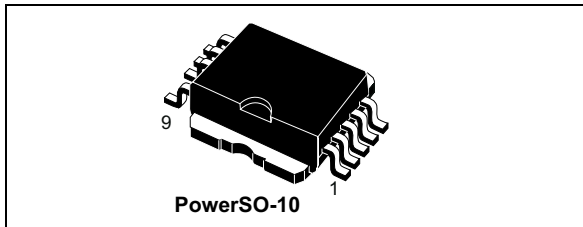


## Quad high-side smart power solid state-relay

Datasheet - production data



- Built-in current limiter
- Undervoltage shutdown
- Open drain diagnostic output
- Fast demagnetization of inductive loads
- Conformity to IEC 61131-2

### Features

Type	$V_{\text{demag}}^{(1)}$	$R_{\text{DS(on)}}^{(1)}$	$I_{\text{OUT}}^{(1)}$	$V_{\text{CC}}^{(1)}$
VN340SP-E	$V_{\text{CC}}-55 \text{ V}$	$0.2 \Omega$	$0.7 \text{ A}$	$36 \text{ V}$

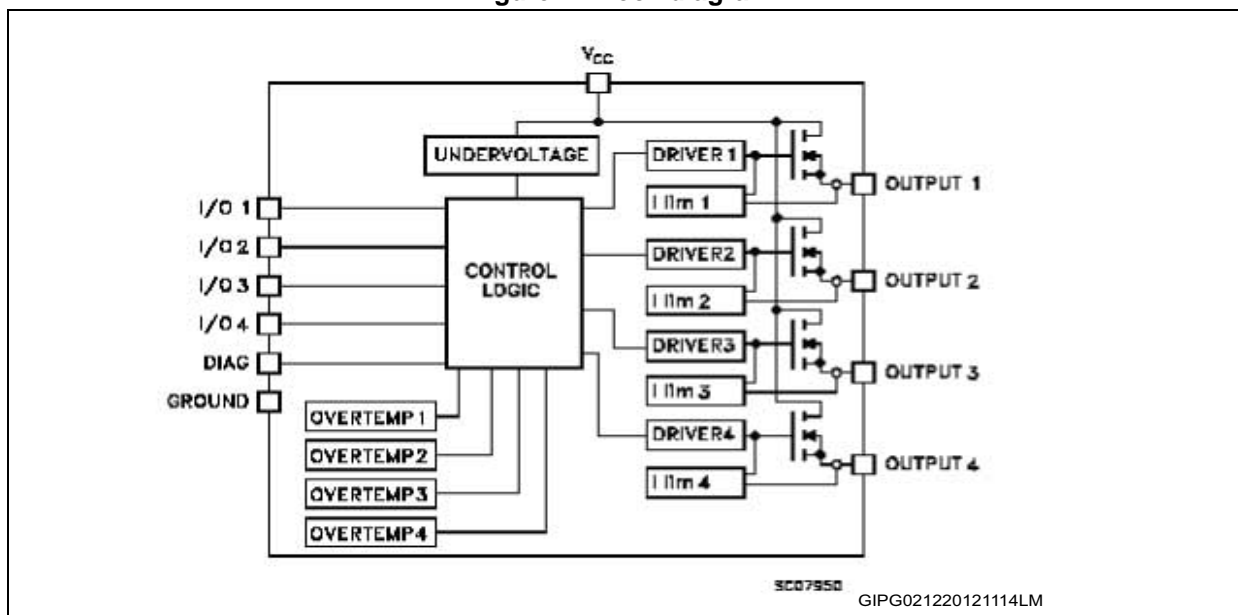
1. Per channel

- Output current: 0.7 A per channel
- Digital I/O clamped at 32 V minimum voltage
- Shorted load and overtemperature protections
- Protection against loss of ground

### Description

The VN340SP-E is a monolithic device developed using ST VIPower™ technology, intended to drive four independent resistive or inductive loads with one side connected to ground. Active current limitation avoids dropping the system power supply in case of shorted load. Built-in thermal shutdown protects the chip from overtemperature and short-circuit. The open drain diagnostic output indicates overtemperature conditions. Each I/O is pulled down when the overtemperature condition of the relative channel is verified.

Figure 1. Block diagram



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# 1 Absolute maximum ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CC}$	Power supply voltage	45	V
$-V_{CC}$	Reverse supply voltage	-4	V
$I_{OUT}$	Output current (continuous)	Internally limited	A
$I_R$	Reverse output current (per channel)	-6	A
$I_{IN}$	Input current (per channel)	$\pm 10$	mA
$I_{DIAG}$	Diag pin current	$\pm 10$	mA
$V_{ESD}$	Electrostatic discharge (R = 1.5 k $\Omega$ ; C = 100 pF)	2000	V
$E_{AS}$	Single pulse avalanche energy one channel active $T_J = 125\text{ }^\circ\text{C}$ , $I_{LOAD} = 0.625\text{ A}$	10	J
	Single pulse avalanche energy all channels active simultaneously $T_J = 125\text{ }^\circ\text{C}$ , $I_{LOAD} = 0.625\text{ A}$	2	
$P_{TOT}$	Power dissipation at $T_C = 25\text{ }^\circ\text{C}$	Internally limited	W
$T_J$	Junction operating temperature		$^\circ\text{C}$
$T_{STG}$	Storage temperature	-55 to 150	$^\circ\text{C}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case <sup>(1)</sup>	3	$^\circ\text{C/W}$
$R_{thJA}$	Thermal resistance junction-ambient <sup>(2)</sup>	50	$^\circ\text{C/W}$

1. Per channel
2. When mounted, minimum recommended pad size on FR-4 board

## 2 Pin connections

Figure 2. Connection diagram (top view)

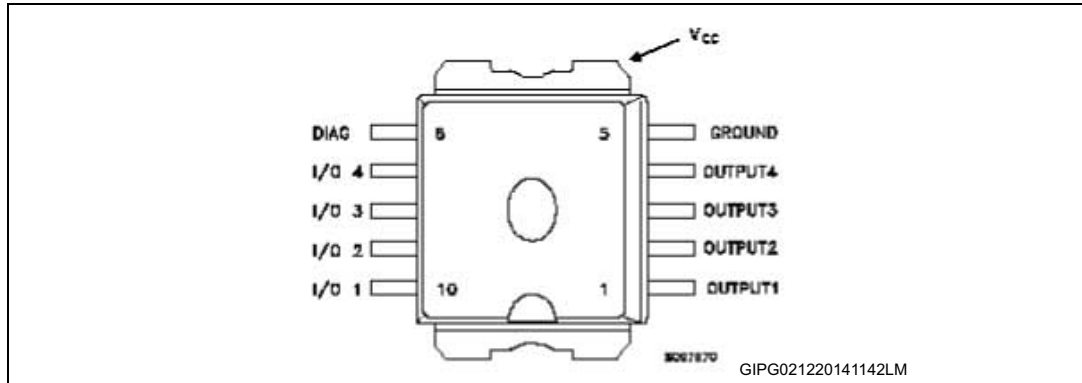
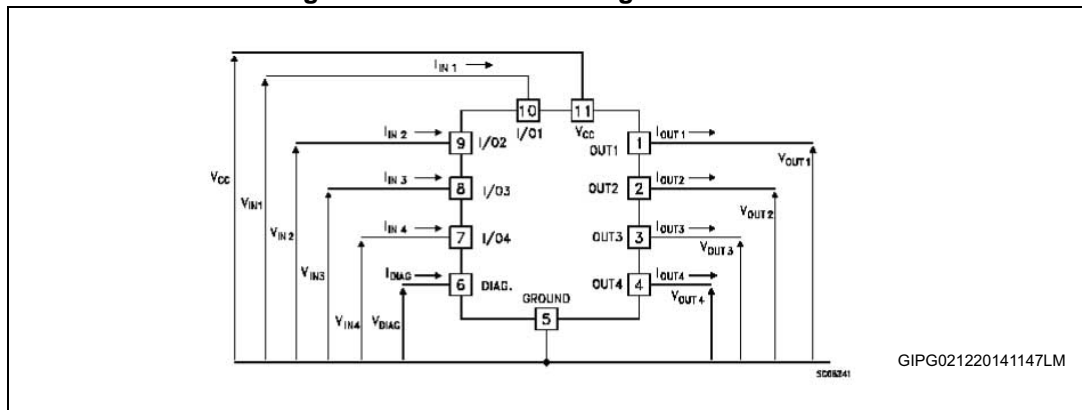


Figure 3. Current and voltage conventions



### 3 Electrical characteristics

10 V < V<sub>CC</sub> < 36 V; -40 °C < T<sub>J</sub> = 125 °C unless otherwise specified

**Table 3. Power section**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply voltage		10		36	V
R <sub>DS(on)</sub>	On-state resistance	I <sub>OUT</sub> = 0.5 A; T <sub>J</sub> = 25 °C			0.2	Ω
		I <sub>OUT</sub> = 0.5 A; T <sub>J</sub> = 85 °C			0.32	
		I <sub>OUT</sub> = 0.5 A; T <sub>J</sub> = 125 °C			0.4	
I <sub>S</sub>	Supply current	All channels OFF			1	mA
		On-state; V <sub>IN</sub> = 30 V; I <sub>OUT</sub> = 0 V (T <sub>J</sub> = 125 °C)			6	
V <sub>OL</sub>	Low-state output voltage	V <sub>IN</sub> = V <sub>IL</sub> ; R <sub>LOAD</sub> = 10 mΩ			1.5	V
V <sub>demag</sub>	Output voltage at turn-off	I <sub>OUT</sub> = 0.5 A; L <sub>LOAD</sub> = 1 mH	V <sub>CC</sub> -65	V <sub>CC</sub> -55	V <sub>CC</sub> -45	V
I <sub>LGND</sub>	Output current at turn-off	V <sub>CC</sub> = V <sub>INn</sub> = V <sub>GNDn</sub> = V <sub>STAT</sub> = 18 to 30 V T <sub>amb</sub> = 25 to 85 °C (see <a href="#">Figure 6</a> )			2	mA

**Table 4. Switching (V<sub>CC</sub> = 24 V)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time of output current	I <sub>OUT</sub> = 0.5 A, resistive load input rise time < 0.1 μs T <sub>J</sub> = 25 °C	-	52	100	μs
t <sub>r</sub>	Rise time of output current			94	250	
t <sub>d(off)</sub>	Turn-off delay time of output current			34	50	
t <sub>f</sub>	Fall time of output current			8	20	

Table 5. Logic input

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IL}$	I/O input low level voltage				2	V
$V_{IH}$	I/O input high level voltage		3.5			
$V_{I(HYST)}$	I/O input hysteresis voltage			0.5		
$I_{IN}$	I/O input current	$V_{IN} = 30\text{ V}$			25	$\mu\text{A}$
$V_{ICL}$	I/O input clamp voltage <sup>(1)</sup>	$I_{IN} = 1\text{ mA}$	32	36		V
		$I_{IN} = -1\text{ mA}$		-0.7		

1. The input voltage is internally clamped at 32 V minimum, the input pins can be connected to a higher voltage via the external resistor without exceeding 10 mA

Table 6. Protection and diagnostic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DIAG}^{(1)}$	Status voltage output low	$I_{DIAG} = 5\text{ mA}$ (fault condition)			1	V
$V_{SCL}^{(1)}$	Status clamp voltage	$I_{DIAG} = 1\text{ mA}$ $I_{DIAG} = 1\text{ mA}$	32	36 -0.7		V
$V_{USD}$	Undervoltage shutdown		5		8	V
$I_{LIM}$	DC short-circuit current	$V_{CC} = 24\text{ V};$ $R_{LOAD} < 10\text{ m}\Omega$	0.7		2	A
$I_{OVPK}$	Peak short-circuit current	$V_{CC} = 24\text{ V}; V_{IN} = 30\text{ V};$ $R_{LOAD} < 10\text{ m}\Omega$			4	A
$I_{DIAGH}$	Leakage on DIAG pin in high-state	$V_{DIAG} = 24\text{ V}$			25	$\mu\text{A}$
$I_{LOAD}$	Output leakage current	$V_{CC} = 10\text{ to }36\text{ V};$ $V_{IN} = V_{IL}$			50	$\mu\text{A}$
$t_{SC}$	Delay time of current limiter				100	$\mu\text{s}$
$T_{TSD}$	Thermal shutdown temperature		150	170		$^{\circ}\text{C}$
$T_R$	Thermal reset temperature		135	155		$^{\circ}\text{C}$

1. Status determination > 100  $\mu\text{s}$  after the switching edge

Note: If INPUT pin floats, the corresponding channel automatically switches OFF. If GND pin is disconnected, the channel switches OFF provided that  $V_{CC}$  doesn't exceed 36 V

# 4 Test circuits

Figure 4. Avalanche energy test circuit

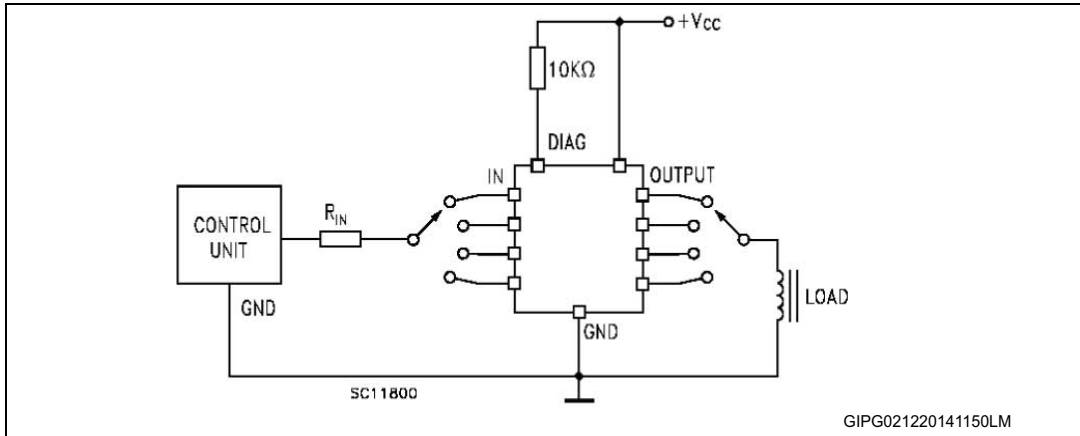


Figure 5. Peak short-circuit test diagram

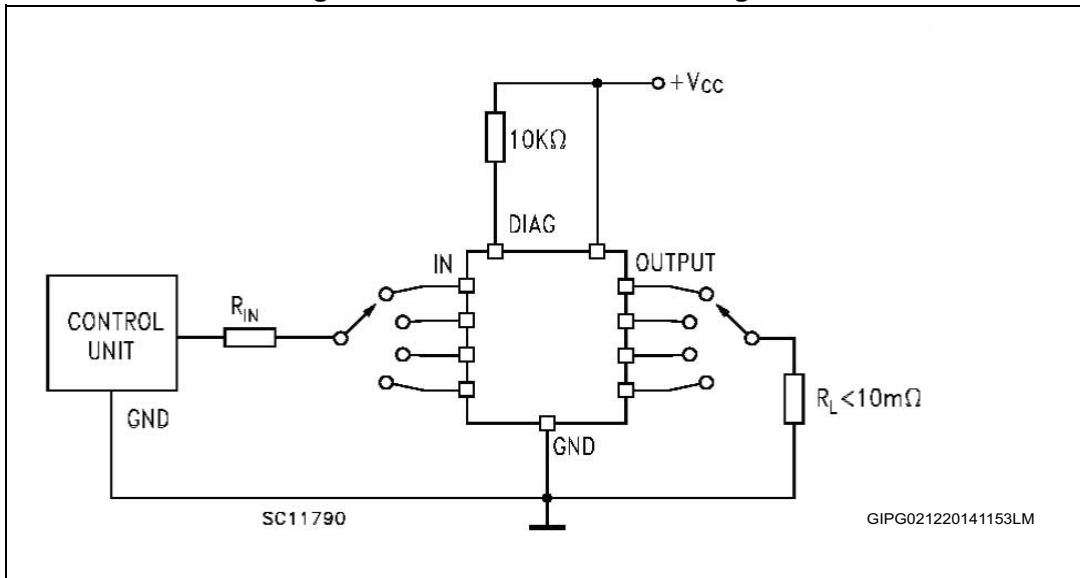
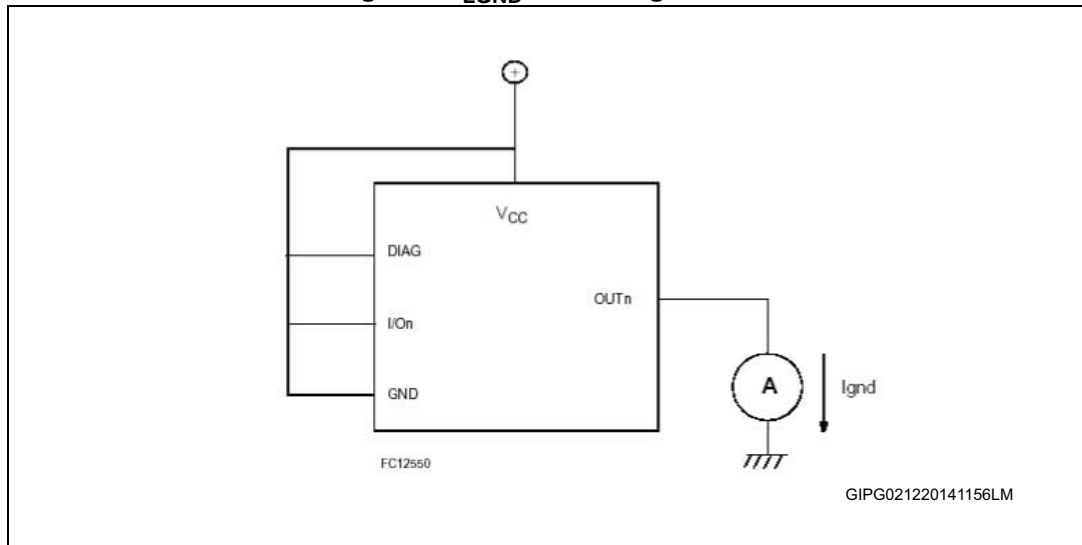


Figure 6.  $I_{L\text{GND}}$  test configuration





## 5 Switching time waveforms and truth table

Figure 7. Switching waveforms

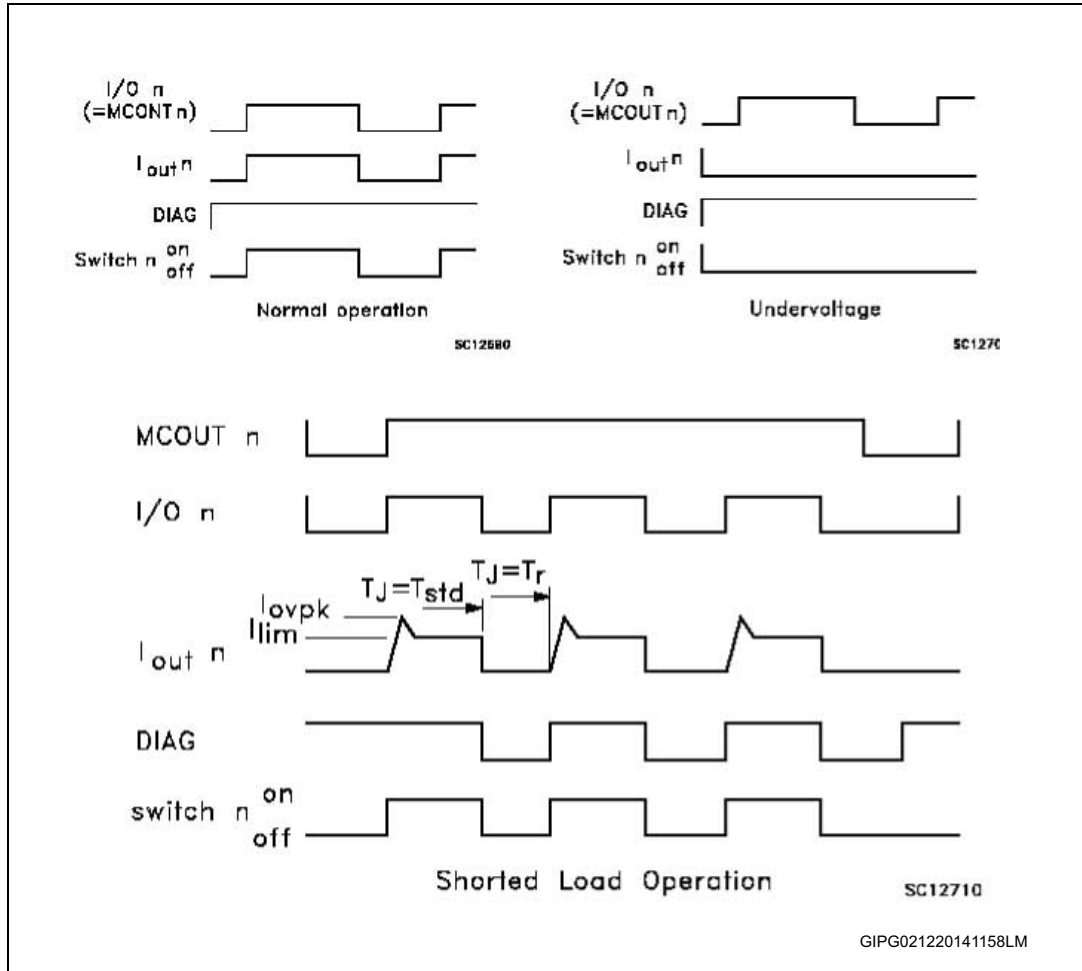


Figure 8. Switching parameter test conditions

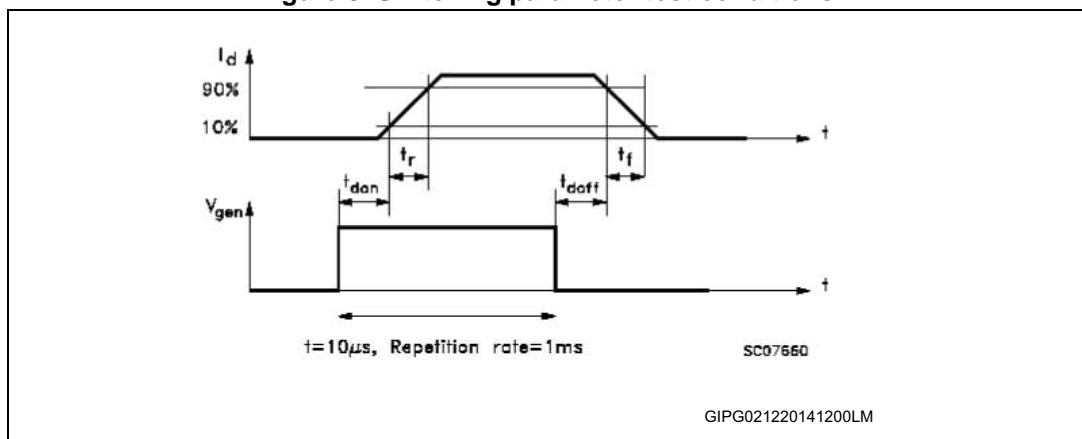
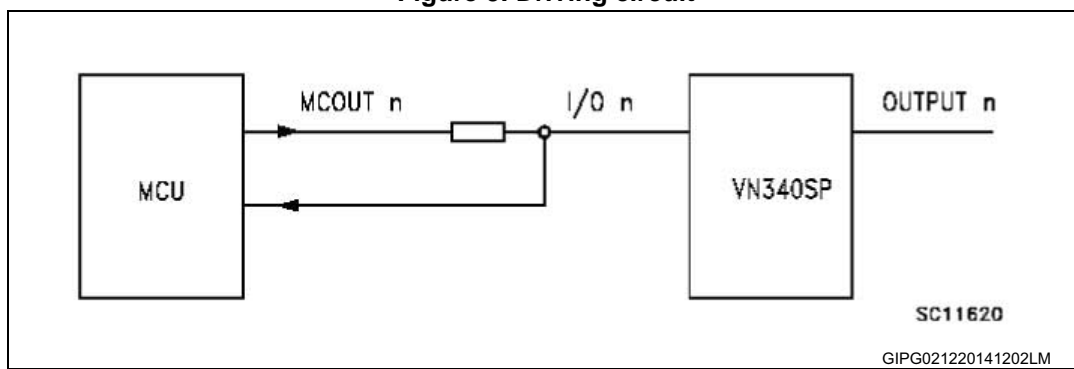


Table 7. Truth table

Conditions	MCOUTn	I/On	OUTPUTn	Diagnostic
Normal operation	L	L	L	H
	H	H	H	H
Overtemperature	L	L	L	H
	H	L	L	L
Undervoltage	L	L	L	H
	H	H	L	H
Short load (current limitation)	L	L	L	H
	H	H	H	H

Figure 9. Driving circuit



## 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 6.1 PowerSO-10 package information

Figure 10. PowerSO-10 outline

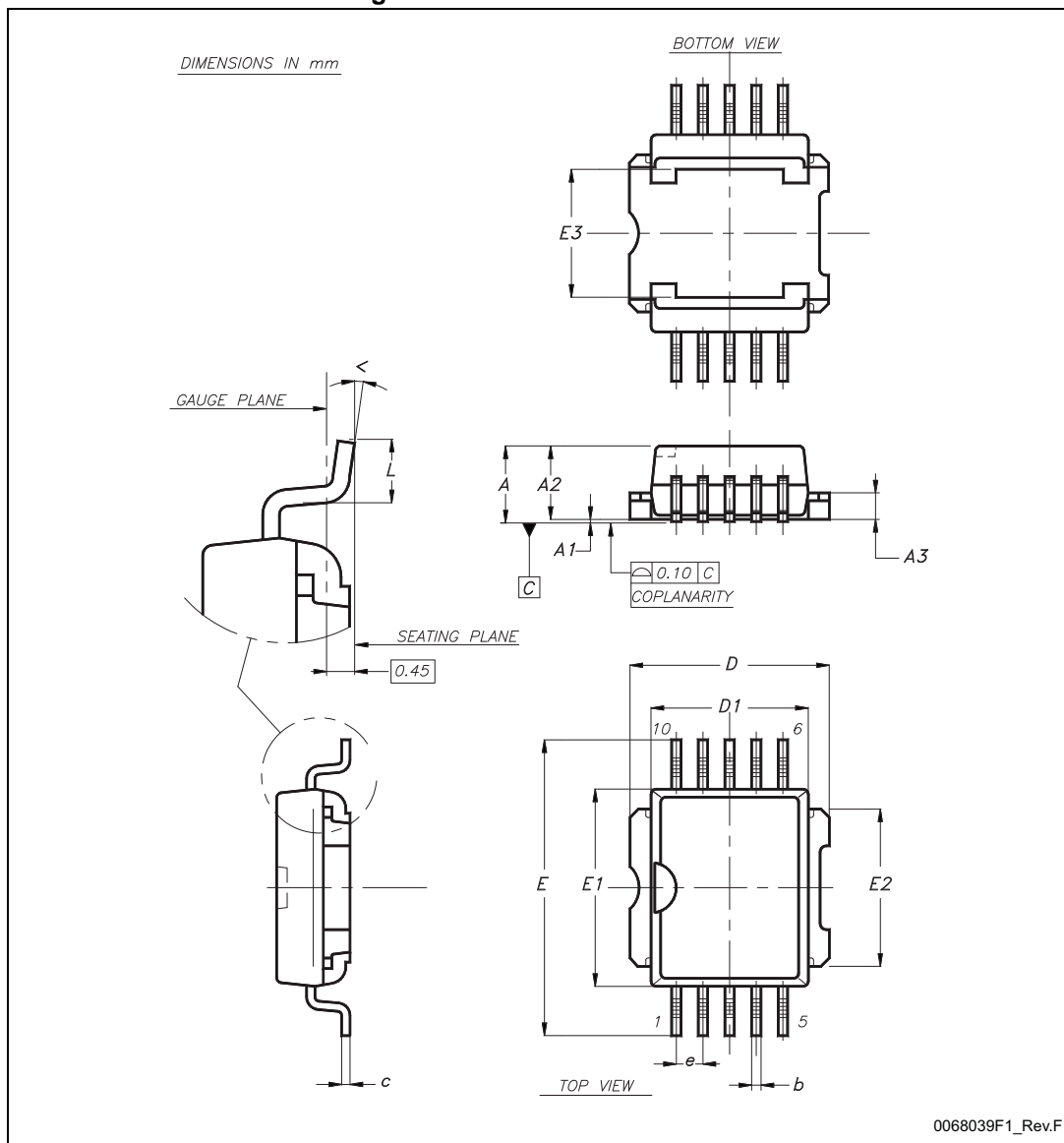


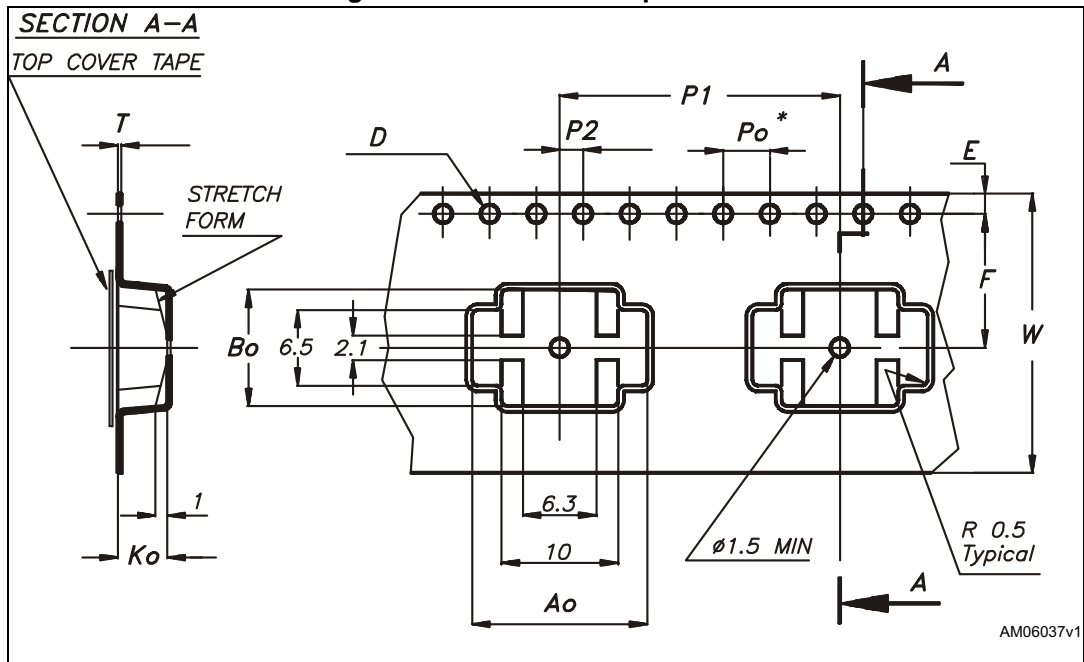
Table 8. PowerSO-10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			3.70
A1	0.00		0.10
A2	3.40		3.60
A3	1.25		1.35
b	0.40		0.53
c	0.35		0.55
D	9.40		9.60
D1 <sup>(1)</sup>	7.40		7.60
E	13.80		14.40
E1 <sup>(1)</sup>	9.30		9.50
E2	7.20		7.60
E3	5.90		6.10
e		1.27	
L	0.95		1.65
<	0°		8°

1. Resin protrusion is not included (max. value 0.20 mm per side)

## 6.2 PowerSO-10 packing information

Figure 11. PowerSO-10 tape outline



Note: Drawing is not in scale

Figure 12. PowerSO-10 reel outline

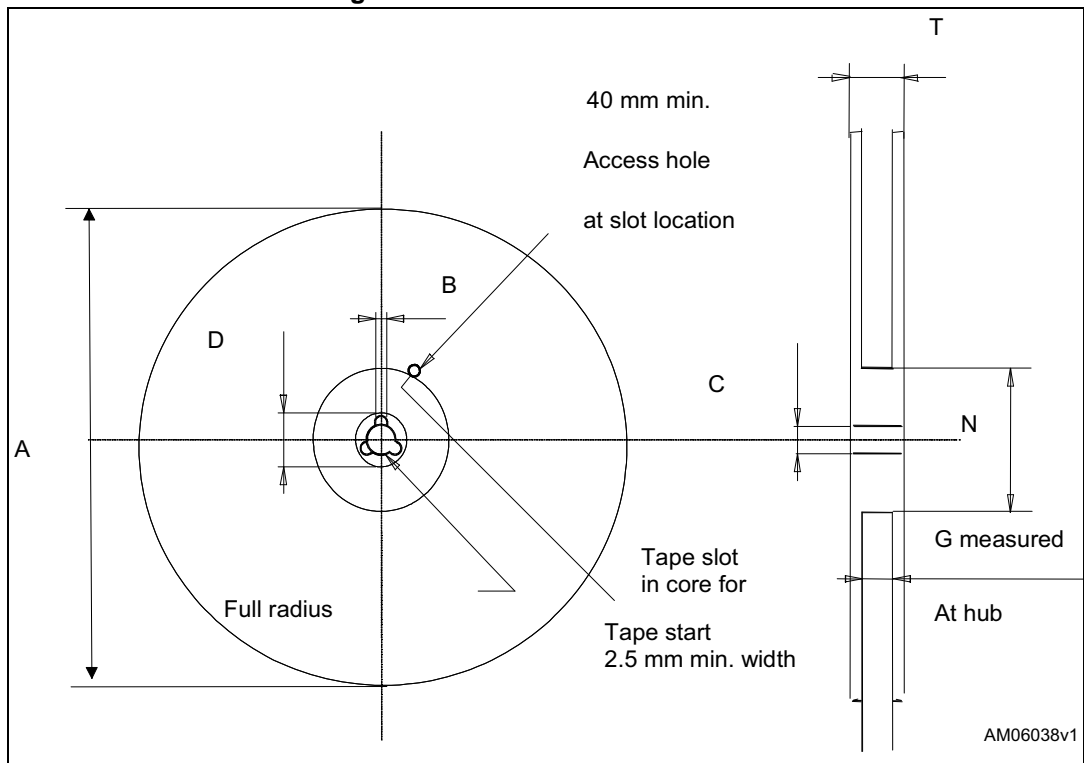


Table 9. PowerSO-10 tape and reel mechanical data

Ref.	mm		
	Min.	Typ.	Max.
A0	14.9	15.0	15.1
B0	9.9	10.0	10.1
K0	4.15	4.25	4.35
F	11.4	11.5	11.6
E	1.65	1.75	1.85
W	23.7	24.0	24.3
P2	1.9	2.0	2.1
P0	3.9	4.0	4.1
P1	23.9	24.0	24.1
T	0.025	0.30	0.35
D(Ø)	1.50	1.55	1.60

Note: 10 sprocket hole pitch cumulative tolerance  $\pm 0.2$  mm

## 7 Ordering information

**Table 10. Ordering information**

<b>Order code</b>	<b>Package</b>	<b>Packing</b>
VN340SP-E	PowerSO-10	Tube
VN340SPTR-E		Tape and reel

## 8 Revision history

**Table 11. Document revision history**

Date	Revision	Changes
05-Sep-2005	1	Initial release.
27-Jun-2006	2	Updated mechanical data.
18-Sep-2006	3	Updated mechanical data and added PowerSO-10 tape and reel.
31-Oct-2006	4	Updated typo in electrical characteristic temperature conditions.
05-Mar-2007	5	Document reformatted, typo in note 1.
04-Dec-2014	6	Updated the title. Updated $E_{AS}$ parameter in <a href="#">Table 1</a> and updated <a href="#">Table 5</a> and <a href="#">Table 6</a> . Minor text changes.



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